

The ATLAS Pixel Sensor
— properties, characterization and quality
control

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Abstract

The planning, construction and commissioning of multi-purpose physics detectors for the LHC proton-proton collider at CERN poses new challenges to the involved institutes regarding scientific, technological and organizational aspects of the process. In the case of the central vertex tracking systems, very complex assemblies have to be produced in large numbers and integrated into a device reliable enough to function for a planned experimental lifetime of at least ten years and in a radiation environment up to doses of several hundred kGy and fluences well above 10^{14} (1 MeV neutron equivalents)/ cm^2 for the innermost parts of the tracking system. A quality assurance plan has to be implemented to ensure high quality of all parts according to the necessary performance parameters, define technical specifications accordingly and provide a good understanding of particle-detector interaction and the physical properties of the detector to extrapolate detector behaviour during the experiment. This thesis gives a detailed overview of the motivation, physics and organizational aspects and results of the quality assurance program for the silicon sensor used in the pixel sub-detector for the ATLAS multi-purpose experiment. The sensor design used is shown to be well suitable for assembly and long term operation within the ATLAS experiment, and the quality plan implemented for sensor production has proven highly indicative for monitoring crucial aspects of sensor quality. In addition, problems within sensor production could be pinpointed at an early stage and further insights into the physical properties of sensors and parameters of their operation could be gained.

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1 Introduction

During the second half of the twentieth century experimental particle physics has seen an astonishing development, yielding insights into the properties of subatomic particles on increasingly smaller distances and higher energy scales, and has helped to find and confirm the so-called standard model of particle physics explaining the electromagnetic and weak nuclear interaction (formulated as a common electroweak interaction) and the strong nuclear interaction and all their constituents within a framework consistent with relativistic dynamics. The experimental breakthroughs have been made possible by a series of developments concerning accelerator and detector physics, as well as the increase in easily affordable computing power and significant organizational changes in the international physics community.

Two of these defining trends in experimental particle physics are central to this thesis, the development of micro vertex detectors for particle collider experiments, designed to allow for the reconstruction of particle tracks back to possible secondary vertices and the improved indirect identification of low lifetime primary particles, and the formation of increasingly larger collaborations, able to construct and maintain increasingly bigger and more complex detector systems, incorporating a large amount of high quality parts. These developments have led to the construction of intricate tracking systems to be installed very close to the experimental interaction point, now mostly consisting of layered semiconductor tiles, finely segmented to optimize spatial resolution. Some efforts are necessary to construct a complex and accurate subdetector to be put in a location close to the interaction point of the experiment and thus subject to high radiation levels and hardly accessible for later maintenance. Among these are the projection of behaviour throughout the lifetime of the experiment and the exact monitoring of the detector production to assure the full long-term functionality of the tracking system. This has to be based on a good knowledge of the characteristics of all detector parts when assembled and of changes in behaviour caused by irradiation. This is the basic description of the aim of a quality assurance plan for a particle physics detector or subdetector, in this case for the sensor tiles of the ATLAS pixel detector.

The aim of the work presented in this thesis has been the formulation and implementation of a quality plan specifically for the silicon sensors of the pixel detector. From a scientific point of view this includes choosing sensor parameters and tests representative of sensor functionality in operation, verifying the adequacy of the chosen sensor concept and manufacturers as well as demonstrating the relevance of the measured data regarding the task of quality control at hand as well as the aspects of device physics involved. To achieve this, the role of the pixel sensor within the ATLAS experiment had to be considered as well as the specific properties of the sensor design (chapter 2). Regarding the possibilities of quality assurance strategies and knowledge about the intended sensor properties, test devices have been chosen and procedures have been defined for measurements and assessment of results (chapter 3). The test data has been gathered and analyzed, often together with additional tests to clarify aspects of sensor behaviour or systematic influence of the used test set-up (chapter 4). These results are finally assessed in the context of sensor quality as well as additional information of sensor behaviour before and after irradiation, to gauge the success of the quality plan regarding its scientific aims (chapter 5).

1 Introduction

2 ATLAS Pixel sensor

2.1 ATLAS pixel subdetector

2.1.1 ATLAS experiment

The ATLAS experiment is one of two multi-purpose detectors planned and assembled for use at the LHC (Large Hadron Collider) proton-proton collider ring at the CERN (Centre/Conseil Européen pour la Recherche Nucléaire) site, Geneva (see figure 2.1). The main purpose of the new ring collider, constructed for proton-proton collisions up to a maximum center of mass energy of $\sqrt{s} = 14$ TeV, is the continuing research on new physics phenomena at an energy scale beyond the limit set by experiments at the electron-positron collider LEP at CERN and the proton-antiproton collider Tevatron at Fermilab, especially the verification of the existence and properties of bosons associated with the mass generating Higgs process postulated by the standard model and the test of the supersymmetric theories on the unification of the electroweak theory and quantum chromodynamics.

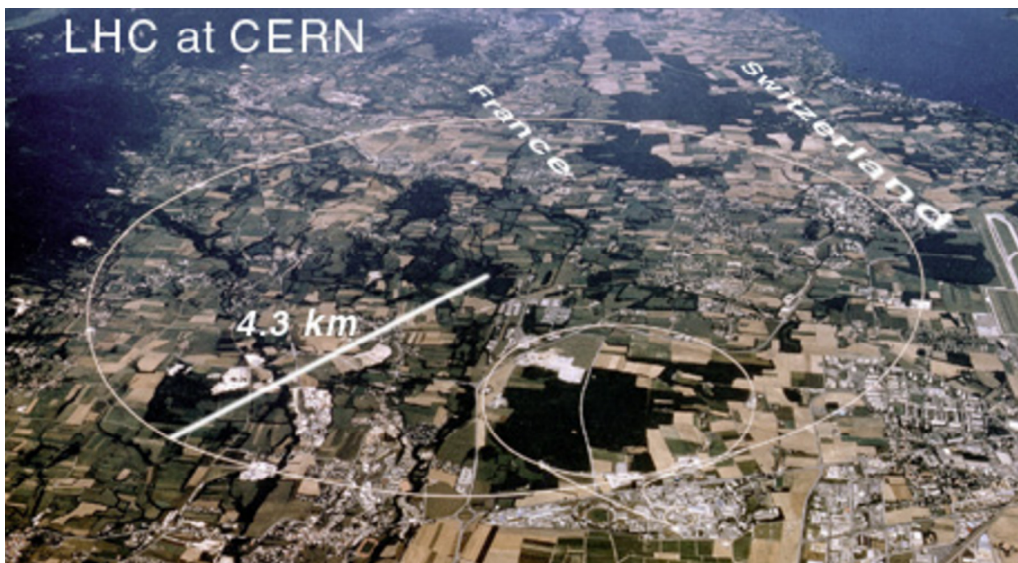


Figure 2.1: Geographical layout of the LHC ring [ATL04]

Among the four experiments to be constructed at the LHC ring, (see figure 2.2) are two specialized detector systems, ALICE for heavy ion collisions up to $\sqrt{s} = A \cdot 2.76$ TeV and LHCb for tests on CP violation in $b\bar{b}$ -systems. The remaining two experiments, ATLAS and CMS, consist of multi-purpose detectors, designed to detect and resolve a wide variety of possibly interesting physics events and generate a comprehensive data set for new physics searches as well as precision analyses of known quantities.

The high design luminosity of the LHC beam focus ($10^{34} \text{ s}^{-1} \cdot \text{cm}^{-2}$) and the bunch crossing rate of 40 MHz [LHC93] [LHC95] (one crossing per 25 ns in each general purpose experiment generating on average 23 inelastic interactions [ATL97a]) lead to the production of a vast amount of detector signal data of which the biggest portion comes from minimum bias events. These events only generate a very small transversal momentum in the particles generated by the colliding protons, producing mostly low energy pion jets, and are not of special interest for probing physical processes at high energies. This creates the opportunity to reduce the amount of event data drastically

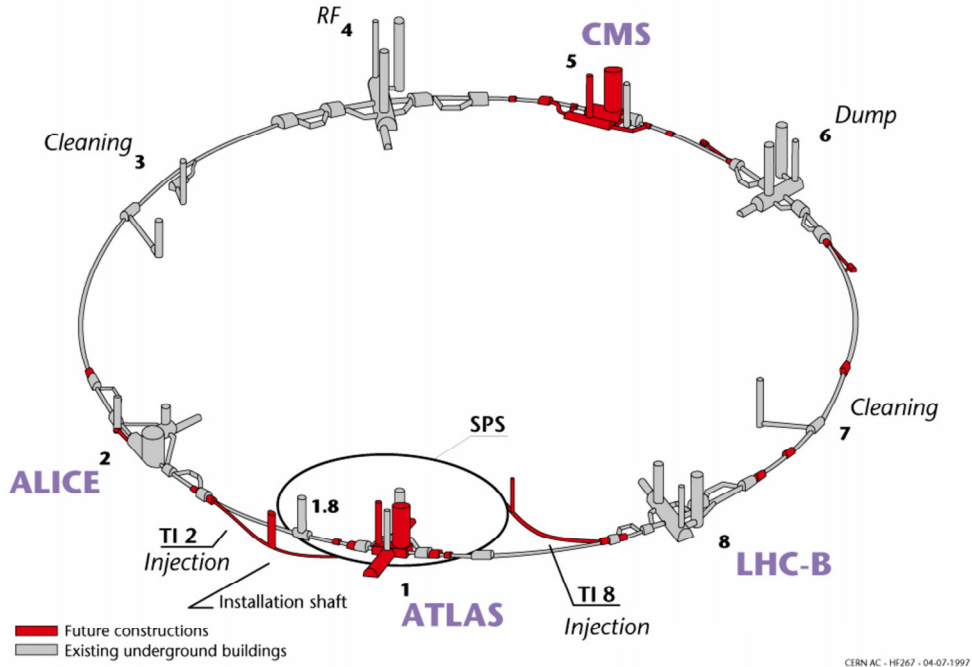


Figure 2.2: The LHC tunnel excavation including caverns for experiments [ATL04]

without losing a comparably large portion of the information relevant for later analyses. To exploit this possibility, it is necessary to implement a trigger system capable of doing a very fast preliminary event reconstruction to effectively suppress irrelevant events and artifacts.

The main topics of the ATLAS physics program, for which detector concept and trigger performance had to be optimized are [ATL99b]:

- Searches for predicted bosons of the Higgs field, favouring coupling to heavy particles like third generation quarks and massive bosons. In supersymmetric extensions of the standard model more than one kind of Higgs boson is expected.
- Searches for supersymmetric partner particles of known particles.
- Searches for unknown massive gauge bosons outside the Higgs sector.
- Searches for evidence for compositeness of elementary particles, especially quarks.
- Precision measurements of masses of heavy quarks and bosons, gauge boson coupling, violation of CP symmetry, and the Cabibbo-Kobayashi-Maskawa unitarity.

The decay channels expected for events generating Higgs bosons that could be seen as resonance in the energy spectra of decay products favour states of relatively high mass particles, as the mass producing process of the Higgs mechanism should lead to a scaling of interaction probabilities with the mass of particles coupling to the Higgs boson, whether real or virtual. For Higgs boson masses m_H with $120 \text{ MeV} \leq m_H < 2 \cdot m_Z$ this leads to a high expected incidence of ZZ production with one virtual boson (called ZZ^* or off-shell production) or for $m_H \geq m_Z$ with two real bosons. This combination can lead to two-lepton/antilepton pair endstates (see figure 2.3), among them a very distinctive, although not highly favoured double muon-antimuon states without missing energy, whose tracks can be detected and whose energy can be reconstructed by using a dedicated muon detector enclosing a significant volume around the interaction point containing a high and well characterized magnetic field.

The favoured expected hadronic decay channel of the Higgs boson is the production of a $b\bar{b}$ -quark-antiquark pair, as this is the heaviest quark carrying less mass than half the expected m_H .

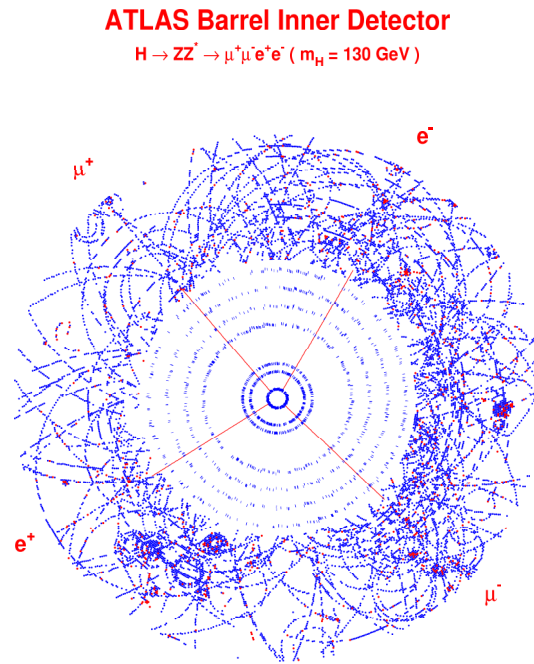


Figure 2.3: Simulated event display of a Higgs boson decaying into two lepton/antilepton pairs [ATL97a]

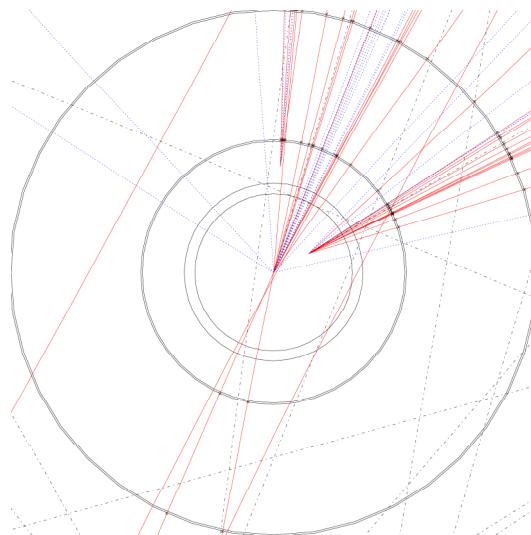


Figure 2.4: Simulated event display showing three hadronic jets, one originating at the primary vertex, two on secondary vertices usable for flavour tagging [BAT00]

To extract these telltale $b\bar{b}$ productions from the background of other hadronic jets abundant in the end states of strong interaction processes, dominating the pp cross section, it is crucial to differentiate the isolated decay of b quarks and antiquarks at secondary vertex points from similar processes involving second family quarks and from jets produced from stable first generation quarks, lacking secondary weak interaction vertices. This can be achieved by comparing the distances of the secondary vertices of hadronic jets (see figure 2.4) from the primary interaction point, as the mixing of b-quarks in the Cabbibo-Kobayashi-Maskava matrix with the lighter quark families is relatively weak, allowing for significantly longer life times of b-quarks compared to c- and s-quarks.

This heavy flavour identification or b-tagging is a crucial feature not only for Higgs searches, but also for searches for supersymmetric particles and precision measurements involving heavy flavoured quarks (known as b-physics) [ATL97a] [ATL99b]. The possible quality and significance of b-tags is one of the most important benchmarks of the ATLAS experiment, as is hermeticity of the detector and the possibility to perform precise measurements of transversal momentum p_T and missing transversal energy E_T^{miss} .

To have the option of a comparison of distances between primary and secondary vertices a fine grained resolution of particle tracks close to the interaction point is necessary, calling for a set-up incorporating a micro vertex detector providing more than three correct space coordinates for every particle track and a good resolution of tracks even within a hadronic jet.

2.1.2 ATLAS detector layout

Similar to the detectors used in the electron-positron collision experiments at LEP as well as many other high energy physics experiments over the last decades designed for experiments exhibiting identical inertial systems for the detector and the center of mass of the collision, the ATLAS detector uses a cylinder symmetric layered detector concept consisting of subdetectors, each specialized in providing certain event information (see figure 2.5). The detector components are specialized for the needs of the ATLAS physics program and thus breaks new ground both in scale and in the characteristics and technologies of its components and subdetectors [ATL99b]. The most distinctive features of the ATLAS concept are a high resolution muon spectrometer with dedicated trigger system, a toroidal outer magnetic system realized with a minimum of added absorbing mass (superconducting air toroids), and a calorimetric system optimized for spatial resolution.

The detector is designed to cover a pseudorapidity range η from -3.2 to 3.2 (-4.9 to 4.9 including the forward detector). The inner parts of the detector are enclosed in a solenoidal magnetic system standard for many earlier particle physics experiments, in this case producing a nearly homogeneous field of 2 T, while the outer part is provided with a magnetic field ranging up to a peak field of (4.2 – 4.4) T by superconducting toroidal air coils. The latter greatly reduce the amount of non-sensitive material present within the detector compared to traditional coil and yoke set-ups [ATL94]. The subdetector farthest from the interaction point is the muon spectrometer array, defining the outer envelope of 46 m length and 24 m diameter of the whole detector set-up. Like all subdetector systems, it consists of multiple barrel-shaped detector layers centered on the interaction point, and several end-cap layers closing the forward and backward ends of the barrels. The muon system's spectrometric precision of better than $50 \mu\text{m}$ spatial resolution for reconstruction of muon tracks is provided by monitored drift tube (MDT) chambers and, in the extreme forward and backward region, by cathode strip chambers (CSCs) of high granularity. Both are triggered by a dedicated system of resistive plate chambers (RPCs) and thin gap chambers (TGCs) [ATL97b]. The next layer inwards is a hadronic calorimeter for measuring the energies of hadronic jets realized as a combination of a tiled set-up of plastic scintillators with a calorimeter using liquid Ar as an active medium and Cu absorbers followed by an electromagnetic calorimeter, realized as a liquid Ar system with Pb absorbers, all sufficiently granulated to yield a space resolution of $0.1 \cdot 0.1$ or better in η and ϕ [ATL96a] [ATL96b].

The ATLAS inner detector within the central solenoid (see figure 2.6) is enveloped by the transition radiation tracker (TRT). It consists of an array of Xe filled straws, oriented axially along a central detector barrel and radially within end-cap wheels. The modularly packed straws exhibit a spatial resolution of $170 \mu\text{m}$ perpendicular to the straw orientation. Still closer to the interac-

2.1 ATLAS pixel subdetector

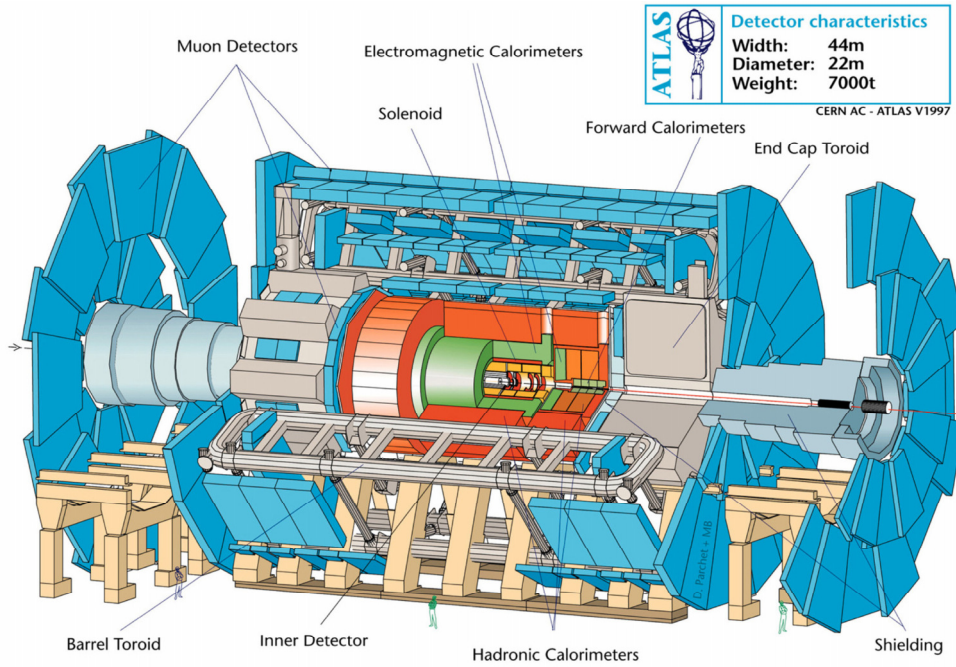


Figure 2.5: Overall set-up of the ATLAS subdetector systems [ATL99b]

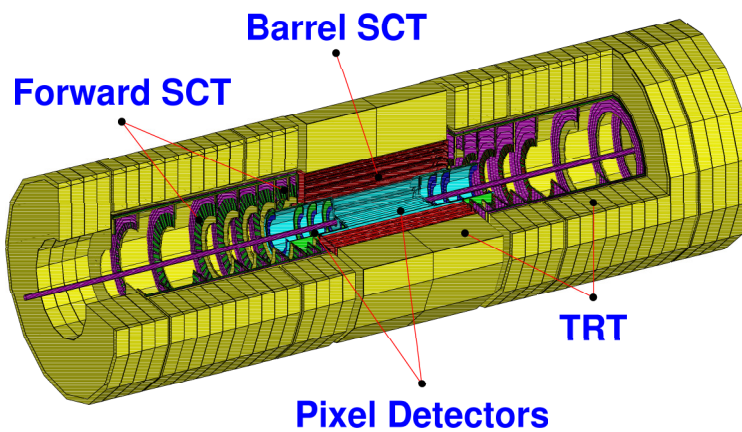


Figure 2.6: Layout of the ATLAS inner detector subsystems [ATL97a]

tion point are the silicon tracker layers, similar to the TRT consisting of central barrel layers as well as wheels for the forward and backward directions. The outer layers are built from single and double sided silicon strip detector modules called SCT (SemiConductor Tracker), while the innermost layers, installed next to or in the case of the so called B-layer barrel on the beam pipe around the interaction point, and again exhibiting disc layers in forward and backward direction, are constructed from tiled hybrid pixel silicon detector modules [ATL97a].

2.1.3 Pixel detector concept

The innermost subdetector for an experiment like ATLAS for several reasons demands the implementation of a silicon pixel system. As is the case with microstrips, a high granularity can be achieved because of the significant progress in silicon processing, providing robust vertex detector components at a low probability of particle absorption or multiple scattering. For a use within the central tracker layers for vertex reconstruction, strips have the drawback of either forgoing spatial resolution in one dimension (in the case of single-sided modules) or, when using double-sided detectors or modules with pairs of single-sided ones set up at a stereo angle, producing ambiguous location reconstruction data for more than one simultaneous particle hit per module. As the expected mean number of visible particle tracks for a bunch crossing producing at least one potentially relevant physics event is above 1000 [ATL97a], and all resulting hadronic jets will produce tracks bundled within a relatively small solid angle the latter effect would be highly detrimental to the detector performance. This problem can be solved by choosing a silicon detector gaining two-dimensional spatial information via one surface segmented into individual pixels. The high bunch crossing rate of the LHC (40MHz) is optimized for producing a massive amount of physically interesting collisions and thus allows for only a minimal detector dead time (significantly below the minimal bunch crossing interval of 25ns). This excludes the use of CCD pixel detectors because of their relatively time consuming serial read-out, leaving a hybrid pixel concept as the only suitable type of semiconductor detector fit for reliable production in sufficient quantities, as monolithic pixel detectors (see [KEM87] and [DEP00]) are only now beginning to be produced in small series suitable for assembly of vertex detectors [WIE04] or at an even earlier development stage [RIC03a] and thus not available when production for the ATLAS pixel detector had to start.

Additionally, as will be discussed later, the detector set-up as a hybrid silicon pixel detector lends itself excellently to applications calling for high tolerance regarding charged hadron radiation.

To achieve the high resolution and fast readout times necessary for the ATLAS tracking system a hybrid pixel detector is being implemented for the innermost tracking layers. The layout of the detector system consists of three concentric barrel layers and two sets of disks, one each in forward and backward direction. The number of discs in each end-cap set has varied historically from five in earlier specifications [ATL98] to the current value of three (see figure 2.7). On each of these mechanical carrier structures detector modules are inclined in an overlapping tile pattern to cover the whole pseudorapidity range of the pixel detector without significant gaps in any single detector layer. Additionally this inclination can be used to optimize spatial resolution (discussed below).

The support structures called staves for the barrel layers and disc sectors for the ring shaped discs provide a mechanical framework and thermal contact to an evaporative cooling system using C_3F_8 as a coolant. The materials used are aluminium and carbon compounds, to minimize scattering and absorption of particle tracks within non-sensitive material. Along the carrier structures each module is supplied with electrical ground, high voltage for sensor depletion and operation voltages for electronics operation, and is controlled and read out via an optical glass fiber connection [ATL98].

2.1 ATLAS pixel subdetector

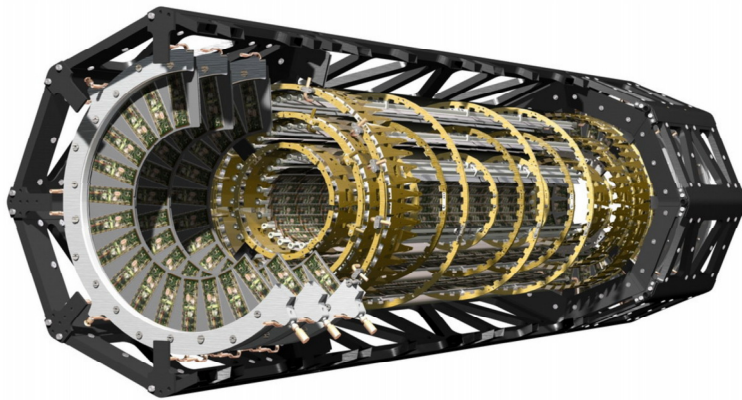


Figure 2.7: Cut-away view of the ATLAS Pixel subdetector [LBL04]

2.1.4 Pixel detector module

As a hybrid pixel detector, each detector module consists of a sensor tile and sixteen front-end electronic chips glued to a flexible kapton carrier acting as a circuit board (see figures 2.8 and 2.9). The nominal dimensions of each pixel cell are $400\ \mu\text{m}$ length oriented along the barrel length or the disk radius and a $50\ \mu\text{m}$ pitch in direction around the barrel circumference or perpendicular to the disk radius. The readout connections between sensor and electronics are realized as bump bond contacts between contact pads of each sensor pixel cell and the corresponding front-end pixel (see figures 2.10 and 2.11a & b). To produce these small pitch micro integration bumps, two distinct technologies will be used, indium bumps remaining malleable at room temperature being set under considerable pressure with an alignment precision well below their dimension of $20\ \mu\text{m}$ diameter [GEM00], while solder bumps are molten in a re-flow step and are self-aligned within the margin of bump dimension during the following cooling down step by surface tension. (For an overview of the use of these technologies in an earlier project, see [CAC01].)

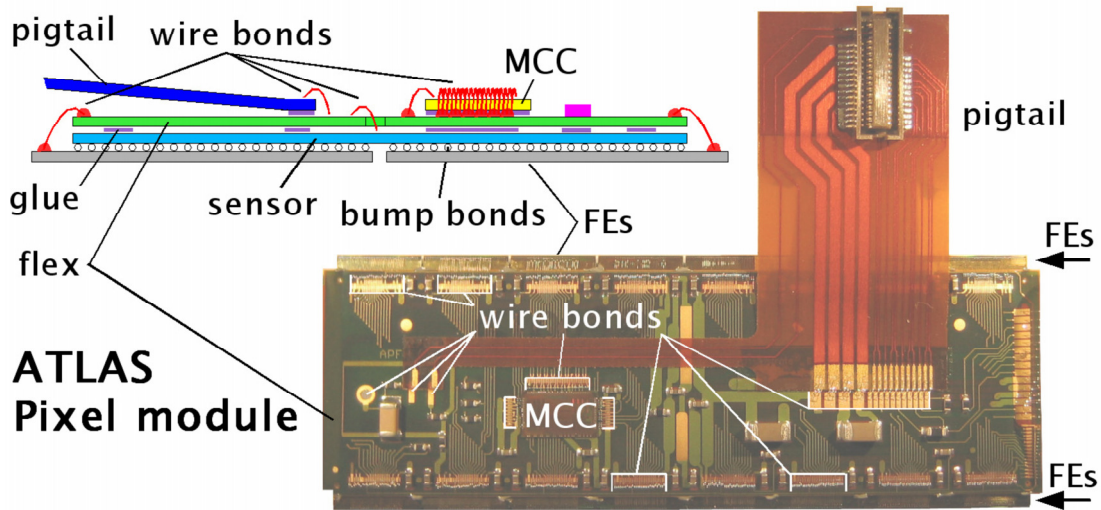


Figure 2.8: Components and assembly structure of the ATLAS pixel module [DOB04]

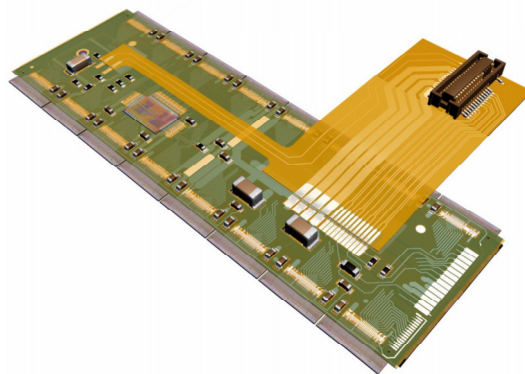


Figure 2.9: Three-dimensional model of the ATLAS pixel module [DOB05]

The so called bare module is glued onto the flexible kapton carrier, and the vias on the carrier are connected to the sensor tile metallization via conductive glue to supply high voltage to the sensor and via aluminium wire bonds ($25\ \mu\text{m}$ diameter) to the voltage supply and signal pads of the front-end chips, not only providing operation voltages for the front-end electronics as well as a connection

2.1 ATLAS pixel subdetector

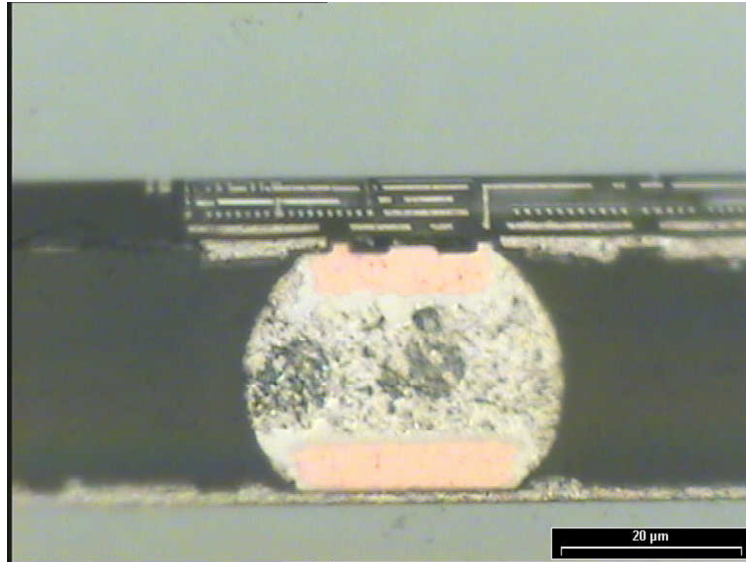


Figure 2.10: Cross section of a solder bump connecting pixel sensor to front-end electronics [IZM04]

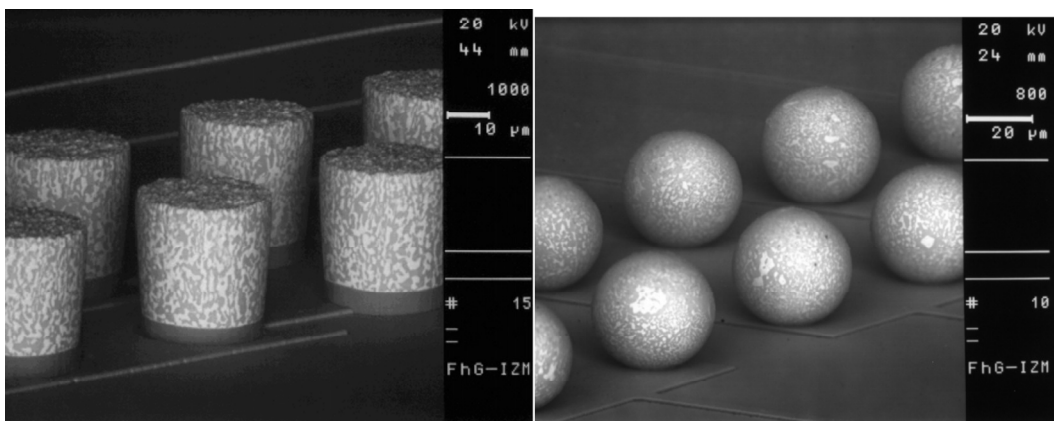


Figure 2.11: Solder bumps a) after photolithographic deposition (left) and b) after re-flow (right) on a carrier surface [IZM04]

2 ATLAS Pixel sensor

for triggers and data read-out, but indirectly grounding the silicon sensor via the DC coupled pre-amplifier transistors and guard connections to analogue ground. The further components of the module (see figures 2.8 and 2.9) besides passive capacitors and resistors are the module control chip (MCC) and a connection to the so-called opto-package located away from the module itself on the nearest patch panel for supply and signal lines. The former is a single electronics chip per module, wire bonded onto the kapton carrier for managing all signals to and from the front-end, setting fast control operation parameters, receiving requests for data of a specific bunch crossing according to level one trigger decisions for the whole ATLAS system, retrieving all relevant data from the front-end buffers and sending them out as zero suppressed event information on module level useable for further event building. The opto-package is an elaborate part of the cable connection of the module to the rest of the world, encompassing several chips and diodes connected to optical signal lines. It is connected to the module via a connector on the kapton pig-tail glued and wire bonded to the flex carrier and containing all signal and voltage supply lines. Within the package, the event information from the MCC is translated into optical signals in a VCSEL (Vertical Cavity Surface Emitting Laser), controlled by the VCSEL driver chip (VDC), and fed into an optofibre connection to the read-out electronics outside the ATLAS detector. Incoming operation commands and test signals to the MCC are in turn received via the fibre connection by a photo sensitive diode read out by a biphasic decoding chip (DORIC). The voltage supply lines are running from the pig-tail as individual micro cables parallel to the optical signal lines via several patch panels.

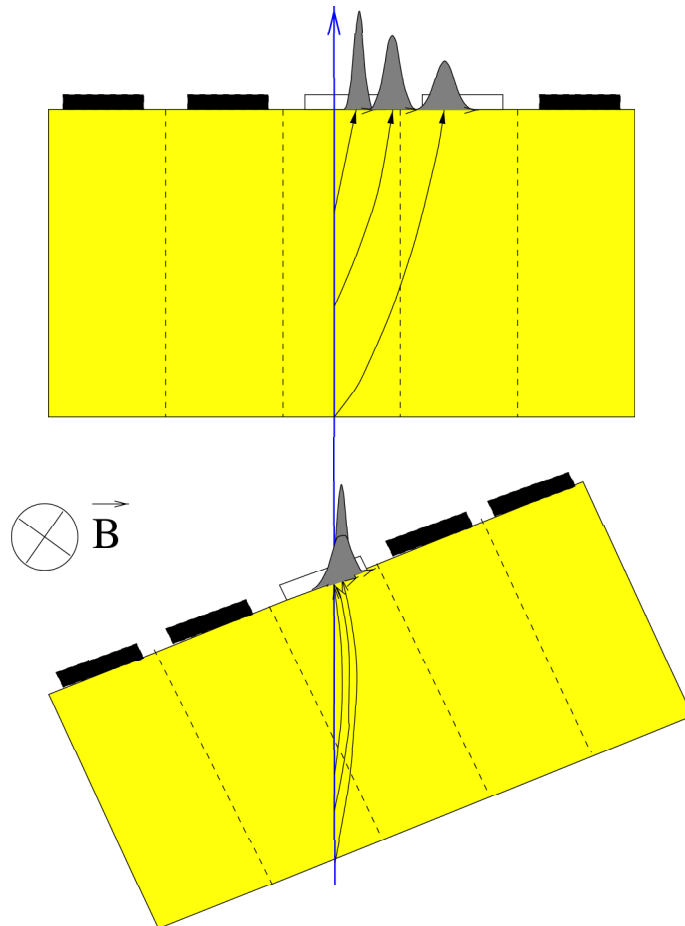


Figure 2.12: Signal clusters within a magnetic field for different incidence angles [GOR01]

The module components having the biggest influence on sensor operation, aside from the sensor

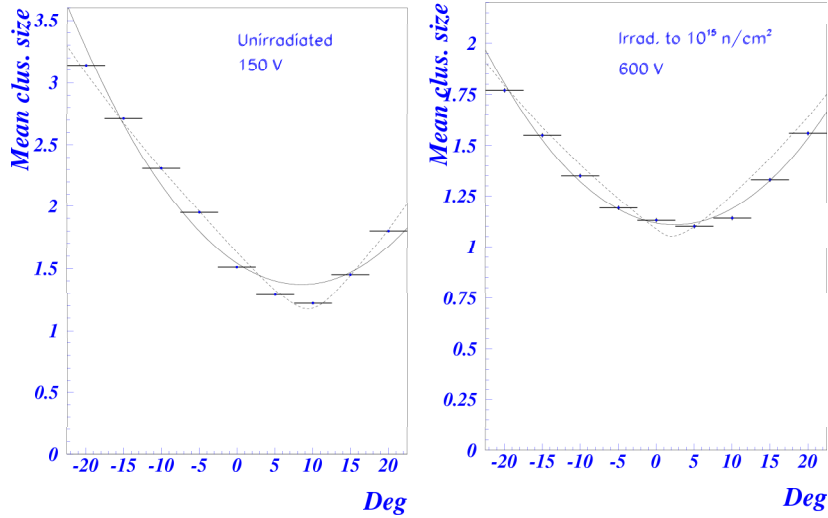


Figure 2.13: Cluster size dependency on incidence angle for modules a) before (left) and b) after (right) proton irradiation [GOR01]

itself, are the front-end electronics chips and the bump connections between them and the sensor. As already mentioned, the sensor pixel cells are set via a DC connector to the input voltage of the pixel cell pre-amplifier, around (1 – 1.5) V more positive than analogue ground connected to the sensor guard structures. This voltage difference adds to the negative bias voltage applied to the sensor p-side and shapes the potential within the sensor for charge collection in the pixel cells. The induced charge fed into the front-end pixel cell is amplified in the pre-amplifier and shaped as a sharp rise in voltage proportional to the collected charge followed by a linear drop induced by a feedback current. This allows for two trigger signals per registered charge, one for the rising and one for the falling flank, with a time over threshold interval proportional to the signal height above threshold voltage respectively above the threshold equivalent charge. The time over threshold as well as the hit time are stored in a designated latch for each pixel cell, to clear the amplifier and sampler for the next hit and are read out into buffers on the end of each pixel double column, where they are either retrieved by a level one trigger request or discarded after being identified as not belonging to a triggered event. Individual pixel thresholds as well as the feedback current can be tuned to minimize threshold dispersion, and produce a time over threshold scenario yielding both a sensible charge resolution and a clearing time of the amplifier comparable to the 25 ns bunch crossing interval.

To improve the spatial resolution of the pixel sensor beyond the limits of the pixel dimensions, double or triple hits of the same particle track in pixels of one module can be used to weigh the shared charge and determine where exactly the track in question has crossed which depth within the active sensor volume. This will only be possible for a significant portion of measured tracks, if the thresholds can be set low enough to measure charges smaller than (0.3 – 0.5) of the total charge deposited by a typical particle track, and the modules are inclined away from the ideal track incidence angle (Lorentz angle) for the inner detector’s magnetic field (see figure 2.12), producing a longer, diagonal particle track through the sensitive volume and thus a higher proportion of multiple pixel tracks, and away from a perpendicular track incidence angle, producing a higher typical total charge deposited per track. As the ideal Lorentz angle and thus the cluster size dependency changes for sensors having received bulk damage from irradiation (figures 2.13a & b), this inclination can be optimized for fast charge collection within the sensor and small cluster sizes after full irradiation, leading to minimized charge loss by charge carrier trapping and increased signal height per pixel, by placing sensors at an optimal Lorentz angle for the magnetic field within the inner detector. (For further discussion see [ALE00] [LAR01] [GOR02] [GOR01].)

2.2 Pixel sensor design

The ATLAS Pixel sensor has not only to meet considerable geometrical constraints concerning its thickness and granularity as well as a high charge collection efficiency within the sensitive volume, most of all it has to remain fully functional for as long as possible, while sustaining a massive amount of both ionizing and non-ionizing particle damage throughout its projected ten year lifetime. To arrive at a sensor concept coping with these requirements, a two-way approach has been taken. On the one hand a selection process for a substrate material readily available and exhibiting the optimal radiation tolerance under the damage scenario expected for ATLAS operation was started in collaboration with people from other high energy physics experiments as well as from physics groups concerned with characterizing semiconductor material and studying effects of radiation damage on semiconductors. This collaborative effort was mostly done under the roof of the CERN ROSE collaboration (a.k.a. RD48).

The other line of development has been concerned with the design process of the pixel structure itself, to make use of the radiation tolerance of the chosen bulk material and add to it with a radiation tolerant surface process as well as to meet the design parameters set for integration and electrical properties before irradiation. This aspect has been a collaborative effort within the ATLAS pixel collaboration, especially benefiting from the technological and experimental knowledge of the semiconductor laboratory (MPI-HLL, Munich) of the Max-Planck-Institutes for physics and for extraterrestrial physics in Munich. In this case the collaboration has been effected on a much narrower scope toward the specific characteristics sought for the ATLAS Pixel detector, as these will inevitably vary significantly from those suited for other experiments run under different conditions and pursuing different scientific goals. These two lines of development have been combined to provide a state-of-the-art device exhibiting the best possible radiation tolerance, fully complying to all ATLAS requirements in the set-up described above.

2.2.1 Sensor concept

As part of a state-of-the-art hybrid pixel detector, the ATLAS pixel sensor (see [HÜG01] for overview of planning and prototyping) is planned to be in principle an array of bipolar diodes created on a high resistivity bulk close to intrinsic charge concentration (n dose around 10^{12} cm^{-3}) by implanting high positive or negative dose regions (n^+ and p^+) on one wafer surface each. Given a bias connection and a high enough voltage tolerance of the diode array, the asymmetric depletion region on the p^+ - n junction can be operated in reverse bias and extended over the whole sensor bulk volume, able to collect and thus detect all charges produced within the volume by ionizing particles. For the kind of functionality needed for the ATLAS experiment this very basic design has of course to be elaborated on to guarantee inter pixel isolation, minimize leakage current and make the sensor testable as well as tolerant to radiation damage and suitable for assembly as a hybrid detector.

The results of the ROSE collaboration on controlled damage engineering [LEM99] as well as follow-up research (e.g. within the RD50 collaboration [CAM03]) provide striking evidence for the high tolerance of silicon with a slightly increased amount of oxygen impurities against bulk damage caused by charged hadrons (an opposite effect has been reported in the presence of a higher carbon concentration). These improvements do not alter the leakage current characteristics, which seem to be adequately described by the NIEL (Non-Ionizing Energy Loss) approach to particle damage. The main difference can be seen in the development of depletion depth after irradiation and annealing. In the parameterization of the Hamburg model (see figure 2.14, [MOL99] and [LEM99]) for an oxygenated sample the constant damage induced charge density is somewhat below the density for samples with average oxygen concentration for fluences $\geq 10^{14}$ (1 MeV neutron equivalents)/ cm^2 (figure 2.15a). While the beneficial effect of annealing is not significantly influenced, a rather dramatic effect has been reported and confirmed concerning additional effective charge production by long term annealing, so-called reverse annealing. The reverse annealing effects are not only slowed considerably (figure 2.16), producing a lower overall effective charge density in similarly irradiated samples after identical annealing scenarios, there is also a marked saturation of effective charge density for high irradiation fluences absent in standard silicon samples (figure 2.15b). This effect

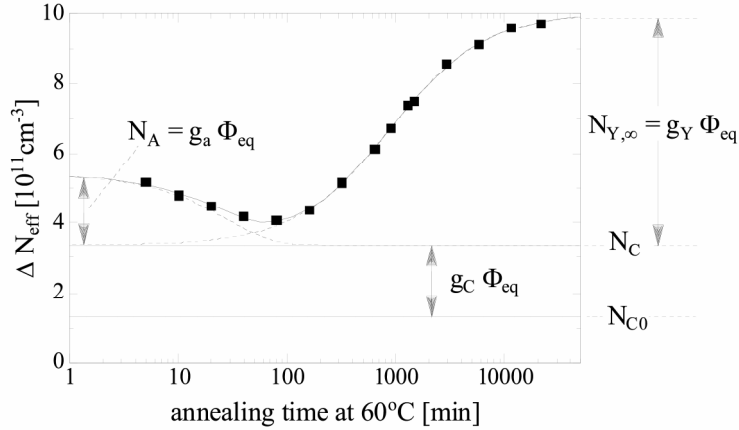


Figure 2.14: Parameterization of radiation damage and annealing effects in the Hamburg model [LEM99]

leads to a much lower effective charge density in oxygenated silicon after high dose irradiation with mainly charged hadrons in long term experiments not constantly cooled below room temperature (see figure 2.17). Sensors built from such material are expected to exhibit deeper depletion zones at the same bias voltage respectively full depletion at a lower bias voltage compared to sensors processed from standard high resistivity silicon.

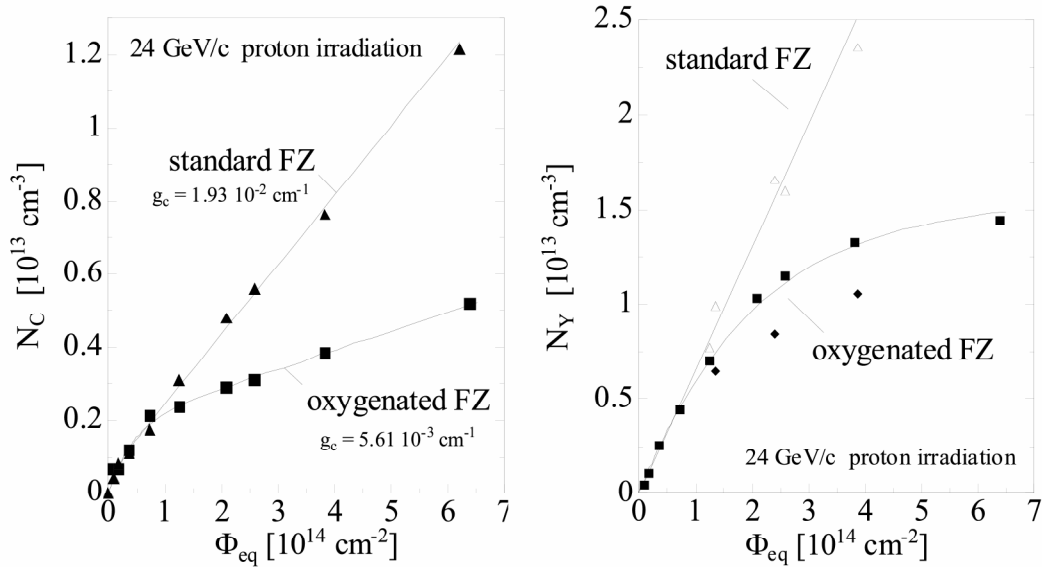


Figure 2.15: Comparison of a) constant effects (left) and b) reverse annealing effects (right) of proton irradiation in standard and oxygenated silicon [LEM99]

These results have been used within the ATLAS pixel collaboration to decide on using an oxygenated high resistivity substrate for the pixel sensor, as most irradiation damage close to the interaction point is expected to come from charged pions from hadronic jets produced in minimum bias events as given in radiation profiles in [KRA04a]. This would be different in regions of the radiation field farther from the interaction point, where the impact of non-ionizing particles (mainly neutral hadrons, especially neutrons) is proportionally big enough compared to charged hadron damage, to make the expected beneficial effect of oxygenation small compared to the overall depletion development.

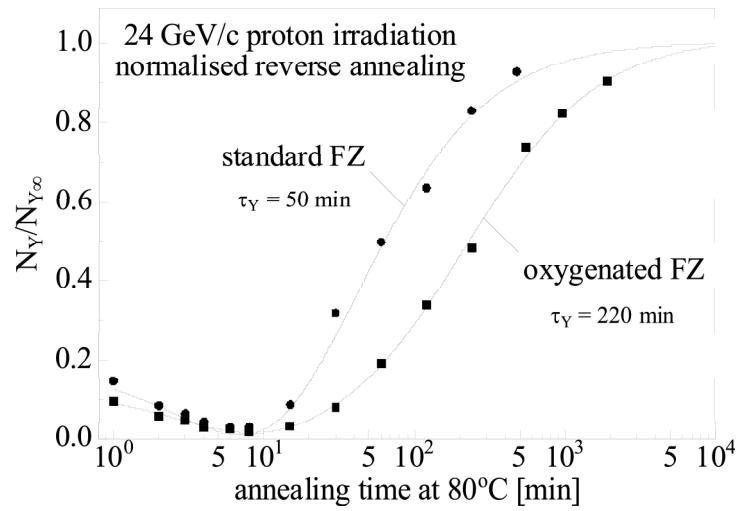


Figure 2.16: Comparison of annealing times of proton irradiation in standard and oxygenated silicon [LEM99]

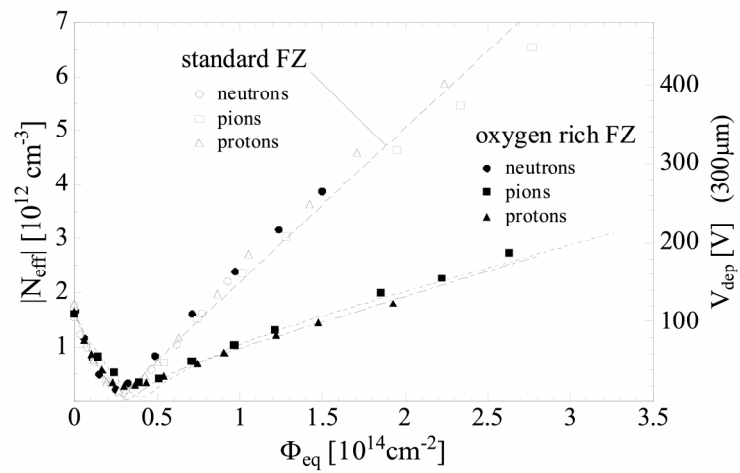


Figure 2.17: Effective charge densities in standard and oxygenated silicon after irradiation with neutrons or protons and controlled annealing steps [LEM99]

High resistivity silicon has been chosen from the start to minimize effects of uncontrolled bulk defects. Only detector grade silicon with low overall charge carrier concentration exhibits the necessary control of unwanted contamination with other trace material, of which some like carbon could be disastrous for long term radiation hardness and which would in any case render controlled damage engineering very difficult. High resistivity provides the sensor with easy to handle low bulk leakage current before irradiation. Together with the decision for n-type bulk material it allows for the technological design choices presented in the following section. The substrate type also postpones the rise of the effective doping concentration by the time needed for the radiation damage to convert the material to effective p-type.

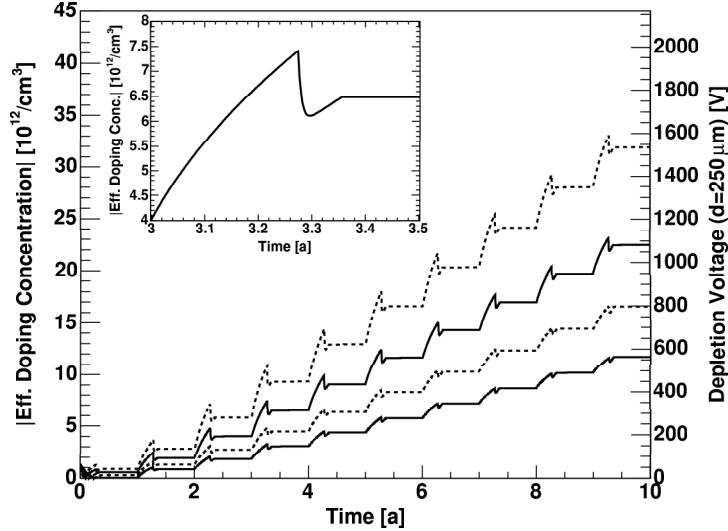


Figure 2.18: Change of voltage necessary for full depletion of sensors according to irradiation and annealing effects expected under the Hamburg model for the two inner pixel detector layers in a standard (solid) and elevated (dashed) radiation scenario [KRA04a]

The price to be paid for choosing a high resistivity substrate can be seen when contrasted with the depletion strategy of strip detectors at LHC experiments, where n-type substrates with higher depletion voltages are chosen. Their absolute effective charge concentration, due to the overall lower radiation exposure compared to the pixel detector, ends up after the full projected operation time at less than twice the starting value, having inverted to effective p-type between $(1 - 5) \cdot 10^{13}$ (1 MeV neutron equivalents)/ cm^2 [DEM02] [DIE03]. This allows for a constant bias voltage for the whole operation run. In the ATLAS pixel sensors at the other hand an early inversion of bulk type is expected, as the effective charge concentration starts out at around $8 \cdot 10^{11} \text{ cm}^{-3}$ and for a wafer thickness of $250 \mu\text{m}$ will invert to effective p-type at only around $(2 - 3) \cdot 10^{13}$ (1 MeV neutron equivalents)/ cm^2 depending on annealing [LEM99] [KRA04a]. Therefore operation in converted bulk type is to be taken into account as normal operation mode and a steady increase of necessary bias voltage from this point on, far beyond the specified voltage for unirradiated sensors, has to be assumed to keep operating at maximum depletion (see figure 2.18).

2.2.2 Pixel design

Within the conceptual process of which production process and sensor material to choose, one decision taken directly concerning pixel design is the doping type of substrate and structured implantations used for sensor processing. Taking into account advantages regarding process technology and radiation tolerance of using high resistivity n-type substrate, there are two possibilities to create both the pixel structure and the bipolar doping type junction necessary for depletion. The technological less demanding way to do this would be using a structured positive doped implantation (p^+) including pixel cells and a guard ring structure to minimize surface leakage currents. The opposite wafer side would then only need a planar high dose negative (n^+) implantation, calling for photolithographic mask processes performed only on one side of the wafer. There are two less than optimal aspects in this approach (see left half of figure 2.19). Firstly the bump bonds between sensor and electronics would be attached on the same side and very close to the guard ring structure. As the effective resistivity across the bulk edge is much lower than that of a guard ring structure, the biggest voltage drop on the surface of a biased sensor will occur on the latter, thus putting the surface area outside the guard ring to the sensor backside potential. The analogue ground of the front end electronics — and in a good approximation the slightly different pre-amplifier potential of the pixel contacts, too — exhibits a potential difference to the outside area equal to the full bias voltage of the sensor. The danger of shorts across the guard ring to the bump metallization or across the sensor-electronics gap would be quite high, especially if there was any condensing moisture within the detector volume.

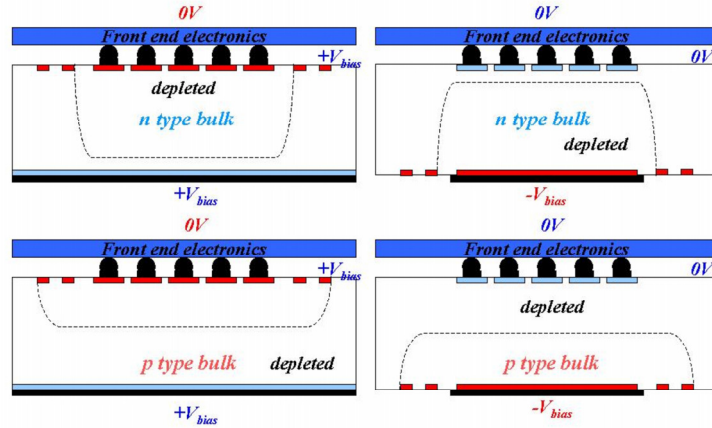


Figure 2.19: Comparison of p^+ -in-n (left) and n^+ -in-n (right) pixel sensors before (top) and after (bottom) type inversion

Another possible problem comes with changes of electric characteristics induced in the silicon bulk by irradiation. Above a certain deposited energy dependent on particle type [WUN92], irradiation damage in the silicon crystal will generate vacancies and interstitials raising the effective positive doping of the bulk material, an effect amplified by ongoing crystal change during reverse annealing. This switches most of the bulk silicon to effective p-type and alters the way the sensor depletes when bias voltage is applied. After type inversion the depletion zone does no longer grow mainly from the structured p^+ implants but can be approximated, while neglecting double junction effects, as growing from the backside n^+ implant (see right half of figure 2.19). If the effective doping concentration of the bulk material has increased beyond a certain point and full depletion is no longer possible with a given maximum bias voltage, the undepleted bulk zone will be situated around the pixel cells. In a configuration like this, charge collection would be deteriorated, as according to Ramo's theorem [RAM39] in small pixels most charge is induced by charge carrier motion close to the pixel contact (small pixel effect [KLA99] [KRA04a]), and even more problematic an undepleted current channel between the individual pixel cells would form, leading to high cross talk within the pixel array.

To avoid these problems a different design approach has been chosen for the ATLAS pixel sensor. The positive and the negative implanted wafer sides are both structured by mask processes for implantation, metallization and deposition of silicon oxide and nitride. This double sided processing creates the need for much more intricate and precise mask steps, especially incorporating front-to-back mask alignment in the order of few μm . But paying this price allows for a segmented n^+ implantation used for definition of pixel cells and a guard ring structure on the p^+ implanted wafer side, locating the main voltage drop on the sensor surface opposite to the bump connections, covered by a layer of high resistivity kapton foil. As the pixels are now realized as n^+ -in-n implantations, the sensor has to be fully depleted before type inversion to achieve full functionality, as the depletion zone will grow from the p^+ implanted backside. This can easily be achieved, as for a few hundred μm thick sensors processed on high resistivity silicon bulk ($(2 - 3) \text{ k}\Omega/\text{cm}$), full depletion occurs below or around 100 V, a bias voltage unproblematic for most sensors in terms of breakdown. After type inversion, the depletion zone now grows primarily from the segmented n^+ implantations into the bulk now converted to p-type, placing the pixel cell not only into the depleted volume, but into the region of the highest electric field, no matter how much of the bulk can be biased.

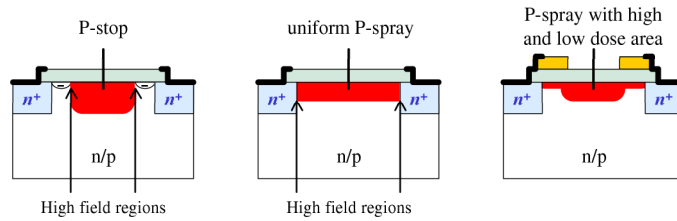


Figure 2.20: Comparison of inter pixel isolation technologies

When using a segmented n^+ pixel implantation in n-type bulk, another aspect of sensor technology has to be taken into consideration. Due to positive charges within the oxide layer, electrons in the neighbouring bulk region are drawn towards the interface, forming a layer of mobile charges functioning as a possible current channel even after full depletion. This situation prevents full electric isolation between the pixel cells and becomes considerably more pronounced after irradiation with ionizing particles creating more charge carriers within the oxide layer. To prevent these effects, an additional p-type implantation has to be added in between the pixel cells to interrupt the current channel formed by the electron layer. This can be done by adding a grid of p^+ implantations in the center of the inter pixel gaps (p-stop) or by implanting a low dose p-type layer over the whole sensor surface (see figure 2.20). But this technology would still have left a large part of the oxide interface in direct contact with the p-type bulk, leading to the forming of aforementioned electron layer. This layer of negative charge creates high electric fields where it touches the p-stop implantation, increasing with a growing electron density after ionizing irradiation of the oxide. This would lead to an increased likelihood of early sensor breakdown after irradiation [HÜG01], a tendency not viable for sensors to be used in a high radiation environment, including a high percentage of charged pions.

The covering of the whole n-side surface with a low dose p-implantation layer does prevent the forming of an electron layer at the interface, but brings the p-spray in direct contact to the n^+ implantation, again creating a high field region bound to increase the tendency of a sensor for electric breakdown. Fortunately, in this case the highest electric fields will occur in sensors with minimal ionizing radiation damage to the oxide interface, as the electron accumulation caused by interface charges lowers the effective p-spray dose [WÜS01]. So every sensor showing no early breakdown before irradiation can be expected to remain functional and even to improve in quality by raising the voltage of electric breakdown with increasing irradiation. This provides an excellent opportunity for quality assurance, making it possible to test produced sensors for electrical breakdown in their worst case state before irradiation. Processing p-spray sensors avoids an additional mask step necessary for p-stop implantation and lowers production cost.

The pixel isolation method finally chosen for the ATLAS pixel sensor uses the advantages of

2 ATLAS Pixel sensor

p-spray technology while minimizing the resulting production yield issues. In a moderated p-spray process developed at the Semiconductor Laboratory of the Max-Planck Institutes for physics and for extraterrestrial physics (MPI-HLL) [LUT97], the p-spray dose is regulated in an additional mask step, creating a slightly deeper high dose p-spray region in the center of the inter pixel gap and a slightly shallower low dose layer everywhere else. This method considerably lowers the electric field at the junction between p-spray and pixel implantation without lowering the effectiveness of the inter pixel isolation and has already been demonstrated to be intrinsically radiation hard [WÜS01] [HÜG01] [RIC02a].

The possibility to test sensors before assembly and irradiation for electrical characteristics in a state of operation, when the electrical field at the implantations is expected to be highest i.e. most prone to break down early, is of additional benefit in this design. Not only does sensor breakdown behaviour improve during bulk damaging irradiation, the design also allows for the implementation of a bias grid based on potential punch through to be used before assembly for current tests on the complete pixel array, thus providing a quality assurance tool to confidently declare a sensor functional from the very start.

3 Planning of quality assurance

3.1 Quality plan concept

The basic aim of quality assurance, no matter whether in physics experiments or in industrial production, is to assess the necessity of certain quality control measures in a given context and implement them into a context of planning and administration. While not always easy to differentiate in real life and not necessarily well-defined in literature, there are different important levels of quality assurance. To create an organizational framework helpful for achieving high quality output is usually described as quality management. Quality control in the strict sense are tests performed to gauge quality after the fact. But additionally, quality assurance can cover many aspects of planning and preparation to avoid possible problems or make them less likely to cause much harm. To optimize the effectiveness of quality control and incorporate it with advance planning within an organized production or operation, a quality plan has to be drawn up, defining the characteristics to be tested for and to analyze the effort needed and adequate to provide a representative picture of the production quality.

A way to systematize and quantify these processes used in commercial quality management is the FMEA (Failure Mode and Effect Analysis) [MAS94] [PFE01], a systematic, if not mathematically exact assessment yielding a quantitative index called risk priority number (RPN). This analysis derives a relative measure of importance for quality control by multiplying three key factors rated between 1 and 10 for the necessity and feasibility of testing.

The first factor and possibly the hardest one to define is one measuring the likelihood of occurrence O of a specific problem, roughly reflecting probabilities of certain production failures or material flaws ranging from close to 0 ($O = 1$) to close to 1 ($O = 10$). The difficulty arising here stems from incomplete knowledge of all the possibilities of malfunction, especially estimating correct probabilities in advance, when a new production step begins or a new production run of a manufacturer starts, with former prototyping or earlier runs, not representative of the new results, being the only available source of information. Thus, important possible sources of failure could be overlooked, if there have not been any pertinent earlier problems or if those causes were not easily extrapolated from theory and prior experience.

The second factor is a measure of the potential severity of a given problem with regard to the final functionality and security of a product — in this case the usability of the pixel sensor for module assembly and operation in the ATLAS detector. This is, while still not possible to exactly quantify, considerably easier to estimate than the likelihood of occurrence of the problem, as potential consequences of many production mishaps are well understood or at least documented in literature. In cases of largely undocumented problems, impact on later functionality can be assessed as soon as a new problem is first detected, as long as adequate means of testing are available. The numeric values for the impact factor I are rated between the extremes 'effects hardly noticeable in operation' yielding a 1 and 'complete breakdown of system function virtually guaranteed' yielding a 10 (a more elaborate, commonly used table of values can be found in [MAS94]).

Finally, a factor representing the inverse relative likelihood of early discovery D of the problem has to be determined — yielding $D = 1$ for a detection probability close to 1 and $D = 10$ for one close to 0. As the overall risk inherent in a production problem is eliminated by the discovery of faulty parts the canonical approach to this factor is just to quantify the likelihood of discovery. In the context of an elaborate and long running experiment in which most malfunctions will finally be discovered, but often late enough to cause considerable repair efforts or data loss, a rating prominently including the integration step during which the malfunctioning component can be identified can be justified.

The overall RPN computed as $RPN = O \cdot I \cdot D$ and ranging from 1 to 1000 is usually compared to a defined threshold value (125 being typical) to decide whether a specific problem has to be

3 Planning of quality assurance

confronted by changing production parameters or quality tests or can be left unchallenged. This threshold value is set arbitrarily and as — in addition to ambiguities caused by insufficient data — it is not clearly defined in the literature (e.g. [MAS94]) whether one step in the probability values O and D represents an equivalent increase on a linear or logarithmic scale of likelihood or something else entirely, RPNs themselves are relatively rough estimates. Within the unavoidable limits of comparability, reliable data do require experience over a long production period with a lot of the possible mishaps actually happening and containment plans to avert said problems being at least drawn up and practically projected, if not carried out.

Considering this, the relative quantification of the importance of quality assurance measures and the effectiveness of steps taken to control and optimize production quality as an RPN cannot be taken as an exact gauge for critical systems. But it can be used as a heuristic exercise to sum up possible problems theoretically known and procedures to avoid them and as an estimate of the urgency and feasibility of such measures. If nothing was known beforehand about the main trouble sources lowering production or assembly yield, further prototyping and engineering runs would be called for. If yield was generally high and the extent of possible complications caused by faulty parts was small compared to the effort of checking and fixing or replacing them, systematic quality control could be minimized in number and effort within a quality plan.

3.1.1 Necessity of quality assurance

In big physics experiments in general and especially in the ATLAS pixel detector this last conclusion cannot be made due to the two central aspects of complexity and accessibility of the system. In the case of sensors discussed here, a faulty sensor tile recognized after module assembly will render the whole module non-functional without a possibility of reworking, not only wasting electronic chips and module material, but also cost and time of the actual assembly process, and putting a strain on the project schedule and budget as additional, not planned for material has to be used and an increased workload has to be coped with. If a similar flaw was detected after incorporation in the mechanical detector superstructure, reworking of the assembly would probably be possible, but painstaking disassembly and re-alignment would be necessary to replace the faulty module. After the commissioning of the whole pixel sub-detector any further repair on a detector part will be prohibitively constrained. The central position of the sub-detector alone does not allow access without dismantling most of the other detector components — in the current baseline design this means opening the calorimeter and muon detector end-cap and removing the whole pixel detector including the part of the beam pipe around the interaction point. Even under the best of circumstances this would take a major effort and a prolonged pause in collider activity and data acquisition [ATL99a] [ATL97a]. In a typical case, after an integrated luminosity equaling a month or more of design luminosity operation, the material — especially the heavy metal absorbers in the calorimeters around the inner detector — will have been activated to a degree requiring a beam shut down followed by a cooling down period of no less than a day before a strictly controlled and limited access to the inner detector can be granted at all without severely endangering the health of those involved [ATL94].

Generally speaking all this is no more than an application of the economic rule of thumb for all large and complex industrial projects (given as a 'Rule of Tens' in [MAS94] and [PFE01] as in figure 3.1): the later in the design or production process a change has to be implemented the bigger the involved effort and the higher the cost in time and money. This increase is quantified at approximately one power of ten per production step a critical malfunction goes unnoticed, starting at a few cents during initial informal planning and going up to the full costs of the entire production after assembly and commissioning. In the special case of a the ATLAS pixel detector and in the light of the distinct needs mentioned above, this general rule is hard evidence for the economic and scientific necessity to make sure that every part used for detector assembly can be confidently assumed to be fully functional and to stay that way as long as possible during operation.

In commercial projects as well as in many scientific ones, much of the responsibility of providing functional parts can be outsourced to contractors by demanding in-house testing and prompt replacement or a contractual fine for the delivery of non-functional parts. For two reasons this

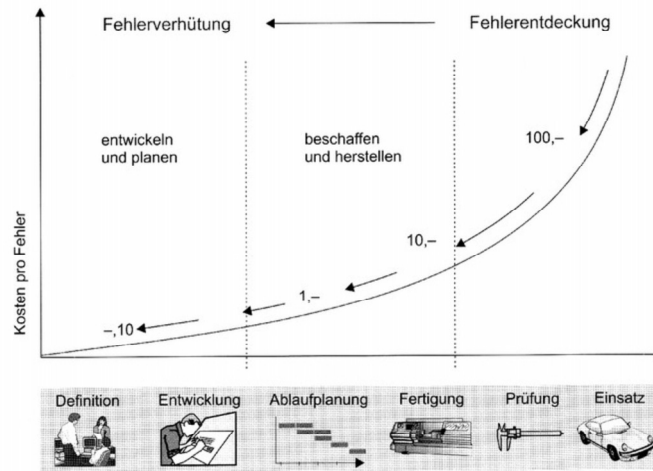


Figure 3.1: Illustration of the 'Rule of Tens' in industrial production from [PFE01]

strategy is only of limited help for the task at hand. On the one hand several of the used parts are of very radical design both in connection density and in radiation hardness, so that a contractual guarantee of functionality beyond some very precisely defined tests is unlikely to be available from any manufacturer. On the other hand, if a crucial part was to prove defective after assembly or even during operation, a fine or replacement could only alleviate the immediate monetary consequences. The loss of time, effort and most of all crucial physics data could never be replaced.

This puts the responsibility to investigate the most likely and gravest dangers to functionality on the physics collaboration, a task necessary because of the novelty of the used devices, which additionally offers opportunity for further insights in device physics and detector behaviour. From this information one can extrapolate test procedures which should be adhered to by the manufacturer or better still which can be used for in-house testing by the institutes involved. The latter possibility does not only provide confidence in the overall behaviour of the tested part concerning known process and assembly risks but allows for adequate reaction to until then unknown difficulties. Existing data sets can be compared for evidence pointing towards behaviour so far not included into quality considerations and testing activity can be stepped up or amended by new or improved procedures looking for new kinds of information likely to exclude faulty parts from further use in a detector assembly.

3.1.2 Aims of the quality plan

In the case of the silicon sensor tiles for the ATLAS pixel detector, planning for systematic quality assurance started already during the period of design development and extensive prototyping [HÜG01] from 1997-2000. Results of prototyping as well as testing procedures described in earlier publications ([HÜG97], [WÜS97], [ROH99], [WÜS01] and [BOR01]) have been used to formulate the technical specifications for tendering sensor production and implement the first systematic testing protocols with the start of pre-production in 2001. These have been continuously updated and amended since then, both to conform to the necessities of detector production and to reflect our increasing knowledge on the actual sensor manufacture and detector assembly processes.

From the start the procedures called for tests to be performed by both the four testing institutes within the ATLAS pixel collaboration. This has proven to provide an effective way for continuously monitoring and crosschecking the quality of the sensors, the correct application of the test procedures and the full functionality and comparability of the used test set-ups.

One specific aim of the quality plan defined early on has been the gathering of data relevant for sensor operation, if possible before any assembly steps are taken and in any case before a module bearing the sensor in question gets eligible for further integration. The main strategy used for

3 Planning of quality assurance

this has already been implemented in the design of the pixel wafers. It is important to test the individual sensor tiles early, directly gathering data on their behaviour before any other step of assembly but without mechanically probing the pixelated n-side surface, as it is prone to damage leading to an early electrical breakdown or problems with the metal deposition process for bump bonding. This has been made possible by the integration of a bias grid in the overall pixel design. The bias grid structure allows for simultaneous grounding of all pixel cells to a potential close to an external ground applied to a common n-side contact or even a p-side contact outside the sensor area guard ring.

Another central approach to keeping the potential damage to the pixel cells at a minimum has been the use of dedicated test devices custom designed for specific diagnostic tests. As the rectangular tiles are set side by side in the center of the production wafer, there is enough room for an array of test devices individually designed for quality control placed along the wafer edges (see figures 3.2a & b and 3.3), and can be accessed either on the complete wafer or after dicing and removing the sensor tiles on individual test sectors. These allow for easy monitoring of general parameters dependent on bulk material and process quality without any necessity to probe the sensors themselves. Only direct functionality tests are to be performed on the sensors themselves, using the sensors' bias grid and thus not having to probe the sensor pixel cells themselves.

The whole testing cycle is thus broken down in steps sorted by the time of testing as well as the nature of test devices illustrated in figure 3.4.

The first category represents tests performed directly on the central tile area of the wafer. These are intended to be performed before dicing, as they are to be used as the main selection criteria which tiles on which wafers should be diced and used for further assembly.

The second category encompasses all tests performed to check characteristics of a sensor wafer or production batch of wafers on the dedicated test structures of the outer wafer sectors before dicing. Together with the direct tile area tests these diagnostic tests should provide sufficient data to decide on the conformity of the delivered wafers with the design specifications and the functionality of the sensors. If these questions are decided positively, the sensors are considered preliminarily approved.

After bump deposition on the approved sensors and wafer dicing, additional diagnostic tests can be performed on the diced test sectors. These will include ones not deemed crucially important for judging functionality and conformity, but interesting concerning process monitoring as well as repeated tests to establish the effects of metal deposition and dicing and new testing routines additionally established later on.

A special case among after-dicing tests are measurements on irradiated structures, as these cannot be easily performed on whole sensor wafers, or at least render the tiles on the wafer in question useless for detector assembly. On diced test devices, including diodes and small sensors exhibiting a pixel design identical to the sensor tiles, wafers can be tested for behaviour after massive radiation damage without sacrificing any functional sensor tile so early in the production chain. Depending on the diagnostic quality intended to be checked for, irradiation is performed with middle to high energy protons for studies on bulk characteristics and low energy electrons for dedicated studies on interface damage.

There is a fifth category of possible tests not included within the original quality plan concept, but easily incorporated in practice. While the responsibility of the testing laboratories and the quality assurance coordinator originally ended with sending preliminarily approved wafers to the bump vendors and declare them finally approved after all additional testing on diced test sectors had been done, a more active role of collaboration with the bump vendors themselves has proved to be helpful. This has not been done with the same regularity as the standard sensor quality tests or production diagnostics. Only when deterioration of sensor quality was suspected, additional tests were initiated. Those have been thorough enough to draw systematic information on the impact of metallization and wafer dicing.

To make the information gained during assembly of the ATLAS pixel subdetector easily accessible to all involved, a data base for production sensor tests has been created based on and incorporated in a similar program created for the ATLAS semiconductor tracker (SCT).

The overall organization of measurements has been put in the hands of one person each at the collaboration ATLAS pixel laboratories. These people are charged with organizing the quality

3.1 Quality plan concept

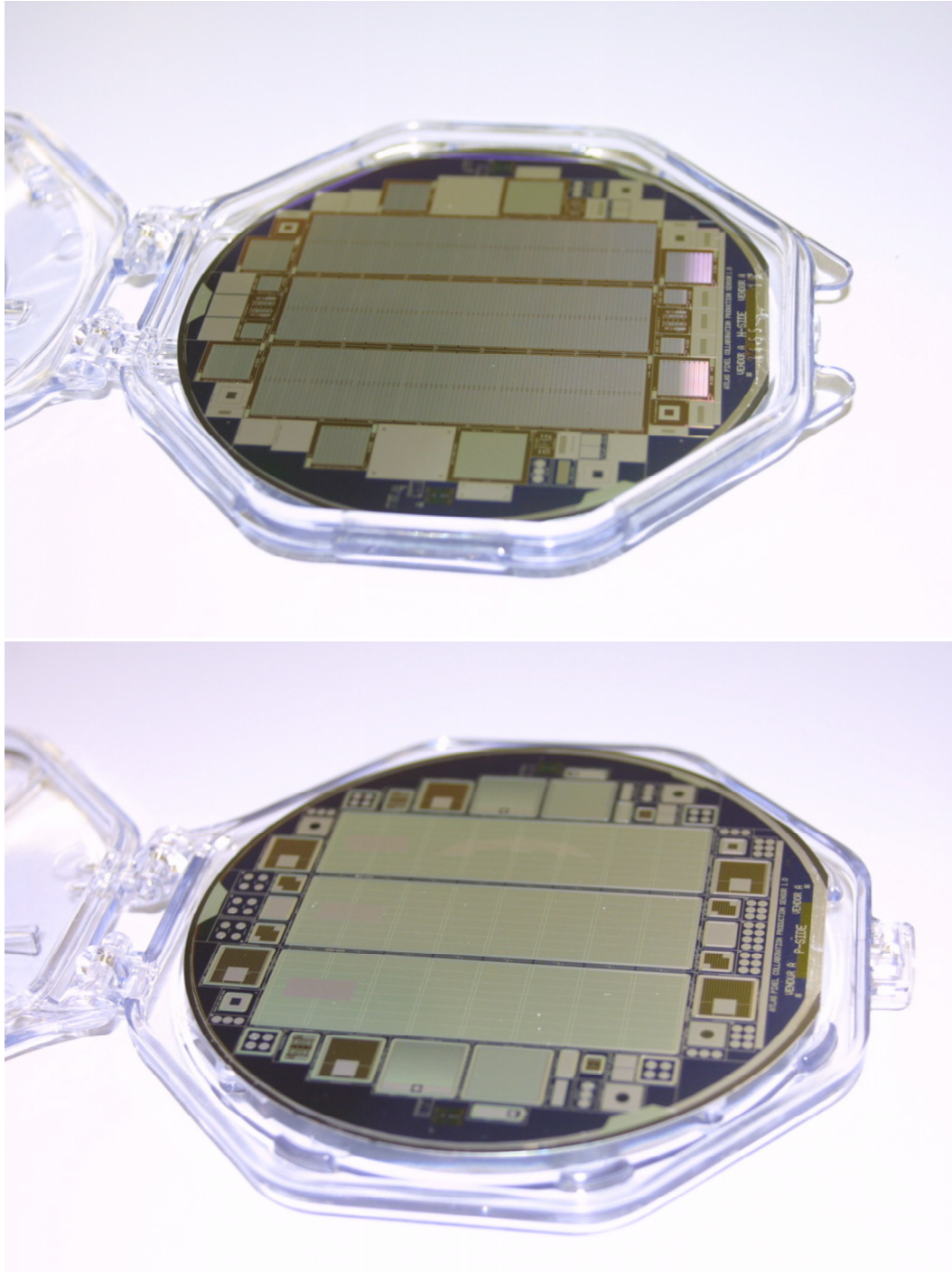


Figure 3.2: Production wafer seen from a) the n-side (top) and b) the p-side (bottom)

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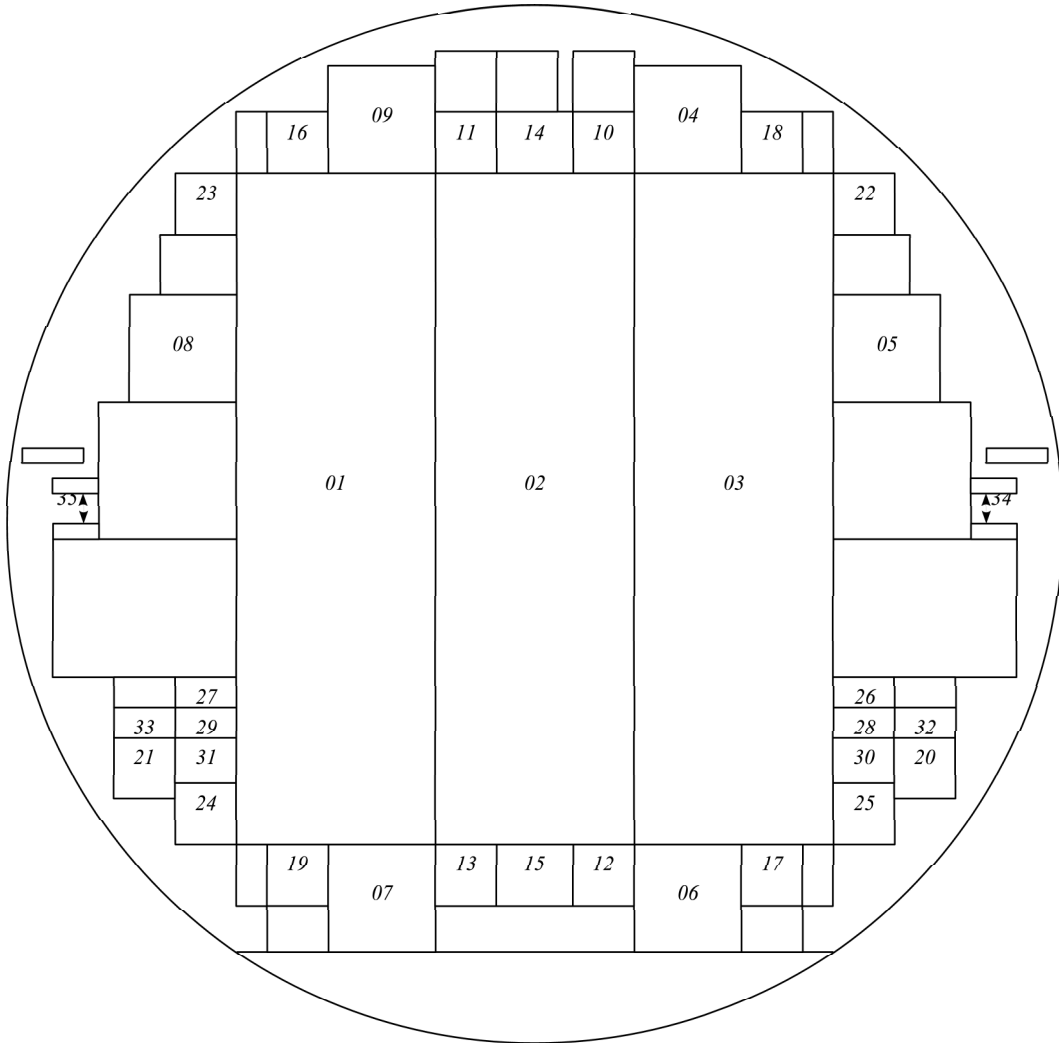


Figure 3.3: Map of wafer p-side with numbered structures:
01-03: sensor tiles 04-09: single chip sensors
10-13: mini chip sensors 14-15: inter pixel test structures
16-17: diodes with guard ring 18-21: ROSE type diodes
22-25: oxide test fields 26-27: n-side test structures
28-29: p-side test structures 30-31: breakdown monitors
32-33: p-side MOS arrays 34-35: mask alignment structures

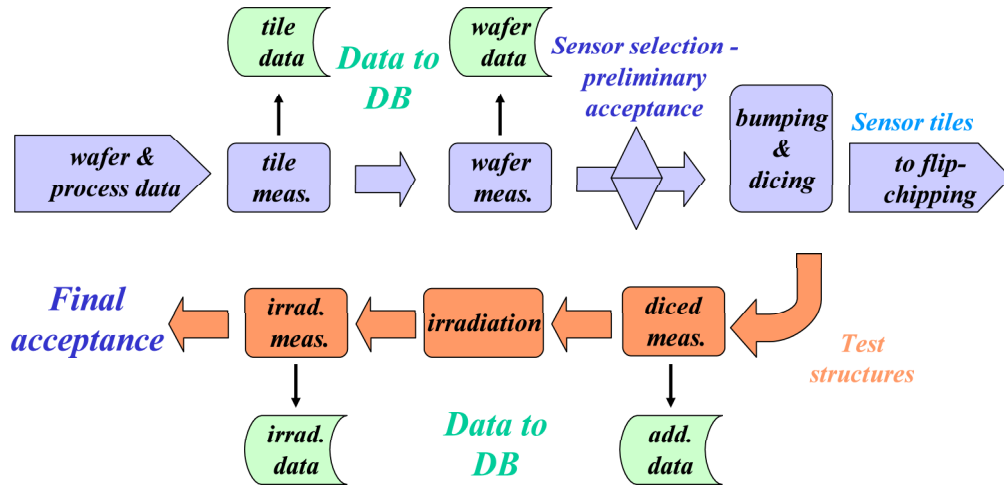


Figure 3.4: Flow of quality testing

tests, keeping track of them, archiving the measurement data and uploading them to the data base. In case of non-conformities of the delivered wafers or discrepancies with the data provided by the manufacturer, the responsible person documents the existing problems and informs the other collaborators and the contact person for the manufacturer. The quality assurance controllers from each laboratory give regular reports to the ATLAS pixel collaboration on problems, non-conformities or ambiguities having arisen during testing.

The central concept of the quality plan in terms of quality management is the provision of a positive feedback loop considering sensor quality (see figure 3.5). This allows for relatively quick detection of production problems and adequate intervention in a setting where aspects of the production process and its management cannot be directly controlled — a precondition for more inclusive quality tools as Total Quality Management (TQM) [PFE01]. So, as no direct influence can be taken on the production itself and the work and management processes at the fabrication sites, an iterative control process has to be implemented, yielding insight into the current sensor quality and the readiness for further production runs, testing for the continuity of production parameters and providing quick feedback on newly arising problems both to the ATLAS pixel group and to the sensor manufacturers. Going through the iterations of the feedback process, the ATLAS pixel group not only gets relevant data on the functionality of the delivered sensors and the ability of the manufacturers to start or resume production — both the production process and the testing routines can be checked and optimized, too. Thus, the likelihood of faulty production can be lowered and the probability of discovery for existing problems can be raised, systematically lowering the RPN for known problems throughout production.

3.1.3 Cross calibration concept

Aspects of cross calibration between the manufacturers and the collaboration laboratories are dealt with in a two-way approach. On the one hand most of the critical measurements are performed by the sensor manufacturers first and later repeated in more detail at one of the ATLAS pixel institutes,

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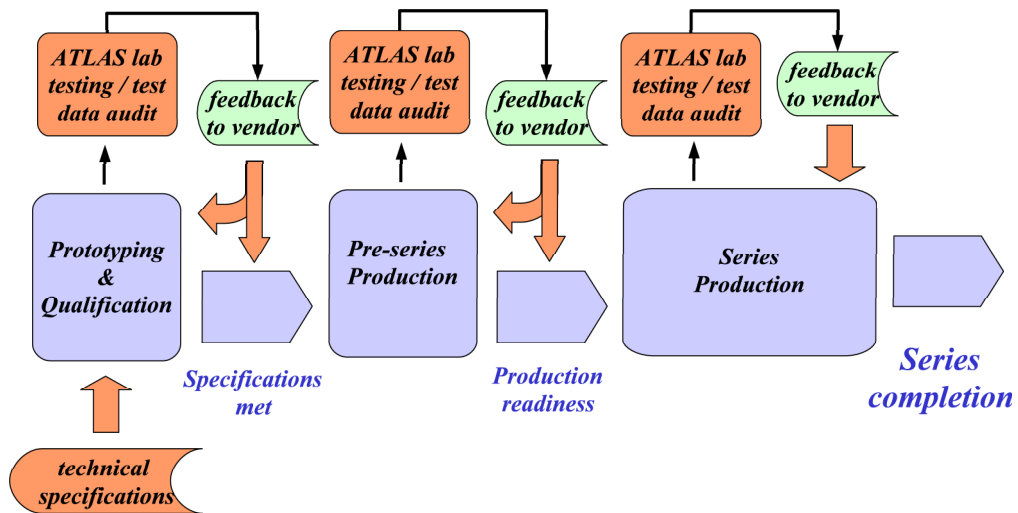


Figure 3.5: Information feedback for sensor quality optimization

providing the possibility of at least one cross-check for sensor quality on all tiles using completely independent set-ups. In addition to this, at the start of the pre-production phase diced samples and wafers were exchanged between the laboratories to test crucial measurement procedures and ensure comparable result in all participating laboratories. During the whole phase of production related tests, representatives of the collaborating laboratories meet on a regular basis. There, extraordinary test results are compared, and, whenever deemed necessary, the concerned wafers exchanged for independent crosschecking. As most of the sensor test data are uploaded into the production data base, the person responsible for quality assurance can directly check the local results against measurement data from other laboratories on wafers from the same vendor and the same production run without having to directly contact the other laboratories or wait for the upcoming meeting.

3.2 Choosing sensor characteristics

Besides general considerations when and by whom quality tests should be performed, the definition of the single tests has to be preceded by a decision, which of the possible parameters of the sensor wafers are important to know and using what kind of set-up on which type of device they can be tested in the easiest and most significant way. As usually the easiest and most sensor friendly measurement method is not necessarily the one yielding the most significant results, deciding the trade-offs to be made between the different ideals aspired to is often central to this problem. The parameters were chosen based on earlier studies on sensor development [HÜG97] [ROH99], the prototyping process [HÜG01], as well as general discussions during the tendering process for the sensor production. Given the facts that the ATLAS pixel sensor is an innovative and radical design prone to come down with problems unknown until then, and that the collaborating laboratories as well as the prospective sensor manufacturers are well equipped and staffed for all kinds of precision tests, the final selection of tests (given in table 3.1) turned out rather inclusive, preferring a very cautious approach within the FMEA.

A lot of the qualities tested are not directly gauged against any limits, but are monitored for later use, when needed for analysis of critical parameters, or for general monitoring of the production process, as this can be useful to notice manufacturing mishaps not immediately visible in cursory sensor inspections. A special case, too, are production parameters obtained from the sensor vendors and checked during wafer identification.

procedure code/ description	performed by	performed on	relevant quantity	criteria
SCR: scratch pattern mark- ing and wafer identification	vendor	every wafer	pattern as given	to be marked on three tiles and three single chips
			wafer thickness d in μm	$260\ \mu\text{m} \geq d \geq 220\ \mu\text{m}$
			resistivity ρ of substrate in Ωcm	$5000\ \Omega\text{cm} \geq \rho \geq$ $2000\ \Omega\text{cm}$
			oxide thickness in μm	to be monitored
			nitride thickness in μm	to be monitored
			substrate vendor and orientation	to be monitored
VIS: visual in- spection	ATLAS labs	every wafer	alignment on four alignment marks	yes/no on a scale of $2\ \mu\text{m}$ (one value for n- and p-side each)
			alignment of front marks to back marks	yes/no on a scale of $5\ \mu\text{m}$
			scratch pattern correctness	yes/no
	vendor and ATLAS labs	every wafer	visible damage	to be monitored
PLA: planarity measurement	ATLAS labs	one or more wafers from each batch	planarity sagitta σ_{pla} in μm	$\sigma_{pla} \leq 40\ \mu\text{m}$

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procedure code/ description	performed by	performed on	relevant quantity	criteria
IVD: I - V curve on diode with guard ring	vendor and ATLAS labs	every wafer	data in nA vs. V normalized for temperature	to be documented
			absolute breakdown voltage V_{bd} (absolute normalized current increases above 25 nA) in V	to be monitored
			absolute normalized operation current I_{op} at V_{op} from CVD in nA	to be monitored
	ATLAS labs	two diodes from each batch	absolute normalized current at -600 V depletion I_{600} in nA after p^+ irradiation with 10^{15} (1 MeV neq.)/ cm^2	to be monitored
CVD: C - V curve on diode with guard ring	vendor and ATLAS labs	every wafer	data in pF vs. V	to be documented
			absolute full depletion voltage V_{dep} in V	$30 \text{ V} \leq V_{dep} \leq 120 \text{ V}$ ($\leq 200 \text{ V}$ after p^+ irradiation with $3.1 \cdot 10^{14}$ (1 MeV neq.)/ cm^2)
			capacitance at full depletion C_{dep} in pF	to be monitored
			absolute operation voltage $V_{op} = \max(150 \text{ V}, V_{dep} + 50 \text{ V})$ in V	$V_{op} < V_{bd}$ from IVD
			resistivity ρ of substrate in Ωcm	$5000 \Omega\text{cm} \geq \rho \geq 2000 \Omega\text{cm}$
IVS: I - V curve on sensor (tile, single chip or mini chip)	vendor and ATLAS labs	every tile, some single chips and mini chips on each wafer	data in nA vs. V normalized for temperature	to be documented
			absolute breakdown voltage V_{bd} (absolute normalized current increases above $2 \mu\text{A}$ in tiles, 100 nA in single chips, 25 nA in mini chips) in V	$V_{bd} \geq V_{op}$ from CVD

3.2 Choosing sensor characteristics

procedure code/ description	performed by	performed on	relevant quantity	criteria
			absolute normalized currents I_{op} at V_{op} from CVD and I_{50} at $V_{op} - 50$ V in nA	current slope $I_{op}/I_{50} < 2$
	ATLAS labs	two mini chips from each batch	absolute normalized current at -600 V depletion I_{600} in nA after p^+ irradiation with 10^{15} (1 MeV neq.)/ cm^2 measured at $-10^\circ C$	$I_{600} \leq 800 \mu A$
BOX: I - V curve on oxide test structure	vendor and ATLAS labs	two wafers from each batch	data in nA vs. V	to be documented
			absolute oxide breakdown voltage V_{bd} (absolute current increases above 100 pA) in V	$V_{bd} \geq 50$ V
COX: C - V curve on oxide test structure	vendor and ATLAS labs	two wafers from each batch	data in pF vs. V	to be documented
			oxide capacitance in accumulation C_{ox} and minimal capacitance in inversion C_{min} in pF	to be monitored
			flat-band capacitance C_{FB} in pF calculated for mean temperature during measurement	to be monitored
			absolute voltage V_{FB} at C_{FB} in V	to be monitored
IVG: I - V_{gate} on gate controlled diode	ATLAS labs	two wafers from each batch	data in nA vs. V normalized for temperature	to be documented
			absolute normalized currents at 3 V below and above V_{FB} from COX I_{bot} and I_{top} in nA	to be monitored

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procedure code/ description	performed by	performed on	relevant quantity	criteria
			current rise around V_{FB} $I_{ox} = I_{top} - I_{bot}$ in nA	to be monitored
MFE: $I-V_{gate}$ on MOSFET struc- ture	vendor and ATLAS labs	two wafers from each batch	data in nA vs. V normalized for temperature	to be documented
			absolute threshold voltage V_{th} (ab- solute normalized current increases above 100 nA) in V	to be monitored
			approximate p- spray dose N_{ps} in 10^{12} cm^{-2} calculated from V_{th} and C_{ox} from COX	$2.2 \cdot 10^{12} \text{ cm}^{-2} \leq$ $N_{ps} \leq 3.5 \cdot 10^{12} \text{ cm}^{-2}$
PUT: $V_{pix}-V$ on punch-through structure	ATLAS labs	one wafer from each batch	data in V vs. V	to be documented
			absolute voltage drop at punch- through V_{pt} in V measured at V_{op} from CVD	$V_{pt} \geq 3V$
ITS: $I-t$ on sen- sor tile	ATLAS labs	one tile of one wafer from each batch	data in nA vs. s normalized for temperature	to be documented
			absolute normal- ized currents at 0 s and 15 h I_{start} and I_{end} in nA	current slope $I_{end}/I_{start} \leq 1.3$
THI: thickness measurement at wafer edge or thickness scan	ATLAS labs	one sample from each batch	thickness values d_1 and d_2 at two points or mean scan value d_m of sample in μm	$260 \mu\text{m} \geq d_x \geq$ $220 \mu\text{m}$
			approximate thickness uni- formity Δd in μm	$\Delta d \leq 10 \mu\text{m}$
IVP: $I-V$ on multi pixel structure	ATLAS labs	one sample from each batch	data in nA vs. V normalized for temperature	to be documented
			absolute linear threshold voltage V_{lin} in V	to be monitored

procedure code/ description	performed by	performed on	relevant quantity	criteria
			absolute normalized inter pixel currents at 0 V and V_{lin} I_0 and I_{lin} in nA	to be monitored
			inter pixel resistivity R_{pix} in $M\Omega$	to be monitored
CAP: $C-t$ or simple capacitance measurement on multi pixel structure	ATLAS labs	one sample from each batch	mean inter pixel capacitance C_{pix} in pF	to be documented
SRE: $I-V$ on test implantations and metallization layer	ATLAS labs	one sample from each batch for metallization, p- and n-implantations	data in nA vs. V (normalized for temperature for implantations)	to be documented
			absolute linear threshold voltage V_{lin} in V for all three cases	to be monitored
			absolute inter pixel currents (normalized for implantations) at 0 V and V_{lin} I_0 and I_{lin} in nA for all three cases	to be monitored
			sheet resistances R_{Sn} for n-implantation, R_{Sp} for p-implantation and R_{Sm} for metallization in Ω/\square	to be monitored

Table 3.1: List of sensor qualities tested for [KLA04]

3.2.1 Mechanical characteristics

The first category of relevant characteristics given does concern the wafer as a whole and can be described as macroscopic or mechanical properties of the sensor wafers. These are the thickness and flatness of the wafer itself and the visual characteristics of the surface structure.

The overall wafer thickness and the thickness uniformity are important for the assessment of charge deposition within the active sensor volume during detector operation as well as for the planning of the final set-up of detector modules within the pixel subdetector. To be able to set the planned amount of detector modules including the necessary cooling, cabling and support within the very limited space available — and thus allowing for the necessary coverage of the pixel detector — all components have to fit within a tight envelope (see figures 3.6 & 3.7). Wafers of a thickness significantly higher than the $250\ \mu\text{m}$ planned for do thus not only increase the overall

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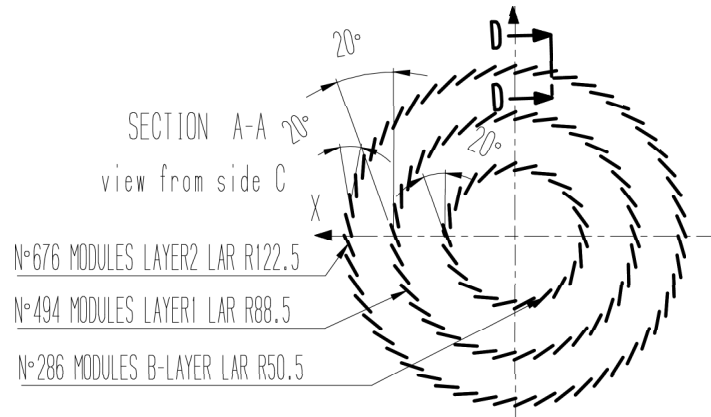


Figure 3.6: Section showing planned orientation of barrel modules [EDM04]

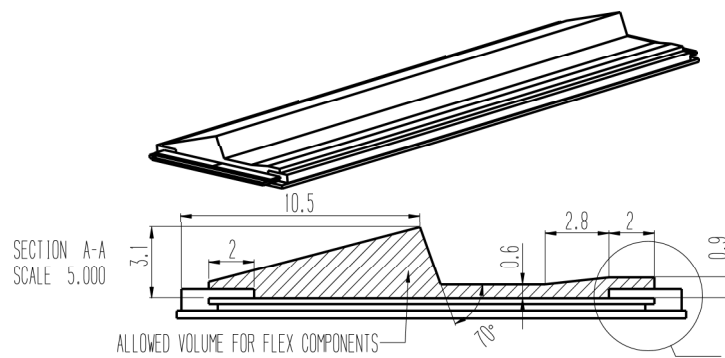


Figure 3.7: Planned module envelope for the pixel sensor set-up [EDM04]

material budget of the innermost subdetector and, more importantly, the probability of multiple particle scattering creating great difficulties for track reconstruction, they prove to be unusable from a strictly geometric point of view, too. The potential problems of wafers slightly thinner than specified, creating a lower mean signal height per particle track, are deemed to be less dramatic. Besides increased fragility during assembly only a slight decrease in the expected mean particle signal is expected. As long as the front-end pre-amplifiers work according to specifications, ionizing high energy particle tracks (assumed to be MIPs i.e. Minimum Ionizing Particles) should still be easily above threshold and within an acceptable time walk for a 25 ns bunch crossing interval (for a discussion of time walk behaviour see [ATL98] and [STO04]). This is quite important, as after a certain amount of high fluency bulk irradiation and the effects of reverse annealing (after (4–6) years of projected ATLAS operation for the innermost b-layer) the sensor bulk is expected to not be fully depleted anymore at a operation bias 600 V, thus decreasing the active sensor volume and effectively creating a thinner sensor with lower signals (discussed in [KRA04a]). The tolerances taken from these considerations lead to the acceptance of wafers with a thickness $230 \mu\text{m} \leq d \leq 260 \mu\text{m}$ and a maximum thickness variance of $\Delta d \leq 5 \mu\text{m}$. The latter criterion has been added to avoid possible difficulties with non-uniform tiles during flip-chipping and excessive errors in gauging necessary bias voltage for full depletion or expected signal height within one tile.

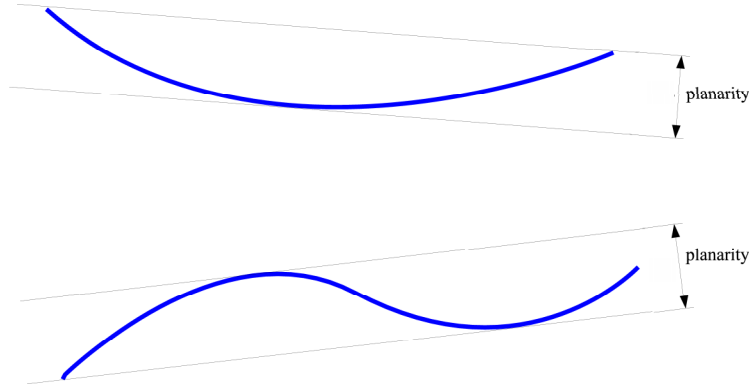


Figure 3.8: Definition of planarity value simplified to two dimensions

The planarity of the sensor wafers and its influence on the tile geometry has to be considered mainly concerning the flip-chipping of the front-end electronics. While the manufacturers eligible for performing bump deposition and assembly of bare modules have not been able to give hard limits for tile bow, beyond which their respective flipping processes would become unreliable, an excessively twisted or bowed sensor could clearly compromise the alignment of front-end chips on the sensor or — if a sensor was straightened on a vacuum chuck during assembly and released afterwards — create damaging stress on both the bump bonds and the bulk crystal. As the analysis of different types of bow and twist would add additional parameters to be kept track of, without having any known specific effect, an overall measure of planarity has been opted for. This value has been defined as the minimum distance between two parallel planes enveloping all measured points in a surface scan covering the tile area of the wafer (illustrated in figure 3.8). The limit imposed, a number all prospective bump bond vendors claimed to be comfortable with, was $40 \mu\text{m}$.

Visible quality of processing has been added as a characteristic both very basic and very complex. Its importance for the later processing of tiles can be illustrated by comparing the dimensions of the relevant sensor structure with typical sources of surface problems. The bump pads on the sensor ($12 \mu\text{m}$) and the bump diameter ($25 \mu\text{m}$) are equal in size or smaller than macroscopic fibers or droplets (some $(10 - 100) \mu\text{m}$). Likewise, the typical depth of scratches inflicted by probing needles or metal tweezers can well exceed the thickness of the oxide (150nm), nitride (100nm), passivation (500nm) or metal ($1 \mu\text{m}$) layers. Besides the need for careful handling of the sensors, avoiding unnecessary probing and providing a clean room environment for all handling before sensor hybridization, this documents the necessity to inspect especially the n-side pixel cells and the p-side

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guard ring structure for residue or dust hampering the contacting of the bump pads or scratches damaging important sensor areas. An additional consideration is the possibility to check for the quality of mask alignment, as up to five structured masks for each sensor side have to be used and to be properly aligned. The critical limit for misalignment are the dimensions of the bias dots integrated in the pixel cells. As these exhibit gap widths of $5\ \mu\text{m}$ between dot implantation and pixel implantation and dot diameters of $10\ \mu\text{m}$, a tolerated alignment difference of $\Delta a \leq 2.0\ \mu\text{m}$ for each wafer side and $\Delta a \leq 5.0\ \mu\text{m}$ between p-side and n-side has been defined.

Another task of quality control not directly connected to a single measurement, but relevant for the assessment of the whole wafer is the monitoring of production information. The data provided by the sensor manufacturer have to be checked for completeness and consistency and the identity of the single wafers verified by using wafer stamps, scratch patterns on the edges of the individual sensors and statements in the manufacturers' shipping information.

3.2.2 Bulk characteristics

The electrical characteristics of the silicon bulk material are the ones most obviously and directly affecting overall sensor performance. Electrical bulk behaviour is monitored closely for all sensors, as any anomaly in these characteristics indicates changes in sensor performance, in the best case altering the operation parameters to be chosen for the sensor, in other cases even rendering it completely inoperable as particle detector components.

Depletion voltage of the sensor bulk should not only be known for immediate application when determining detector operation parameters, but constitutes a diagnostic value to test bulk resistivity of the unirradiated sensors, reflecting substrate purity, and to test for effects of irradiation and annealing on bulk depletion, indicating the use of oxygenated silicon. This characteristic can be derived from the capacitance-voltage dependence of diodes and diode arrays, by using the capacitance change levelling out when full depletion is reached and the depletion zone can not grow any further. The appropriate limits can be derived from the acceptable values for wafer thickness and substrate resistivity ρ (see above). This is done by combining the expression for the depletion depth in semiconductors for a highly asymmetric p⁺-n junction

$$d = \sqrt{\frac{2 \cdot U_{bias} \cdot \epsilon_{Si} \cdot \epsilon_0}{e \cdot N_{eff}}} \quad (3.1)$$

(U_{bias} being the absolute reverse bias voltage, $\epsilon_{Si} = 11.75$ the permittivity of silicon [DIN82], $\epsilon_0 \simeq 8.854 \cdot 10^{-12}$ As/Vm permittivity of vacuum and $e \simeq 1.602 \cdot 10^{-19}$ C the absolute electron charge [PDB00]) with the dependence of the bulk resistivity concerning effective charge carrier concentration N_{eff} under the assumption of effective carrier concentration consisting only of shallow traps ionized regardless of bias at room temperature (a realistic approximation in not irradiated high resistivity silicon; for a more exact model for silicon containing a significant amount of deep donors or acceptors before or after irradiation, see [ERE95] [KRA04a])

$$\rho = \frac{1}{e \cdot \mu_e \cdot N_{eff}} \quad (3.2)$$

($\mu_e \simeq 1450$ cm/Vs being the electron mobility in silicon [LUT99]).

This yields

$$\rho = \frac{d^2}{2 \cdot V_{dep} \cdot \mu_e \cdot \epsilon_{Si} \cdot \epsilon_0} \quad (3.3)$$

for full depletion, i.e. $U_{bias} = V_{dep}$. The resulting tolerances for intrinsic high resistivity sensors exhibiting $2000\ \Omega\text{cm} \leq \rho \leq 5000\ \Omega\text{cm}$ are $30\ \text{V} \leq V_{op} \leq 120\ \text{V}$ before radiation.

Under irradiation of sufficient particle mass and energy to induce damage in the crystal structure of the silicon bulk (see [WUN92] for discussion), the charge concentration within the sensor will change, as both positively charged shallow defects and deep defects potentially working as either donors or acceptors are created, and will change by annealing processes — thermally induced

3.2 Choosing sensor characteristics

transformations of lattice defects — over time. For an approximate calculation of the resulting effective charge concentration a field-independent mean value is assumed, instead of considering deep donor and acceptor states dependent on the electric field and field-independent shallow acceptors separately. This allows for an approximation only depending on equivalent 1 MeV neutron fluence Φ_{eq} of the irradiation, irradiating particle and irradiated bulk type, and annealing time t normalized for annealing temperature T_a given in the Hamburg model as

$$N_{eff} = |(N_D - N_A)| \simeq |N_{eff0} + N_C(\Phi_{eq}) + N_a(\Phi_{eq}, t(T_a)) + N_y(\Phi_{eq}, t(T_a))| \quad (3.4)$$

Here, the initial value N_{eff0} of n-type silicon provides donors and equals the donor density N_D , while the constant damage term N_C and the long term annealing term $N_y \propto (1 - e^{-t/\tau_y})$ with a time constant τ_y introduce acceptors, thus contributing positively to the acceptor density N_A and therefore having to be parameterized with a negative sign. The short term annealing term $N_a \propto e^{-t/\tau_a}$ with a time constant τ_a finally reduces acceptors and has to carry a positive sign (see figure 2.14). Characteristic constants for N_C and the terms representing annealing in the Hamburg model depend on the particles used for irradiation as well as bulk characteristics influencing the defect dynamics, as seen in figures 2.15 - 2.17, and are discussed in more detail in [LEM99] and [KRA04a], where more exact expressions for the individual terms of the Hamburg model are given as well.

As all of the empiric values within the Hamburg model are derived from capacitance measurements on irradiated sensors, extrapolated values of N_{eff} for oxygenated silicon according to the model can be compared to capacitance tests on diodes from production wafers irradiated to a known fluence. Any major discrepancy between these values would point towards unexpected properties of the bulk material, in the case of high measured values after irradiation with charged hadrons usually a lack of oxygen or surplus of carbon is indicated, both potentially devastating to long-term detector operation in ATLAS environment. Thus, tests on diodes irradiated with middle to high energy protons to $\Phi_{eq} = 3.1 \cdot 10^{14}$ (1 MeV neutron equivalents)/cm², a fluence at which sufficiently oxygenated sensors after short annealing periods should still deplete completely below $U_{bias} \leq 200$ V, have been implemented. The necessary irradiation runs are performed at the cyclotron of the Lawrence Berkeley National Laboratory (LBNL) with 55 MeV protons and at the Proton Synchrotron (PS) irradiation facility at CERN [SSD04] using 24 GeV protons.

Bias tolerance is the core of sensor quality testing, having to be performed on each sensor, as small irregularities of each sensor's surface structure can lead to high local fields inducing early avalanche breakdowns. In the case of more dramatic interface damage, the breakdown will even occur at bias voltages just depleting the bulk next to the surface [HÜG01]. In both sensors and test diodes with an n-type bulk, the expected dominant factor in dark leakage current in the absence of a breakdown is volume generation current of the bulk, which can be treated for reverse bias as [LUT99]

$$I_{bulk} = A \cdot e \cdot \frac{n_i}{\tau_g} \sqrt{\frac{2 \cdot \epsilon_{Si} \cdot \epsilon_0 (N_A + N_{eff})}{e \cdot N_{eff} \cdot N_A}} (\sqrt{U_c + U_{bias}} - \sqrt{U_c}), \quad (3.5)$$

A being the cross-section area of the depleted volume (usually defined by guard ring geometry), U_c the built-in contact potential between the p⁺ implantation and the intrinsic n-type bulk n_i the intrinsic charge concentration and τ_g the generation lifetime. For highly doped implantations — leading to $N_{eff} \ll N_A$ — and bias voltages $U_{bias} \gg U_c \approx 0.5$ V, this can be simplified to

$$I_{bulk} = A \cdot e \cdot \frac{n_i}{\tau_g} \sqrt{\frac{2 \cdot \epsilon_{Si} \cdot \epsilon_0}{e \cdot N_{eff}}} \sqrt{U_{bias}}. \quad (3.6)$$

Obviously, depletion depth can never be increased past total bulk thickness, rendering the above expressions valid only for $U_{bias} \leq V_{dep}$. After full depletion has been reached, bulk current in an ideal silicon diode of bulk thickness d_b saturates at

$$I_{bulk} = A \cdot e \cdot \frac{n_i}{\tau_g} \sqrt{\frac{2 \cdot \epsilon_{Si} \cdot \epsilon_0}{e \cdot N_{eff}}} \sqrt{V_{dep}} = A \cdot e \cdot \frac{n_i}{\tau_g} \cdot d_b. \quad (3.7)$$

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As the diodes and sensors to be tested are obviously not ideal ones, two other effects besides volume generation current and avalanche breakdown have to be taken into account. One of them is the interface generation current induced by defects on the oxide-bulk interface leading to an elevation of interface recombination velocity. This additional current only becomes relevant if there is a significant area of interface between the oxide and the bulk itself as opposed to high dose implantations, and if those interfaces are depleted. The latter happens when the potential difference between the bulk below the interface and a gate atop the oxide — usually a metal layer — more than offsets the contact potential of the oxide-silicon interface as well as the potential induced by positive oxide charges, thus lies above the so-called flat-band case, but does not become large enough to accumulate minority charges, which could isolate the interface from the bulk. (The characterization of interface behaviour is discussed in the following sections and in more depth in [WÜS01].) Because of this interface generation current is only to be expected in devices exhibiting direct oxide-bulk interfaces on the n-side, and can be easily spotted as a steep but limited increase in leakage current at a field configuration consistent with flat-band conditions.

A more dominant contribution are ohmic currents. These can stem from the bulk itself, as even fully depleted silicon has a not completely negligible ohmic conductivity. This should be very small in the case of detector grade high resistivity material, but can be increased by micro cracks created by physical stress during production, shipping, testing or assembly. Another source of ohmic behaviour are defects in or conductive residue on top of the guard ring structure, creating an ohmic resistive channel parallel to the diode.

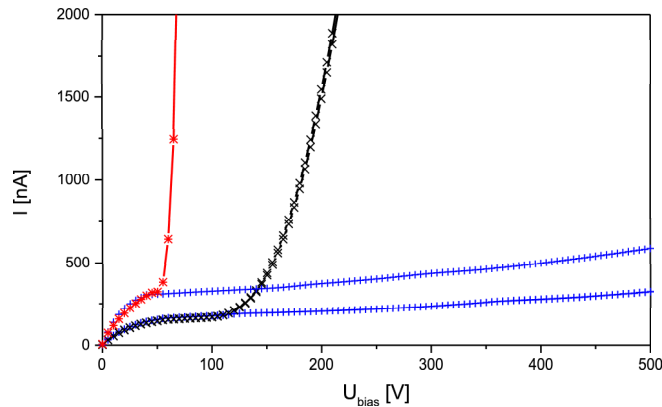


Figure 3.9: Current vs. bias curves from various sensor tiles showing a combination of volume generation current, ohmic currents and avalanche breakdown at and above full depletion

Thus, on unirradiated sensors high currents, whether caused by ohmic behaviour, interface generation current or a beginning avalanche breakdown point towards problems concerning crystal purity, initial interface defects, guard ring effectiveness and inhomogenities in the electrical field. The criteria defined for sensor leakage currents for the unirradiated sensor are thus two-fold. At the initial operation voltage (or smaller bias voltages), dark current has to stay below $2.0 \mu\text{A}$ at room temperature (293.15 K) for a full sensor tile, about twenty times the value derived for a high resistivity sensor exhibiting volume generation current exclusively [HÜG01]. This value can be scaled by approximated depleted volume for smaller test structures like small sensors or diodes. The initial operation voltage — although in most cases given as a positive number usually applied as a negative potential on the p-side contact — is usually defined as $V_{op} = 150 \text{ V}$, in cases of low bulk resistivity leading to high voltages for full depletion (V_{dep}), it is calculated instead as $V_{op} = V_{dep} + 50 \text{ V}$, if this value is higher. To avoid sensors exhibiting good leakage current levels up to V_{op} , but already in the process of slow breakdown at this point, the slope of bias dependent leakage current $I(V)$

3.2 Choosing sensor characteristics

below operation voltage has to conform to the criterion $I(V_{op})/I(V_{op} - 50 \text{ V}) < 2.0$.

After irradiation with particles massive enough and with high enough energy to cause defects in the silicon crystal lattice, the overall bulk resistivity of the sensor will decrease after an initial increase at low fluences, and one of the main causes for breakdown — high electric fields between p-spray layer and pixel implantations — will gradually lessen as explained above. So, the occurrence of earlier breakdown (or breakdown due to anything but severe interface damage) is unlikely [HÜG01], although the general level of bulk leakage current will rise. This rise can be scaled by NIEL (Non-Ionizing Energy Loss) scaling, i.e. expressed as proportional to an equivalent fluence of 1 MeV neutrons, and thus parameterized as [WUN92]

$$\Delta I_{bulk} = A \cdot d \cdot (\alpha_n \cdot \min(\Phi, \Phi_{inv}) + \alpha_p \cdot \max(0, \Phi - \Phi_{inv})), \quad (3.8)$$

$\alpha_n = 8.0 \cdot 10^{-17} \text{ A/cm}$ being the proportional factor at room temperature before bulk type inversion at Φ_{inv} , and $\alpha_p = 9.8 \cdot 10^{-17} \text{ A/cm}$ after inversion [WUN92]. So the overall current after irradiation can be expressed as

$$I_{bulk} = A \cdot \left(e \cdot \frac{n_i}{\tau_g} + \alpha_n \cdot \min(\Phi, \Phi_{inv}) + \alpha_p \cdot \max(0, \Phi - \Phi_{inv}) \right) \sqrt{\frac{2 \cdot \epsilon_{Si} \cdot \epsilon_0}{e \cdot N_{eff}}} \sqrt{\min(U_{bias}, V_{dep})}. \quad (3.9)$$

The annealing behaviour of volume generation currents does not exhibit the same effects of damage engineering as annealing of charge density [LEM99]. For both standard float zone silicon and DOFZ silicon, there is a short term drop $\Delta\alpha \propto e^{-t/\tau_i}$, bringing the proportional constants approximately to $\alpha_n \approx \alpha_p \approx 4 \cdot 10^{-17} \text{ A/cm}$ [WUN92] after several days at room temperature, combined with a slight rise $\Delta\alpha \propto \ln(t/t_0)$ dominant for long annealing times [MOL99].

Not only electrical breakdown and manufacture problems, but high currents, too, can have an impact on sensor operation. While they do not in themselves prevent the application of sufficiently depleting bias, the additional current adds significantly to the generated heat having to be managed by the cooling system, and to the current noise level forcing the front end thresholds to be set to higher levels, potentially pushing the typical time walk of particle transitions above 25ns. Therefore for irradiated sensors (which can be assumed not to exhibit an electrical breakdown if not doing so before irradiation), the main leakage current criterion is directly derived from the amount of cooling per area projected as manageable for the detector cooling system. The corresponding limit at the highest planned bias $U_{bias} = 600 \text{ V}$ is $I_{600} \leq 100 \mu\text{A/cm}^2$ of active surface at 263.15 K [ATL98], scaling for a full tile surface and a negligible part of sensor leakage current into the guard ring or the bias grid (thus allowing for temperature scaling as bulk current) to approximately $I_{600} \leq 2.2 \text{ mA/cm}^2 \approx 22 \text{ mA/tile}$ at room temperature. To measure this under conditions similar to detector operation without having to irradiate good sensor tiles, tests are performed on mini sensors and diodes with 6.6 mm² after irradiation with the full design fluence of $\Phi_{eq} = 1 \cdot 10^{15} \text{ (1 MeV neutron equivalents)/cm}^2$ active surface at 263.15 K, with a maximum current scaled to $I_{600} \leq 36 \mu\text{A}$.

Stability of leakage currents is an important third topic in bulk characterization, as the leakage current values tested for can only be considered as indicative of long term detector behaviour, if no dramatic change in current can be shown for constant biasing over longer periods. For the most problematic aspect of current stability, the increase of current by higher temperatures in irradiated sensors, in turn rising current, can be countered. This thermal runaway behaviour is to be held in check by sufficient cooling of the detector modules. Sensors are already tested by the irradiation tests mentioned above to be thermally manageable within the detector cooling system, as long as the electronic chips on the module adhere to the set thermal budget, too. This leaves us with possible problems already apparent in sensors without irradiation bulk damage, namely unstable field configurations within the bulk, and the generation of current channels across the guard ring structure. As a full measurement of even a small sample of tiles for several days or weeks, as necessary to simulate stability during initial operation, would go beyond the possibilities of any of the testing laboratories, thus potentially increasing the necessary effort in the quality assurance equation overproportional to the expected benefit. So a relatively short measurement period of 15 h at room temperature and operation bias $U_{bias} = V_{op} = \max(150 \text{ V}, V_{dep} + 50 \text{ V})$ has been incorporated within the quality plan, possible to perform during nights between testing

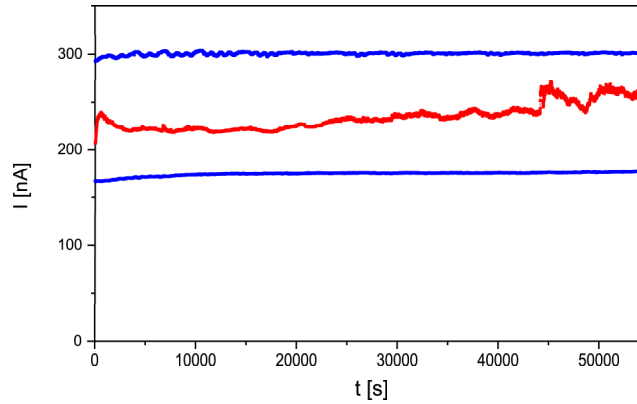


Figure 3.10: Current vs. time curves at $U_{bias} = 150$ V showing cases of stable current saturation as well as one case of erratic overshoots

shifts. Fortunately a period of several hours already yields valuable results, as observed during early prototyping (similar to results presented within chapter 4). While looking at the overall behaviour of the current vs. time curve (see figure 3.10) gives a good indication of leakage current stability, the specified upper limit for current increase during the test interval is defined by the ratio of final and initial current $I_{end}/I_{start} \leq 1.3$, leaving enough space for minor thermal effects and saturation processes due to mobile space and interface charges reaching equilibrium.

3.2.3 Interface characteristics

As the structuring of the sensor diode array involves several layers, whose properties will influence the performance and stability of the pixel sensor, at least some of them have to be investigated to guard against malfunctions of the sensor.

The oxide layer is situated directly on top of the sensor bulk isolating the latter from the metallization where no electrical contact is needed. As a shorting of bulk and pixel implantations to a common metal layer can mean a deterioration of spatial resolution, a rise of noise or a complete loss of signal with influenced charge directly fed into a voltage supply contact, the absence of pinholes in and the voltage stability of the oxide is critical for detector operation. SiO_2 being an excellent isolator, the expected voltage vs. current characteristic for a high quality oxide layer of around 100 nm thickness should be consistent with zero, showing only the fluctuations of the test set-up. A sharp increase in current means a breakdown of the oxide and thus a clear fail. In many cases of real test devices with metallized oxide layers on top of an undepleted silicon bulk, a slow steady rise of current might be observed (see figure 3.11), pointing towards an ohmic current channel across non-metallized surface, which, if of sufficiently low resistivity, can pose a problem too. To take into account both possibilities, the current has to conform to $I \leq 100$ pA for a MOS pad with an area of $A_g \approx 1.8$ mm² at least up to a potential difference of 50 V. As the actual potential drop across the oxide layer should not exceed values around 20 V, this is clearly on the safe side.

The capacitance of the oxide layer and the depletion layer forming below a metal-oxide gate interface are no critical properties of the sensor in themselves, but a necessary input for the assessment of other tests and indicative of parameters in wafer processing important for sensor production. The oxide capacitance can be measured on a simple metallized oxide with a defined area, as the underlying undepleted bulk does not function as a capacitance, and the oxide-bulk interface does neither, as long as it is accumulated with free electrons drawn towards positive oxide charges at the

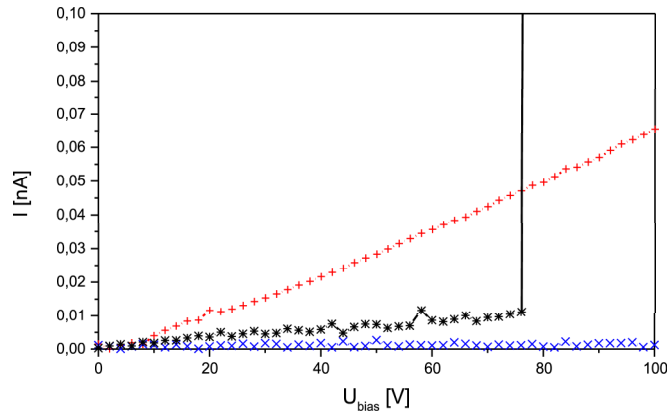


Figure 3.11: Current vs. bias curves on good and problematic MOS test devices showing different types of behaviour

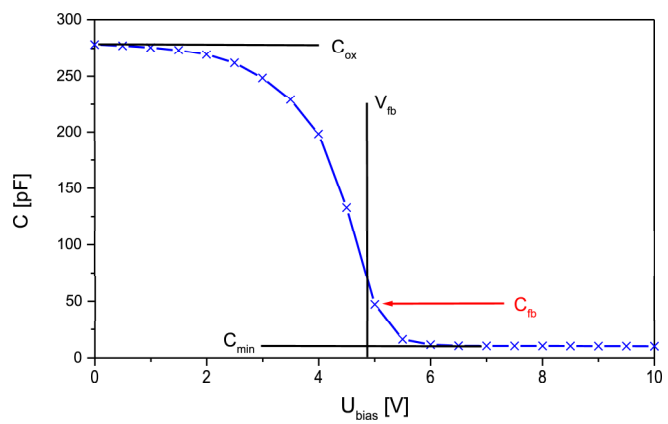


Figure 3.12: Capacitance vs. bias curve on a MOS test device and relevant parameters

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interface. This yields

$$C_{ox} = \frac{\epsilon_0 \cdot \epsilon_{SiO} \cdot A_g}{d_{ox}}, \quad (3.10)$$

$\epsilon_{SiO} \approx 3.4$ being the dielectric constant of silicon dioxide grown in dry atmosphere [WOL86], A_g the gate area and d_{ox} the oxide thickness.

When measuring a capacitance vs. voltage curve (see figure 3.12) by applying a positive potential on the metallized oxide gate, first the electrons in the accumulation layer and then bulk electrons near the interface are repelled, forming a depletion layer of significantly low conductivity, functioning as an additional serial capacitance. Thus the oxide capacitance C_{ox} and the capacitance of the depletion zone

$$C_{si} = \frac{\epsilon_0 \cdot \epsilon_{Si} \cdot A_g}{d_{dep}} \quad (3.11)$$

(d_{dep} being the thickness of the interface depletion zone) are added inversely to yield a total capacitance

$$C_{tot} = \left(\frac{1}{C_{ox}} + \frac{1}{C_{Si}} \right)^{-1} \quad (3.12)$$

with the lower capacitance dominating. As the depletion depth in the flat-band case is given by the extrinsic Debye length [NIC82]

$$d_{dep} = \lambda_{deb} = \sqrt{\frac{\epsilon_0 \cdot \epsilon_{Si} \cdot k \cdot T}{e^2 \cdot N_{eff}}} = \sqrt{\frac{d^2 \cdot k \cdot T}{2 \cdot e \cdot V_{dep}}} \quad (3.13)$$

($k \approx 8,61734 \cdot 10^{-5}$ eV/K being the Boltzmann constant and T the temperature) the flat-band capacitance

$$C_{fb} = \left(\sqrt{\frac{k \cdot T}{2 \cdot e \cdot V_{dep}}} \cdot \frac{d}{\epsilon_0 \cdot \epsilon_{Si} \cdot A_g} + \frac{1}{C_{ox}} \right)^{-1} \quad (3.14)$$

can be derived from C_{ox} and V_{dep} . The absolute flat-band voltage V_{fb} can be derived from the capacitance vs. bias curve from the measurement point closest to C_{fb} in capacitance. For a possible comparison with existing values for charge density within the oxide N_{ox} , an approximation

$$N_{ox} = (V_{fb} + \Delta\Psi) \cdot \frac{\epsilon_0 \cdot \epsilon_{SiO}}{e \cdot d_{ox}} \approx V_{fb} \cdot \frac{\epsilon_0 \cdot \epsilon_{SiO}}{e \cdot d_{ox}} \quad (3.15)$$

for small contributions of the work function difference $\Delta\Psi$ between metal and n-type silicon [HÜG01] [SZE81] can be used.

Interface generation current is another parameter important for the overall assessment of oxide interface quality and damage induced by physical stress or irradiation of the surface layers of the sensor wafers. This parameter can be tested by using gate controlled diodes (GCDs), devices combining an implanted diode with metal gates on the neighbouring oxide [WUN00]. When depleting the interface below the gates next to a reverse biased diode, the depletion volumes of diode and gate join, draining the interface generation current into the diode. The current injected around a gate potential of V_{fb} from a well defined gate area equals [NIC82]

$$I_{ox} = A_g \cdot e \cdot S_0 \cdot n_i, \quad (3.16)$$

S_0 being the surface recombination velocity which depends on the effective cross section and density of interface recombination centers. Like N_{ox} , this parameter can be used for geometry independent comparison of interface characteristics on different wafers.

To gauge the impact of radiation damage on the oxide interface, a current vs. gate potential measurement has been implemented for test devices after irradiation with low energy electrons. These irradiations can be performed in-house at Dortmund University by using the DEBE (Dortmunder Elektronen-Bestrahlungs-Einrichtung, see figure 3.13), a modified Philips EM300G electron microscope fitted for device irradiation with electrons in an energy range of (20 – 100) keV with

3.2 Choosing sensor characteristics

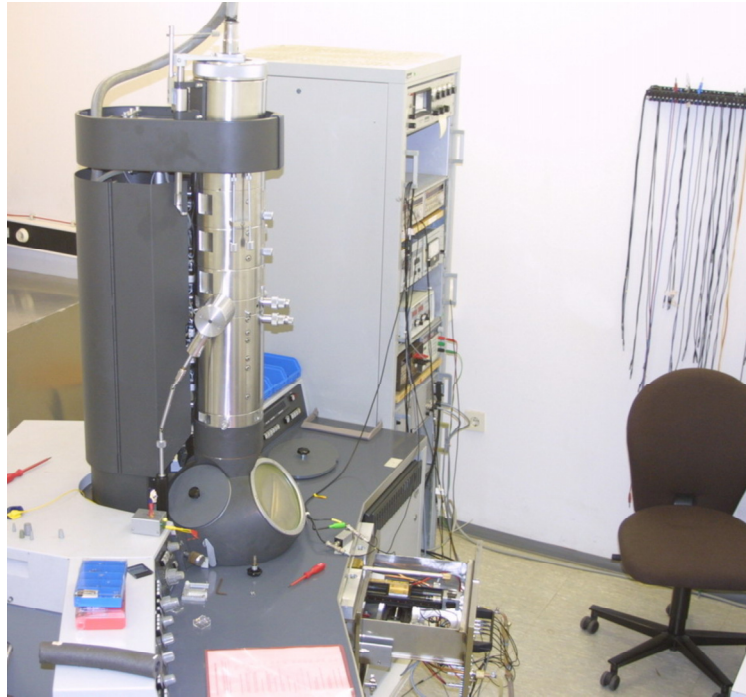


Figure 3.13: The Dortmund electron irradiation facility DEBE built from a converted electron microscope

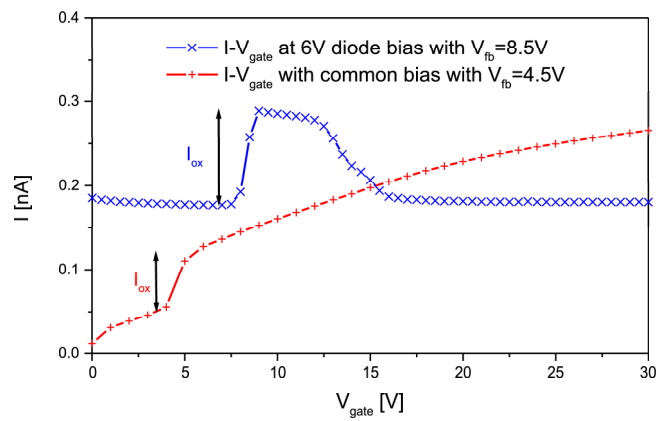


Figure 3.14: Examples of current vs. V_{gate} curves from two different gate controlled diodes, measured with constant and with common diode bias

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a dose rate of up to 100 Gy/s, setting the required irradiation time for the ATLAS pixel design dose of 500 kGy at only about two hours. Electrons at the lower end of the chosen energy range do only penetrate the passivation, metal and oxide layers of a wafer and induce ionization within the oxide, leading to an accumulation of positive charges near the interface (increasing N_{ox}), while the free electrons generated can leave the oxide via metal gates. They also increase the number of defects at the oxide/silicon interface acting as recombination centers and thus adding to S_0 , but the momentum of 20 keV electrons is still well below the threshold for Si atom displacement (minimal electron energy for point defects would be 260 keV and significantly more for cluster defects [WUN92]), where non-ionizing energy loss within the bulk would start to play a significant role. This allows for observing effects of damage to oxide and interface independent of changes in the charge type and density of the bulk silicon. While dose dependency and annealing of irradiation effects on oxide and interface have been studied [WUN92] [WÜS01], there is so far no commonly used parameterization like there is for bulk damage.

For practical purposes there are two possibilities for scanning GCD current dependent on gate potential V_{gate} . The bias applied to the diode contact can be held constant while different gate potentials are applied, or $U_{bias} = V_{gate}$ can be raised simultaneously (see figure 3.14). The former method yields a clearer result concerning the exact value of I_{ox} as well as information on the gate inversion process, lacking in curves obtained by the common biasing of gate and diode. This latter method shows the I_{ox} rise superimposed on the diode's leakage current characteristic and testing the diode quality at the same time as the interface. In all cases in which I_{ox} is significantly higher than the rise of diode current around V_{fb} the precision of a common bias measurement is acceptable; other cases indicate either a defect diode or an interface exceptionally devoid of recombination centers, both remarkable in their own right and useful for quality assessment, even without exact I_{ox} values. As the more complicated method does not provide any information significant for wafer quality not also obtainable by the less complicated one, the latter has been chosen for standard tests.

The current rise in these characteristic curves happens around the flat-band case — a possibility to crosscheck V_{fb} measurements on MOS gates for consistency — but is not abrupt. Due to charged interface defects there is a stretch-out of the effect, making a definition using a potential interval as

$$I_{ox} = I(V_{gate} = V_{fb} + x) - I(V_{gate} = V_{fb} - x), \quad (3.17)$$

with $x = (2 - 3) V$, useful for GCD devices before irradiation. After the generation of additional charges by ionizing radiation, the interval has to be chosen wider due to the increase in interface charges.

The functionality of the p-spray inter pixel isolation is of critical importance for detector operation, as a low resistivity connection between individual pixel cells, whether via a biasing structure or directly across an inter pixel gap, will deteriorate the space resolution of the detector and increase the noise in each channel by higher capacitive load and possibly additionally injected current. There are two largely independent criteria used to ensure proper functionality in this regard.

The first is used for the direct control of the more sensitive, i.e. narrower, bias dot gaps. For this, devices incorporating bias dots have to be tested by depleting the bulk with the bias implantation connected to a voltage source and a surrounding implantation, into which the bias dots are implanted, floating at V_{pix} . The quality of isolation as well as biasing can then be derived from a sweep of the potential difference ΔV between the implantations vs. U_{bias} . In the case of a bipolar junction between implantations and bulk, this should typically lead to a rapid rise of ΔV while the depletion zone under the bias contact is growing independently, saturating during the gradual joining of the depletion zones and the stabilization of the current channel between the implantations [KEM88]. The values for high biases are expected to be nearly constant, the other implantations following the potential of the biasing structure with a constant offset, defining a characteristic punch through voltage V_{pt} [HÜG01]. In the case of unirradiated ATLAS pixel sensors, where the depletion zone is grown from the back plane, the structured implantations are connected at low bias voltage via undepleted bulk and thus exhibit negligible potential differences. Close to full depletion a beginning rise of ΔV is expected, when the bulk current is pinched off and only a narrow current channel between bulk and p-spray layer is held open by the beginning

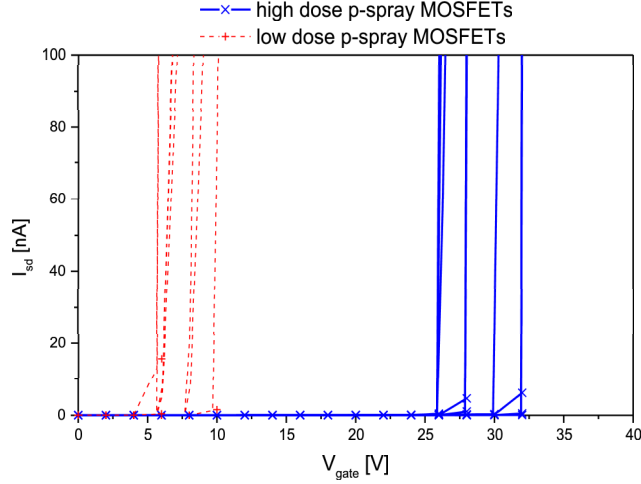


Figure 3.15: Measurements of source-drain currents of MOSFETs on p-spray layers of high and low dose, each showing a sharp current increase at a certain threshold voltage

potential difference. As the full potential difference U_{bias} thus has to be dynamically split between ΔV and the voltage drop across the bulk, a significant saturation effect is not expected. Therefore no characteristic value corresponding to the saturated V_{pt} exists, and to define a potential gauging isolation and biasing behaviour, an arbitrary bias has to be defined, in our case the operation voltage V_{dep} , as it represents both stable overdepletion and a realistic value for initial sensor operation. To prevent a too low effective resistivity resulting in high currents across the bias gap, the criterion $V_{pt} = \Delta V(U_{bias} = V_{op}) \geq 3 \text{ V}$ has been set. Implicitly an extremely high value is ruled out, too, but has not been defined numerically.

Another method to spot problems in p-spray isolation is by measuring the p-spray dose itself using n-channel MOSFET structures with a high dose p-spray layer isolating source from drain. According to threshold voltage criteria [HÜG01] [LUT99], the current channel in the p-spray below a metal gate opens (as seen in figure 3.15) at an absolute drain-source voltage

$$V_{th} = 2 \cdot \Psi_{fi} - V_{fb} + \frac{Q_g}{C_{ox}} \cdot \sqrt{1 - \frac{V_p}{2 \cdot \Psi_{fi}}}, \quad (3.18)$$

Q_g being the total localized charge under the gate. $\Psi_{fi} \leq 1 \text{ V}$ is the potential difference between Fermi level and intrinsic level of the channel, which can be neglected, as it is of the same order of magnitude as the silicon band gap. The negative channel bias V_p is harder to assess for measurements taken on a fully depleted bulk, but without the p-spray layer itself being set on a defined potential. Without this, the bias pinches off current channels within the non-doped bulk, influencing V_{th} in the floating p-spray layer — an effect saturating for higher U_{bias} [HÜG01]. Fortunately these data are unnecessary to gauge the effective p-spray dose N_{ps} per area under normal operation conditions, as it can be defined as

$$N_{ps} = \frac{Q_g}{e \cdot A_g} \cdot \sqrt{1 - \frac{V_p}{2 \cdot \Psi_{fi}}} = \frac{C_{ox}}{e \cdot A_g} \cdot (V_{th} + V_{fb}) \approx \frac{C_{ox}}{e \cdot A_g} \cdot V_{th} \quad (3.19)$$

for $U_{bias} = V_{op}$. Neglecting V_{fb} can be problematic, especially in the case of low p-spray doses, but technical problems when measuring flat band voltages through a p-spray layer or using values from p-side oxides are strong arguments for not using V_{fb} data at all, but instead relaxing the production criteria according to the now larger margins of error. To define the full opening of the MOSFET channel a drain current $I \geq 100 \text{ pA}$ has to be reached and according to specifications and additional errors by approximations the resulting high dose p-spray value has to conform to

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$2.2 \cdot 10^{12} \text{ cm}^{-2} \leq N_{ps} \leq 3.5 \cdot 10^{12} \text{ cm}^{-2}$. For low dose p-spray no clear criterion has been given but for sensor wafers produced according to specifications, a value of $N_{ps} \approx 0.5 - 1.0 \cdot 10^{12} \text{ cm}^{-2}$ is expected.

P-spray testing devices can be studied after irradiation, too, yielding information on realistic sensor behaviour if irradiated with protons, or specific data on interface states and oxide charges after irradiation with low energy electrons. Tests during prototyping [WÜS01] [HÜG01] have already shown, that even low dose p-spray does not completely lose its isolating qualities after intensive irradiation at the DEBE. It shows an onset of channel opening at lower gate voltages due to compensation of some of the doping by electrons drawn from the bulk by positive oxide charges, but also a stretching out of the current rise by charged interface defects, moving the full opening of the current channel to higher V_{gate} . While this does not necessarily prevent some amount of increased inter pixel current, it renders moderated p-spray an intrinsically radiation hard technology.

Other non-critical parameters are collected by directly testing aspects of the wafer. Those are resistivity of implantations on a depleted bulk, of the metal layer (both usually given as sheet resistivities independent of sheet thickness and normalized for a length to width ratio) and between pixel cells under bias, measured by current vs. potential difference. Similarly, capacitance between pixel cells as discussed in [GRF01] and [WÜS97] is measured by taking the mean value from a capacitance vs. time curve.

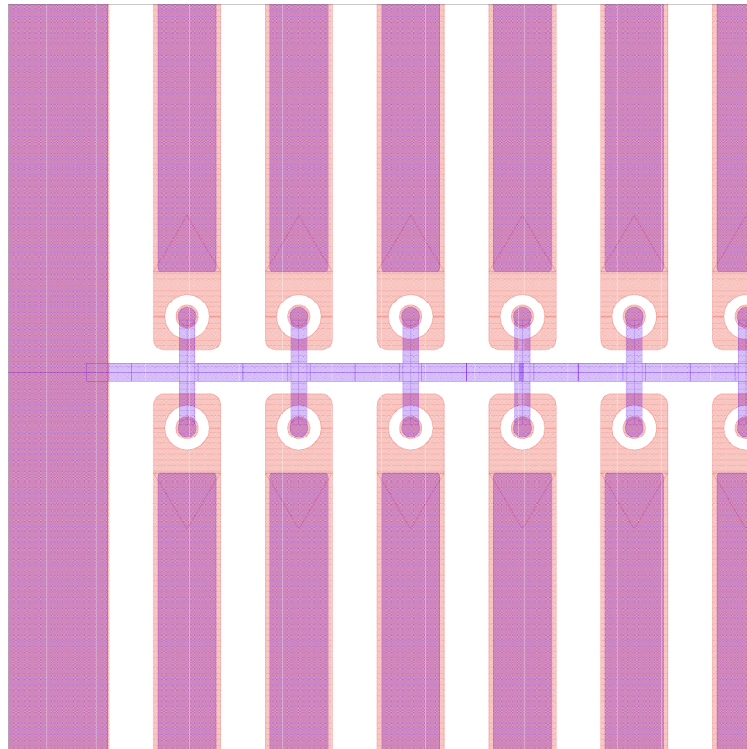


Figure 3.16: Layout detail of the bias grid visible in the production masks for a pixel double row [HÜG01]

3.3 Development of test structures

There are several characteristics that have to be measured either on the whole wafer or on the sensor tiles themselves. Among these, the mechanical characteristics wafer bow, wafer thickness and mask alignment quality are relatively easily accessible by means of touch free testing methods or without having to probe or touch structured parts of the wafer surface. For all other measurement tasks

except the ones directly testing the functionality of sensor tiles, dedicated test structures have been designed and placed around the edges of the wafer (see figures 3.2a & b and 3.3).

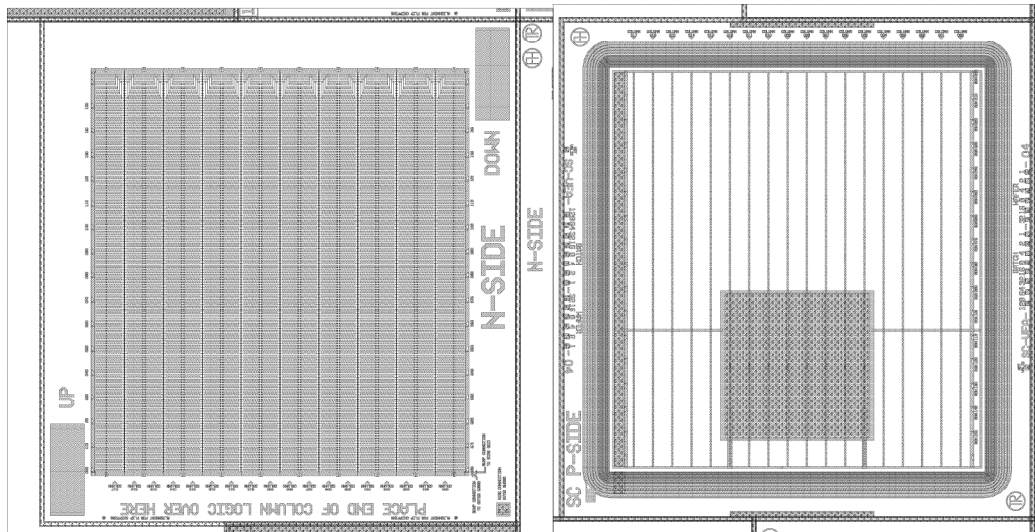


Figure 3.17: a) n-side mask (left) and b) p-side mask (right) of a single chip sensor [KLA04]

In the case of direct testing of the sensors before hybridization (IVS and ITS procedures), features for on-wafer measurements had to be implemented in the sensor design. The most distinctive testing feature is the bias grid pattern connecting all n-side pixel implantations with each other and with a bias ring running around the sensitive sensor area. During the prototyping process [HÜG01] the exact geometry and technology of the bias grid had been tested and optimized for production quality, sensor charge collection and unwanted impact on sensor testing. Finally a concept of small implant dots, one implanted within each pixel cell and connected with all other pixel cells in a double row and the bias ring by ladderlike metal vias on top of the oxide has been implemented. This parallel connection of all pixel cells functioning as individual diodes provides a useful tool for current measurements, as a breakdown in any pixel cell will dominate the overall characteristic, due to the inversely additive resistivities.

The n^+ implantation around the pixel cells is divided into a bias ring connected to the metal layer of the bias grid and an additional guard ring running around the whole structure without a direct connection. This allows for test biasing from outside of the pixel array, even from metal pads on the p-side by punch through across undepleted bulk, but, by introducing an additional resistivity on the sensor edge, suppressing leakage currents flowing from the sensor edges into the bias grid and possibly into the pixel cells generating noise. To improve on this effect, grounding contacts on the guard ring have been implemented.

Another feature important to sensor quality is the multi guard ring structure around the p-side implantation. Consisting of concentric p^+ implantations, of which counted from the center, there are eleven narrow rings, five wider ones and an outermost narrow ring exhibiting a wider inter ring gap, this structure for managing sharp potential drops in a controlled way, has originally been developed for the ATLAS SCT strip detector [AND00]. All guard ring implantations have a metallized surface improving potential distribution along the ring, with the outermost one and the next one in having been designed with a contact pad. This allows for probing the multi guard ring structure itself, but, as the silicon nitride passivation is not opened on top of those pads on the production wafers, only a pretty forceful setting of probing needles will actually achieve contact — an option that should only be employed on non-critical devices. The p-side sensor surface within the multi guard ring structure on the other hand is fitted with a grid like metallization on top of its entire p^+ backplane implantation as well as one or two big metallized contact pads on top of which all passivation layers have been removed. These are easily accessible both for wafer probing and for later connecting with the module voltage supply via conductive glue.

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In addition to the sensor tiles, smaller sensors are supplied on each production wafer, identical to tiles in design of the sensor cells and the contacting and isolating structures, but specifically intended for testing purposes (see figure 3.17). Among these are single chip sensors, designed to be fitted with a single front end readout chip for tests concerning hybridization of sensor and electronics and signal readout. Still smaller with only $6 \cdot 6 \text{ mm}^2$ of active surface are so called mini chip sensors, implemented as test devices for irradiation studies, as they are of equal active volume as the tests diodes for similar measurements and the currents and temperature of these small sensors are much easier to manage than those of full size tiles after significant bulk damage.

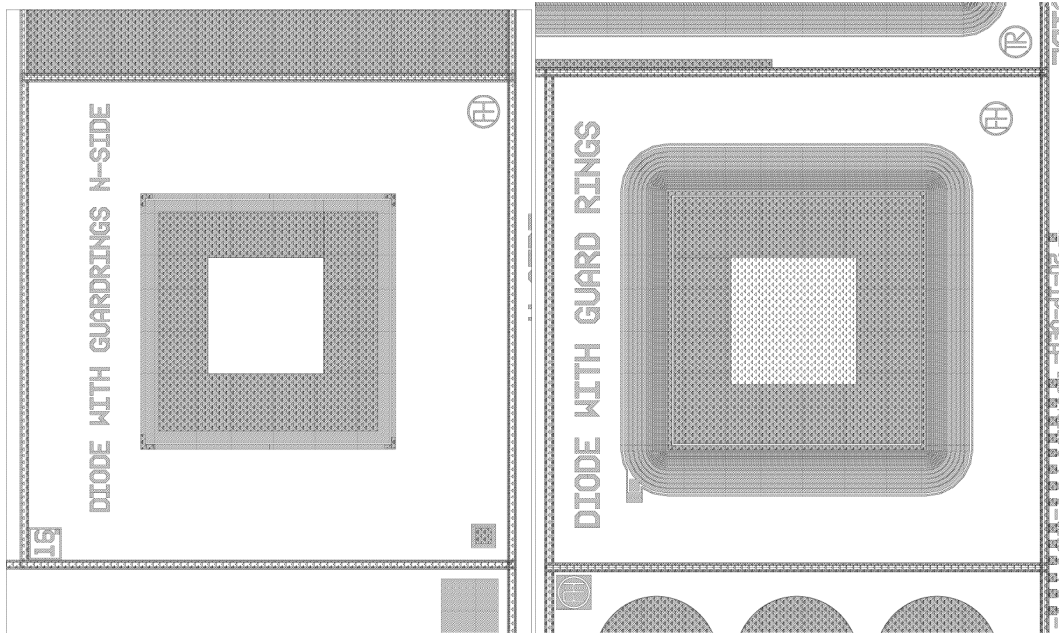


Figure 3.18: a) n-side mask (left) and b) p-side mask (right) of a test diode with multi guard ring [KLA04]

Similar to the sensors, the diodes used in IVD and CVD tests as well as for characterization of the sensor substrate after proton irradiation are fitted with contact pads on the p^+ implantation, an implanted n^+ ring around the n-side and a complete multi guard ring structure around the p-side (see figure 3.18). The latter two features set the ATLAS test diodes apart from simpler diodes with only a very straightforward guard ring on one side, as they have been used for irradiation studies within the ROSE and the RD50 research and development projects (e.g. see [MOL99] and [KRA04a]).

Tests on the quality and properties of the SiO_2 and the substrate-oxide interface (BOX, COX and IVG) are performed on a common oxide test field structured on the p-side. It is similar to the test field used for dedicated oxide studies in [WÜS01], containing two MOS pads, simple round metal pads with opened passivation on top of the p-side oxide (see figure 3.20a), as well as circular two gate controlled diodes, all combined with a multi guard ring and a simple biasing contact on the wafer n-side. The main difference to the original circular GCD proposed and tested in [BEC00] is that only one of the diodes is designed with five connectable gate rings of equal pitch — ideal for studying the quantitative influence of the gate area on the depletion behaviour of the interface layer —, while the other one is implemented with only one broad gate ring for depletion studies, while a second outer metallization ring is to be grounded to define the outer limit of the tested interface area (see figure 3.20b). To avoid difficulties created by having to assess oxide and interface characteristic through a p-spray layer and measuring I_{ox} without a bipolar junction on the same wafer side as the gate rings, only measurements on the p-side are taken and when necessary extrapolated to equivalent n-side properties (increasing systematic errors, but, as long as both sides are actually processed to the same parameters, not misleading the quality assessment).

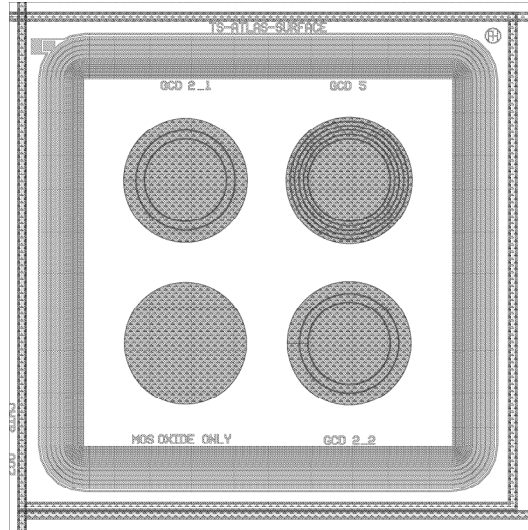


Figure 3.19: Mask of a p-side oxide test field [KLA04]

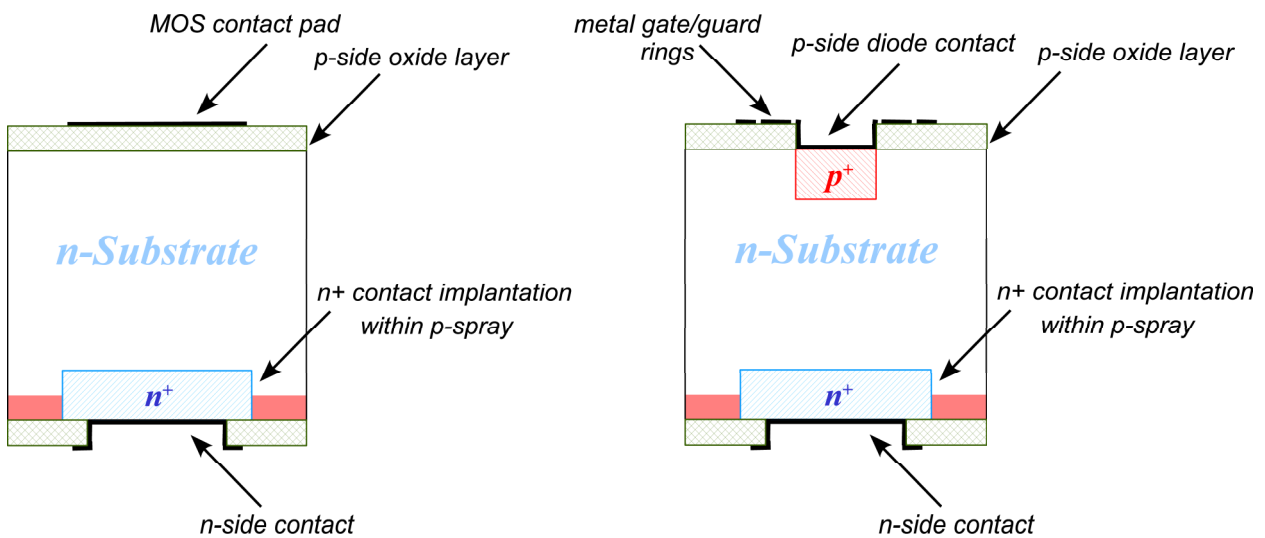


Figure 3.20: Cut-away views of a) a MOS pad (left) and b) a two ring GCD (right) used on the oxide test field (not to scale)

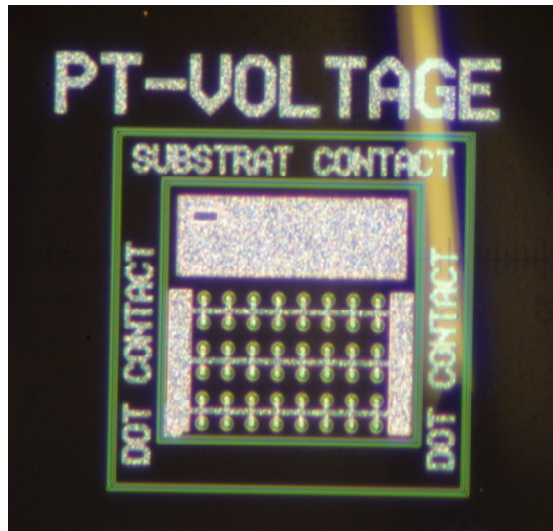


Figure 3.21: Punch through test device with 48 bias dot implantations and the reflection of a probe needle to the right

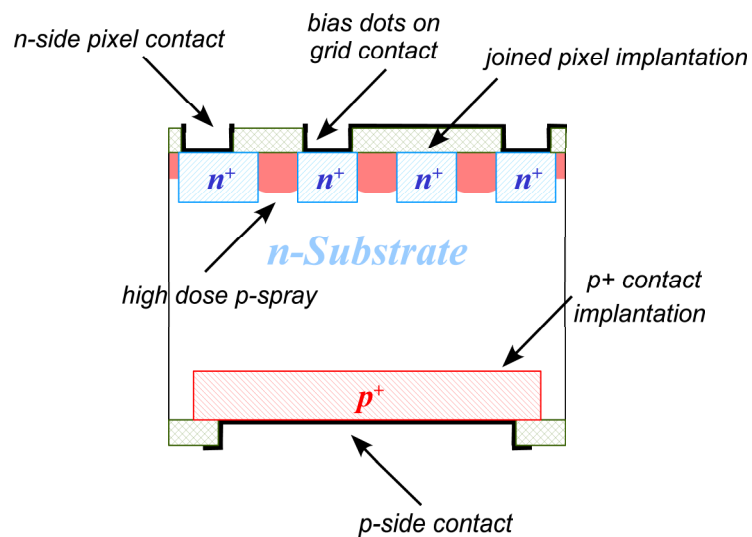


Figure 3.22: Cut-away view of a punch through test device (not to scale)

Characteristics of the sensor pixel array itself as well as the bias dots (tested for with the PUT, IVP and CAP procedures) are tested on an inter pixel test structure, segmented on the n-side. It consists of four inter pixel test structures, arrays of pixel cells of double length without a bias grid, but with spacing and p-spray profile identical to sensor cells, usable for inter pixel capacitance and current measurements. Two of the devices are fitted with metal vias to external contact pads for a central pixel cell as well as its neighbours towards the long pixel edges. These pads are easy to probe, but add capacitance to the pixel cell and make the device generally not an exact representation of pixel cells. Thus the preferred test devices are the two pixel arrays without contact pads, but with an opened passivation on top of the central and neighbouring pixels allowing for a direct probing of the pixel cell metallization. As these metallizations are quite narrow and the implantations easy to damage, this calls for very exact and cautious probing, but is expected to yield more reliable and realistic results.

Besides an additional contact to the n-side bulk and a multi guard ring around the metallized p-side backplane, there are two more devices implemented on the structure. They are special punch through devices consisting of a single n^+ implantation fitted with an array of 48 bias dots (see figure 3.21). These bias dots are connected with three bias grid ladders on top of the oxide, each branching off to eight dot implantations on each side. On each end of the ladder structures there are metallized contact pads with an opened passivation layer, as well as on top of a part of the big n^+ implantation not structured with bias dots. Thus, the behaviour of realistic bias dots can be tested, studying punch through across a dot gap implanted with high dose p-spray (see figure 3.22), without having to probe individual pixel cells and independent of other inter pixel dynamics.

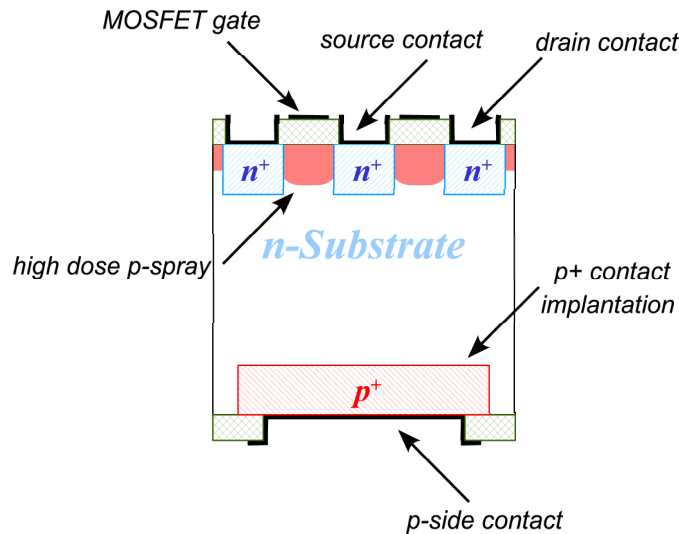


Figure 3.23: Cut away view of a p-spray test MOSFET (not to scale)

As a way to extract process parameters in the MFE and SRE tests for implantations, metal layers and most of all, the isolating p-spray layer, another test device had to be included on both wafer sides. In the case of the n-side multi test structure, the most important features are MOSFETs designed with circular implantations and gates for direct tests of p-spray dose. There are two big transistor devices on each side of the structure, each centered around the n^+ source implantation with a metallization and a passivation opening on top. Around this implantation there is a defined circular gap with a width of $30\ \mu\text{m}$ and a circular gate metallization elongated on one side to an opened contact pad. This gap is implanted with either a high or a low dose p-spray layer. Finally there is a n^+ drain ring implanted around the gap, fitted with another contact pad situated to the side opposite the gate pad. Together with a p^+ implantation covering the whole back plane and fitted with a contact pad and a multi guard ring structure, these structures can be used to probe the MOSFET on a depleted substrate and gauge the high and low p-spray doses (see figure 3.23).

Next to the two main high dose MOSFETs placed to one side of the structure and their low dose

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counterparts on the other one there are four smaller ones each as a back up, scaled down to a gap width of only $16\ \mu\text{m}$ [HÜG01]. Other devices on the n-side multi test structure are two implanted and metallized n^+ bulk contacts for better substrate biasing and sheet resistance test devices. The latter are four n^+ implantations and four metallization strips, each with an opened contact at each end. Two devices of each type have a dimension of $50 \cdot 400\ \mu\text{m}^2$ yielding a sheet parameter of $8\ \square$ (being defined as length/width in a dimensionless unit of squares = \square), two are sized $25 \cdot 400\ \mu\text{m}^2$ yielding a sheet parameter of $16\ \square$, which is preferable for SRE tests, as the measured currents are lower and easier to manage.

On the p-side, the only relevant devices on the multi test field structure are a bulk contact and sheet resistance test devices. Those are exact analogues to the ones on the n-side structures, but here the p^+ implantations and the p-side metallization are tested. The six small MOSFET structures could be used for studies of the bulk and the oxide substrate interface by measuring their switching behaviour and conductivity, but as there is no p-spray layer to be tested here, they are not part of the regular quality testing schedule.

Finally there had to be several structures included to gain visual information used in a number of ways during the testing and assembly process. Besides alignment marks on the sensor tiles themselves, there are several marks near the wafer edges. Two structures of this kind are custom designed for checking the alignment of the different process masks on each wafer side during visual inspection. As can be seen on an example from the wafer n-side, there are four sets of inspection marks, respectively comparing the mask alignments of the implantation relative to the metallization, the implantation relative to the oxide, the implantation relative to nitride used for p-spray moderation (invisible in the mask plot) and the metallization relative to the passivation openings. These can be checked qualitatively by inspecting the four nested crosses in the center of each set. As long as the smaller structure stays within the larger one, the misalignment limit of $2\ \mu\text{m}$ has not been exceeded. For quantitative information, a vertical and a horizontal vernier structure has been included at the ends of each set. The scales of the vernier are spaced to reflect misalignments of $0.5\ \mu\text{m}$ per unit i.e. a match of the two central lines means a misalignment of $< 0.5\ \mu\text{m}$, while a match of the outermost pair (five lines out) indicates a misalignment of about $5 \cdot 0.5\ \mu\text{m} = 2.5\ \mu\text{m}$.

3.4 Testing procedures

In addition to definitions of the quantities to be tested for and the design of the devices to be tested on, the circumstances and external parameters of the measurements have to be kept as constant and similar as possible between the participating laboratories. For this, heuristic tests during prototyping had to be performed, and possible influences on data consistency have to be analyzed throughout cross calibration and standard quality testing of the series and pre-series. According to results from these analyses, adequate and consistent choices in tools, testing parameters and testing environment have been made. Additionally, general logistics and housekeeping tasks have been defined for smooth collaboration between the participating manufacturers and laboratories as well as for minimal potential damage during shipping, handling and testing.

3.4.1 Devices and set-ups

The instruments used for measurements have to be chosen according to the requirements of the tests defined and to the reliability called for in an ongoing quality control operation, especially concerning the consistency of test results. This calls for the use of standard measuring devices built for continual use at a high accuracy level needing only a minimum of additional calibration done in the laboratory. For this reason, proven high precision products have been chosen by all laboratories. In terms of measurement accuracy, currents have to be tested on a scale down to several pA, especially for BOX tests, while capacitances to be considered typically come down to several pF. The latter have been decided to be tested on a high frequency LCR analysis device, as most comparable tests in other projects and publications are done this way, and as quasi-static measurements, besides producing significantly different results when it comes to switchable space charges, require a very vibration free environment for conclusive measurements, putting undue

constraints on laboratory activities. Potential differences call for measurements down to several mV, while temperature has to be logged at an accuracy of at least 0.5 K, but preferably below 0.1 K. Temperature logging has to occur parallel to other measurements at all times to allow for temperature correction of individual data points, so implementing an automatic data taking system combining the output of several measurement devices is of importance, not only for the ease of quick repeated testing, but also for the possibility to measure multiple variables synchronizedly and in systematic sequence. Voltage supply has to go up to at least 500 V, but needs only a minimum step width of 0.1 V for most measurements. Only for inter pixel and sheet resistance tests step size should be as small as feasible, ideally not above several mV.

In the case of Dortmund, the central device for both current measurements and voltage supply is the Keithley 487 picoammeter with an integrated voltage source, able to supply either up to 500 V bias in 10 mV steps or up to 50 V bias in 1 mV steps. In cases in which this voltage source does not supply a sufficiently high potential, a Keithley 248 high voltage supply has been used. The capacitance measurements are done using Hewlett-Packard 4284A and 4284B LCR-meters and custom built bias boxes for joining the high frequency sense lines with the voltage source output for capacitance vs. bias sweeps. These reach a resolution of well below 1 pF for capacitances up to 100 pF, but have to be calibrated for the exact configuration of cable, connectors and probing equipment, a process that can only be done up to an accuracy of the order of 0.5 pF under typical laboratory conditions, so that a minor offset can remain. For tests of potential differences a Keithley 617 electrometer is used, exhibiting a resolution below 1 mV for voltages up to 20 V (even less for smaller potential ranges) and an internal resistivity of over 200 T Ω , orders of magnitude above what is expected from any test device it is used on and thus not significantly influencing measurements parallel to the device. Temperature logging is being done using PT100 resistors connected to four pole sensing Keithley 196 and 2000 multimeters, programmed to directly convert the sensed resistivity measured at an 100 $\mu\Omega$ accuracy into temperature values. All devices used are built to be addressed, operated and read out using a GPIB interface (IEEE-488 standard) and have been connected to a computer equipped with an interface card for this standard and running the Labview program package to address and operate the measurement set-up and manage the data returned. This selection of hardware and read out software is representative of all involved laboratories and has been compared during cross calibration to ensure comparable testing conditions.

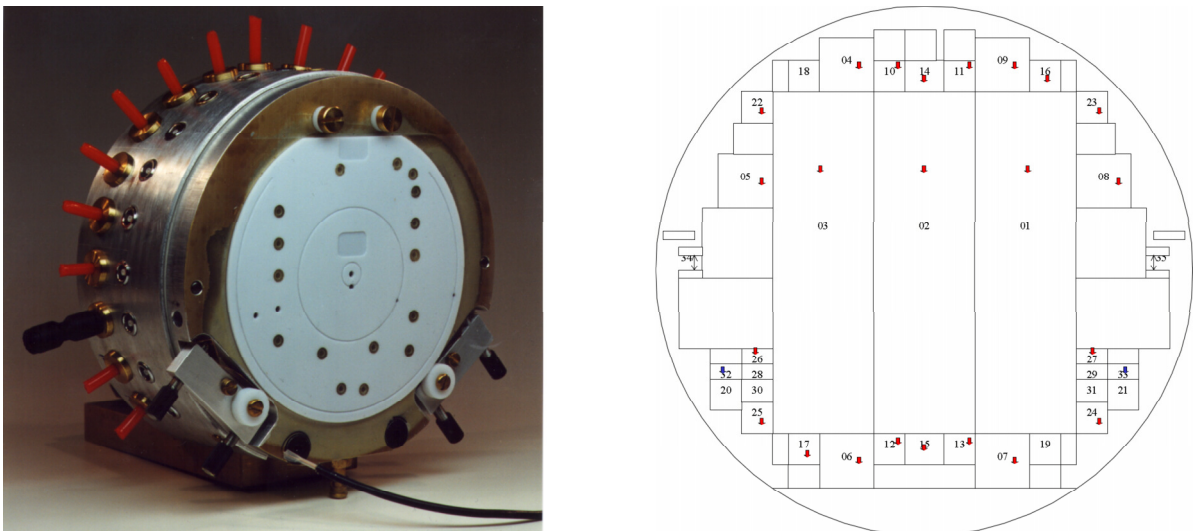


Figure 3.24: a) Custom built needle chuck for automatized probing of production wafers (left) and b) needle placement relative to test structures (right)

Measurement set-ups are done using coaxial Lemo cables and connectors as well as coaxial and triaxial sensing cables designed for the measurement hardware to connect the latter to two probe stations, one a standard Karl Suess machine and one custom built for the Dortmund laboratory.

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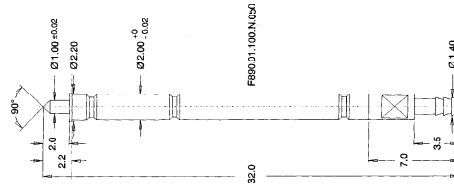


Figure 3.25: Blueprint of a pneumatic probe needle

These probe stations are both fitted with microscopes and can be used with probe needles of different tip diameter, depending on the device being probed. One of the stations is equipped with a flat steel vacuum chuck with openings for holding test devices down by applying air pressure, the other one has a teflon ring chuck for holding a complete wafer around the edges while being probed from above and below. The latter is also tooled with two video cameras taking microscopic pictures of the wafer surface from above and below to facilitate needle placement and with motors controlling the movements of the chuck and designed for external automatic control of its position.

All electrical measurement set-ups are enclosed within metal boxes to shield them against light and stray fields. The former would prevent any meaningful measurement of leakage current — being dark current as opposed to signal current —, the latter could lead to significant pickup within the test set-up leading to artifacts stemming from nearby power lines, high power electronics or radio emitters. Again, the Dortmund set-ups described here are similar to those at other ATLAS pixel laboratories and have been used as examples for the planning and improvement of some of the latter.

For automatization purposes, only complicated two-sided contacts are done by hand on the probe stations. For other, repetitive, test steps an automated probe chuck (figure 3.24a) has been designed to replace the steel vacuum chuck. Its teflon surface is tooled for wafer alignment and has a central opening for a low pressure pump connection to hold the wafer flat to the chuck. Integrated into the chuck's body are 25 pneumatic needles (figure 3.25), connected individually to a switching relay via air tubes and coaxial cables. This relay, which can be operated automatically by the measurement software, switches on air pressure connections to the needles, extracting them towards the wafer surface, and connects the needles electrically to the measurement set-up needed. The needles are placed for the most part to probe contact pads on the wafer p-side (see figure 3.24b). This avoids damage to the more sensitive n-side structure and allows for automatic measurements of all tests needing only one contact per device on the p-side and only a common bulk bias contact on the n-side, which can be set before starting the automatized sweeps.

Probe chucks like this have been produced at the Dortmund workshops for all interested laboratories and have been extensively tested for influences on the test results and possible damage to the wafer. The latter has proven to be negligible.

Devices and methods for measurements of wafer planarity could not be completely harmonized between the laboratories. They, as well as the related cross calibration effort, are discussed in the following chapter.

3.4.2 Measurement settings

Using comparable measurement settings during all quality tests is a second step towards harmonization of testing, after implementing comparable set-ups. Before agreeing on testing parameters, the potential influence of those has to be understood and estimated to choose a range of allowed settings producing results representing actual sensor behaviour.

In the case of most bias dependent sweeps the main variables in testing are voltage step size and time intervals between voltage steps, as all devices under test react non-instantaneous to a change of bias, but will need some time to reach a stable space charge configuration. Even without dynamic effects within the wafer itself the capacitance and inductivity of the test set-up including the device will lead to transient potential differences and currents directly after a bias step. In the

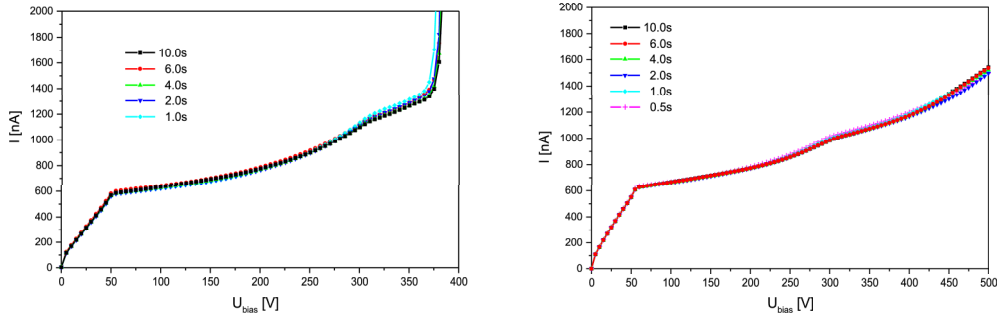


Figure 3.26: Bias stepping time dependence of I - V sweeps on prototype sensors a) exhibiting a breakdown at high voltages (left) and b) without breakdown (right)

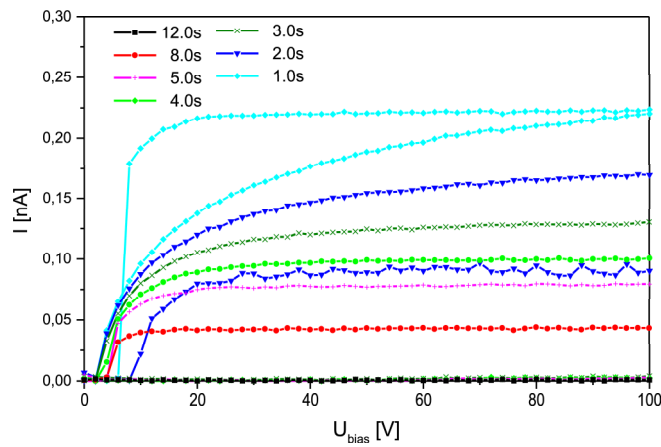


Figure 3.27: Bias stepping time dependence of I - V sweeps on two MOS pads using the probe chuck set-up

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case of most testing processes there is very little impact by varying the stepping times within a range from (1 – 10) s per step of up to 5 V bias, as can be seen in figure 3.26b for a current vs. bias test on a prototype sensor tile. The maximum effect typically seen happens in cases of rapid current rises like during breakdown as shown in figure 3.26a, but even there the current level is only raised and the breakdown voltage lowered to the order of a few % at worst. This has been deemed an acceptable loss in accuracy compared to the gain in quicker measurements for series testing, so a standard stepping time of 2 s has been agreed upon.

The only case in which transient effects pose a problem are measurements of very low currents with a set-up of relatively high capacitance or inductivity, like BOX tests on good MOS structures performed using the probe chuck. Results from test sweeps on several pads (two of them shown in figure 3.27) show great variations between individual pads, but in all of them a significant current is introduced by transient behaviour at small stepping times. In some cases this effect is so pronounced it can only be suppressed by increasing the stepping time above 10 s. For this type of measurements stepping time can not be fixed on an agreed upon value, as doing so with a safety margin would make all comparable tests rather time intensive for the sake of a few problem cases. For this reason, the behaviour of the measured value during the individual testing steps should be monitored by an operator. If the quantity tested for shows a marked time dependence during all stepping intervals, the test will have to be repeated with a significantly higher stepping time.

In capacitance vs. bias curves, several additional parameters have to be taken into account, as a high frequency LCR analysis can be influenced by more settings than just the development of the bias. The amplitude of the high frequency test voltage should be kept around or below 0.05 V, as high amplitudes will decrease the accuracy of the capacitance sweep. For the AC frequency itself a value in the range of (10 – 30) kHz has been shown [BOR01] to yield the most consistent results for V_{dep} of non-irradiated sensors and diodes with regard to temperature change as well as values comparable to those obtained from charge collection curves. As frequencies this high have been observed to produce higher noise in capacitance tests on devices with a radiation damaged bulk, for these measurements a slightly lower frequency range is advisable.

A last parameter necessary for the LCR-meter is the model of the device under test used for the analysis. As generally devices with non-negligible leakage currents are being tested, the model used is a capacitance parallel to a resistivity. For better comparability it has been decided to consistently use the setting characterizing the parallel ohmic resistor by a dissipation factor ($C_p - D$ mode).

The extraction of V_{dep} itself from the capacitance sweep is another not completely trivial aspect, which has been discussed to some extent [WUN92] [BOR01]. As the characteristic capacitance drop at full depletion is hard to spot in a linear C vs. U_{bias} plot, alternative plotting scales like C^2 vs. U_{bias} or C vs. $1/\sqrt{U_{bias}}$ are used, the latter one preferred for ATLAS pixel sensors, as it successfully suppresses constant stray capacitances. Especially for precision tests on irradiated diodes, much more rigid systems of test harmonization have been proposed [CHI03], but have been deemed unnecessary to assess unirradiated devices or overall sensor functionality after irradiation.

3.4.3 Dust, humidity and temperature

Generally speaking, the testing environment has to conform to two main requirements of the ATLAS pixel project: it has to allow for test results indicative of later operation behaviour and it must not reduce the quality of the sensor wafers concerning assembly and operation. The latter condition has to be regarded under the constraints of the assembly steps to follow after quality testing. While wire bonding in the case of electronic chips or strip detectors has been observed to suffer only very little from environmental dust deposition, the necessity for homogeneous metal deposition and the very small size of bump pads make dust particles a critical concern for sensors later to be bump bonded using solder or indium bumps.

For this reason all testing, handling and storage of sensors still to be assembled is done under conditions as dust free as achievable with relatively easy means. In the case of the Dortmund laboratory, two laboratory rooms have been converted into clean rooms, with controls for air pressure, temperature and humidity and a filtered air supply. All equipment and furniture within those rooms has been selected not to produce any dust and human operators are required to wear protective

coats, shoes, hair nets and sometimes gloves, minimizing added dust from clothes, hair and skin. The clean room clothing is kept within air locks at the entrance of each clean room, which additionally serve to limit dust coming in from the outside. For this purpose the air pressure within the rooms is always kept higher than on the outside, blowing floating dust particles out of any openings possibly remaining instead of allowing it to accumulate.

Using these relatively simple methods, hindering the testing effort marginally if at all, a clean room quality of < 1000 particles/m³ as measured inside the Dortmund clean rooms could be achieved.



Figure 3.28: Climate chamber with sealed cable openings, set-up for wire bonded test devices and sensor for temperature logging

The basic humidity control provided by the clean room controls can also be used to prevent problems with moist wafer surfaces, leading to additional surface currents, artificially producing high leakage current results or even registering as breakdowns. To assess the humidity range potentially leading to this kind of problem, a measurement set-up has been installed within a Weiss SB22160 climate chamber (shown in figure 3.28), for which both temperature and relative humidity could be controlled. Measuring the leakage current of a single chip sensor at a low fixed bias voltage at room temperature, the effects of increasing or decreasing humidity have been studied (see figure 3.29). While next to no impact of humidity can be observed below 60% relative humidity, at higher values the current rises sharply when a current channel on the moist surface begins to form and stays at a characteristic but still rising level when kept for a while at high humidity levels around 90%. When ramping down humidity again the current does not drop instantaneously, but stays high for several minutes, as not only the ambient air but the moist sensor surface has to dry for the current channel to close.

By directly comparing current sweeps for several prototype single chips at different relative humidities and temperatures (figure 3.30) even more can be learned of the potential impact on test results. All of the curves shown are normalized to a temperature of 20 °C according to the formula for bulk currents given below. As can be seen, only in the case of very high humidities around 95% the measured V_{bd} value drops significantly, at around 80% the surface current channel is pronounced enough to add a relevant ohmic component to the measured current, but not enough to provoke an early breakdown. No significant influence of humidity changes below 60% has been observed, leading to a decision to keep the relative humidities in all laboratories and storage areas around or below 45% at all times, to prevent a moisture film forming on sensors and test devices.

The temperature dependence of the different measurements is of importance, as a significant

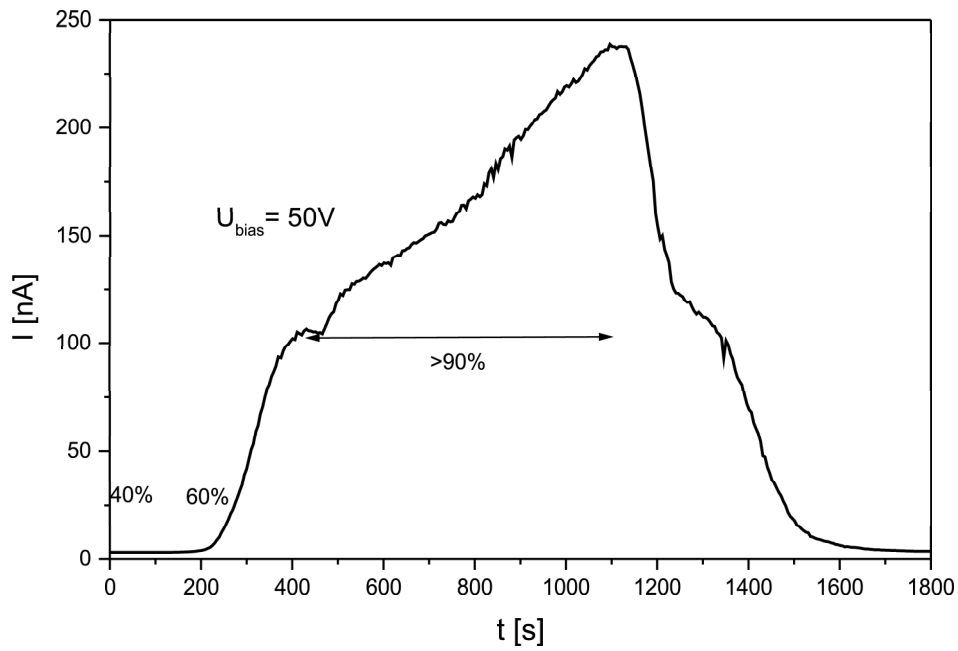


Figure 3.29: Leakage current at $U_{bias} = 50\text{V}$ measured on a sensor prototype single chip while ramping relative humidity up and down

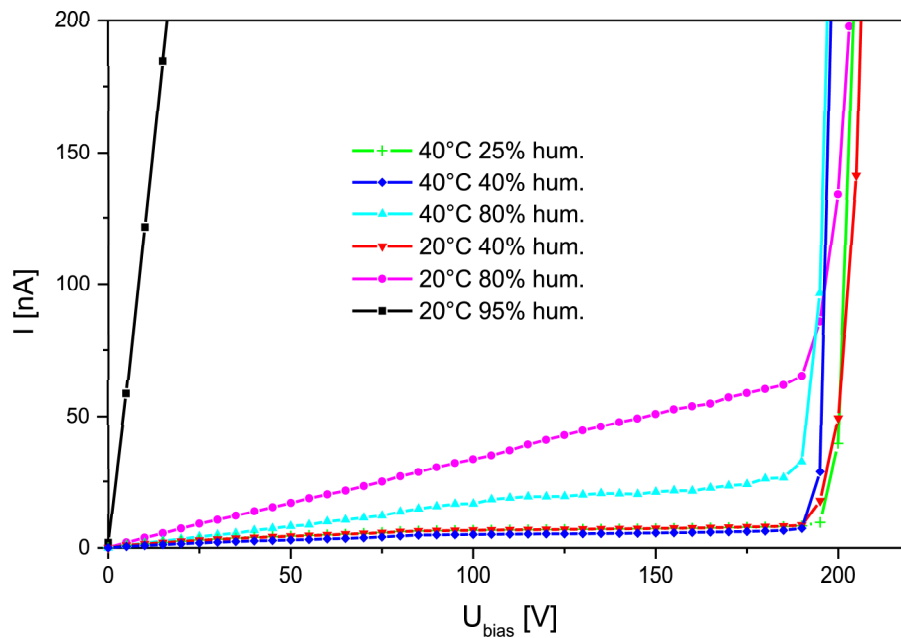


Figure 3.30: Normalized leakage current vs. bias sweeps measured on sensor prototype single chips at different temperatures and relative humidities

influence creates the necessity of either keeping the temperature as constant as possible, or of correcting the obtained data. In most media, at least the effective conductivity can not be assumed to be temperature independent. This is the case for silicon, too, as a rise of temperature leads to thermal excitation across the band gap and increases the number of free charge carriers. Assuming most generation centers to lie near the band gap center, this effect can be parameterized for a temperature T in K as a change of the intrinsic charge carrier density

$$n_i \sim (k \cdot T)^{3/2} \cdot e^{-\frac{\Delta E_G}{2kT}}, \quad (3.20)$$

$\Delta E_G = 1.21$ eV being the silicon band gap width [LUT99].

Most of the current measurement results — neglecting faulty devices with significant ohmic currents — should be dominated by volume generation current within the depletion zone. The temperature dependence of this bulk current can be given as

$$I_{bulk} \sim \frac{n_i}{\tau_g} \sim (k \cdot T)^2 \cdot e^{-\frac{\Delta E_G}{2kT}}, \quad (3.21)$$

as the only temperature dependent factor besides charge carrier density is the generation lifetime τ_g — inversely proportional to the mean thermal velocity v_{th} — [SPE65]

$$\tau_g \sim \frac{1}{v_{th}} \sim \frac{1}{\sqrt{kT}}. \quad (3.22)$$

Therefore volume currents measured at a temperature T can be normalized to a set temperature T_N by using the formula

$$I_{bulk}(T_N) = I_{bulk}(T) \left(\frac{T_N}{T} \right)^2 \cdot e^{-\frac{\Delta E_G}{2k} \cdot \left(\frac{1}{T_N} - \frac{1}{T} \right)}. \quad (3.23)$$

When interface generation currents are being tested for in a current vs. bias sweep — even if it is not the dominant current contribution, the temperature dependence of I_{ox} has to be considered. Here the other factor besides n_i , the recombination velocity S_0 , scales with temperature as [GRV66]

$$S_0 \sim v_{th} \cdot k \cdot T \sim (k \cdot T)^{3/2}. \quad (3.24)$$

As a resulting normalization formula this yields

$$I_{ox}(T_N) = I_{ox}(T) \left(\frac{T_N}{T} \right)^3 \cdot e^{-\frac{\Delta E_G}{2k} \cdot \left(\frac{1}{T_N} - \frac{1}{T} \right)}. \quad (3.25)$$

For most other quantities relevant for quality testing, the influence of small temperature differences can be assumed to be small, as has been studied for V_{dep} in [BOR01] for temperature differences up to 36 °C. But, as there is always the possibility of defects being activated or deactivated by drastic changes in temperature, leading in turn to problems when comparing tests performed under conditions differing in this way, decisions have been taken, to measure all devices not having sustained bulk damage as close as possible to 20 °C, and if necessary to normalize to this temperature. In the case of devices after bulk irradiation with high energy hadrons, the temperature should be kept low enough to prevent thermal runaway during all measurements. While sometimes a cool thermal contact to a heat sink like a massive metal chuck can suffice even at room temperature, to simulate realistic operation conditions, this can be done by keeping the ambient temperature in the range of -10 °C to 0 °C and normalize resulting currents for comparison with other tests.

3.4.4 Part identification

For the exchange of testing data and information on movement and status of wafers, tiles and test devices, an identification system and a mode of data storage has to be implemented. Fortunately, a

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basic part identification system is already laid down in the ATLAS collaboration guidelines [BAC99], and only had to be adapted for the needs of the pixel sensor quality plan. Every item used in the assembly of a subdetector of ATLAS is to be identified by a code of fourteen digits, of which the leading ones are 20 for the whole detector assembly. In the case of the pixel sensor, they are followed by a 2 for the inner detector systems, a 1 for the pixel subdetector and 01 for unassembled silicon sensor components. The remaining eight digits are free for definition in a way sensible for device identification, as the original proposal to use three digits after the first four for laboratory identification and the remaining six digits as a simple sequential counter has been modified by the ATLAS pixel collaboration [NET01]. In the numbering system for sensors, the following digit (1 or 2) represents one of the wafer manufacturers, the next three are reserved as production batch numbering for each vendor, and the following two digits a wafer numbering within each production batch.

This leaves two additional digits for device identification, which is defined as 00 for a whole wafer 01-03 for sensor tiles and 04-37 for other devices according to figure 3.3. Beyond this fourteen digit code, each relevant substructure can be identified by an appended number defined in [KLA00]. Measurements performed on either the whole device or a substructure are marked by its full number as well as the three letter identification for the type of test and a sequential number for repeated tests on the same structure.



Figure 3.31: Mask of scratch pattern on sensor tile

To identify the sensor tiles themselves after dicing, possibly even check the correctness of book-keeping after module assembly, each detector tile bears several metallized scratch patterns around its p-side edges (see figure 3.31). Here, sensor vendor (here given as A or B) and tile number are implemented within the mask and part of the metallization, while batch and wafer number have to be binary encoded by the manufacturer by engraving marks into the metallized squares in the center of the scratch pattern. These marks can be cross checked with the wafer stamp at the flat of the sensor wafers and the statements in test data and the shipping manifesto during a first visual inspection.

Each device and measurement is to be uploaded into a common production data base shared with all other ATLAS pixel manufacture and assembly tasks. Upload protocols have been defined for sensor wafer including all their substructures, each type of test as well as assembly and shipment tasks, to allow for a complete documentation of all relevant steps in the life cycle of the sensor up to commissioning in the detector. The devices and all tests performed on them are tagged with their fourteen digit ATLAS identifier and are rated as passing conformance tests, posing general problems or not. To simplify these tasks, a ROOT based program has been implemented in Dortmund to read the original measurement data, normalize and analyze them, to check them against existent conformance criteria and write them into upload files with a correct data base syntax. In complicated cases this automated assessment can not actually do justice to the information contained within the data, but in the hands of competent operators checking and amending its output, it proves a handy and time saving tool.

3.4.5 Shipping and handling

Not only the more delicate pixelated n-side, but also the guard ring structures, contact pads and implantations on the p-side are bound to be damaged by scratching or residue and have to be handled with care and using appropriate tools. As already described, wafers and test devices are

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places on clean teflon and steel chucks p-side down and are tested, stored and packed in a dry clean room environment. Laboratory personnel has to wear tight fitting clean room gloves whenever operating a probe station or manipulating a wafer or test device, and only clean steel and teflon tweezers are being used for the latter task. These are either broad enough to grip the whole wafer flat, to grip a whole wafer without exercising too much torque leading to possible cracks in the wafer, or small and elastic to grip a single test device at an edge. Vacuum tweezers are explicitly forbidden, as they leave rubber residue on non-passivated parts of the surface.

During shipping and storage, i.e. whenever not actually under test, all wafers and test dice should be kept within closed containers, only touching elastic or soft, dust free surfaces. These containers should close tight against dust from the outside, as they are used to be carried around outside the clean room environment. To avoid transportation mishaps shock absorbing material is to be used, and especially when closing the containers, stressing the wafers or diced structures has to be avoided. In shipping boxes holding several wafers, they should be spaced widely enough to allow for easy manual packing and unpacking, and around the shipping boxes enough packaging material has to be added, as experience has shown that a significant amount of damage to the packages can be caused by rough handling during shipping. Another consideration during shipping and storage is clear labeling as discussed in the paragraph above.

Finally, as the storage takes place in a controlled environment, temperature and humidity at the laboratories poses no problem for most wafers and samples. Irradiated samples have to be kept cold (i.e. below 0 °C) to avoid uncontrolled annealing. Therefore the temperature of such samples during shipping or longer measurements outside a cool environment should be logged to gauge the expected effect on annealing. For wafers and samples being shipped often between locations with differing climates a possible higher humidity and slight mechanical stress has to be taken into account — and therefore unnecessary shipments avoided.

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4 Results of quality testing

The amount of specific data potentially gained on the manufacturing process and the individual wafers from an extensive testing plan, although favouring high throughput over maximum accuracy, is immense and hard to digest within the day to day work of the collaboration. For this reason the following sections focus on highlighting the effects of a systematic quality plan on the understanding and improvement of the manufacturing process. This selection of topics provides justification for the scientific and technical effort made for systematic quality testing as a conclusive way to improve and control detector performance, as well as documentation from the physics point of view of the principles used and relevant insights gained by this effort on several aspects of sensor behaviour.

The data used were gained during the testing of prototypes for manufacturer qualification as well as during pre-series and main series production performed by two manufacturers. The ATLAS institutes taking part in these tests are the New Mexico Center for Particle Physics at the University of New Mexico in Albuquerque, the Lehrstuhl Experimentelle Physik IV at Universität Dortmund, the Fyzikální Ústav at the Akademie věd České Republiky in Praha and the Gruppo collegato di Udine I.N.F.N. at Dipartimento di Fisica dell'Università di Udine. For confidentiality reasons the sensor manufacturers are not to be named in printing, but are only identified as vendor A and vendor B.

4.1 Consideration of errors

This being a study of the reliability of sensor design and production and most of all of the effects of the quality plan designed, implemented and overseen in the course of this work, the role of error consideration differs somewhat from its role in a test program aiming for a specific quality under controlled conditions. The main source of error on a specific derived value consists of variations between the devices under test, a clearly systematic error independent of the statistics accumulated — and an acceptable one given the variations staying within the specified requirements. Similarly, variations between set-ups and testing conditions at the different measurement sites are systematic in nature. These have been tried to be minimized by using similar measuring devices and cross calibrating between the laboratories. In cases of persistent systematic differences between laboratories, those have been documented and their distribution considered when assessing the reliability of the gained information.

Due to the largely non-statistic nature of the distribution of measured values, the standard deviation of the mean is usually not considered as a relevant parameter for results, while the deviation of the distribution is a highly useful measure of the consistency of both samples and measurements, as long as the values show a distribution similar to a normal distribution. In cases of highly asymmetric distributions of values or groups of extreme outliers, those are mentioned, intervals and typical values given and sometimes means and deviations provided for sub-samples obviously showing systematically different behaviour.

4.2 Mechanical characteristics

The mechanical and optical requirements of the sensor wafers are relatively straightforward to describe and by and large represent obvious indicators of a high quality production process complying to the requirements of the ATLAS pixel detector. The very lack of technical parameters and intricate standard procedures for assessments of qualities not tied to an electrical measurement necessitates the consideration and definition of additional procedures and techniques of how to arrive at results

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comparable between the ATLAS laboratories and indicative of specific problems in the production process.

4.2.1 Visible residue and damage

One of the most prominent tasks in testing macroscopic characteristics of the whole wafer is the visible check for mask alignment and surface anomalies. At the Dortmund laboratory inspections take place after receiving new wafers and again after the end of testing. This is done on both wafer sides by scanning them on the automatic hollow chuck with microscope mounted video cameras from above and below. Screen shots from these scans can then be stored and studied later and, if needed, repeatedly on a monitor.

The repeated checking of the wafer surface does not only allow for the identification of scratches and residue on the wafer, but also for gaining information on potential sources of mechanical surface damage and dust during handling and measurements. Together with feedback on surface related problems by the contractors doing bump deposition for module assembly this information can even yield insight into small scale damage during shipping, and for each wafer a history of surface quality can be documented, clearly establishing responsibility for scratches and residue, important for contractual reasons concerning wafer replacements and the elimination of process steps dangerous for sensor quality.

The main problems checked for during visual inspection of the sensor tiles themselves are scratches and residue on the most critical parts of the sensor, namely the n-side pixel cells and the p-side guard ring. On the metallized main p-side implantation on the other hand all but the deepest scratches or most extensive residue layers will probably not cause any problems, and the ones caused will become readily apparent in the electrical tests or during probing. So, in these areas only changes relative to the first inspection or peculiarities connected to other measurements have to be considered.

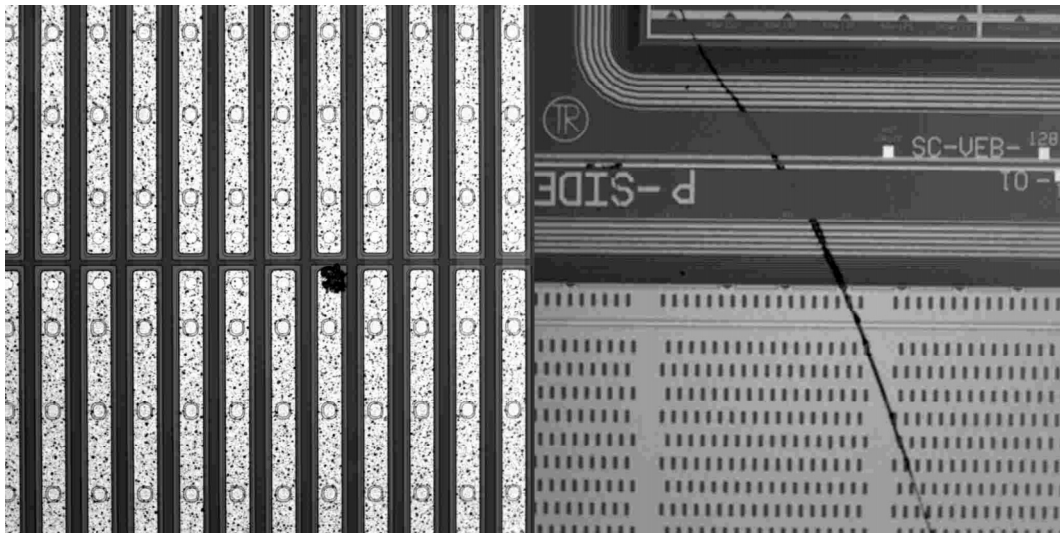


Figure 4.1: a) Particle on n-side obstructing bump opening (left) and b) scratch on p-side damaging guard ring and implantation (right)

Remains of residue across the guard ring structure or the pixel cell surface have to be assessed carefully, as they can not only pose isolation problems, but also block the open vias for bump bonding. These areas are passivation openings at one end of the pixel metallization, which in turn is routed through the oxide layer contacting the pixel cell implantation. As bump bonds are set on an under bump metallization deposited directly on the bump openings without applying any pressure on the pads, even a very thin residue layer can effectively prevent contact. So, residue or dust particles, which can not be easily rinsed away, on top of a bumping via (see figure 4.1a)

will create a dead pixel and will pose a problem in themselves that can not be neglected. Residue covering several implantations but not blocking contact has to be assessed regarding a possible increase in surface currents. If there are larger areas on the wafer covered, more detailed studies can be done on dedicated test structures like the inter pixel or oxide test fields or on single chip sensors not needed for further testing or assembly.

Scratches across sensitive parts of the sensor n-side have to be inspected closely, too, as they can damage the surface to a degree posing problems for metal deposition during the bump bonding process. Therefore scratches close to bump via openings have to be assumed to render the tile problematic for further assembly. Deep scratches damaging pixel cell implantations or guard rings (as seen in figure 4.1b) can again be observed in sweeps of the sensor's leakage current. Damage freshly appearing in the end of testing visual inspection, as it might have been caused during or after the electrical sensor tests, calls for a reevaluation of the sensor tiles' breakdown behaviour.

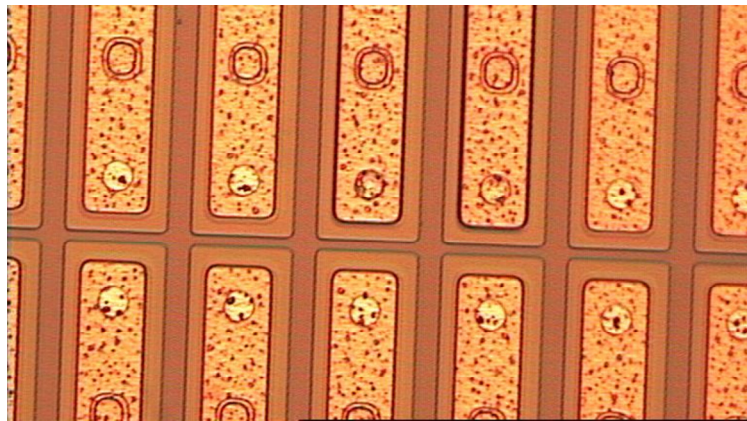


Figure 4.2: Incompletely opened bump openings showing lack of contrast

The contact openings for deposition of bump bonds have not only to be checked for dust and visible residue, but also for effects of incomplete etching, leading to partially or completely closed vias. This problem has come into consideration, after one of the bump vendors found a lack in contrast in a dedicated scan of the contact vias. These scans could not have been easily done at the ATLAS laboratory sites, as it could not be seen in the standard magnification scans (magnification of $40\times$) done for initial and final optical inspection as readily as dust or scratches. To notice the often slight differences in contrast caused by incomplete etching (see figure 4.2) without knowing beforehand where exactly to look for it, would not only have required awareness of the possibility of this problem, but also a set-up either providing a significantly higher magnification or tooled towards a better identification of contrast. Sure enough, the information from the bump vendor gained using a fully automatized contrast scanner, could be verified by inspecting the tile areas in question with a $200\times$ magnification microscope, but performing and checking n-side scans on this scale would have caused an increase of working time by a factor of 25, a drawback deemed prohibitive. As the bump vendors' reaction in effect implied that they would find unopened or suspicious bump openings before metal deposition anyway, and as a possible responsibility for this problem on part of the testing labs could be rejected out of hand, another way to deal with questionable vias has been implemented. The bump vendors have sent back all wafers of dubious quality to one of the ATLAS institutes with a description of the observed anomalies, which can then be cross checked under a high magnification microscope. With this data the ATLAS institutes can then contact the sensor manufacturers to discuss replacing or reworking of the affected sensors.

Generally the visual inspections have yielded significant insight into the surface quality of the sensors and potential problems concerning this characteristic arising during production, shipping and testing. In addition to helping define responsibility for surface damage and production problems and thus clarify replacement claims, in several cases damage done during testing mishaps could be identified, the submission of faulty tiles to bump bonding avoided and handling procedures altered

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to prevent a repetition of similar occurrences. Applying these measures, damage by testing and handling in Dortmund could be minimized to over 95% showing no surface damage save minimal probing marks on the contact pads attributable by the double inspections to in house handling. On the remaining wafers, the accidentally sustained damage could either be identified and its source pointed out to be avoided, or it could be shown to be superficial and of no impact on the sensor quality.

Furthermore, incomplete removal of protective resist layers applied during production could be spotted on a few production batches of both vendors, allowing for timely reworking or replacement without having to bother the bump vendors. The overall quality of the clean room environments and dust sealing of transport boxes could be monitored by the amount of dust particles observed during the individual inspections. In the case of the Dortmund clean rooms as well as the transport containers used both on the way to and from Dortmund a high environment quality could be verified, as no significant amount of dust has been observed in either the initial or final inspections, nor has there been any complaint by the bump vendors about dust regarding the Dortmund wafers.

4.2.2 Mask misalignments

Alignment checks are a regular part of visual inspections, but as misalignments on the scale of $1\ \mu\text{m}$ have to be observed, a higher magnification than in the automatized scans has to be used. With a $200\times$ microscope can not only significant misalignments be identified, but also more exact readings at the vertical and horizontal verniers be taken.

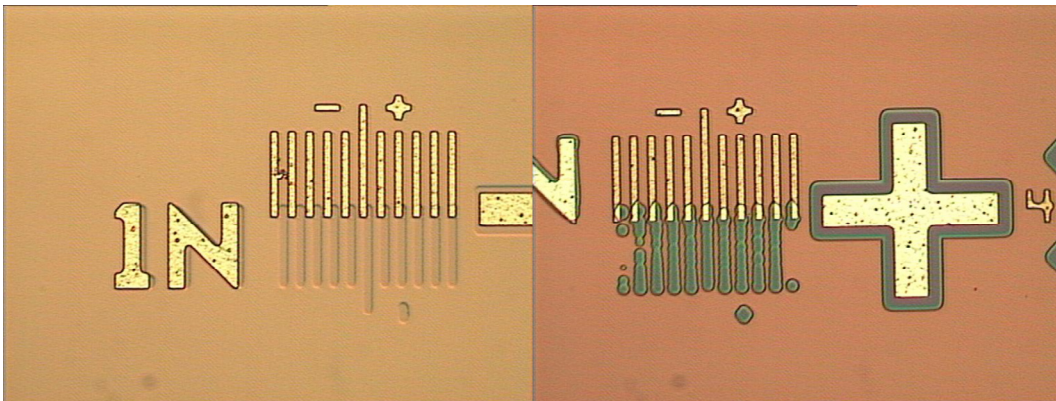


Figure 4.3: Alignment mark vernier showing a) critical degree of misalignment (left) and b) bad implantation processing leading to irregular edges (right)

Among 126 main production wafers from vendor A and 111 ones from vendor B which have been inspected in detail for mask misalignments in the Dortmund laboratory, in 36 wafers from vendor A and 6 wafers by vendor B a misalignment significantly $> 2\ \mu\text{m}$ has been documented (an example is shown in figure 4.3a), as well as wafers from vendor A and ones from vendor B with misalignments $\simeq 2\ \mu\text{m}$. In the case of vendor A all but one of grave misalignments occurred between the metallization and passivation masks, while for vendor B all serious cases were between the implantation and metallization masks, while oxide and nitride openings are usually very well aligned with the implantations, save in one remaining case from vendor A. As the exact alignment of the passivation openings on this scale is only critical for the bumping vias, a comparison of the opening size ($12\ \mu\text{m}$ diameter) with the implantation width ($30\ \mu\text{m}$) has been performed. The collaboration has decided on an unofficial relaxation of the alignment criterion to $\leq 2.5\ \mu\text{m}$ in this specific case, leaving only 8 vendor A wafers to be rejected for non-compliance with alignment criteria. Misalignments of the metallizations or the oxide layer are less straightforward to assess, as they can have effects on the pixel cells, the bias grid network, the multi guard ring and the functionality of test devices. Therefore a cautious approach to quality assurance demands not to relax any other criteria and to reject all 6 vendor B wafers as well as the atypical vendor A wafer.

Another problem becoming apparent during the visual inspections are alignment structures that are not clearly visible. In some cases certain mask layers appear to lack completely in one of the structures, on other wafers some very fine structures like vernier lines are not clearly defined (see figure 4.3b). The number of wafers suffering from illegible alignment structures are 10 from vendor A and 17 from vendor B. Some of those wafers could be ruled conforming on the basis of other, intact structures on the same wafer or showed anomalies in the alignment marks of masks clearly not problematic on other wafers from the same batch. The remaining wafers have been rejected due to other quality tests, rendering a final ruling on alignment conformance unnecessary.

In several cases, especially illegible alignment marks on vendor B wafers and metal vs. passivation misalignments on vendor A wafers, a coincidence with certain production batches has been noted, thus pointing towards systematic problems in the photolithographic mask steps involved for those production runs. In both cases the vendors have been informed as soon as possible of the exact nature of our observations and have been able to avoid similar occurrences in later production.

4.2.3 Methods of planarity and thickness measurements

As has already been mentioned, several different methods for measurements of thickness and planarity have been used by the different participating ATLAS laboratories. In the case of thickness measurements only two different approaches have been taken. Those are a mechanical measurement with a micrometer screw performed on already diced wafer sectors and a capacitive measurement performed with several needle probes hovering above and measured against and across the tested wafer. Only the latter is able to test for differences in thickness between the wafer edges and center. Fortunately, the values gained from both methods as well as the data provided with the wafers (usually by the foundries cutting their silicon ingots and preparing raw wafers) show no significant inconsistency with each other and are within the thickness interval allowed by the quality criteria.

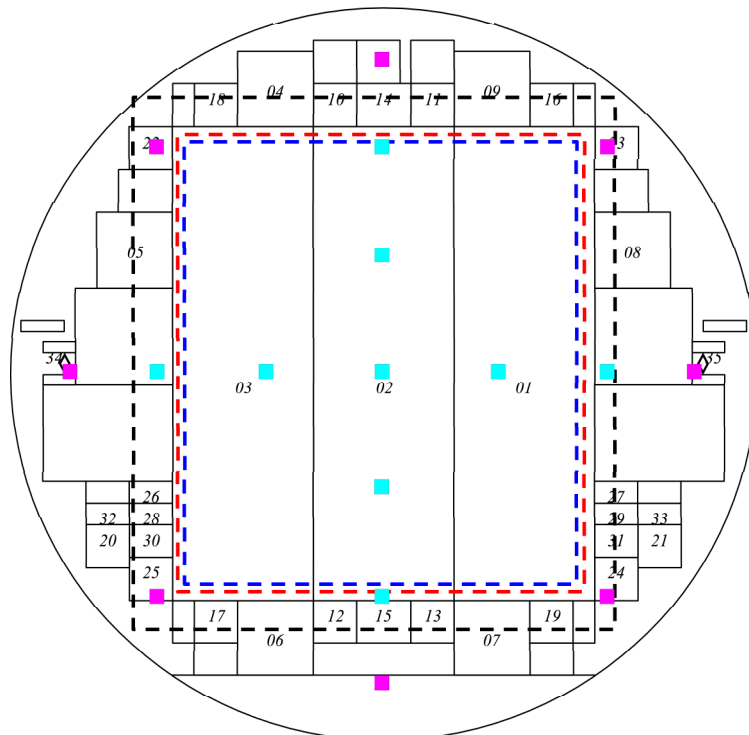


Figure 4.4: Scan patterns of planarity scans performed in New Mexico (points marked by boxes) and Dortmund (areas within dashed lines)

The planarity value has been measured by three of the participating ATLAS laboratories as well as vendor B, which all differ significantly in their measurement approach. The laboratory at the

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University of New Mexico at Albuquerque employs the same capacitive measurement set-up used for thickness tests, in this case not measuring the capacitive effect of the introduction of a wafer of unknown thickness, but the distance of the probes to the wafer surface. The probes used are positioned above the wafer in distinct patterns focussed on the wafer center. The patterns used are one cross shaped small area pattern consisting of nine measurement points and a wide area pattern adding another eight points positioned around the central cross shape (see figure 4.4). The Udine laboratory has set up an optical scan performed on a wafer chuck designed to automatically move the wafer in all three dimensions under a microscope fitted with a video camera while a pattern recognition software analyzing the pictures from the microscope for the wafer position perpendicular to the chuck surface yielding the best focus. Unfortunately, this method can only be performed on wafer areas exhibiting a distinctly repetitive pattern like the active area of the sensor tiles.

The Dortmund set-up is based on a Rodenstock RM 600 Laser Stylus, using a focussed 800 nm laser reflected on the scanned surface to gain data on the distance relative to a calibrated focus plane. The testing head incorporating the scanning laser, the movable lens set-up and the focus analyzing system has been placed above a hollow wafer chuck into a box built of plywood, polystyrene and metal foil, isolating the set-up from external light and changes in temperature. The scan of the wafer surface can then be performed on a square surface of up to $65 \cdot 65 \text{ mm}^2$ (the outermost dashed line in figure 4.4) in 40 lines in y-direction, each consisting of 4000 individual measurement points, producing arrays of 160000 distance values given with a nominal accuracy of 0.3%, leading to errors well below $1 \mu\text{m}$. Using a known alignment of the tested wafer on the scanning chuck, the area relevant for the planarity of the tiles can then be constrained to cover only the tile area of $56 \cdot 63 \text{ mm}^2$ or a smaller $54 \cdot 61 \text{ mm}^2$ area mainly covered by active surface (see figure 4.4 again).

In all these cases the data yielded by the measurements consist of distances from a plane defined by the measurement set-up. These data have to be analyzed to get a measure of the enveloping distance largely independent of the tilt of the wafer during measurement. To achieve this in the case of the Dortmund data, a three dimensional least square fit has been performed on a preliminary area of interest, the data points transformed to represent the coordinates relative to the newly defined central plane and within the final area of interest the maximum distances above and below the plane added up to yield the depth of the envelope. (A measured surface before and after transformation is shown in figure 4.5b & c.)

The different approaches, including an inspection of the wafer planarity using x-ray reflection on the silicon crystal performed by vendor B, could not be assumed to be fully comparable, as they do not only use different measuring principles, potentially producing different systematic errors, but also different scanning points and effective areas of interest. Therefore, the systematic differences had to be assessed, both between the scanning technologies and regarding parameters set for a specific procedure.

In the planarity data taken at Dortmund, most raw scans have been noted to contain one or more distinct spikes consisting of only one measurement point and not linked to any observable feature or residue on the wafer surface (see figure 4.5a) and not exactly reproducible in later rescans. Taking into account the measurement technology used an anomalous laser reflection on the wafer's metal layer leading to an erroneous reconstruction of depth has been identified as the most likely cause for this phenomenon. To correct for single point artifacts of this kind, the scan data of each measurement point are compared with a set of closely neighbouring points before any other analysis step is taken. If the point value represents a sudden step of $\geq 1 \mu\text{m}$, it will be replaced by a depth value interpolated between its neighbours. This very simple smoothing technique successfully suppresses artificial spikes (as seen in the transition between figures 4.5a & b), while no loss of relevant data in this procedure has been observed.

Even corrected for artificially high measurement values, the tile area Dortmund scans have yielded significantly higher results than other procedures, both in direct comparison for tests on the same wafer and on average for wafers from the same production run. This is easy to understand when looking at the scans, as the parts of the scan closest to the wafer edges are contributing highly to the planarity value, as do to a lesser degree small scale irregularities of the wafer surface. Both the Udine optical method and the New Mexico capacitive test with a small area pattern sample either no points along the tile edges or very few points, and both use a measurement method

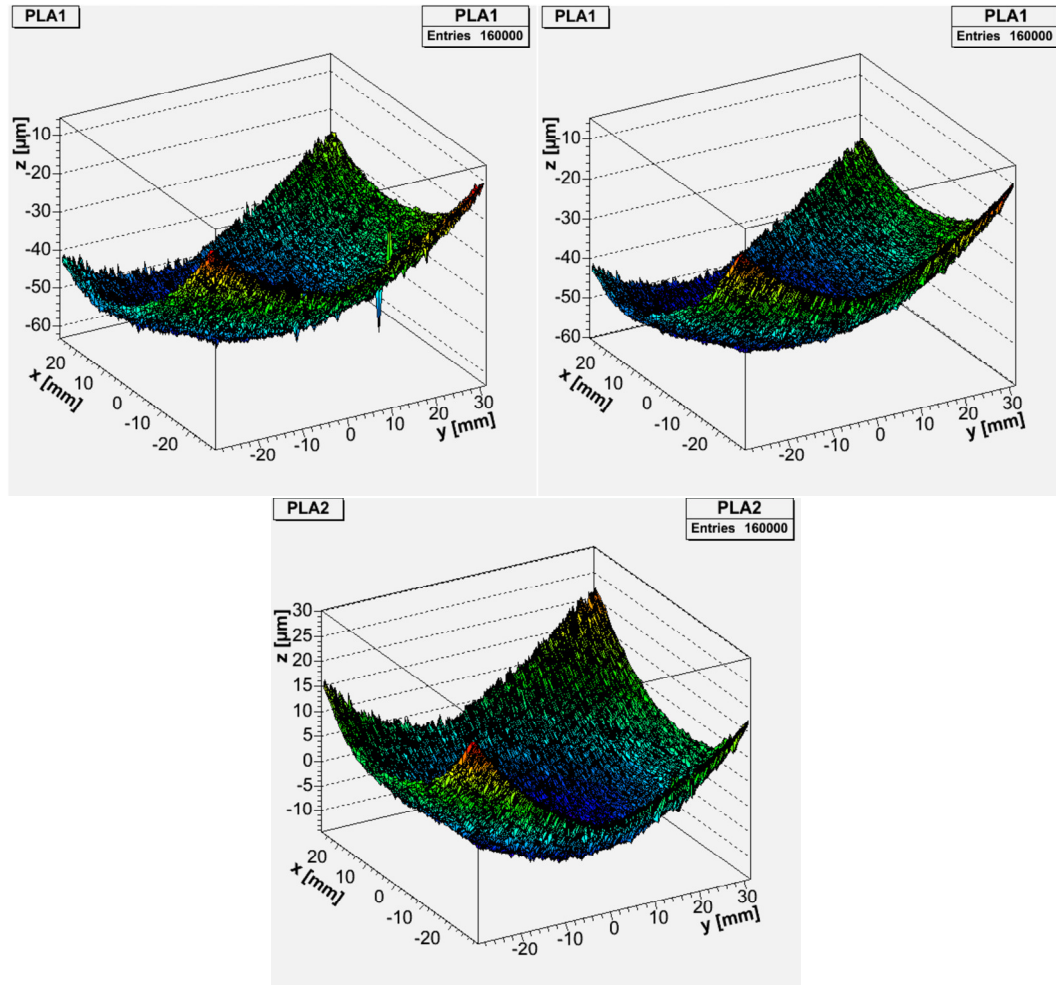


Figure 4.5: Planarity scan data from the Dortmund laboratory a) raw data cropped to a preliminary area of interest (left), b) after removal of single point artifacts (right) and c) after transformation into coordinates yielded by a least square fit and cropped to final area of interest (bottom)

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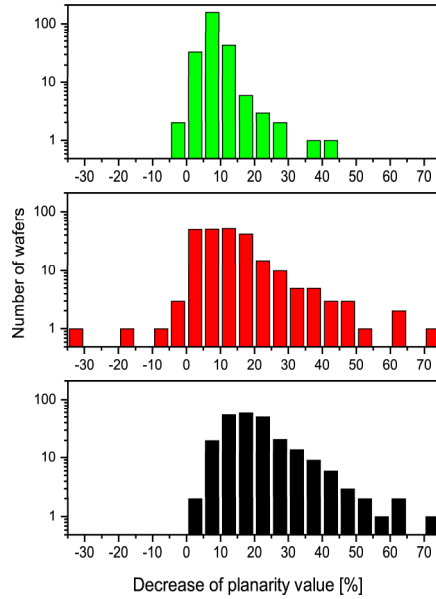


Figure 4.6: Distribution of reductions of planarity values by using filtered small area relative to a filtered full tile area (top), b) unfiltered small area (middle) and c) unfiltered full tile area (bottom)

automatically integrating for each measurement point over a wider area than the tight laser focus (spot size $\simeq 2 \mu\text{m}$). The New Mexico wide area pattern covers points even farther away from the wafer center than the Dortmund scan, but again samples only very few surface spots and, measuring against the wafer surface as whole, is very unlikely to resolve finer surface structures. To provide measurements closer to the data provided by other institutes by suppressing the effects of warp near the wafer edges, the analysis of the smaller area around the active pixel surface has been put forward.

The systematic effects of the different corrections of analyses performed in Dortmund can be seen in figure 4.6, depicting the distribution of relative decrease of planarity values by filtering the data to remove single point artifacts (figure 4.6a), cropping the full tile area to a smaller area of interest (figure 4.6b) and doing both at once (figure 4.6c). The mean reduction of planarity value is $(8.4 \pm 0.3)\%$ with a standard distribution deviation of 4.9% for area cropping alone and $(13.4 \pm 0.8)\%$ with a deviation of 12.2% for filtering alone. In both cases there are wafers actually gaining in planarity value, for area cropping only at a scale of $\leq 0.3\%$ or absolute values of ≤ 0.1 , not above the error expected from our measurements. The filtering process on the other hand produces significantly higher increases in three cases, adding up to 32% to the planarity value, amounting to absolute increases of up to $9 \mu\text{m}$. Looking at these cases, the increase is caused by an atypical enhancement of clustered spikes near a corner of the area of interest. The rest of the filtered surface is both smooth and yields significantly lower planarity values than the unfiltered ones. Unsurprisingly, using both cropping and filtering does not suffer from this problem, as the affected areas are not within the area of interest anymore, yielding a mean reduction of $(20.9 \pm 0.7)\%$ with a distribution deviation of 10.9% and no cases of increased planarity values.

Direct comparison of cross calibration measurements on six different wafers between Dortmund and New Mexico shows results from the latter laboratory to be $(46.3 \pm 2.8)\%$ lower than the filtered Dortmund small area results with a 6.8% standard deviation when using the New Mexico small area pattern and $(8.1 \pm 4.7)\%$ lower with a 11.5% deviation when using the wide area pattern. Within the relatively wide distribution of differences, the approach yielding systematically the lowest results

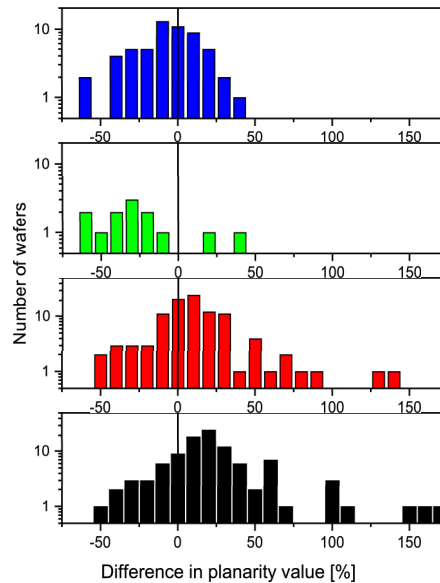


Figure 4.7: Distribution of differences between planarity values provided by vendor B and a) New Mexico small area tests (top), b) Udine tests (upper middle), c) Dortmund filtered small area scans (lower middle) and d) Dortmund filtered full tile area scans (bottom)

for the Dortmund scans appear to be comparable to the full area tests from New Mexico, which unfortunately have been performed only on a smaller sample of wafers than the standard small area tests.

A comparison of measurement values from the different ATLAS laboratories with planarity values provided by vendor B during the main series yields distributions of difference (see figures 4.7a-d) with the New Mexico results on $(6.0 \pm 2.8)\%$ lower than manufacturer tests with a 21.1% standard deviation, Udine measurements $(25.0 \pm 7.7)\%$ lower with a 27.9% deviation and filtered Dortmund scans $(24.0 \pm 3.6)\%$ higher with 36.8% deviation for full area analysis and $(11.7 \pm 2.9)\%$ higher with 29.7% deviation for small area analysis. These distributions confirm the New Mexico and the small area Dortmund values to be relatively well comparable with each other as well as with the vendor data, with both full tile area results from Dortmund and test results from Udine being too far off to be considered as clear indication of compliance or non-compliance. The very broad shape of all four distributions implicates a cautious approach to the vendor data, as they appear to exhibit a behaviour systematically different from any of the institute results and not readily open to assessment by the collaboration. Therefore a sole reliance on the measurements performed by the manufacturers would be dangerous and the tests at the ATLAS institutes have been decided to be continued on as many vendor B wafers as possible, no matter whether provided with or without planarity data.

4.2.4 Planarity related problems

As can be seen in an overview giving a selection of test results on the whole pre-series and main series run for both manufacturers (see figures 4.8a & b), the systematical differences between the testing methods of the laboratories seen in cross calibration are representative of the distribution of the measurement values. Knowing this, the different sensitivity and tolerance of the approaches can be used to judge the wafer quality regarding the criterion for a planarity value $\leq 40 \mu\text{m}$.

As the Dortmund scans are very sensitive for all kinds of planarity related problems and tend to

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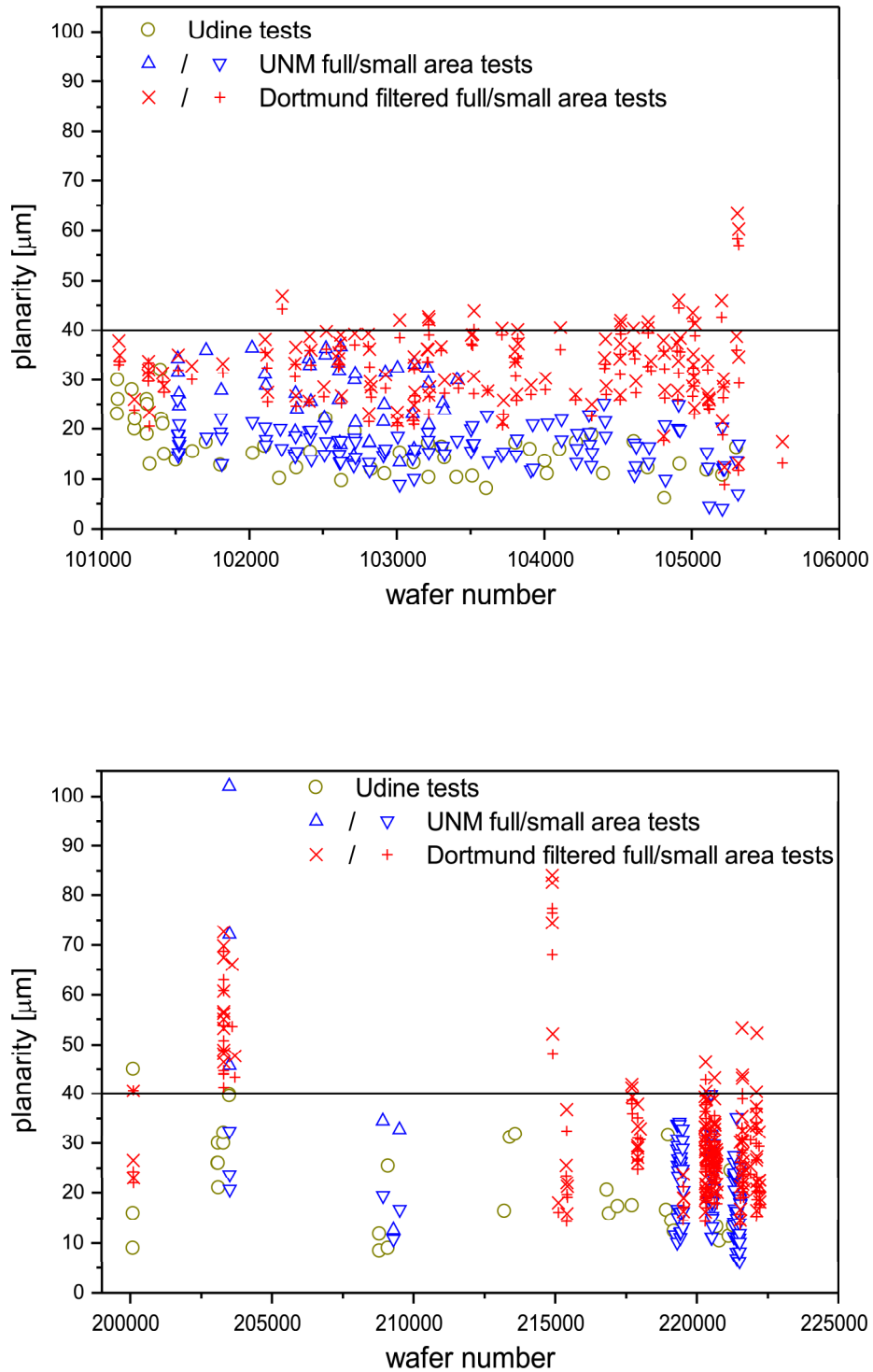


Figure 4.8: Planarity values measured by the ATLAS institutes a) for vendor A wafers (top) and b) for vendor B wafers (bottom)

overstate the planarity when gauged against other methods, a wafer placed below the critical limit by a test performed at Dortmund can be confidently declared conforming with specifications regarding planarity. On the other hand, the small area test performed at the University of New Mexico and the Udine tests are very tolerant concerning some aspects of planarity increase, especially warp near the wafer edges, so a value returned from those measurements above or just below the planarity threshold is a clear indication of a significant problem.

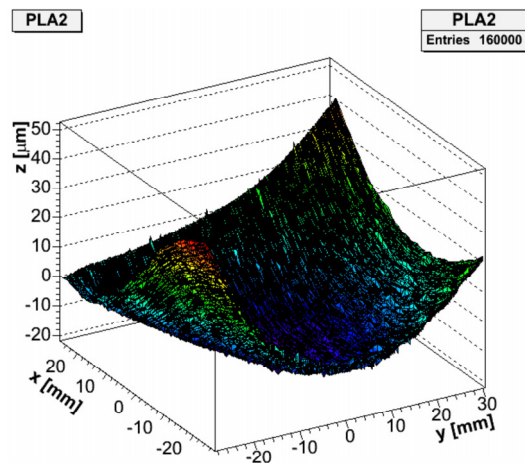


Figure 4.9: Scan of wafer 203303 showing a drastic increase in curvature near the wafer edges

Keeping this in mind, we find no alarmingly high planarity value for any of the non-Dortmund scans among the tests of pre-series and production wafers from vendor A. The Dortmund results show several cases of non-conforming planarity values, but at least considering the filtered small area analysis only two cases drastic enough to be alarming. These two cases, exhibiting planarity values around $60\ \mu\text{m}$ are both from the same production badge and show a uniform, although high bow in all directions, and have shown no non-conforming behaviour in other tests. Other wafers from the same badge have yielded values as low as $12\ \mu\text{m}$, rendering a processing problem affecting the whole production run unlikely. To assess the effects of high bow in the hybridization process and not to put unnecessary pressure on the production schedules, these two wafers have been preliminarily accepted and will be checked again for planarity and bond quality on module level.

The tests on wafers processed by vendor B on the other hand show a behaviour clearly related to production runs, most clearly to be seen during the late pre-series and early main production. In the first case several wafers exhibit planarity values well above $60\ \mu\text{m}$ together with a surface structure sloping dramatically in a warped S-shape near the wafer edges (see figure 4.9). This shape has been observed even on wafers from the same production run with planarity values conforming to specifications and leads to a high impact on the extracted planarity value for methods measuring closer to the wafer edges, as can be observed for the Dortmund and New Mexico full area tests. This could be very easily an effect of asymmetric deposition of surface layers on one or both wafer sides. Another production run affected by systematically high planarity values (around wafer 2149xx) has shown a relatively homogeneous bow but goes up to values around $70\ \mu\text{m}$ and has been tested

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exclusively at Dortmund. This coincided with attempts by vendor B to start in-house planarity testing, first leading to results systematically below even the Udine tests, but later yielding values representative of actual wafer quality (see above). The affected wafers in these two production runs have either been rejected - in most cases failing other criteria, too - or have been kept to perform tests regarding other aspects of the vendor B production process. After feedback on the planarity problems and the introduction of in-house testing, the processing at vendor B has been optimized to avoid an increased bow or warping of wafers by inhomogeneous or one-sided layer deposition, and the remaining main series could be received without any further planarity non-conformities.

4.3 Bulk characteristics

Characterization of the sensor bulk is central to the efforts of the quality plan. Direct control of basic functionality of the sensor tiles as well as two critical diagnostic tests are influenced primarily by the behaviour of the sensor bulk during depletion. Of all the routines of quality testing, data taken on sensor tiles, test sensors and diodes represent the largest overall number of parameters, providing fifteen to eighteen different measurements for each individual wafer. Due to the redundant nature of some of the measurements, e.g. individual current sweeps on single chip sensors not used for further studies, this high data volume can be reduced to several key factors. Among those are the functionality of the individual tiles, the development of tile currents over time, the overall bias tolerance of the wafer bulk considering smaller structures and the growth of the depletion zone.

4.3.1 Sensor tile current sweeps

The current measurements on sensor tiles are indicative of a number of characteristics concerning the bulk and the depletion zones and can point to several types of problems occurring during processing of sensors. As can be seen on a sample of tile measurements from pre-production runs in figure 4.10 several types of behaviour can be identified.

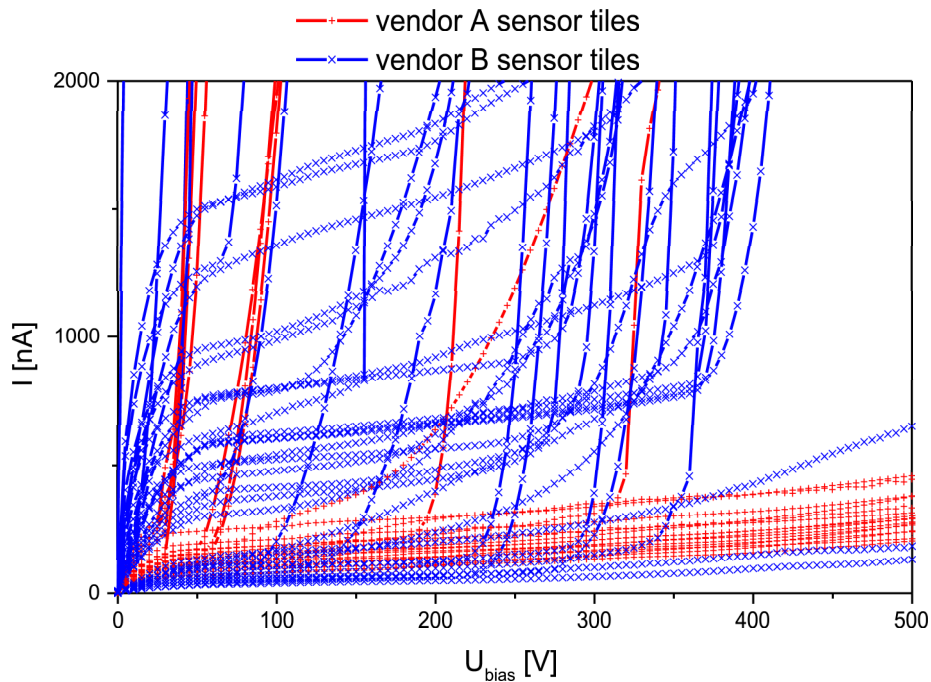


Figure 4.10: Dark current vs. bias voltage curves on pre-series sensor tiles from both vendors

The most conspicuous cases are early breakdowns visible below 70 V. The apparent causes of this behaviour are processing defects in the implantation boundaries, leading to breakdowns as soon as the depletion zone covers the critical area. For V_{bd} values below 10 V this is a clear indication of a damaged p-side implantation. As can be extrapolated from the pre-series tile data, this problem is relatively rare, occurring in only one clear case of the sample shown and one more contender not showing a strong immediate effect, but breaking down before reaching full depletion - both cases on vendor B wafers. This indicates that serious defects in the p-side implantation are either rare

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or are usually spotted easily by the manufacturer and damage the wafer sufficiently for it not to be sent to the ATLAS laboratories in the first place.

Breakdown at or shortly above full depletion is much more common, as can be seen on 10 tiles (16% of the sample) exhibiting breakdowns with $40\text{ V} \leq V_{bd} \leq 105\text{ V}$ on wafers processed by both manufacturers. This behaviour indicates defects at the interfaces of the n-side pixel implantations, inducing avalanche breakdowns as soon as the depletion zone reaches the pixel cells or shortly after. The relatively high number and equal distribution of this type of defects on sensor wafers deemed good by the manufacturers is evidence for localized problems in the processing of the highly segmented n-side masks, apparently hard to avoid even during state of the art fabrication, but without adverse consequences for other structures on the wafers. Breakdown patterns of this type have been common throughout the main production series of both manufacturers, but could usually be correctly identified by the vendor, thus not creating any complications for the ATLAS laboratories or the production schedule. Unexpected breakdowns indicating damage to the implantation interface actually do occur in cases of mechanical damage during shipping and handling, incidents usually traceable due to macroscopic damage on the wafers or containers or by a sudden change in behaviour directly after a shipment or handling task.

Breakdowns at higher bias voltages up to a maximum tested voltage of 500 V are not equally distributed between the pre-series productions of the two manufacturers, but significantly more prevalent in vendor B tiles than vendor A ones. Only three of the latter show any significant increase of current between full depletion and the maximum voltage, and none of them breaks down between 100 V and the demanded pre-irradiation operation voltage V_{op} . Among the vendor B production on the other hand only three tiles do not break down below 500 V and two of those which do, cross the critical value below or very close to $V_{op} = 150\text{ V}$. The modes of breakdown are diverse in both vendors' sensors, ranging from instantaneous catastrophic breakdowns to slightly increased ohmic behaviour after a leveling out of current at a high level after depletion. Still, the most typical kind of breakdown for both manufacturers is an exponential current increase out of a relatively shallow slope after depletion, consistent with a gradual avalanche breakdown.

The overall current level in the sensor tiles before breakdown as well as the current slope after full depletion are other significant differences between the pre-series of the two manufacturers. The behaviour of the vendor A tiles shows normalized absolute currents $< 500\text{ nA}$ throughout the test and comparably shallow slopes for all tiles not breaking down and similar characteristics for two of the three tiles breaking down above full V_{op} . Vendor B tiles on the other hand exhibit current levels ranging between 20 nA and $1.5\text{ }\mu\text{A}$ at full depletion and nearly flat slopes as well as ones sufficient to push the tile into breakdown. Within the vendor B pre-series a clear dependence on production batch and wafer geometry can be observe. All tiles with a very high current level, additionally exhibiting a high linear current rise, are from the first pre-series batch and are tiles situated closer to the wafer edge. Tiles from production runs later in the pre-series are significantly improved in current level and slope, with both tiles showing the lowest and most stable currents being central tiles from the same production batch, but still vary much more widely than their vendor A counterparts. This marked improvement could be achieved after intensive feedback from the ATLAS laboratories concerning the tests on the first pre-series batch mentioning high surface currents due to a faulty realization of the multi guard ring as a possible cause (more on this effect in the following section).

During cross calibration and internal calibration at the ATLAS laboratories it has been shown, that most tested tiles behave in a comparable fashion in all labs and during repeated measurements. But some variation appears to be unavoidable, as can be seen in a direct comparison of test results from the same vendor A pre-series wafer performed at all four laboratories (see figures 4.11a & b). As can be seen in figure 4.11a, the breakdown voltage is excellently reproducible in breakdowns at full depletions (tile 03 and single chip 08), but less so in other cases showing breakdowns below 500 V. Among those, the biggest discrepancies (single chip sensor 06 and mini sensors 12 and 13) of up to 200 V are caused by linear increasing currents passing the breakdown threshold and not by avalanche breakdowns. The relatively shallow, and in fact well reproduced slope of these currents leads to big discrepancies in V_{bd} for moderate offsets in current level. Errors caused by overall current level can be traced to inevitable discrepancies in the impedance of the measurement set-up,

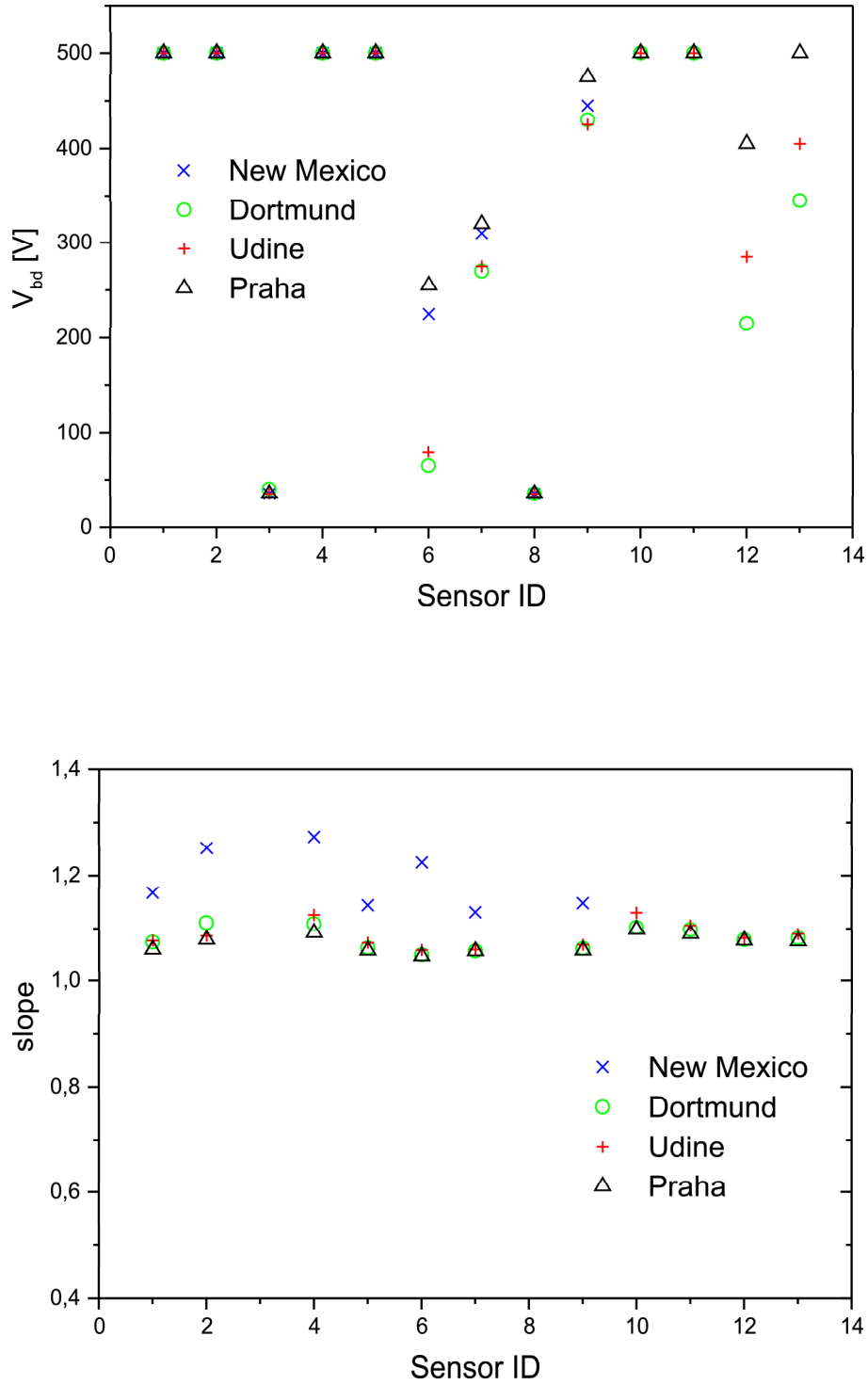


Figure 4.11: Cross calibration results on a) breakdown voltage (top) and b) current slope below operation voltage (bottom)

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humidity in the laboratory and the resolution of the logged temperature data (specified as $\leq 0.5^\circ$), limiting the accuracy of the normalization of current for temperature.

The two remaining cases of avalanche breakdown (single chip sensors 07 and 09) vary up to 60 V. While they appear not to correlate directly with the current level, they show a similar distribution pattern as the V_{bd} caused by linear current increase do. On the other hand, a similar spread of breakdown voltages has been observed in some devices when testing the same device repeatedly in the same laboratory. In these cases current level and slope unsurprisingly turned out to be identical for all measurements within the margin of error. Therefore, though resistivity of the set-up and the device surface might play a role in systematic differences in the occurrence of avalanche breakdowns, the main contributing factor appears to be a change of the field distribution within the device itself, possibly brought about by local changes in temperature distribution and concentration of space charge and interface charge, allowing for the onset of breakdown to fluctuate without any macroscopic change in the device.

The slope criterion on the other hand (see figure 4.11b) seems to be reproduced considerably better between all ATLAS laboratories but one. While the relative difference between the other three laboratories stays below 5%, the New Mexico slope values differ up to 20% from them. In the absence of an area related effect typical for surface currents — and New Mexico being the laboratory with the lowest humidity anyway — the systematic influence of the laboratory might indicate a difference in set-up behaviour compared to the other laboratories not completely understood so far.

The discrepancies observed in cross calibration and internal calibration efforts show potential problems assessing breakdowns occurring above full depletion. The slope criterion, besides being invoked only in relatively few cases, would only be considered problematic in connection with tiles tested as bad in New Mexico, while considered good by the manufacturer — a case fortunately never having become reality so far. Variations of breakdown voltage on the other hand has already been observed in many cases, in some of them (as can be easily seen from the two breakdowns around 150 V in figure 4.10 and sensor 06 in figure 4.11a) changing the conformity status of a tile. Although the slope criterion can help excluding tiles only marginally conforming on V_{bd} , more dramatic changes have to be dealt with differently. While breakdowns at full depletion or below are treated as definitely damaged, breakdowns at higher voltages differing from vendor information are re-measured once or more during the following weeks until a consistent picture emerges. In cases of sensors considered bad by the vendor but tested good, the manufacturer is just informed. If the ATLAS groups are forced to declare tiles delivered as good to be non-conforming, a statement by the vendor will be asked for, whether there is agreement on this decision or further tests on the contentious tile by the manufacturer are requested. For vendor A after re-measuring and feedback, only a total of less than 5% of the tiles delivered as good had to be rejected and replaced, most of them from a problematic production run early in the main production series.

The prevalence of observed breakdowns and overall high currents seen in the vendor B pre-series tests unfortunately carried over into the main production and affected many production batches, leading to a high rate of discrepancies in tile quality and a considerable drop in tile yield, rendering a contractual provision of an equal split between wafers with two and three good tiles impossible to meet. Surprisingly, several of the unexpectedly faulty tiles show breakdowns around full depletion, pointing towards damage to the pixel cells' n-n⁺ interface after vendor testing, possibly during handling or an internal re-work. But in most cases breakdowns around operation bias have been observed, thus being easily influenced by small variations in testing set-up, conditions and sensor characteristics, stressing the importance of repeated testing — at least one test independently confirming the manufacturer's information — to allow for the still slightly changing properties of silicon pixel sensors.

4.3.2 Current stability in sensors

The stability of the bulk current, and thus the relevance of the short term current vs. bias test, has not been tested on every wafer, but a sample of each batch has been taken, stepped up to at least one measurement per wafer in batches apparently exhibiting problematic behaviour. For both manufacturers by far the most measured tiles show a transient behaviour over the first few

hours, either dropping or raising asymptotically from an initial value to a stable long term current, or showing an overshoot settling down again during the following hours. In nearly all these cases the overall increase, if any, saturates after less than half the measurement time and is low enough not to come close to constituting a non-conformity. This does call into question the accuracy of the absolute current level observed in short term current sweeps, but currents appear to stay within a manageable interval, confirming as intended the absence of a runaway long term increase of current endangering detector functionality. Thus, simple current vs. bias tests results are of indicative value, but cannot be naively extrapolated to represent long term sensor leakage current for accuracies better than 30%.

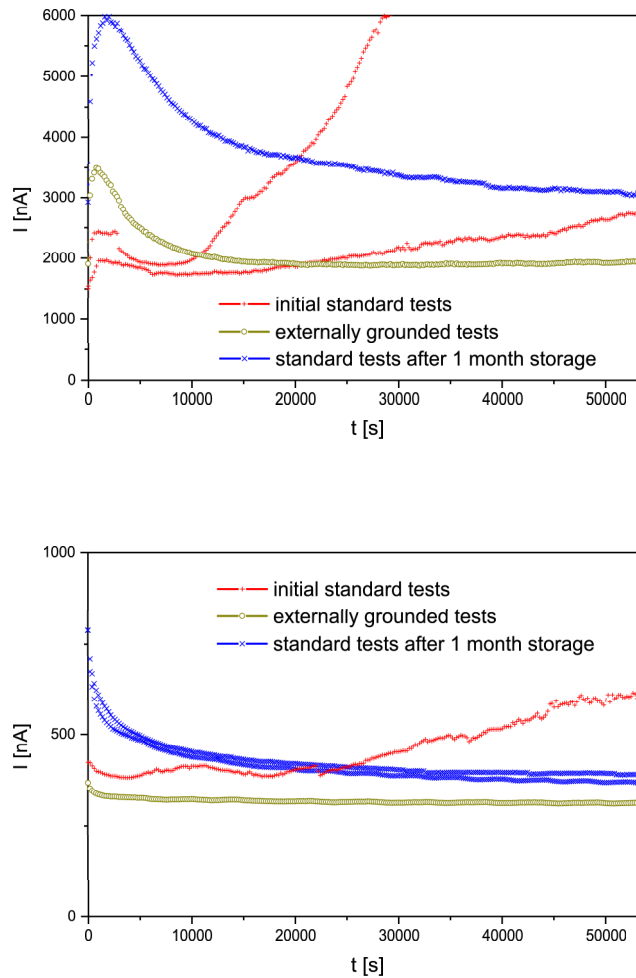


Figure 4.12: Anomalous I - t measurements on two sensor tiles changing after external grounding and a storage period of several weeks a) remaining non-conforming (top) and b) settling within specifications (bottom)

Rare cases of severe instability of the current level have been observed on wafers from an early main production run by vendor B. In several ATLAS laboratories tiles exhibiting a steady increase of current over the whole testing interval after an initial current drop have been measured (see initial test in figures 4.12a & b), in most cases exceeding the allowed increase factor of 1.3, in some dramatically and increasingly so in immediately repeated tests (figure 4.12a). Even in cases staying within the specifications or exceeding them only marginally (figure 4.12b), this pattern is cause

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for alarm, as no saturation is evident and an extrapolation of the current rise for longer depletion periods does indicate the potential for current levels significantly outside the margins tolerable for regular use in the detector. Thus, current stability tests for a broader sample of tiles from the production run in question had to be performed, to find all affected wafers and to avoid the later use of sensor tiles with unstable current characteristics.

As generation of a surface current channel across the guard ring structure is one possible explanation for the increasing current level, tests have been performed to gauge the impact of this factor concerning the current rise. To achieve this, the bulk outside the guard ring structure is set directly to ground by probing with the picoammeter connection onto the sensor bias grid itself and setting another probe needle on a metallized implantation outside the n-side guard ring. As can be seen from the grounded tests in figures 4.12a & b, this change in the test set-up successfully removes all signs of sustained current increases, indicating a dominant contribution of surface currents to the stability problems. An increased level of transient currents before saturation observed in one of the tiles shows additional capacitance and inductivity of the measuring system suppressing external currents into the bias grid and supplying an additional ground contact.

While there is an external n-side ground contact integrated into the module hybrid, a sensor constantly injecting an unknown high level of current into this can not sensibly be used in the detector set-up, although not inducing any additional noise. Firstly, the unknown current, if sufficiently high, will reduce the effective potential drop across the sensor and all other sensors biased by the same voltage source limited by maximum power, thus potentially limiting depletion depth. Secondly, any current through the assembled pixel modules would produce additional heat increasing the difficulties to keep the detector at a constant temperature. Thus the affected tiles could not be declared compliant, but have been tested again after approximately one month storage in a dry clean room environment under constant temperature. As surface current channels could be caused by a conductive residual layer on top of the guard ring structure, a drying process under constant environmental conditions can be expected to influence the current behaviour. As visible in the repeated standard test in figures 4.12a & b, this actually is the case. Concerning all but one of the effected tiles, the new measurements conform with all relevant criteria and show normal current saturation instead of a steady increase in current, although the lack of the additional grounding contact appears to increase the overall current level as well as the amplitude of transient currents. The one remaining tile (figure 4.12a) now exhibits a high transient peak followed by saturation on a level above the $2\ \mu\text{m}$ defining a breakdown in unirradiated sensor tiles. This and current sweeps showing a steep ohmic current rise in the tile in question indicate continuing current channels across the guard ring structure having stabilized during storage, instead of vanished like in the other re-measured tiles. Thus a consequent and flexible use of the tools proposed in the quality plan could verify the usability of all but one of the contentious wafers and prevent a use of a sensor potentially disruptive to detector operation, eventually rejecting the whole concerned wafer due to low tile yield. In reaction to feedback from the ATLAS pixel collaboration, vendor B has introduced an additional drying step at the end of sensor fabrication and no further problems of this nature have been observed.

Long term tests of sensor behaviour after irradiation as well as measurements running longer than 15 h are usually delegated to quality control after hybridization, but have been performed once as a non-standard measurement on an irradiated mini sensor. As intended, using the small test device allows for simple measurements at room temperature without danger of thermal runaway, and alleviate the necessity of using good sensor tiles for irradiation studies instead of detector assembly. A series of measurements has been taken on a mini sensor from a vendor A pre-series wafer after gluing on a kapton carrier and proton irradiation at the CERN PS up to a fluence of $\Phi = 10^{15}$ (1 MeV neutron equivalents)/ cm^2 . Seven consecutive tests have been performed at a bias of 150 V, five of them lasting for approximately 24 h and two, running over a weekend, lasting for approximately 72 h (see figure 4.13). The individual measurements exhibit stable currents after dropping from an initially very high current spike, dropping asymptotically to a slightly lower saturation level, as well as a few additional erratic current spikes apparently representing artifacts induced by external factors like glitches in ground level or power supply. All measurements considered together indicate a slow decline of the saturation current level consistent with the expectation of annealing effects

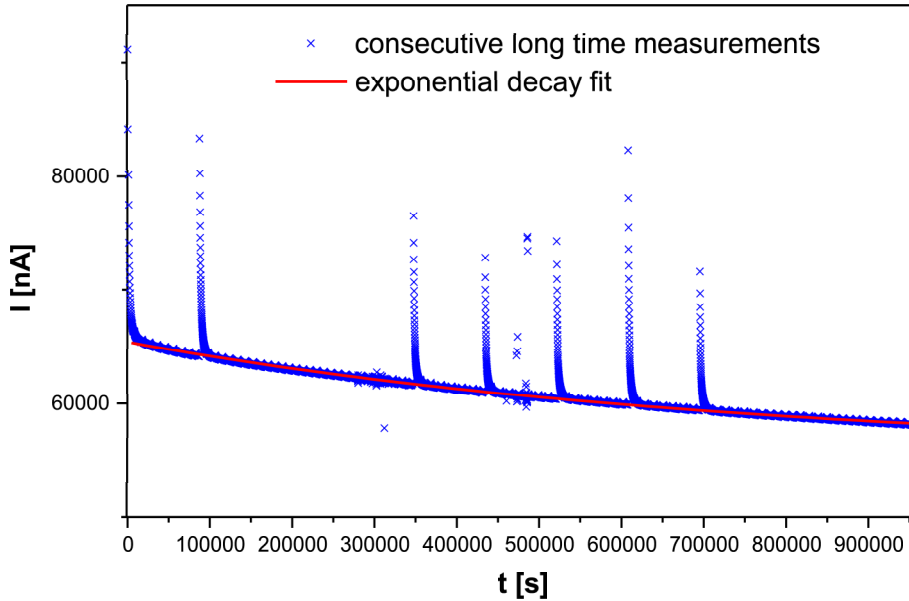


Figure 4.13: Long term current stability test on an irradiated mini sensor showing annealing with exponential fit

at room temperature. Assuming exponential short term annealing to be the dominant factor for the current decrease $\Delta I_{bulk} \propto e^{-t/\tau_i}$, the time constant for room temperature (measured at around 24 °C and normalized) can be extracted. After removing the artificial current spikes from the data set and suppressing high transient currents by only using data taken after the first hour of a new measurement, the best fit yields a time constant $\tau_i = (8.86 \pm 0.02)$ d. This value and the good fit is consistent with a value of $\tau_i \approx 10$ d for room temperature annealing as well as the identification of a simple exponential process as the main shorter term annealing model, both used for projections of the expected radiation effects in the ATLAS pixel sensors [MOL99] [KRA04a]. Thus, the assumptions made for the dominant factors for the annealing of bulk leakage current have been confirmed as realistic for ATLAS pixel sensors.

4.3.3 Current sweeps on test devices

As already seen in the preceding section, small test devices are of significant utility for irradiation tests, but offer other advantages to tests performed only on the sensor tiles themselves. Besides minimizing possible damage to the tiles, testing diodes offers data on the sensor bulk without the influence of pixel cell structures. Additionally the smaller sensors allow for an assessment on the influence of surface area and surface to circumference ratio. Concerning surface area, the statistics on tiles and single chip sensors from prototyping runs in [HÜG01] exhibit a breakdown distribution with early breakdowns roughly scaling with active surface area. This is what can be expected, if localized defects equally distributed on the wafer surfaces are the main cause for early breakdowns. On the other hand, production defects concerning the whole wafer, larger surface areas or specific points on the wafer lay out will produce different scaling patterns.

One of these cases could be observed on several early main series batches from vendor A, showing apparently leaking oxide structures (discussed in the following chapter) and sensor leakage current data with a steep ohmic rise superimposed over the depletion behaviour and relatively early breakdowns, especially in small test structures. This differs not only from a statistic surface area scaling,

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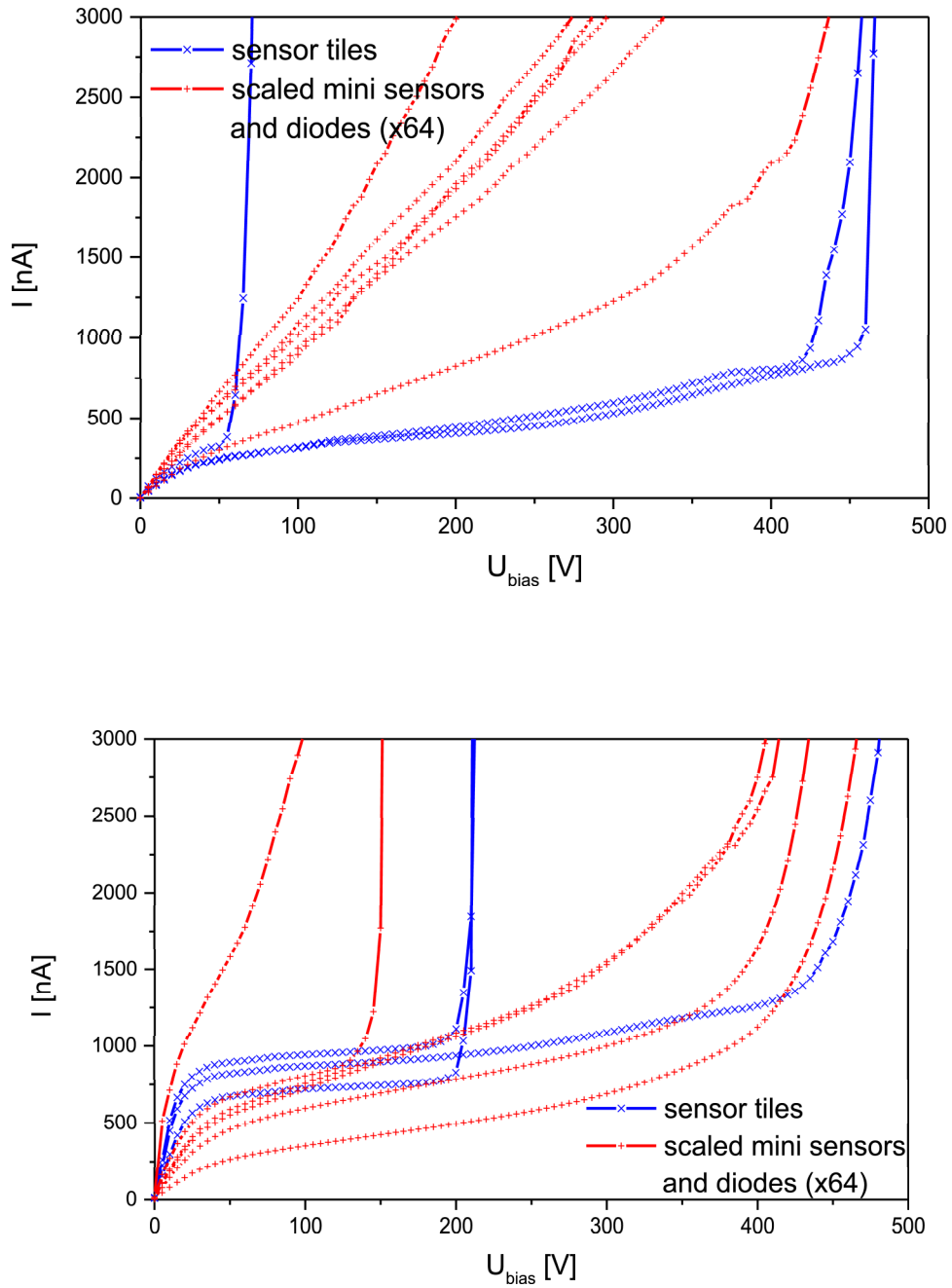


Figure 4.14: Ohmic behaviour in scaled up leakage current sweeps on mini sensors compared to neighbouring sensor tiles a) on a seriously non-conforming wafer (top) and b) on a barely acceptable wafer (bottom)

the current level itself does not scale with device size either. As can be seen in figures 4.14a & b, there is little effect of ohmic currents on the tiles even on the wafer generally exhibiting a higher current increase (figure 4.14a), while mini sensor currents — scaled up for size by a factor of $64\times$ to allow for comparison with tiles — show effects ranging from noticeable but harmless to a dramatic breakdown below full depletion. This tendency of relatively higher influence on smaller structures as well as the ohmic behaviour of most of the additional currents points towards an effect of surface current channels across the guard ring structure, as those will scale with the circumference of the device, or when normalizing for comparable volume currents with the ratio of circumference to volume or surface area.

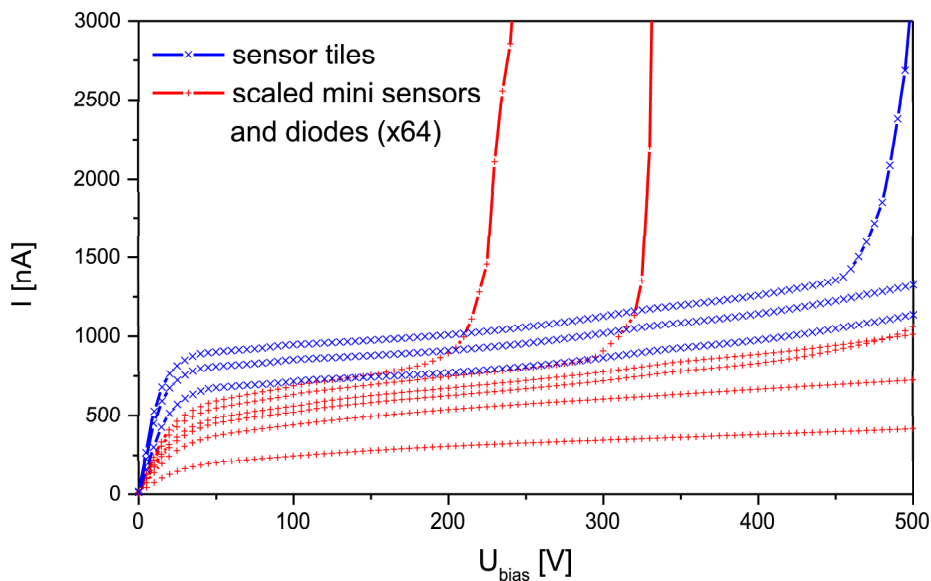


Figure 4.15: Absence of significant ohmic behaviour in scaled up leakage currents sweeps on mini sensors compared to neighbouring tiles after 6 months of storage

Different to the surface currents observed in the long term tests of vendor B tiles, surface currents on the wafers in question do not show a strong time dependence. But based on the assumption of surface currents being favoured by residue containing moisture from incomplete drying during manufacture or from humidity settling on the wafers during storage and shipping, the wafers were stored under dry clean room conditions and those not exhibiting other serious problems remeasured half a year later. As can be seen in figure 4.15, the slopes of the scaled mini sensor currents have become significantly shallower compared to figure 4.14b. Additionally, breakdowns in both sensor tile and mini sensors occur at higher bias voltages, not all of them directly explained by the decrease of surface currents. This could be an indirect effect of a more stable field configuration within the sensor in the absence of currents across the guard ring or an independent effect of redistribution of interface charges by tempering of the sensors leading to a higher bias tolerance also seen in microstrip sensors for the ATLAS SCT [RIC03b]. Given this considerable improvement, a much larger part of the vendor A early main production than feared has been ruled conforming, and feedback to the vendor has led to the implementation of greater efforts in residue removal and wafer drying, apparently eliminating the danger of significant surface currents in later production runs.

Post irradiation measurements on sensors without electronics are exclusively performed on single chip sensors and mini sensors, as they are on diodes, to check for current levels and depletion behaviour according to specifications, as well as the influence of specific conditions concerning

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irradiation and environment. Interestingly enough, no specific check for avalanche breakdown is necessary, as highly irradiated sensors and diodes do not tend to exhibit steep breakdown curves within the range of bias voltages allowed by the detector set-up. This is easily explained by the lowered effective resistivity of the radiation damaged bulk and the decreased effective p-spray dose at the p-spray to implantation interface lessening local maxima in the electrical field.

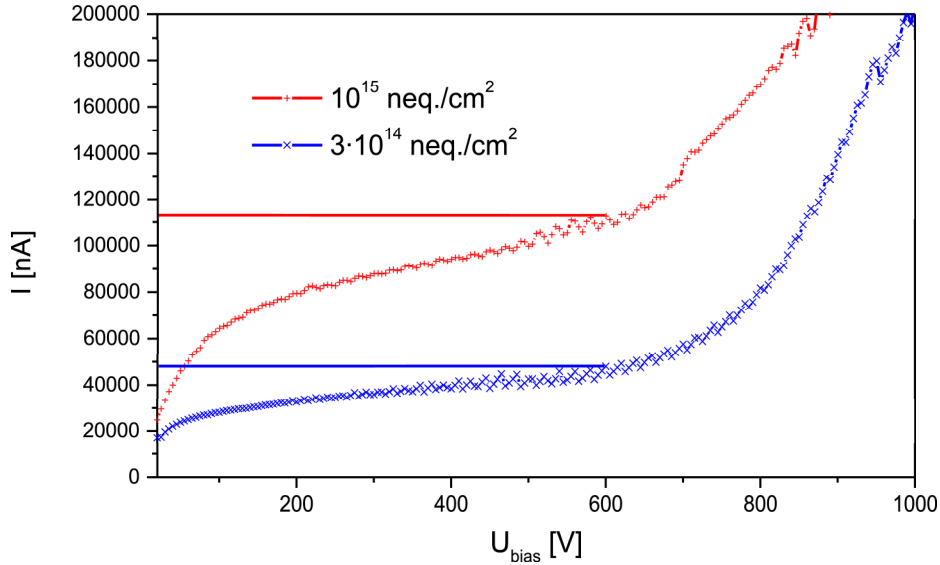


Figure 4.16: Current sweeps to high bias on mini sensors irradiated with high energy protons

Standard current sweeps of irradiated mini sensors include high volt measurements running up to at least $U_{bias} = 600$ V. The sweeps shown in figure 4.16 are performed using a Keithley 248 high voltage supply creating an artificially high initial bias, but allowing for stepping the bias up to 1 kV. The samples, two vendor A pre-series mini sensors, are cooled in the climate chamber during high voltage measurements to approximately -10°C and kept as dry as possible to avoid icing over of the samples. The currents shown are normalized for temperature and have been taken on two vendor A pre-series mini sensors after irradiation with 24 GeV protons from the CERN PS irradiation facility up to fluences of $3 \cdot 10^{14}$ (1 MeV neutron equivalents)/cm² and 10^{15} (1 MeV neutron equivalents)/cm².

The results show a typical current vs. bias curve for depleting devices in both cases, but do not level completely and show effects of slightly asynchronous temperature feedback cycles (a time lag between temperature measured at the resistive sensor and affecting the device under test) and a slow breakdown at $U_{bias} > 700$ V. Due to the incomplete levelling of overall current the bias voltage of full depletion is not readily visible, but from the initial indications of depletion, it is safe to assume full or nearly full depletion at $U_{bias} \leq 200$ V for the lesser fluence case and $U_{bias} \leq 300$ V for the full fluence case. While an exact value is hard to determine and a comparison with an expected value could only make sense in the context of a known annealing scenario, for an approximate annealing of 1 – 2 months at room temperature this is already enough evidence to confirm the use of oxygenated silicon as per specifications. The total current levels at a maximum planned bias voltage of 600 V of $48 \mu\text{A}$ for the lesser fluence and $113 \mu\text{A}$ for the full fluence curve (marked with bars in figure 4.16), are both significantly below the $800 \mu\text{A}$ margin allowed by the specifications for currents normalized to room temperature. While the remaining current slope after depletion and the slow breakdown could be an indication of a less than perfect management of thermal effects

by cooling during the relatively quick ramping of bias — increasing the overall slope of the curve —, this confirms the usability of production sensors after considerable charged hadron irradiation concerning current noise, high voltage power consumption and cooling requirements.

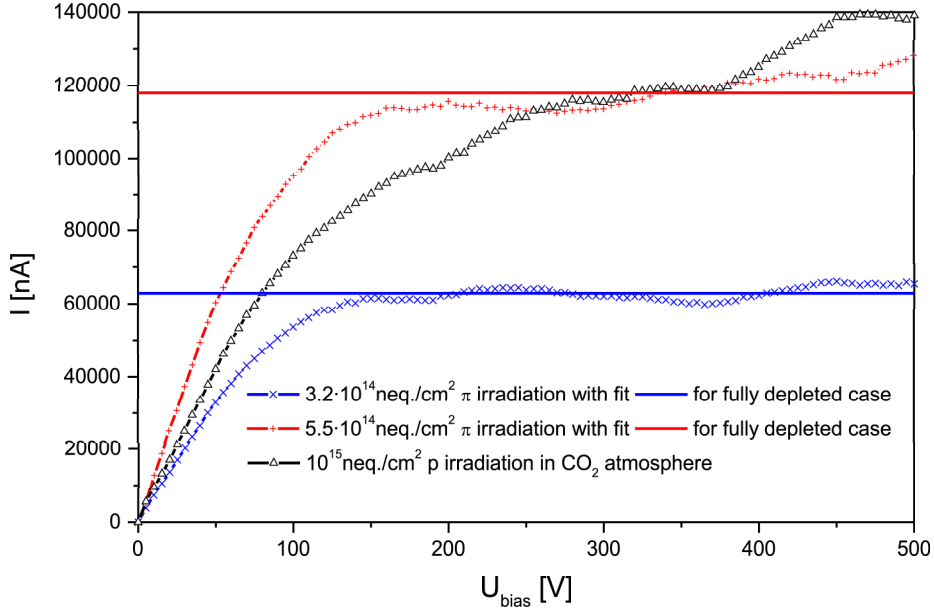


Figure 4.17: Current sweeps on prototype sensors after irradiation with charged pions or with protons in a CO_2 atmosphere

As the most common particle type expected to damage the sensor bulk are charged pions, for a more realistic irradiation test, several prototype single chip sensors (four times the size of mini sensors) have been irradiated with pions at the Paul-Scherrer-Institute (PSI) in Villigen, Switzerland. Two of those samples, one irradiated to an equivalent fluence of $3.2 \cdot 10^{14}$ (1 MeV neutron equivalents)/ cm^2 and one to $5.5 \cdot 10^{14}$ (1 MeV neutron equivalents)/ cm^2 , have been measured at -30°C and the data have been normalized to room temperature. Current levels remain fairly constant after full depletion and surprisingly low at $(63 \pm 3) \mu\text{A}$ and $(118 \pm 10) \mu\text{A}$, partially due to better control of thermal effects at very low temperatures and possibly because of an undocumented beneficial annealing scenario. As both samples have been stored and shipped together, depletion voltage and current level can be directly compared. Within the margins of error, the current values are consistent to a linear scaling with fluence, while the depletion voltage can not be easily extracted, but approximated at $U_{bias} \approx 140 \text{ V}$ for the lower and $U_{bias} \approx 180 \text{ V}$ for the higher fluence. These values are both within the range of expected effects when assuming a minimum of reverse annealing effects. As the irradiation effects of pions in these tests prove equivalent or, if different more beneficial than those from protons, the latter can be confidently used as a conservative scenario in ATLAS pixel detector tests and projections.

Further irradiation studies have been performed to study the influence of gas composition and the use of glues within the detector under constant irradiation from the particle collision products. To simulate the use of other gases besides N_2 and Ar as protective atmosphere within the inner detector cavity, one prototype single chip sensor has been irradiated under a CO_2 atmosphere to an equivalent fluence of 10^{15} (1 MeV neutron equivalents)/ cm^2 to check for any adverse effects. The resulting curve from a sweep taken at -30°C and normalized to room temperature (see figure 4.17) does not show a clearly identifiable depletion voltage, especially no levelling of leakage currents up to 450 V, but a markedly shallower current slope for $U_{bias} > 200 \text{ V}$ and a relatively low current

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level not exceeding $140 \mu\text{A}$. Due to possible differences in annealing history, these values are not directly comparable to other tests, but no significant adverse effects of the differences in atmosphere composition are indicated.

Another possible problem concerning the composition of atmosphere within the inner detector is potential leaking of coolant from the cooling tubes within the detector superstructure into the detector cavity proper. To look for the impact of C_3F_8 coolant, four vendor A single chip sensors have been irradiated at the CERN PS under different atmospheric conditions. One sample has been irradiated to an equivalent fluence of $3 \cdot 10^{14}$ (1 MeV neutron equivalents)/ cm^2 with only traces of $\leq 1\%$ coolant, the other three up to 10^{15} (1 MeV neutron equivalents)/ cm^2 fluence, one in an atmosphere with $\approx 5\%$ and two with $\approx 17\%$ coolant contamination. All four samples have been irradiated and shipped together and thus are fully comparable. The tests on them have been performed at room temperature on a metal chuck working as a heat sink and yield the data plotted in figure 4.18a. Full depletion occurring in the less irradiated control sample can be gauged at $(140 \pm 10) \text{V}$ by the significant levelling of the current curve. The fully irradiated samples do not show as clear a structure, but in all three curves the current slope decreases steadily up to approximately 300 V. The current levels of the three high fluence samples show no systematic differences and fall all within a range of $(700 \pm 20) \mu\text{A}$ at $U_{bias} = 500 \text{V}$. The corresponding current value of $250 \mu\text{A}$ for the lower fluence sample is systematically low compared to the other tests, but the overall current level is consistent with a proportional scaling of leakage current with equivalent fluence when taking into account additional thermal effects for higher bias values. A linear extrapolation of the sweeps on full design fluence samples to $U_{bias} = 600 \text{V}$ would conform to the specified maximum currents per area. Thus, significant systematic impact of coolant leaks on sensor operability can be excluded.

Possible additional leakage currents running through gluing layers are another problem to be inspected by using sensor samples already glued onto flexible kapton carriers as used for module manufacturing. Three mini sensors and two single chip sensors from a vendor A wafer have been glued with their p-sides onto kapton pieces cut out to allow for contacting of the sensor, but with multi guard rings covered with glue using different glue brands considered for later use. These samples have been irradiated to the full equivalent fluence of 10^{15} (1 MeV neutron equivalents)/ cm^2 together with a single chip sensor not glued on kapton as a control sample. Again, all samples have been stored together to keep them fully comparable and have been measured at room temperature using a metal chuck. The values yielded by current sweeps of mini sensors have been scaled by a factor of 4 to gain curves comparable with the sweeps on single chip sensors (see figure 4.18b). All six curves show no clear levelling point indicating full depletion, but decreasing slope up to approximately $U_{bias} = 300 \text{V}$. The scaled up current values from the mini sensors show no systematic differences to those directly derived from single chip sensors and are thus equally indicative of gluing effects. Linear extrapolation of all curves to 600 V fall within the allowed margin, but the control sample sweep exhibits a significantly shallower current slope for $U_{bias} > 300 \text{V}$ than any of the glued samples, indicating the forming of additional current channels through the gluing layers at higher bias voltages. But none of the glued samples, whose current values at 500 V all fall within a range of $(850 \pm 80) \mu\text{A}$, shows sufficiently problematic behaviour to exclude the use of any one glue out of hand, no more than any shows so little effect as to promote its use especially. Accordingly, selections on glue among the tested brands could be made solely based on gluing performance, ease of handling and radiation hardness.

4.3.4 Depletion behaviour

Depletion tests are primarily necessary to confirm the use of the specified material (high resistivity DOFZ silicon) for sensor manufacturing as well as to gauge the correct parameters for setting the correct bias voltages during detector operation to achieve full depletion. To make the capacitance tests as simple as possible, they are taken on diodes instead of structured sensors with bias grids.

The shape of curves taken on ATLAS diodes is less straightforward than those from simpler diodes developed for R&D projects like ROSE, probably caused by the more elaborate guard ring structures. As can be seen by comparison of capacitance curves shown in figure 4.19 taken on

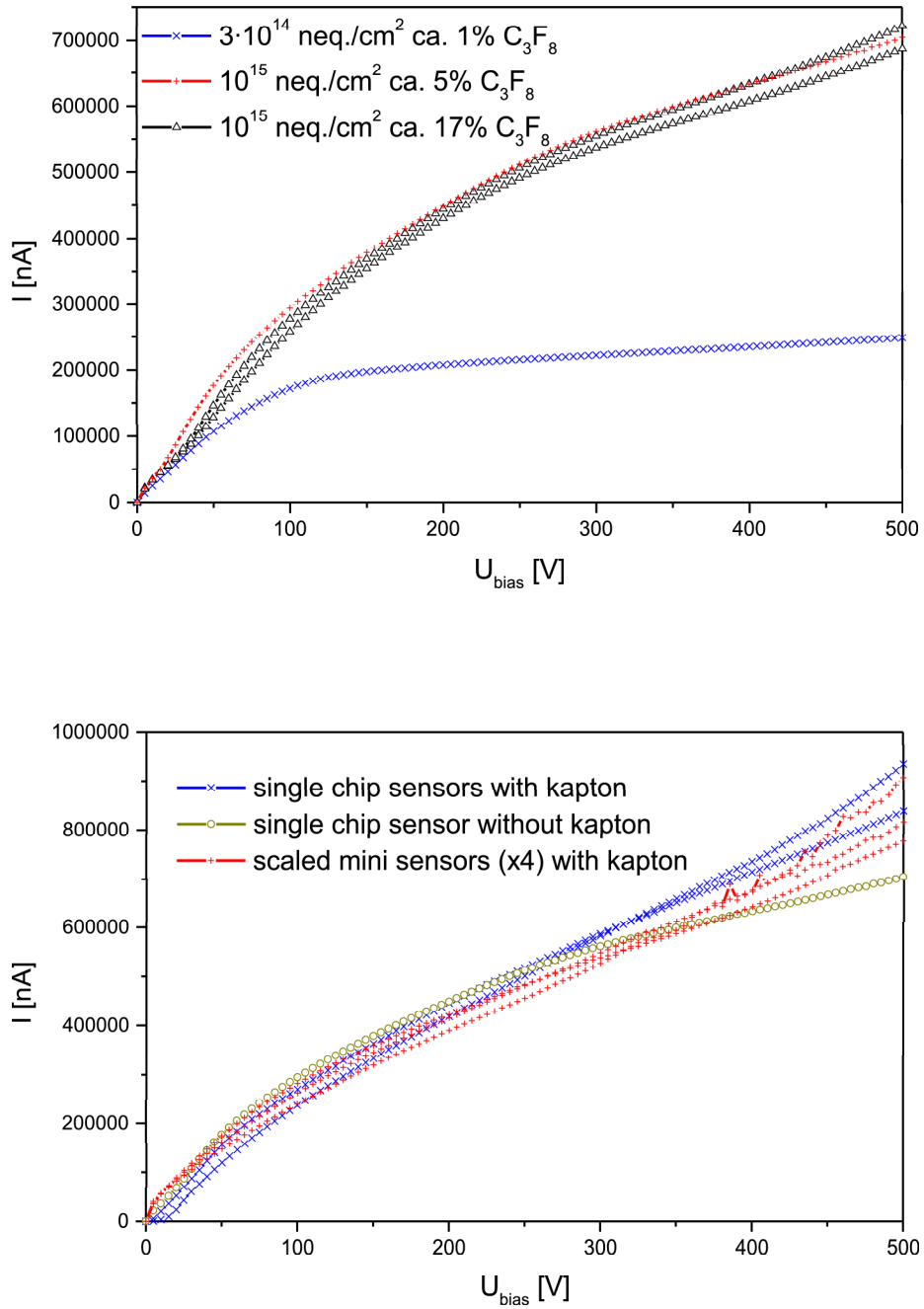


Figure 4.18: Current sweeps on irradiated single chip sensors and mini sensors (scaled up) a) irradiated in coolant contaminated atmospheres (top) and b) glued on kapton carriers with different glue types (bottom)

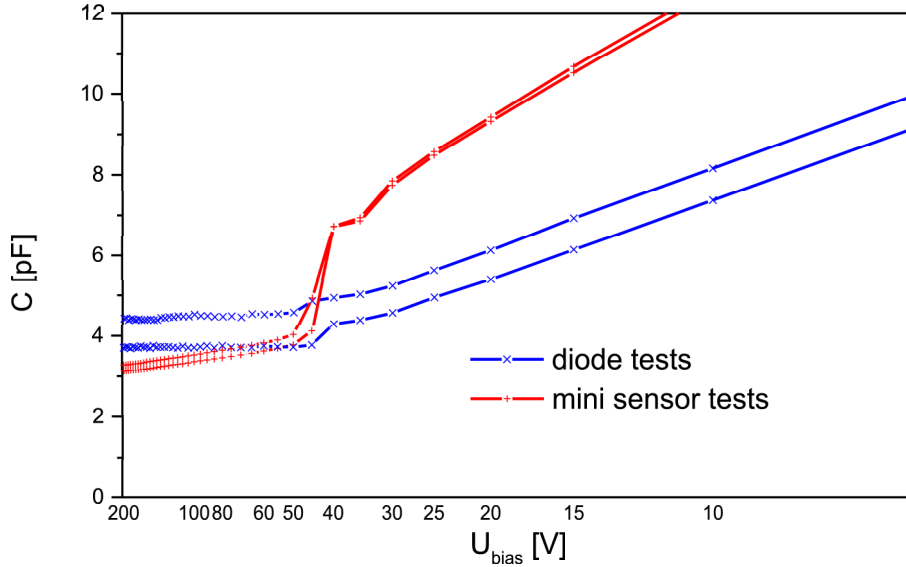


Figure 4.19: Capacitance sweeps on diodes and mini sensors

diodes and mini sensors from the same vendor A pre-series wafer, they also differ considerably from sensor capacitance curves. Both the height of the capacitance drop at full depletion and the capacitance slope before depletion are considerably higher in sensors. Additionally, a second drop and levelling of capacitance at a lower bias voltage can be seen, caused by the pinch off between pixel cells. Importantly, these differences do not significantly influence the depletion voltage V_{dep} , which is consistent within an error of ± 5 V for all devices tested on the same wafer, so it can be confidently seen as representative of properties of the wafer bulk proper. The additional effects stemming from the sensor structure get more dominant when testing irradiated devices, virtually preventing consistent determination of V_{dep} on sensors, a fact increasing the importance of diode testing.

Capacitance tests on diodes from all production wafers, of which all pre-series wafers tested in Dortmund are plotted in figure 4.20, have not indicated any significant problems concerning the bulk material. Nevertheless, V_{dep} values range all over the interval $30 \text{ V} \leq V_{dep} \leq 120 \text{ V}$ allowed by specifications. While the capacitance slope and capacitance level before full depletion are relatively similar for all production diodes, the capacitance level and development above full depletion are varying between production batches and have been shown to heavily depend on the capacitance of the measurement set-up.

While most vendor A wafers show relatively clear and small capacitance drops and cluster towards high substrate resistivity, i.e. low V_{dep} values, vendor B diodes tend towards lower resistivity and vary widely between batches, wafers and even individual structures in shape and capacitance level at and above full depletion even when tested on exactly the same set-up. Especially during the early production runs in the main series this led to several borderline cases of diodes identified as just above the $V_{dep} \leq 120 \text{ V}$ limit, a phenomenon also seen on two vendor A wafers from different main production batches. Nevertheless, no production wafer had to be rejected as non-operable due to bulk capacitance problems and data from vendor B diodes have become more consistent in later production runs.

For a determination of irradiation effects on the depletion behaviour of the substrate and especially verification of the use of radiation tolerant oxygenated silicon, several diodes have been

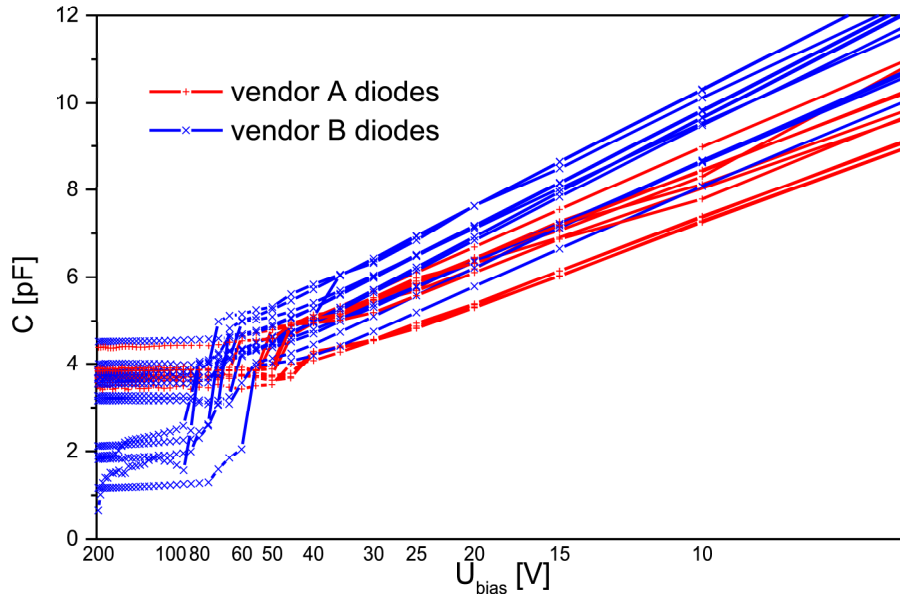


Figure 4.20: Capacitance sweeps on pre-series diodes from both manufacturers

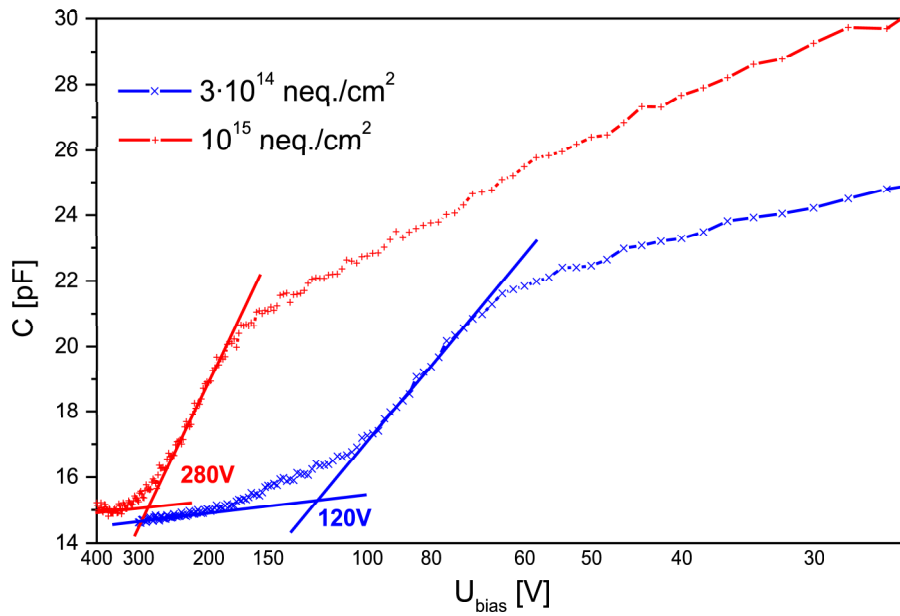


Figure 4.21: Capacitance sweeps on diodes irradiated with protons to fluences of $3.1 \cdot 10^{14}$ and 10^{15} (1 MeV neutron equivalents)/ cm^2

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proton irradiated at the CERN PS irradiation facility. Measurements taken on two diodes from prototype wafers at room temperature (see figure 4.21), have been graphically analyzed to get a measure of the depletion voltage after irradiation and several weeks of storage at room temperature. The sample irradiated with an equivalent fluence of $3.1 \cdot 10^{14}$ (1 MeV neutron equivalents)/cm² yields an extrapolated intersection point between capacitance drop and depleted capacitance level at (120 ± 10) V as V_{dep} . This value conforms excellently with the specified post irradiation criterion of $V_{dep} \leq 200$ V even taking into account additional errors from the analysis and the annealing scenario. The corresponding value for the fully irradiated sample (10^{15} (1 MeV neutron equivalents)/cm²), is $V_{dep} = (280 \pm 20)$ V.

These values are consistent with the models used for extrapolation of sensor behaviour during operation of the ATLAS experiment [KRA04a] as well as the depletion behaviour seen in current sweeps on irradiated devices from both vendors and the operation of irradiated detectors in the test beam. Thus, the bulk material used for sensor manufacture can be confidently considered as exhibiting all the properties needed for prolonged operation within the ATLAS inner detector.

4.4 Interface characteristics

The characterization of the surface and implantation layers as well as their interfaces requires the most diverse category of tests, under which both measurements of absolutely crucial parameters as well as mainly informative and marginal ones are subsumed. This stems from the complexity of the structuring processes on both wafer surfaces — more so on the n-side — and the number of different layers involved in the process. Several of these monitored parameters have proven to shed light on aspects of production quality not explicitly covered by the specifications, as discussed in the following sections.

4.4.1 Oxide breakdowns and surface currents

Tests on bias tolerance of the MOS structures are primarily intended to check the oxide layer for breakdowns and pin holes. Typical breakdown behaviour below the specified voltage of $U_{bias} = 50$ V has been observed only very rarely in structures not already mechanically damaged by intense earlier probing, as can be seen by optically inspecting the contact pads. Any significant density of oxide pin holes can thus be excluded for all production runs.

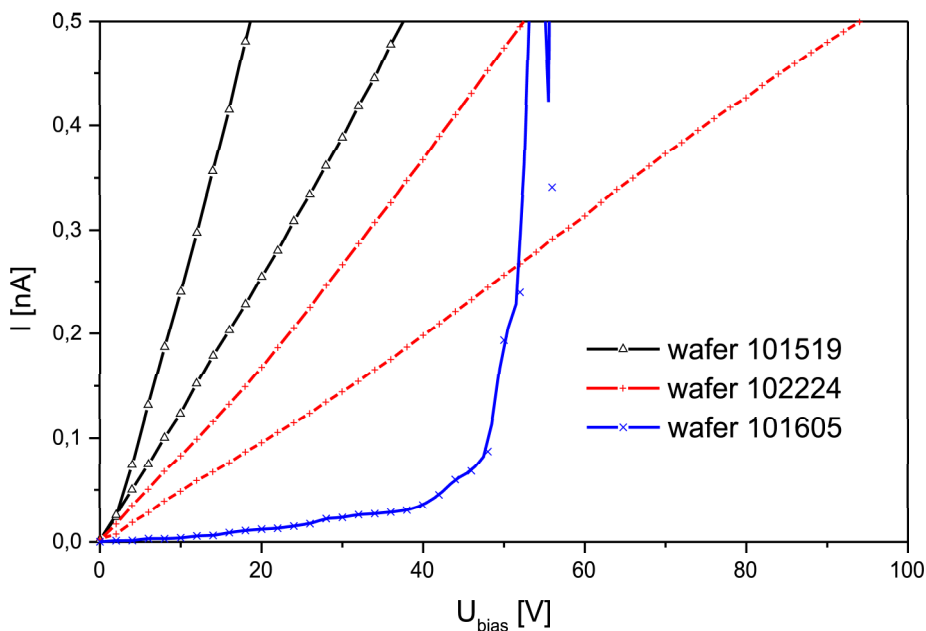


Figure 4.22: Ohmic oxide leakage currents measured on MOS structures from different production wafers

A completely different cause for high currents on oxide test fields has been observed on several wafers, mostly in connection with ohmic currents in sensors and diodes in the early vendor A main series. The currents on the MOS structures in question show a linear rise consistent with an ohmic resistivity (see figure 4.22), and are most easily explained as effects of surface current channels forming in residue on the wafer surface. The sample presented includes two wafers showing linear ohmic currents of different strength as well as one case from the production runs in question exhibiting a rather shallow current rise. The latter rises exponentially into a series of current spikes of increasing height at medium bias voltages, possibly indicating breakdown within the surface channel rather than of the oxide itself.

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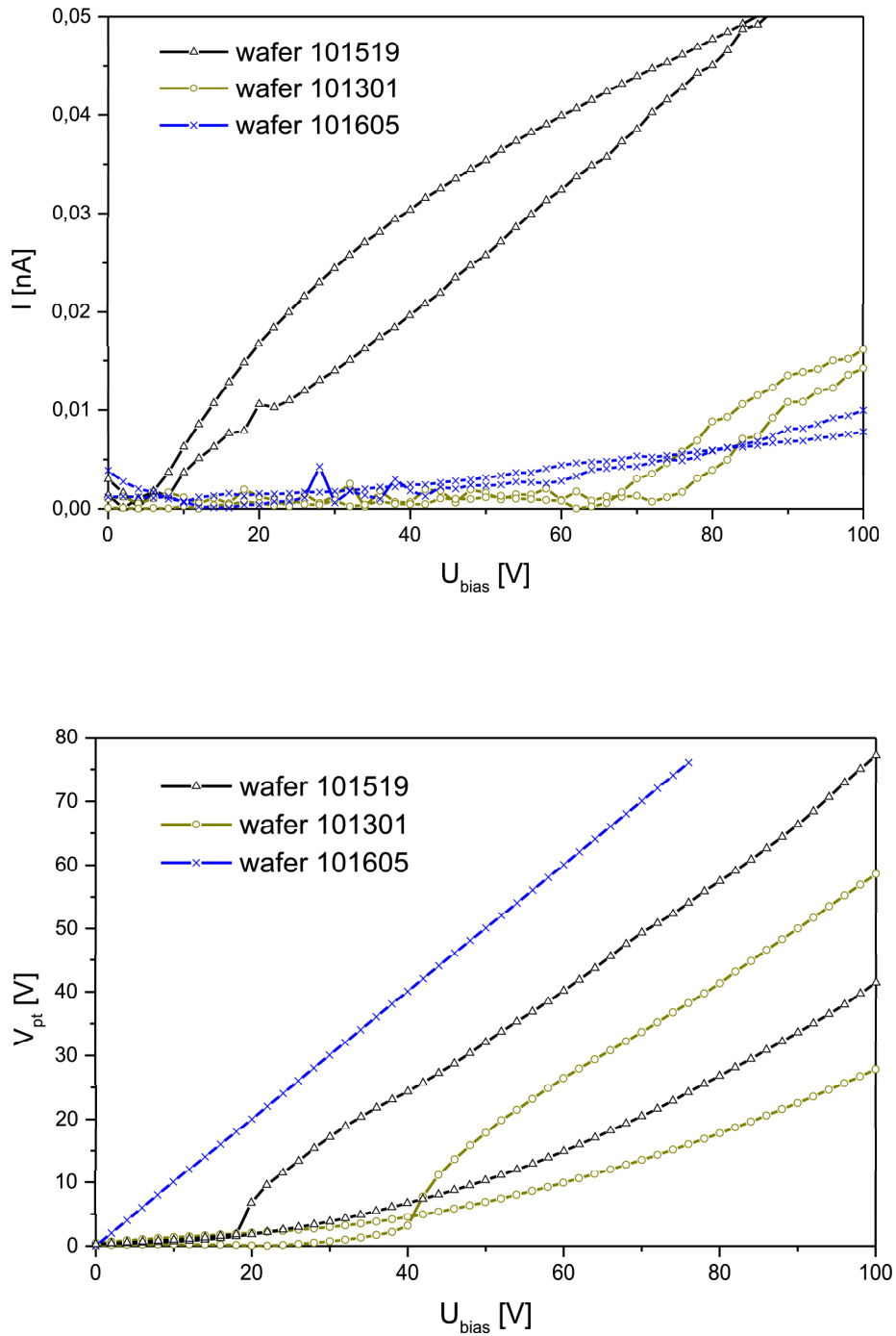


Figure 4.23: Additional tests on two main series samples and a pre-series sample a) measuring current between surface metallizations (top) and b) measuring potential drop across the guard ring (bottom)

To verify this, other measurements not included in the standard test program have been performed on some of the affected wafers. For assessing the prevalence of surface currents, two metal pads on the same p-side oxide test field are contacted and a current sweep between them is taken, without an intervening guard ring or a bulk contact (results in figure 4.23a). For a check on guard ring effectivity the voltage drop between the outermost guard ring and the contact pad within the guard structure is measured vs. increasing forward bias (see figure 4.23b). The results for two of the three main series wafers considered as well as one pre-series sample from a non-conforming wafer, on which some mini sensors exhibit an unusually high current level.

The results of the special tests show a clear influence of surface currents in the case of the more strongly affected main series wafer, exhibiting a steady increase of current between isolated metal pads and a voltage drop across the guard ring significantly below the total bias voltage, providing evidence for an effective resistivity across guard ring structure and wafer surface similar to the one across the non-isolated device edge. The main series sample exhibiting a shallow rise in MOS leakage current and a breakdown shows a slight increase in inter metallization currents as well. The potential drop measured is identical to the bias voltage within the sensitivity of the measurement set-up, confirming a very effective isolation by the guard ring, as long as no breakdown occurs. The absence of any indications of breakdown in the potential difference test show that no permanent damage has been inflicted by the current increase — an effect that would be expected after an oxide breakdown —, and clearly indicate the result of the current sweep not to be reproducible. This may be explained by a changing conductivity of the wafer surface leading to a more uniform voltage drop across the guard ring and no longer inducing local electric fields sufficient for breakdown.

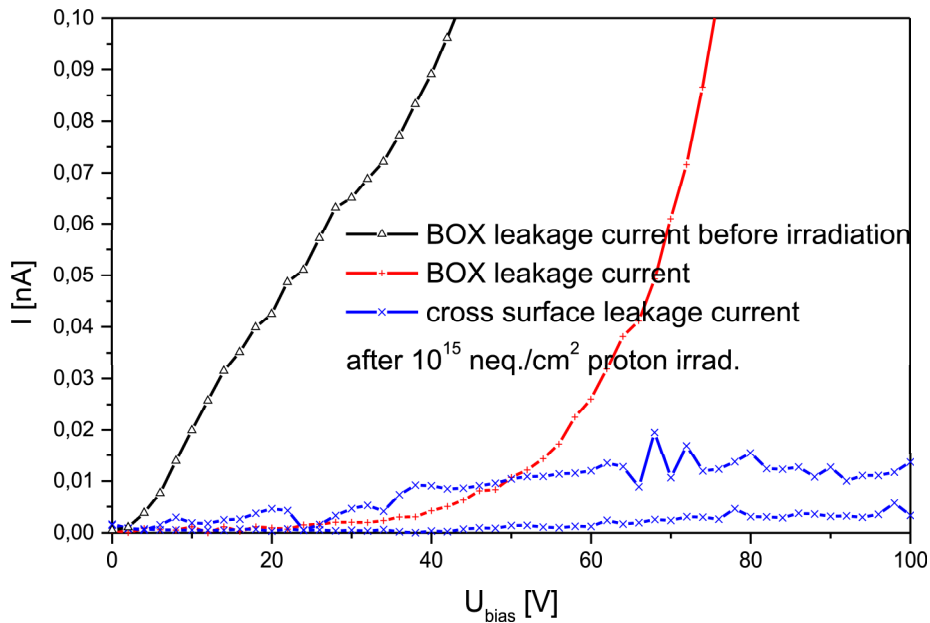


Figure 4.24: Standard MOS current sweep and inter metallization current sweeps after proton irradiation

The pre-series sample exhibits an apparently mixed behaviour, on the one hand showing a current rise for high inter metallization bias only slightly steeper than for the previous sample, but a rather low potential drop across the guard ring. This seems contradictory, but can be explained by local differences in effective surface resistivity, possibly being significantly lower across and near some portions of the guard ring than between the metallization pads. This effect cautions against

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assuming a homogeneous surface conductivity of large parts of a wafer and against generalizing from one type of test indicating insufficient guard ring functionality.

To assess the effects implicated by high currents in oxide test fields, the tests have to be considered in common and in the light of visible influence of surface currents on sensor behaviour. A repetition of problematic tests has shown a beneficial influence of storage in dry clean room environments on current levels on oxide test fields, too, and all wafers finally rejected because of leakage currents in BOX tests are ones exhibiting problematic and persistent ohmic behaviour in sensor and diode tests as well. Oxide breakdown proper as opposed to ohmic leakage currents has not played a significant role for wafer rejection for either vendor.

There is no well known effect of irradiation on surface currents across the guard ring or between metallizations, but to make sure not to run the danger of inducing a dramatic increase of these effects, an irradiated sample has been studied. One sample from an early main series vendor A wafer already declared bad by the manufacturer has been irradiated with protons at the CERN PS irradiation facility to 10^{15} (1 MeV neutron equivalents)/ cm^2 . One standard BOX current sweep and the results of two inter metallization current tests can be seen in figure 4.24 in comparison to a BOX result from the same sample before irradiation. The measurements do not lend evidence to the existence of significant bias dependent surface currents between metallizations. Nor do the changes in leakage current indicate a worsening of the MOS device's guard ring efficiency. The considerably delayed rise of leakage current, looking more like a breakdown across the guard ring than a steady ohmic increase, could be an indication of the less straightforward field distribution of a highly irradiated bulk (as tested and simulated in [KRA04a]) apparently biased in forward direction, but also possible effects of drying during storage, irradiation and annealing. These results are consistent with current sweeps performed on a mini sensor from the same wafer, clearly dominated by high bulk currents and not more problematic in performance than other irradiated sensors not exhibiting ohmic surface currents. Thus the tests allow to exclude significant adverse influence of hadron irradiation on surface currents with confidence.

4.4.2 Flat band capacitance and interface generation currents

Capacitance measurements on MOS test fields are primarily a source for oxide capacitance and flat band voltage as parameters for the assessment of other tests, namely IVG and MFE tests. The COX test is thus usually not an indicator for compliance to production specifications or sensor operability. A defect oxide would show up in the capacitance sweep, as would an oxide of a thickness considerably different from the standard d_{ox} of (150–200) nm. The former would already be apparent in an oxide current measurement, so there is no new information to be expected concerning oxide breakdown. The oxide thickness and homogeneity can be gauged from the maximum capacitance level in the tests. This value proves to be influenced by bad contact and transient phenomena on a freshly contacted device, both identifiable when re-measuring the MOS pad, studying the resulting curve for abnormal shapes or comparing the result with values from neighbouring devices.

After removing obvious artifacts from the measurement sample, three different groups of wafers can be easily recognized from the test results. The measurement curves from all vendor A wafers are all relatively similar yielding an overall distribution of maximum capacitance values of $C_{ox} = (274.0 \pm 6.2)$ pF. The vendor B wafers fall into two categories, one encompassing the pre-series and the first series run with a capacitance distribution of $C_{ox} = (273.2 \pm 16.6)$ pF and another covering the rest of the main series yielding $C_{ox} = (192.2 \pm 6.9)$ pF. The wider distribution of capacitances from the vendor B pre-series is caused by significant variations between wafers. Assuming a dry oxide of uniform thickness and a contact pad area of $A_g \approx 1.77 \text{ mm}^2$, the corresponding oxide thickness values are (194.2 ± 4.4) nm for the vendor A production, (194.7 ± 11.8) nm for vendor B pre-series exhibiting wider variations of values between wafers and (276.8 ± 9.9) nm for later vendor B wafers. These values differ systematically from the process information provided by the manufacturers, which have been stated as being around 150 nm for vendor A wafer, around 250 nm for vendor B pre-series wafer and around 350 nm for later vendor B batches. These discrepancies — interestingly not showing the same systematics for both manufacturers — could be caused by etching regimes differing from vendor to vendor and leading to variations of oxide thickness

between the MOS oxide layer and the oxide tested by the vendors, they also could be effects of different SiO₂ qualities possibly resulting in variations of dielectric behaviour between vendors (see e.g. [LUT99] for differing values for ϵ_{SiO}). A significant variation in the effective gate area A_g of the MOS structures appears unlikely, as a lateral etching variation of this magnitude would have posed significant problems for all smaller metal structures like pixels and bias grids and should be evident in a visual inspection. While these results rise serious reservations on the accuracy of the vendor information and assumptions on oxide properties, they represent correctly the order of oxide thickness, although (20 – 30)% off from the provided data and correctly reflect the relative increase in thickness between the vendor B pre-series and main series.

The flat-band voltages gathered from the capacitance curves are a lot less uniform and thus present no clear categories beyond a slight vendor dependent tendency, yielding a distribution of (4.2 ± 1.2) V for vendor A wafers and (7.0 ± 4.4) V for ones from vendor B. The significantly higher variation in vendor B tests is an effect of the occurrence of drawn out capacitance drops, which are typical of MOS devices having been damaged by radiation. In the latter case, the shallower drop in capacitance is caused by oxide charges near the substrate interface induced by ionizing particles. Some vendor B wafers appear to have suffered from effects during production generating charged defects similar to oxide or interface charges caused by irradiation. This behaviour could not be directly linked with certain batches and does not appear to have any direct impact on sensor functionality. Thus, no wafer has been rejected due to drawn out oxide capacitance drops.

Oxide currents measured on gate controlled diodes are providing information on the density of interface states and provide a cross check on the homogeneity of the oxide characteristics on a wafer as visible from the gate bias needed to produce a flat-band situation under a MOS gate. The IVG tests have suffered quite frequently from high transient currents, artificially increasing the initial current values and thus rendering the results of the measurements inaccurate or even meaningless. As this current overshoot is reproducible in repeated tests — varying in height due to the exact set-up used — but affects only the first point in the data set, a slight change in the data analysis only using unaffected data points can successfully suppress this effect. In many cases the voltage of the sharp current rise designating flat-band voltage differs by up to 2 V from COX results on the same wafer. There are no extreme cases or clear dependence of flat-band voltage homogeneity on vendor, production run or batch, allowing the discrepancies between V_{fb} values to be explained sufficiently by a combination of relatively small variations in oxide thickness and charge concentration and ambiguities due to size of measurement steps. Whenever the bias interval around the flat-band value yielded by the capacitance curve is not reflected by the actual interface current rise, the interval has to be shifted accordingly.

The interface current values show a distribution of (0.46 ± 0.48) nA for vendor A wafers and (0.41 ± 0.30) nA for vendor B wafers. The slightly higher values and significantly broader distribution of the vendor A test devices are due to a higher incidence of oxide current increases of over 1 nA not apparently dependent on batch (in some cases not even on wafer) and not obviously linked to any other manufacturing problems. Two rather likely causes for such behaviour would be either a local concentration of interface defects below the gate ring or defects in the diode junction or bulk itself, producing an abnormally high leakage current not directly linked to the interface quality itself. As no otherwise good wafer has shown consistently high oxide currents above a few V before assembly or irradiation, no rejects have been made due to interface current data.

Intensive studies on effects of irradiative damage to the oxide and bulk interface have been performed at Dortmund during the ATLAS pixel prototyping phase and have been documented in [WÜS01]. Of the results gained in those studies some of the most relevant for later experiments in high radiation environments are the saturation of oxide charge densities at $N_{ox} \leq 3 \cdot 10^{12} \text{ cm}^{-2}$ below a dose of 500 kGy and indications of a similar saturation behaviour at higher irradiation doses of surface recombination velocity responsible for interface currents within a range of $500 \text{ cm/s} < S_0 < 4500 \text{ cm/s}$. These properties appear to be no direct results of any specific silicon foundry production process, crystal orientation, oxygenation or wafer fabrication, and are thus assumed to apply for all ATLAS pixel sensor wafers as limits for the irradiation damage to oxide and interface to be expected.

To assess the direct effects of oxide currents on pixel sensor operation, mini sensors from the pre-

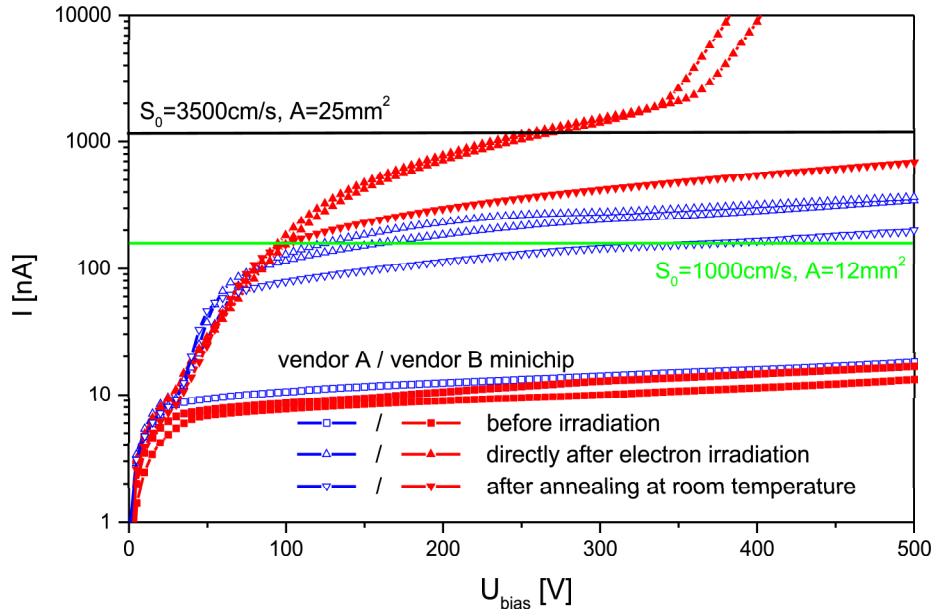


Figure 4.25: Current sweeps on mini sensors irradiated with electrons, before and after irradiation to 300 kGy and 500 kGy and after one week annealing at room temperature

series of both vendors have been irradiated with low energy electrons at the DEBE in steps up to a dose of 500 kGy without affecting the substrate bulk in any way. Current vs. bias measurements on these sensors (see figure 4.25), show a dramatic increase in leakage current, setting in after full depletion i.e. when the n-side interface might start to contribute to the overall current. The current sweeps directly after irradiation show no significant difference between the final irradiation to an integrated dose of 500 kGy and the previous irradiation step to 300 kGy, both included in the figure and confirming the expected saturation behaviour. The two lines drawn for comparison are calculated interface generation current values for $S_0 = 1000$ cm/s and approximately one third of the sensor surface as a relevant area as a lower bound and for $S_0 = 3500$ cm/s and approximately two thirds of the sensor surface as a relevant area as an upper bound of the expected current range. The vendor B sample, which belongs to a pre-production batch under investigation for other leakage current issues, shows currents directly after irradiation surpassing even the latter value and showing a sensor breakdown apparently caused by the field configuration altered by interface defects and the resulting high currents. These dramatic and potentially detector destroying effects are alleviated by annealing during approximately one week storage at room temperature. The annealing of the interface defects also lowers the leakage current of the vendor A sample by about a factor of 2 and brings both samples within the current range agreeing with expected recombination velocities. This confirms the results of [WÜS01], which have been assessed after sufficient annealing, too, and points toward clear limits for the potential impact of interface currents on detector operation.

Current curves similar to the ones derived from electron irradiated sensors have been measured on hybridized sensors after bump metallization or on bare modules [WEB04], exhibiting a sharp but limited current rise setting in at bias values just above full depletion. This indicates the possibility of n-side defects introduced by the metallization process acting similar to interface defects caused by ionizing radiation. But in the case of these additional currents, annealing behaviour seems to distinguish them from radiation damage, often diminishing more sharply over several weeks of storage at room temperature.

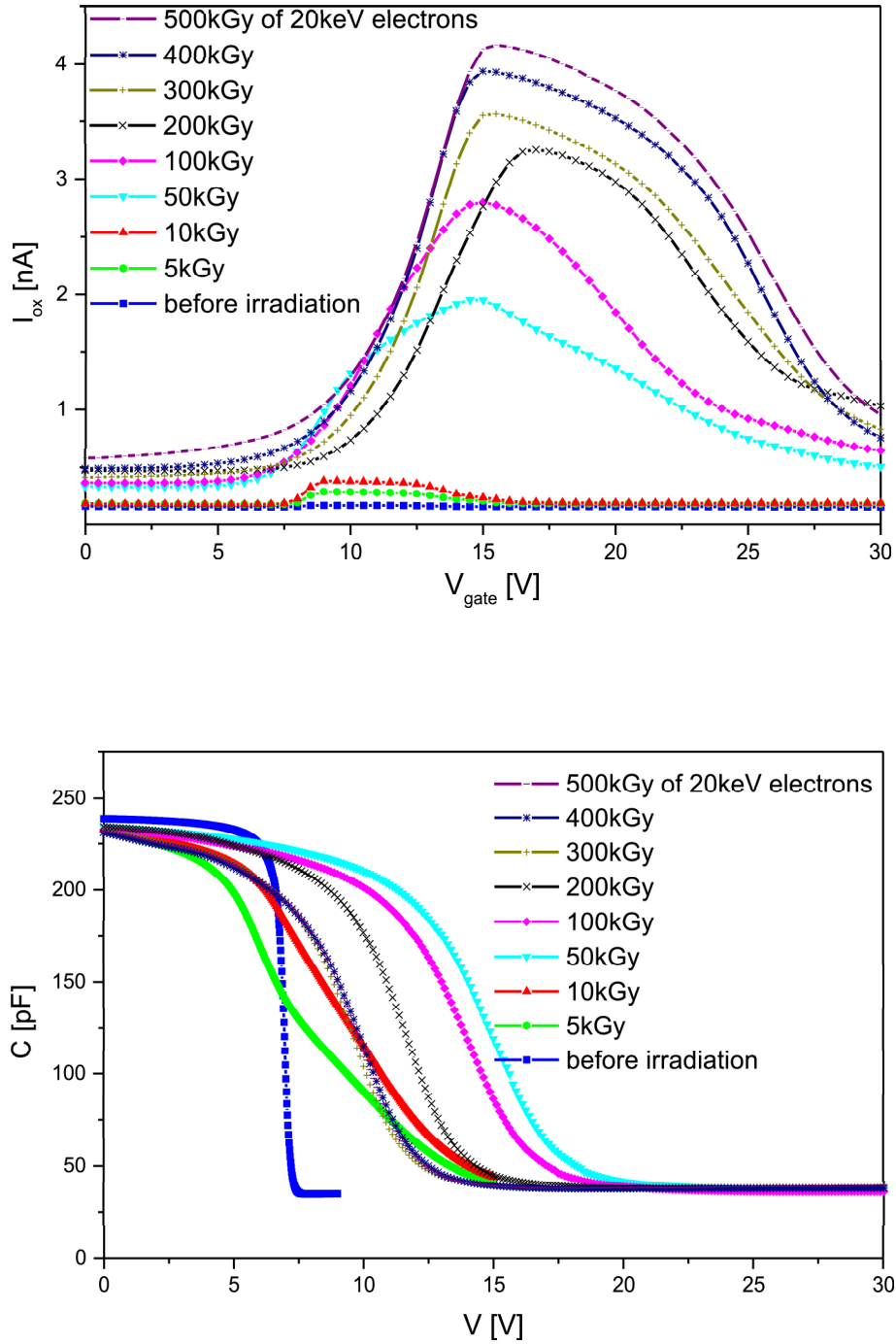


Figure 4.26: Sample results of tests performed during incremental electron irradiations: a) current vs. gate potential with constant diode bias on a GCD (top) and b) capacitance vs. forward bias on a MOS pad (bottom)

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The relevance of high dose electron irradiation performed within only a few irradiation and annealing steps for the very low dose rates expected during ATLAS operations are not immediately obvious and thus have required further investigation. As documented in [KLA03], a long term program of incremental irradiation and annealing has been implemented at the DEBE using a vendor A prototype test field. The electron irradiation has been performed in dose steps starting at 5 kGy and gradually increasing up to 100 kGy per step and a total integrated dose of 1 MGy, with each step followed by an annealing period of seven days at room temperature. Whenever a longer storage of the sample was unavoidable, it was kept in a freezer to avoid uncontrolled annealing. Directly after each irradiation step as well as after each annealing period measurements have been performed on the test field. On both gate controlled diodes of the test field precision current sweeps have been taken each time, varying only the potential of the inner gate rings while keeping the reverse bias of the diodes constant. Both MOS pads have been repeatedly tested for capacitance vs. forward bias behaviour. The results, of which samples are plotted in figures 4.26a & b, show a steady increase of the interface generation current raise I_{int} in the IVG curves, saturating slowly at several hundred kGy, but a more complex development of the flat-band voltage V_{fb} visible in the COX tests, increasing fast, but peaking around 50 kGy. Unfortunately, one of the GCDs has apparently been damaged during handling and bonding and produces erratically high initial currents, preventing a clear determination of I_{int} for this sample.

When plotting the extracted interface current values against the total dose (figure 4.27a), a clear saturation behaviour can be seen, without any significant difference between the results before and after annealing. So, both sets of results can be fitted together to an exponential asymptotic saturation function in dependence of the integrated dose D

$$I_{int}(D) = I_0 + I_1 \cdot \left(1 - e^{-\frac{D}{D_i}}\right), \quad (4.1)$$

yielding an exponential constant of $D_i = (95.3 \pm 4.1)$ kGy. The quality of the fit confirms the compatibility of the data sets used and the resulting value agrees with the trend hypothesized from the results in [WÜS01], putting the clear onset of saturation above 50 kGy but below 500 kGy. The absence of recognizable annealing effects between the two data sets as well as within each set itself can be taken as an indication of annealing time constants being too high or too low to effect relevant changes in interface currents when regarding time intervals ranging from one hour (i.e. during irradiation) to a few weeks. Comparing the overall current level of the curves to values derived from comparable devices used for the prototype studies (same silicon foundry, similar process and crystal properties), the typical ranges of I_{int} for both 50 kGy and 500 kGy from the three step irradiation scenarios are significantly higher than the results from the incremental scenario. This could be an effect of the specific samples used, but could also indicate a systematic overestimation of interface damage by irradiation tests done in only a few irradiation and annealing steps compared to incremental approaches or the continuing damaging and annealing in an experiment. Neither interpretation poses a problem for the ATLAS pixel detector, as the expected upper limits from [WÜS01] are valid in both cases, and for the latter case would even represent an overly pessimistic worst case scenario.

The development of flat band capacitances (plotted in 4.27b) shows significant differences in voltage levels between the two measured samples, as well as between the levels measured before and after annealing. A common trait, besides the marked drop in flat band voltage levels during annealing, is the asymptotic decline superimposed on a saturating dose dependent rise, leading all four curves to peak between 30 kGy and 80 kGy. This effect can be interpreted primarily depending on annealing time t_a , producing a fitting function

$$V_{fb}(D) = V_0 + V_1 \cdot \left(1 - e^{-\frac{D}{D_v}}\right) + V_2 \cdot e^{-\frac{t_a}{t_v}}, \quad (4.2)$$

which, assuming common exponential constants, but different voltage values and factors for the four data sets, yields $D_v = (13.7 \pm 1.0)$ kGy and $t_v = (66.5 \pm 22.4)$ d. The less than ideal fit of time dependence highlights the discrepancies between the curves, but still produces better results than individual fits to each curve, strengthening the assumptions made. On the bias dependence on

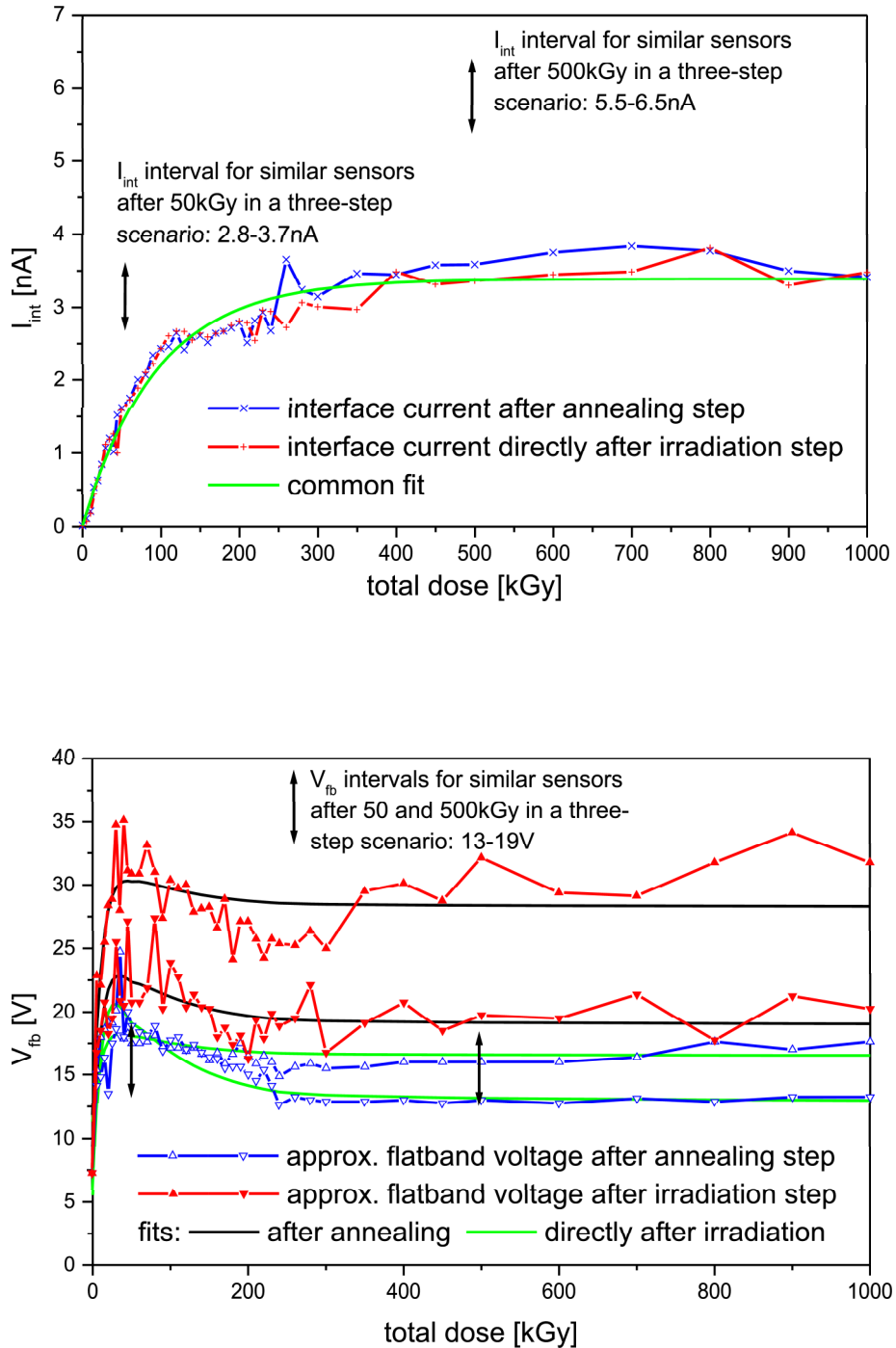


Figure 4.27: Development of and asymptotic fits to test field characteristics during incremental electron irradiation: a) interface generation current on one GCD (top) and b) flat band voltage on two MOS pads (bottom)

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the other hand, the fit shows good agreement and confirms the beginning of dominant saturation well below 50 kGy. The values derived from prototype tests agree with the after annealing curves and confirm the relevance of those studies for incremental or continual irradiation and annealing scenarios. These results provide a basis to consider the problems arising directly from interface currents and increased flat-band voltage to be well under control.

4.4.3 P-spray dose in the MOSFET

The MOSFET measurements are a critical aspect of the wafer tests, as they lend themselves a possibility to control the correct implementation of pixel isolation technology vital to detector operation, namely avoidance of early electrical breakdown and the retaining of spatial resolution after the forming of oxide charges near the oxide-bulk interface under irradiation. Therefore, tests of the crucial high p-spray dose region have been decided to be performed on as many production wafers as possible.

Two different sources of artificially faulty data have to be considered when comparing the threshold voltages extracted from the resulting data sets and the effective p-spray doses per area computed from these and the oxide capacitance values. Firstly, there are MOSFETs exhibiting a bad gate contact, possibly caused by an incomplete passivation opening on the pad, preventing a switching on of the transistor channel. Instead of yielding a repeatable measurement of the threshold voltage, a sudden current increase in these structures represents a breakdown of the residue preventing contact — typically above 100 V gate bias —, usually damaging the gate itself and leading to high currents at very low voltages in repeated tests. Furthermore, MOSFETs working correctly can yield low p-spray dose value, whenever the measured threshold voltages V_{th} are combined with capacitance data from measurements providing artificially low oxide capacitance values due to bad contact or surface leakage currents. In both cases, special care by the operators performing measurements and analysis is needed to identify test output data not representative of overall wafer performance and replace them with the necessary quantities from tests on other structures on the same wafer. Even if these problems are noticed only after measurements are completed, insights into the likely p-spray quality can still be gained, if either redundant tests from the wafer are available or the values from the production batch in question are sufficiently consistent with each other to justify an extrapolation to underdocumented wafers.

The distributions of effective doping densities N_{ps} from high p-spray dose measurements on pre-series and main series wafers are (2.40 ± 0.25) V on vendor A wafers and (2.83 ± 0.45) V on vendor B wafers. Among tests not clearly identifiable as faulty, 7.8% on vendor A structures and 12.4% of vendor B fall below the allowed interval with $N_{ps} < 2.2 \cdot 10^{12} \text{ cm}^{-2}$ and 0.4% of tests on vendor A structures as well as 3.9% of tests on vendor B structures fall above the interval with $N_{ps} > 3.5 \cdot 10^{12} \text{ cm}^{-2}$. Those very close to the respective limits have been considered uncritical on otherwise fully functional wafers or if other test results from the same wafer have shown conformance to the specifications. In more dramatic cases, insufficient, excessive or very inhomogeneous high dose p-spray has been ruled — usually among other reasons — a cause for rejection of a wafer or even a production batch as non-conforming, and has been quickly relayed to the manufacturer in question as a production problem to be resolved.

Data from tests on the low p-spray dose region performed on pre-series wafers yield distributions of N_{ps} of (0.80 ± 0.19) V for vendor A output and (0.25 ± 0.25) V for vendor B output. The lower values and broader distribution of the vendor B data stem from the second pre-series production run exhibiting extremely and atypically low p-spray doses in low dose structures, often indistinguishable from no p-spray at all within the resolution of standard testing (limited both by gate voltage steps of 2 V and ambiguities in the relevant characteristics of the gate oxide). As low p-spray dose values had not been specified as critical quantities for contractual acceptance of sensors, the affected wafers have not been rejected out of hand, but the observed effect has been taken in consideration, when other, possibly related operation problems had come under scrutiny (see the following section).

The functionality of p-spray technology after irradiation can be tested under a variety of aspects using the high and low dose p-spray MOSFETs on the n-side test fields as well as the sensors themselves. The latter approach, mainly a test of electrical breakdown behaviour of the inter pixel

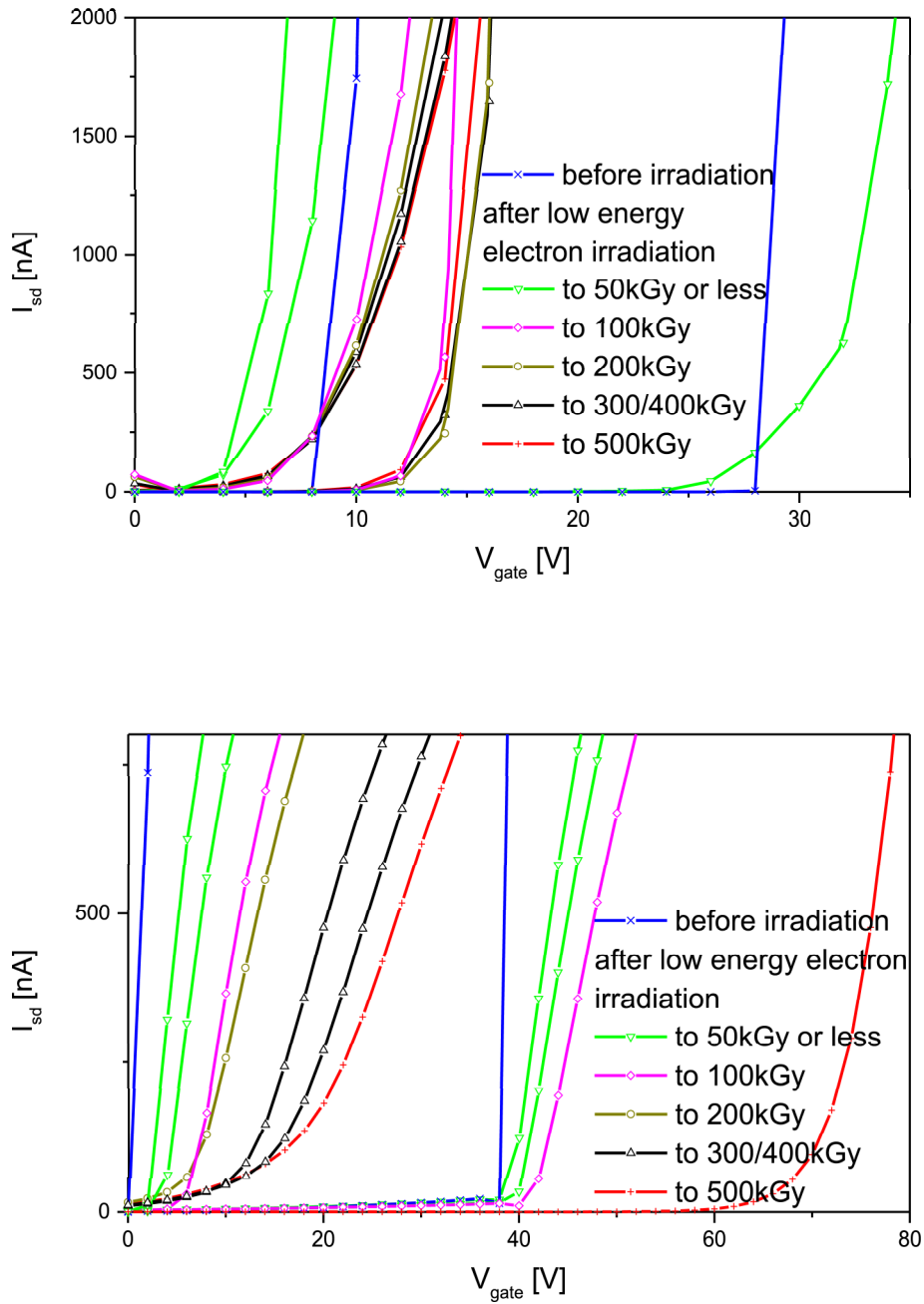


Figure 4.28: Source-drain current tests on electron irradiated high dose and low dose MOSFET structures a) from vendor A wafers (top) and b) from vendor B wafers (bottom)

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isolation, had already been studied repeatedly before and during prototyping (e.g. [ROH99]) and had confirmed the decreasing tendency of p-spray isolated pixels to show electrical breakdown after increasing irradiation. Irradiation tests on low p-spray dose MOSFETs have also been carried out on prototypes [HÜG01] [WÜS01], using electron irradiation at DEBE and yielding an indication that initial effective p-spray dose is reduced by electrons drawn to the interface by positive oxide charges, generating an onset of MOSFET conductivity at lower gate voltages. On the other hand, the interface defects appear to result in a shielding effect drawing out the source-drain current rise over a wide gate bias interval before reaching a linear rise, exhibiting a shallower slope due to changes in effective charge carrier mobility. Considering a sample irradiated successively up to 560 kGy with following annealing periods, i.e. to a level where all significant effects on the interface can be considered in saturation, low level leakage currents seem to be able to pass through the MOSFET, but the p-spray isolation seems to be very much effective considering higher currents, even in low p-spray dose areas.

Experiments intended to reproduce these results on test devices from both vendors (see figures 4.28a & b) have been performed by irradiating n-side test fields with 20 keV electrons at the DEBE in steps of up to 100 kGy per step up to the full design dose of 500 kGy and taking measurements on high and low dose MOSFETs after each step. The results show clearly different kinds of behaviour, with the vendor B samples (figure 4.28b) exhibiting a steady increase in effective threshold voltage even in the shown low p-spray case starting out close to $V_{th} \approx 0$ V, while in vendor A samples (figure 4.28a) not only does the onset of the MOSFET switching decrease, but in the irradiation dose range up to 100 kGy so do the V_{th} values. In test structures from both vendors the typical stretching out of the source-drain current rise can be seen after irradiation, and, being the most important aspect for quality control, even at the highest irradiation levels the MOSFET channel remains closed without positive gate bias, and at least in the high p-spray dose case remains that way at non-negligible gate bias values. This indicates the persistence of a non-zero effective p-spray dose potentially capable of pixel isolation even at the highest expected levels of ionizing irradiation, an indication supported by an apparent saturation of all irradiation effects on the vendor A MOSFETs above 200 kGy.

While the low energy electron irradiation lends itself to logistically uncomplicated repeated irradiations and has been shown as a sensible approach to study the effects of ionizing irradiation on oxide and interface under a close to worst case scenario, it not necessarily yields a realistic picture of sensors within the ATLAS experiment. Therefore, vendor A samples have been irradiated with high energy protons at the PS irradiation facility at CERN to a fluence of $3 \cdot 10^{14}$ (1 MeV neutron equivalents)/ cm^2 and annealed for approximately a week at room temperature. At this fluence, type inversion and a significant increase in effective charge carrier density and leakage current in the bulk is expected. This becomes visible in the source-drain current curves taken after irradiation in a climate chamber cooled to -10 °C and normalized to room temperature (figure 4.29), not only showing a reduced threshold voltage and a drawn out current rise, but also an increase in V_{th} for $U_{bias} > 150$ V and a negative current into the MOSFET below the switching threshold of the gate. The former shows the bulk not being overdepleted when biased with 150 V because of the increased bulk depletion voltage, the latter can best be understood as a constant contribution by the high bulk leakage current flowing into the drain independent of MOSFET behaviour. This additional current contribution can be corrected against by subtracting it from the measured current values, as done in the coloured plots in figure 4.29. The resulting curves exhibit indications of a functional p-spray layer, enabling typical switching behaviour even without bias applied to the sensor bulk. This is due to the type inversion of the sensor bulk leading to the spontaneous formation of depleted zones around the interfaces of the source and drain implantations and the now p-type bulk. These results confirm an intrinsic radiation hardness of the p-spray layers postulated from earlier results not only for electron irradiation, but also for the effects of bulk damage caused by charged hadrons.

An intriguing feature of the curves resulting from the MFE measurements is a saturation of the source-drain current of the MOSFET around a maximum value. Opposed to the saturation of currents at high source-drain voltages, this phenomenon seems usually not of great interest for characterization of MOSFETs and would not necessarily be considered in the context of a sensor quality plan, if not for unusually low saturation values observed on many vendor B pre-series and main series wafers. This anomalous behaviour, markedly different from both vendor A production

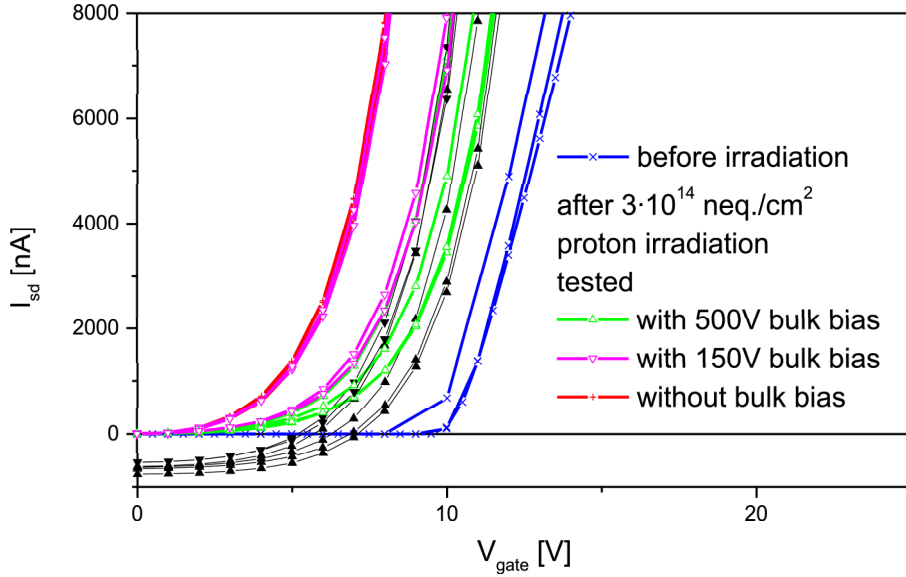


Figure 4.29: Source-drain current tests on vendor A low dose MOSFET structures irradiated with high energy protons before (thin, black lines) and after bulk current correction (thick, coloured lines) normalized to room temperature

and all prototyping runs with saturation occurring well beyond $2 \mu\text{A}$ and thus normally not observed, could be an indication of a fundamental difference in wafer processing, possibly affecting other aspects of sensor operation in ways so far not obvious. Source-drain current measurements performed with varying bulk bias on a vendor B MOSFET saturating around 650 nA (figure 4.30) show a clear bias dependence of current without gate bias up to depletion at $U_{bias} \approx 50 \text{ V}$ and of V_{th} up to overdepletion at $U_{bias} \approx 120 \text{ V}$. For higher bias values the current characteristics appear to be bias independent, and the state of bulk depletion seems to have no influence on the current saturation level whatsoever. This points towards geometry and doping profile of the p-spray layer itself, apparently sufficiently isolated from the depleted substrate, to limit the maximum source-drain current. Using a very simple model, the concentric MOSFET with an inner gate radius $r_s \approx 70 \mu\text{m}$ and an outer radius of $r_d \approx 100 \mu\text{m}$ can be approximated as a rectangular gate area with a length to width ratio of

$$\frac{L}{W} = \frac{1}{2\pi} \cdot \ln \frac{r_d}{r_s} \approx 0.0568 \quad (4.3)$$

and a homogeneous electrical field. For a small source-drain potential difference $V_{sd} \ll V_{gate}$ — a so-called linear state — and an current channel at equilibrium, differences in charge density and channel depth can be neglected, yielding an absolute source-drain current based on minority charge (i.e. electron in p-spray) mobility [LUT99] [HÜG01]

$$I_{sd} = V_{sd} \cdot \frac{e \cdot \mu_{ei} \cdot N_{ns} \cdot W}{L}, \quad (4.4)$$

with N_{ns} being the area density of electrons below the gate and μ_{ei} being the electron mobility at the interface, which typically is much lower than μ_e in the silicon bulk [HÜG01] [ROH99]. The area charge density is a potentially limiting factor for the maximum source-drain current, as the apparent independence between bulk and p-spray would allow only minority charge carriers generated within the p-spray layer and sufficiently close to the interface to participate in the generation of the

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conductive inversion layer forming the current channel (see [LUT99] for discussion of maximum inversion depth). Assuming a homogeneous depth profile of p-spray doping and an abrupt border to the bulk, the apparent maximum density of conduction band electrons per area within the p-spray layer can later be compared to the effective p-spray dose and typical doping densities. The remaining unknown quantity μ_{ei} can be derived from the current slope $\delta I_{sd}/\delta V_g$ of the linear rise around V_{th} under the assumption for a linear, not saturated state [LUT99] [TYA91]

$$e \cdot N_{ns} = C_{oxi} \cdot (V_g - V_{th}) \Rightarrow \mu_{ei} = \frac{L}{W} \cdot \frac{1}{C_{oxi} \cdot V_{sd}} \cdot \frac{\delta I_{sd}}{\delta V_g}, \quad (4.5)$$

with $C_{oxi} = C_{ox}/A_g$ being the oxide capacitance normalized for the measured area.

Thus the resulting saturation condition for parameters derived under the same conditions (especially no changes in V_{sd}) is

$$I_{sd} \leq \frac{e}{C_{oxi}} \cdot \frac{\delta I_{sd}}{\delta V_g} \cdot N_{ns}. \quad (4.6)$$

For the vendor B sample inspected in figure 4.30 with $C_{oxi} = (10.99 \pm 0.03) \text{ nFcm}^{-2}$, $\delta I_{sd}/\delta V_g = (0.2 \pm 0.05) \mu\text{AV}^{-1}$, $V_{th} = (38 \pm 2) \text{ V}$ and a saturation at $I_{sd} = (660 \pm 30) \text{ nA}$ for a measurement at room temperature with $V_{sd} = 100 \text{ mV}$ these relations yield a p-spray area density $N_{ps} = (2.6 \pm 0.2) \cdot 10^{12} \text{ cm}^{-2}$, an interface electron mobility $\mu_{ei} = (10.3 \pm 2.6) \text{ cm}^2(\text{Vs})^{-1}$ and a maximum minority charge area density $N_{ns} = (2.3 \pm 0.6) \cdot 10^{11} \text{ cm}^{-2}$. For a vendor A wafer with $C_{oxi} = (15.67 \pm 0.05) \text{ nFcm}^{-2}$, $\delta I_{sd}/\delta V_g = (2.7 \pm 0.3) \mu\text{AV}^{-1}$, $V_{th} = (24 \pm 2) \text{ V}$ and a saturation at $I_{sd} > 10 \mu\text{A}$ the results are a p-spray area density $N_{ps} = (2.3 \pm 0.2) \cdot 10^{12} \text{ cm}^{-2}$, an interface electron mobility $\mu_{ei} = (98 \pm 10) \text{ cm}^2(\text{Vs})^{-1}$ and a maximum minority charge area density $N_{ns} > 3.6 \cdot 10^{11} \text{ cm}^{-2}$. So at least a part of the differences in saturation can be attributed to different interface electron mobilities. While the value for the vendor A sample falls well within the range seen in prototype measurements on $\langle 111 \rangle$ substrate in [HÜG01] and [ROH99], the vendor B tests — at least in this rather extreme example — exhibit an unusually low mobility value. This could be influenced by the doping concentration in the p-spray layer, according to [SZE85] able to lower electron mobility significantly, with μ_e dropping to around $100 \text{ cm}^2(\text{Vs})^{-1}$ between doping concentrations N_p of 10^{16} cm^{-3} and 10^{20} cm^{-3} , even under otherwise ideal conditions.

This effect alone can not account fully for the vendor B sample, but has to be considered in connection with further reductions due to scattering of electrons on interface phonons, an effect so much more pronounced in $\langle 111 \rangle$ silicon compared to $\langle 100 \rangle$ silicon, that it could produce a mobility difference of an order of magnitude in otherwise similar prototype samples analyzed in [ROH99]. Thus, the vendor A sample can be assumed to be typical in doping concentration ($N_p \approx 10^{17} \text{ cm}^{-3}$) as well as influence of interface phonons, while the p-spray layer in vendor B samples would be likely of a significantly higher concentration. The scaling of the maximum inversion depth with $N_p^{-1/2}$ would lead to a shallower current channel in these cases, explaining the apparently higher likelihood of phonon scattering directly below the interface. Possible high N_p values also offer an explanation for further limitation of maximum source-drain currents beyond a low mobility, as minority charge carriers contributing to N_{ns} are rarer and harder to generate.

Consideration of electron mobility in irradiated samples as seen in figures 4.28a & b under the assumption of only minor changes in C_{oxi} (see figure 4.26b for examples) confirm the analysis in [HÜG01], as a decrease in mobility is evident, saturating towards high doses between twice and five times the initial value before irradiation with low energy electrons. Proton irradiated samples can not be easily compared to unirradiated MOSFETs regarding mobility, as the former have to be measured in a cooled environment and exhibit radically different temperature scalings for mobility and overall current level. No clear indication of a change of source-drain current saturation by radiation induced effects has been found in the test data for any measured structure, although a more drawn out saturation curve for MOSFETs after irradiation appears plausible. So far, no problems with p-spray isolation before or after irradiation is expected based on this behaviour.

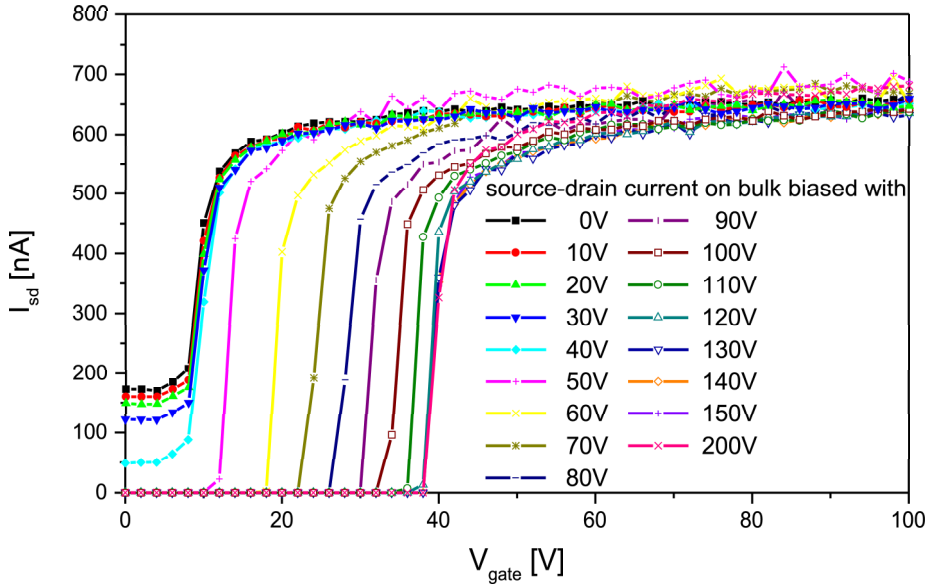


Figure 4.30: MOSFET drain-source current sweeps on a high p-spray dose device with varying bulk bias

4.4.4 P-spray behaviour in the bias dot

In how far the effective p-spray doses measured in the MFE tests actually do reflect the quality of pixel isolation is not immediately in evidence, although both effects are influenced by the p-spray layer; but while the MOSFET threshold measurements tests only the formation of a conducting electron layer directly below the oxide interface, the possibility of a punch through connection between implantations as a current channel through the depleted bulk is not considered. To assess this aspect of pixel isolation, pixel arrays without bias grids can be used for inspection of isolation across inter pixel gaps. But the narrowest and thus most critical p-spray isolated gap is the bias dot, lending great importance to measurements on dedicated punch through structures to complement other p-spray data.

To study the relevance of measurements on the test devices for the operation of the bias grid in tiles, comparisons of sensor tiles with neighbouring test structures have been performed as well as studies on the consistency of punch through behaviour across a tile surface and at various temperatures [GLI02] [KLA03]. These tests involving probing on active wafer surfaces could only be performed on prototype wafers and faulty tiles, as resulting damage to the probed pixel cells, rendering the sensor unbondable or inducing breakdown is quite likely. The main difference to curves from test devices observed in measurements of the voltage drop across tile bias dots is a significant sensitivity to the used stepping times. Apparently, the elaborate grid and pixel structure of the tile exhibits capacitive and inductive qualities prolonging the time needed after an increase in U_{bias} to reach a stable field configuration. This can be seen in a comparison of ΔV_{pix} vs. time measurements on two tiles and one punch through test array from a wafer exhibiting low and inhomogeneous V_{pt} (see figure 4.31)a. The time constants derived from fits of this data are (4.4 ± 0.1) s and (10.0 ± 0.1) s respectively, indicating a minimum stepping time interval of several 10 s to avoid a misleading influence of transient behaviour on test results from sensor tiles.

These studies on prototype sensor tiles show no significant influence of using stepping intervals longer than 40 s, and have been used to demonstrate the similar behaviour of bias dots on tiles and test devices (see figure 4.31b). Even on a wafer exhibiting inhomogeneities in V_{pt} of over 25%,

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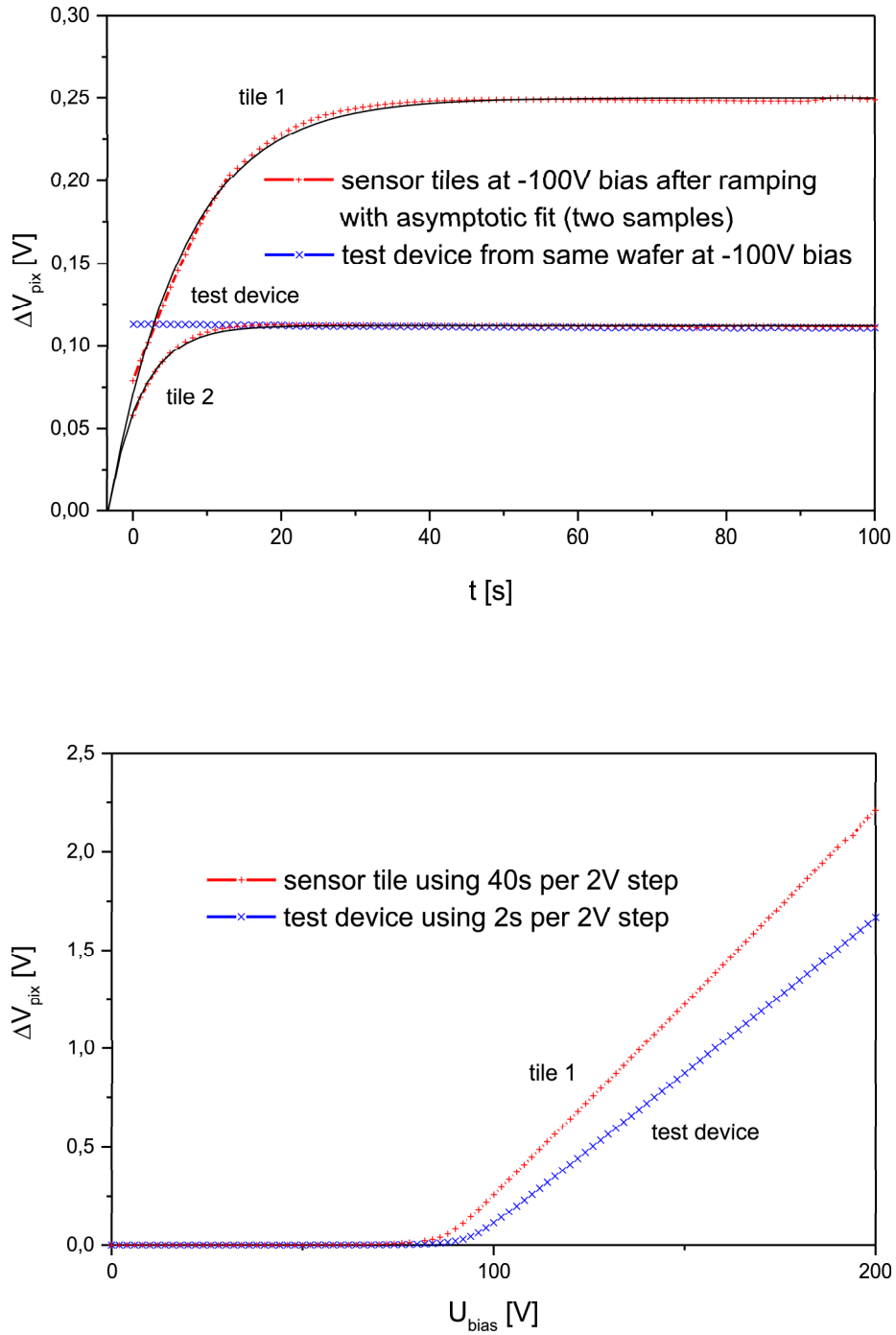


Figure 4.31: Potential drop across test structure bias dot arrays compared to bias dots on sensor tiles a) measured time resolved at $U_{bias} = 100$ V (top) and b) measured bias dependent with adequate stepping times (bottom)

discrepancies between or on tiles appear not to be smaller than between sensors and test arrays with respect to depletion voltage, slope and curve shape, confirming test devices as a suitable and time efficient alternative to tests on sensor bias dots.

While discrepancies in ΔV_{pix} of this magnitude have been observed on several wafers — usually in connection with other p-spray related problems — they are not typical. On most wafers the distribution between structures or between individual bias dots are more similar to the results from a sample of bias dots on a prototype tile given in [GLI02]. There, variation between individual bias dots at different degrees of overdepletion ranges from 25% to 5%, decreasing in relative importance at higher bias voltages.

To assess the significance of changes in μ_e and the charge carrier densities with temperature for bias dot operation, individual bias dots on prototype sensors have been measured in the climate chamber and results for different temperature settings have been compared [GLI02]. In tests performed at temperatures ranging from -30°C to 40°C a slight trend towards higher voltage drops for higher temperatures has been observed, possibly caused by the temperature scaling of electron mobility, but V_{pt} changes attributable to temperature add an uncertainty of only around 10% for the whole temperature range, indicating an explicit temperature correction on the scale of several degrees unnecessary and behaviour at room temperature by and large comparable to expected behaviour under operation conditions within the ATLAS detector.

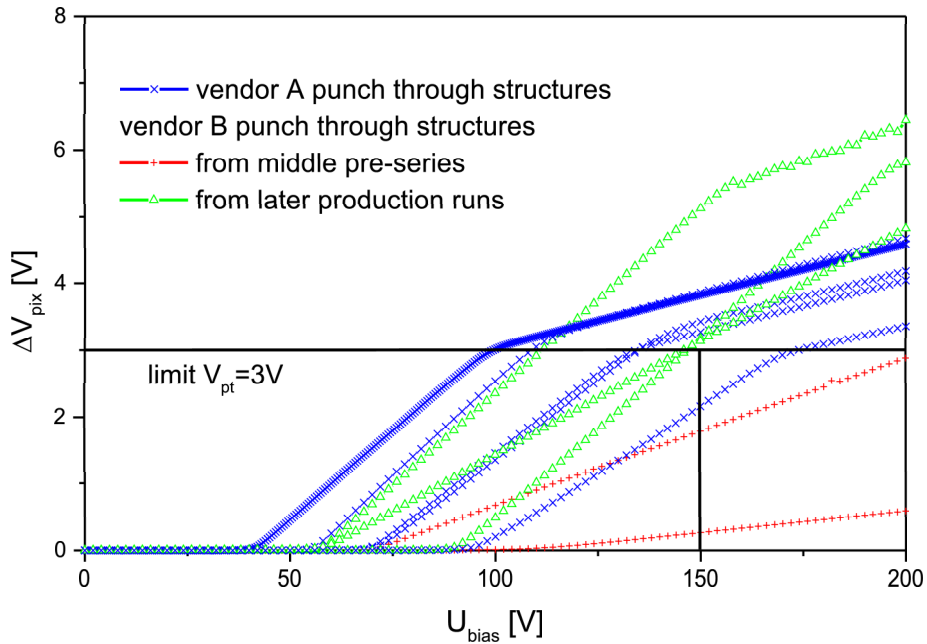


Figure 4.32: Sweeps of voltage drop between bias grid and implantations vs. bias voltage measured on punch through structures from different production runs

In the case of test structures on pre-series and main series wafers from both vendors, the potential difference V_{pt} at $U_{bias} = V_{op}$, which depends on the doping and width of the 48 bias dot gaps in the structure, varies between batches, wafers and individual structures, but yields a relatively consistent picture across nearly the whole production. The only testing artifacts seen in standard punch through tests are effects of short circuits or contact problems, which can easily be corrected by re-measuring or use of another structure, as long as one functional structure is present on the wafer. The distribution provided by the test results for V_{pt} is (3.40 ± 0.93) V for all vendor A wafers

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and (3.13 ± 0.82) V for the vendor B main series and part of the pre-series. While the vendor B values are slightly lower, both vendors have their share of tests falling below a limit of $V_{pt} = 3$ V. Tests on those wafers have been repeated, and only in cases in which all tests on a wafer fall consistently and significantly below the limit or in which a low value revealed a persistently high discrepancy of bias dot behaviour across the wafer, this has been considered a reason for wafer rejection. The only production run consistently producing low punch through voltages are ten batches from the middle of the vendor B pre-series (wafers 202101203xxx), yielding a V_{pt} distribution of only (0.82 ± 0.76) V.

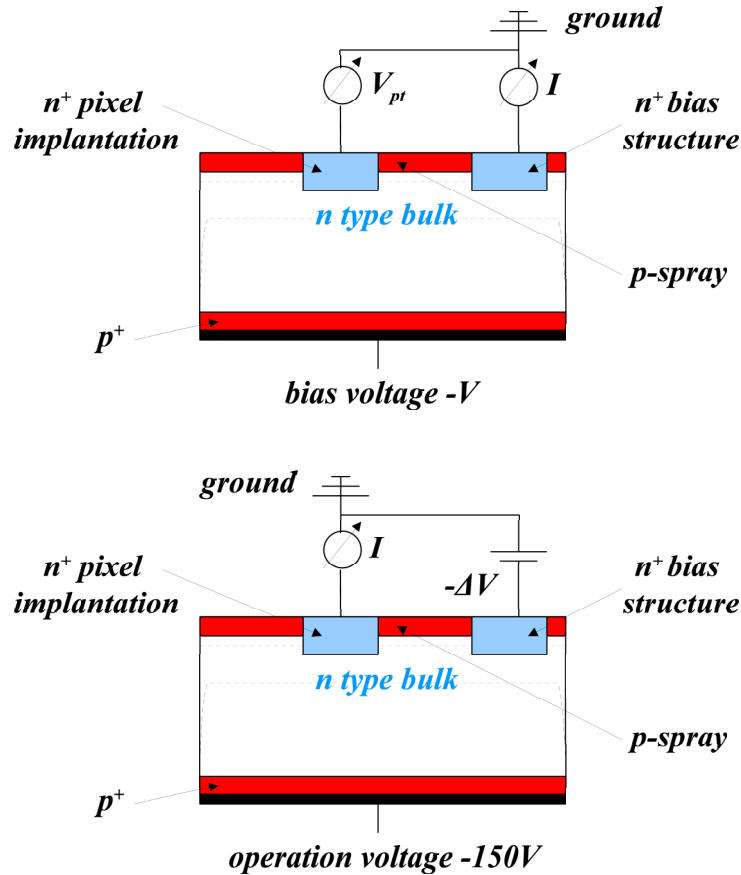


Figure 4.33: Measurement set-up for a punch through device a) for a regular potential difference vs. bias sweep (top) and b) for a special bias dot current vs. potential difference test on depleted substrate (bottom)

These very low PUT results coincide with the extremely low values measured for low dose p-spray — strangely enough not for high dose p-spray which should be present in the bias dot — and a significant leakage current in irradiated and hybridized sensor tiles under test beam conditions. The leakage currents could be shown to increase significantly with a direct grounding of the bias grid, leading to the conclusion that an insufficient isolation in the bias dots might cause the front-end pre-amplifier contact potential of $(1.0 - 1.5)$ V to inject the additional currents from the bias grid into the pixel cells. This effect can not be directly derived from the PUT test results, as the voltage drop is only defined indirectly via U_{bias} and the bias dot current is not measured at all, leading to the proposition of an altered test set-up depicted in figure 4.33b. This set-up, directly measuring the current injected into the pixel implantation at a fixed bias voltage dependent on the potential of the bias grid does not only provide data on the increase of current across the bias dot, while in standard PUT (figure 4.33a) only total leakage current into the bias grid is measured, it also simulates a more realistic field configuration for detector operation with the bias grid potential

between the pixel implantation and the bias voltage. The standard set-up on the other hand is realistic concerning sensor tests, using a grounded bias grid with the pixel implantations floating between ground and bias potential.

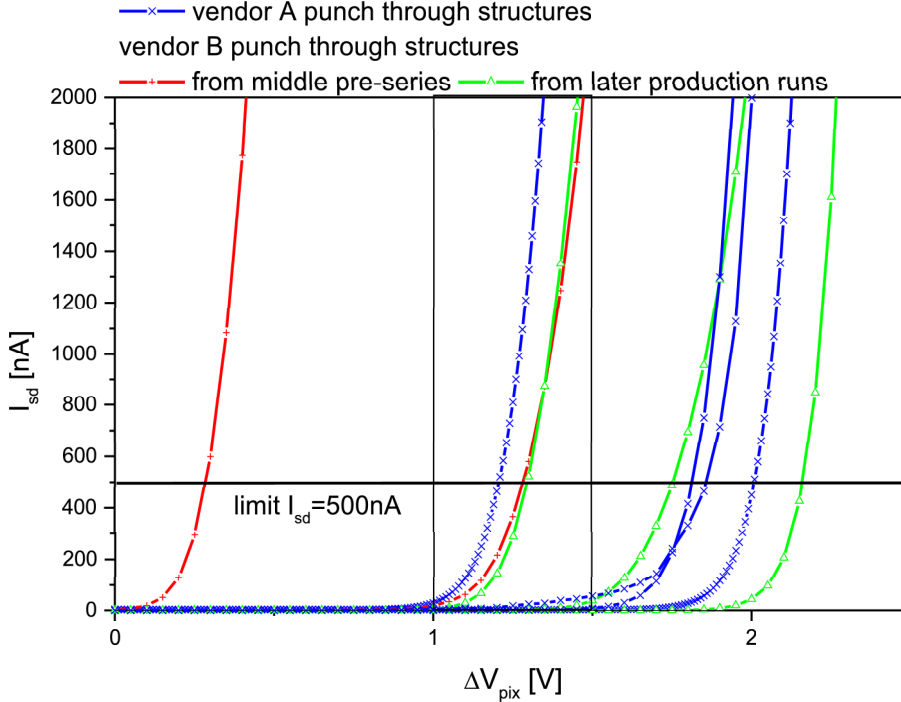


Figure 4.34: Current across bias dots in punch through structures at $U_{bias} = 150$ V dependent on potential difference (critical potential difference interval (1.0 – 1.5) V is marked)

The results of these additional tests (see figure 4.34) show a flat current for low ΔV_{pix} dominated by a small bulk leakage current, and an exponential current rise after the potential difference exceeds several V. The critical interval of potential difference marked in the plot is $1.0 \text{ V} \leq \Delta V_{pix} \leq 1.5 \text{ V}$, chosen because this covers the expected values for the potential of pixel cells connected to the front end electronics relative to ground. As can be seen, most curves start to rise within or above this interval, save for one sample representative for the weak bias dot isolation observed in some vendor B pre-series tiles. Arbitrarily setting the decisive current value in the exponential rise at 500 nA — as several 10 nA of leakage current per bias dot would add an amount of leakage current significant for tile operation —, the resulting distributions of all measured bias dot currents are $(2.0 \pm 0.3) \text{ V}$ for vendor A test devices and $(1.6 \pm 0.3) \text{ V}$ for most of vendor B production, while samples from the problematic middle pre-series yield $(0.7 \pm 0.6) \text{ V}$. These data stress the significance of the observed problem, as the curves from the problematic production runs at best edge into the critical range, being comparable to the very worst of tests on devices from other production runs. For wafers with current rises not even falling within this interval, problems with significant additional leakage current into the pixel cells are likely even before radiation damage occurs. Although most of the tests in figure 4.34 have been taken on the same devices as those in figure 4.32, a definite relation between potential difference at a certain voltage and current rise is not in evidence, although a clear tendency for devices with low punch through voltages to exhibit early current increases is visible nevertheless. As the problematic wafers do not exhibit low effective area dose values for high dose p-spray, but clearly far too low ones for low dose p-spray, this effect could either be caused by mask errors, either incorrectly doping bias dots gaps with low dose p-spray, or implanting bias dots in

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a way creating an effectively too narrow gap, or possibly even both. Data from later vendor B production runs show the problem has successfully been fixed after informing the manufacturer, who could check for errors in the masks and implantation parameters used.

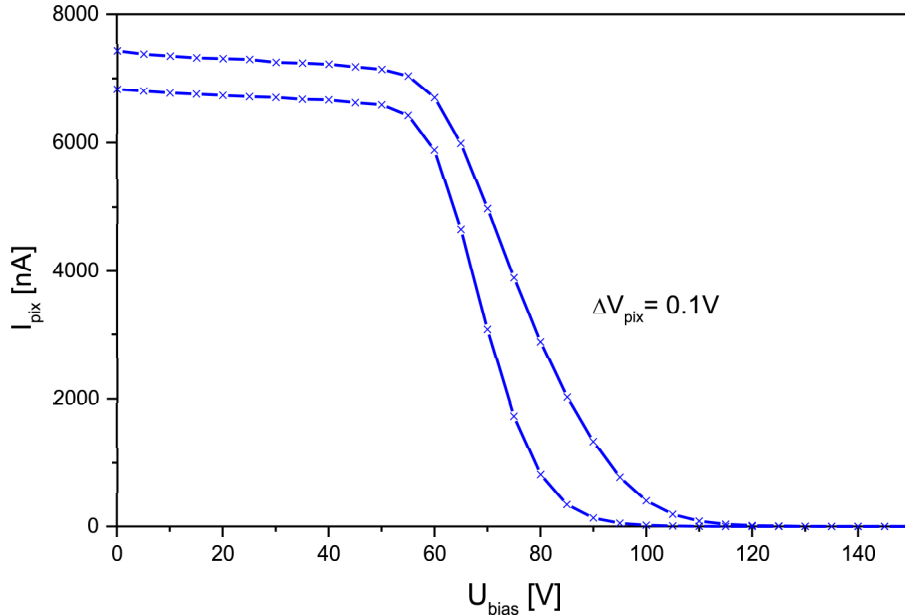


Figure 4.35: Bias dot current vs. bias sweeps at a fixed potential difference on a problematic vendor B wafer

Between pixel cells proper no indication for significant currents at full depletion has been observed in inter pixel tests on a depleted bulk (see following section), not even even on inter pixel structures from one of the middle pre-series vendor B wafers. Even when performing a leakage current sweep with increasing bias potential on a bias dot test structure (shown in figure 4.35) at potential differences $\Delta V_{pix} \ll 1\text{ V}$, as expected between neighbouring pre-amplifiers on the same front-end chip, the current vanishes nearly completely when the bulk reaches overdepletion. Given the lower expected potential differences in this test and the different p-spray dose profile in the inter pixel gap, the existence of some kind of anomaly cannot be ruled out, but evidently if there was a problem, it would show more prominently in the bias dots than between pixels.

After irradiation, the behaviour of currents and voltage drops across the bias dot changes in complex ways not easily predictable. For example, punch through test devices irradiated with an electron dose of 500 kGy or more at the DEBE yield potential difference measurements very different from wafer to wafer (see figure 4.36a). While some devices from both vendors, especially those with low V_{pt} in an unirradiated state see a dramatic reduction in ΔV_{pix} as well as a deformation of the curves probably brought about by space charges at or near the oxide interface, other samples, typically with higher V_{pt} to start with and again from wafers of both vendors, show curves remaining at a high potential difference level after irradiation. The latter curves are considerably smoothed and deformed, sometimes even reaching higher ΔV_{pix} than measured for comparable unirradiated samples. As far as can be seen from a comparison of the potential difference sweeps, no significant change in the U_{bias} value at the onset of the potential difference rise occurs between samples before and after irradiation (see [KLA03]). As this bias value represents the onset of channel pinch off under the bias dot gap by the growing depletion zones, this is a good example for the specialized consideration of interface effects independent of irradiation damage of the substrate,

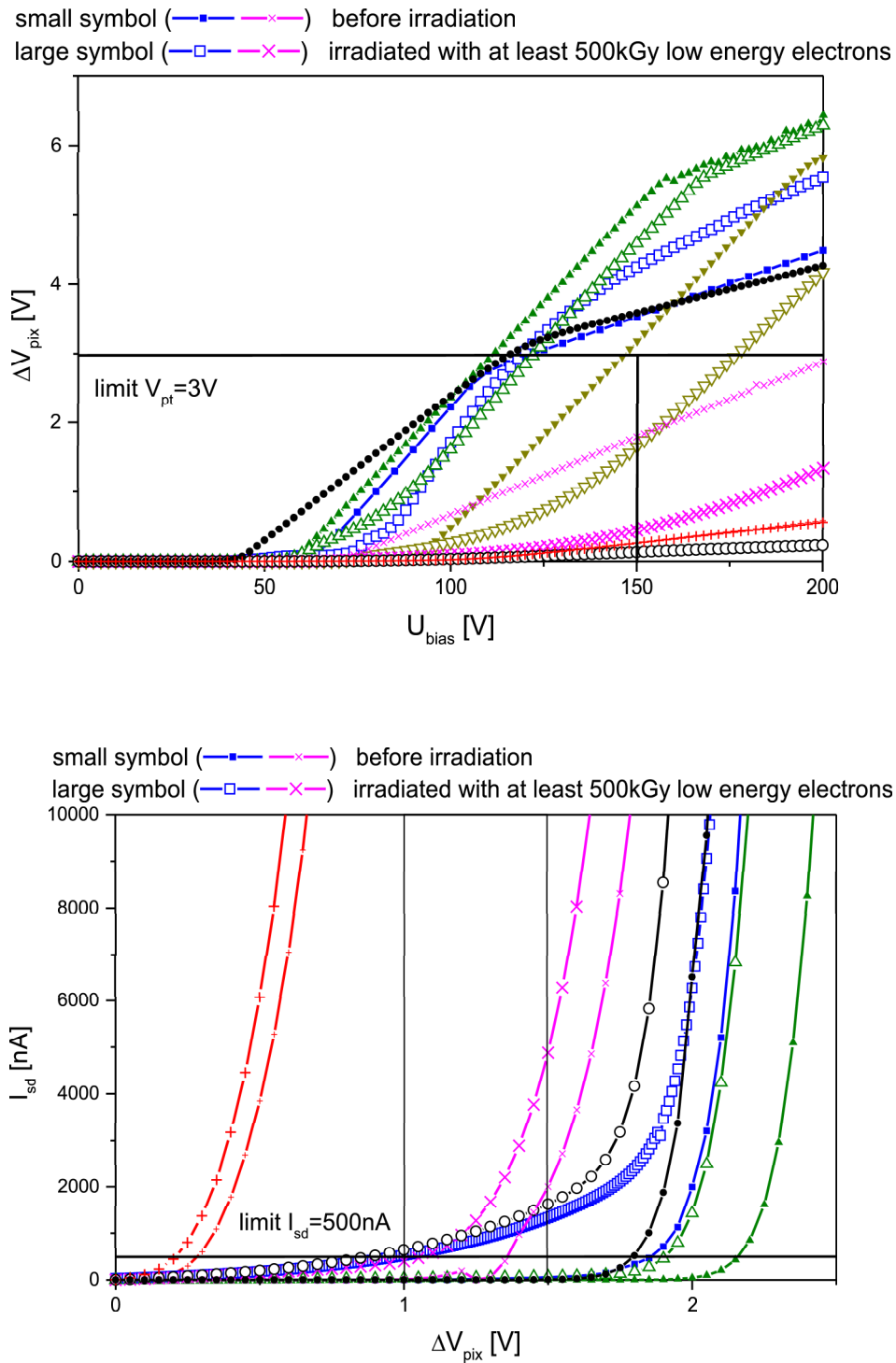


Figure 4.36: Tests on punch through structures before and after irradiation with 500 kGy or more low energy electrons in direct comparison per wafer a) of potential difference sweeps (top) and b) of bias dot current sweeps on depleted substrate (bottom)

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an advantageous option provided by the use of the Dortmund irradiation facility and important in choosing electron irradiation in addition to the more realistic proton irradiation as a tool of quality testing.

Considering bias dot current sweeps on depleted bulk after full dose electron irradiation (see figure 4.36b), the effects of interface radiation damage are more consistent. On all devices the main current rise occurs at a different potential difference after irradiation. While in some atypical cases (not shown), the rise takes place at a higher ΔV_{pix} than before irradiation, mostly a slightly lower value is in evidence. In several after irradiation curves an increased slope before the final rise can be observed, sometimes bringing the bias dot current of the test device to ≥ 1000 nA, which could pose a problem in terms of additional current noise due to current injected from the bias grid into the pixel cells. The final rise, which could impair a pixel cell more dramatically, appears to stay within a relatively small interval from the initial curve, some (10 – 20)% below it in most cases, increasing to about 30% for data sets with rises at extremely low potential differences. Hence, although the exact influence of interface defects and oxide charges could not be derived from the data, a rough extrapolation of the development of bias dot currents under electron irradiation from tests on unirradiated devices is possible, especially since the involved types of radiation damage are known to saturate.

As has already been discussed, the data resulting from standard PUT tests after type inversion of the bulk are quite different from those taken on unirradiated or surface irradiated devices, as the depletion zones within the bulk now form primarily under the n-side implantations, so there is no longer a pinch off across the bias dot. As can be observed from samples from both vendors irradiated with different fluences of high energy protons at the CERN PS, (see figure 4.37a) the potential difference levels across the bias dot vary significantly between wafers and even structures, but all show a slow leveling towards higher biases. While samples like the very high curve might result in ambiguities in sensor tests on irradiated devices of up to 10% of the nominally applied bias and suffer from a lowered effectivity of the bias grid as a safety device for detectors in operation, these effects pose no grave problems for operation or detector functionality. The low curve derived from one of the problematic vendor B wafers on the other hand could imply a saturation of potential difference values at an alarmingly low level and resulting high bias dot currents. A significant fluence dependence beyond a proton fluence of $3 \cdot 10^{14}$ (1 MeV neutron equivalents)/cm² is not indicated by the results, raising the possibility of little change in bias dot behaviour occurring after type inversion.

To test the exact effects of irradiation with charged hadrons on the bias dot current and especially the success of changes in the process at vendor B, samples from vendor B middle pre-series and main series have been compared after proton irradiation to full design fluence (see figure 4.37b). The results after irradiation are dominated by bulk leakage current for measurements on a depleted substrate and have been corrected for these constant currents, to enhance the visibility of current changes with increasing potential difference. As can be seen, the two problematic pre-series devices retain a steady, if shallower current rise starting at low ΔV_{pix} , becoming less pronounced for higher U_{bias} . The other samples, exhibiting less problematic bias dot characteristics from the start, show a significant increase in current within the studied potential interval only in tests performed on an unbiased bulk. For all tests with bias applied, the additional current is negligible compared to the bulk leakage current and not seen to rise considerably. This underscores the significant improvements achieved in the checking of mask and implantation steps in the vendor B production process and the value of feedback of quality testing data to the manufacturers, and fully justifies the rejection of several wafers due to problematic behaviour of bias dot potential drops and currents before irradiation.

4.4.5 Other layer characteristics

As a final set of characteristics, several measurements on inter pixel behaviour and conductive properties of metallization and implantation layers have been taken. Like in some of the other tests, no criteria have been defined in the technical specifications for these qualities, but they can yield information on the manufacture process or additional data as a basis for other analyses or

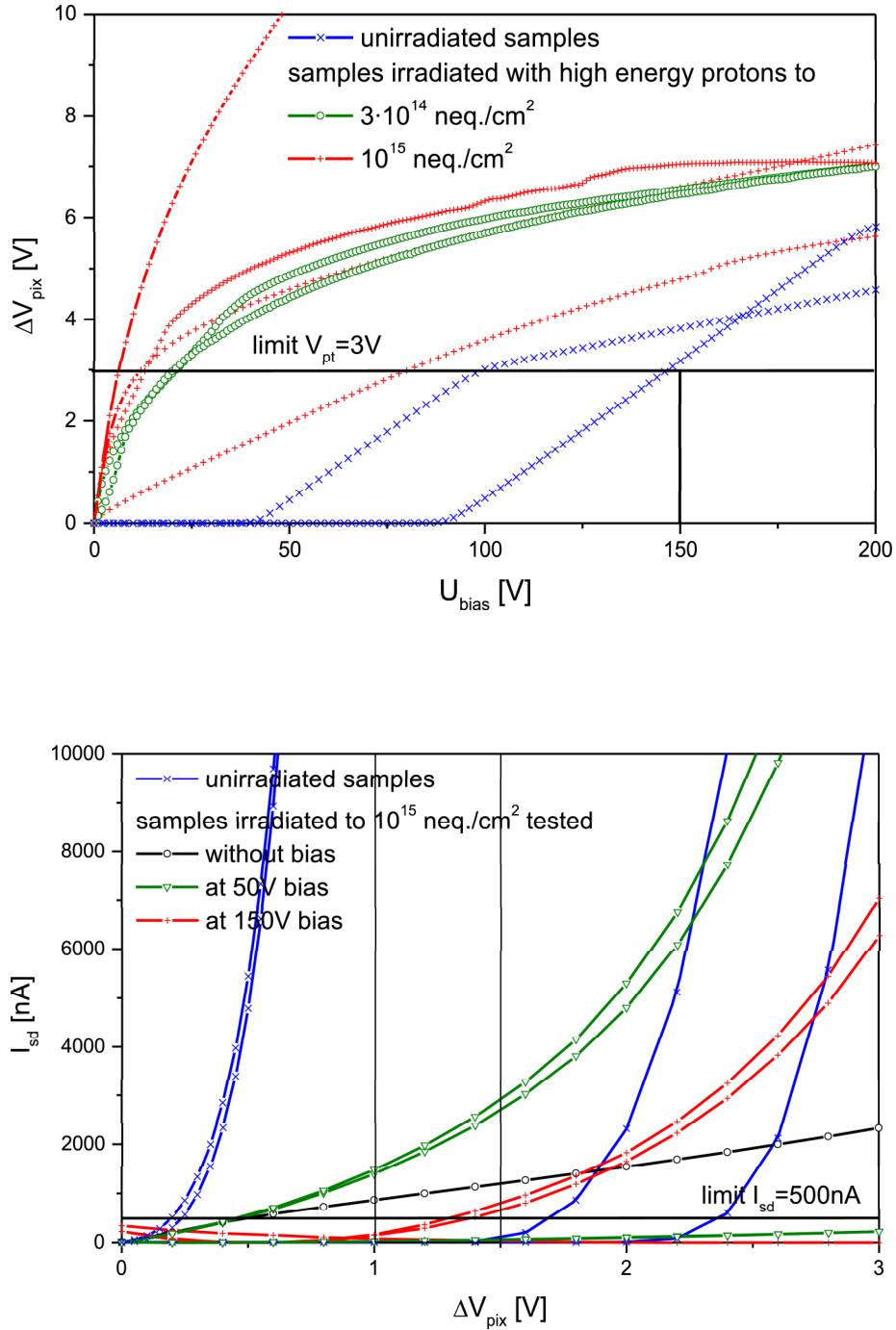


Figure 4.37: Tests on punch through structures before and after irradiation with high energy protons a) concerning potential difference after different fluences of radiation (top) and b) concerning bias dot current change above constant bulk leakage current at different bias voltages (bottom)

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extrapolations of behaviour during operation.

Isolation between the pixel cells proper has been successfully measured on inter pixel test structures without routed contact pads using the IVP procedure. Different grounding schemes have been tested for the n-side bulk outside the test device and the one most successfully suppressing additional bulk leakage currents and avoiding lateral injection artifacts has been used routinely. The degree of inter pixel isolation achievable has been tested at different degrees of depletion as compared in figures 4.38a & b (both illustrating the same data at different scales). On an undepleted bulk a considerable asymmetry concerning the polarity of the central pixel potential can be seen, as a negative pixel potential leads to an effective forward biasing of parts of the bulk, injecting current from the p-side. For positive pixel potential a linear current rise can be observed, going into a slow breakdown around (1 – 2) V. The slope of the linear rise for the tested samples yields an effective resistivity around (200 ± 50) k Ω , fully compatible with similar results gained from tests during prototyping [HÜG01]. The test performed on a partial depleted bulk with $U_{bias} = 50$ V shows much less asymmetry, as even a small amount of reverse bias does offset any forward biasing effects of the test pixel. The curve shape is rather complex, starting with a slope around 20 M Ω for absolute potential differences up to 0.2 V, slowly but steadily increasing without a clear linear area or breakdown. As can be seen, an average resistivity for low V_{pix} values of 5 M Ω is realistic as well as consistent with similar prototype tests performed at $U_{bias} = 40$ V. Fully depleted test devices exhibit a very clear linear behaviour at least up to 1.5 V, extending up to considerably higher ΔV_{pix} in some cases. The resistivity in the linear area is in the interval (200 – 500) M Ω for samples shown here, representing an excellent inter pixel isolation and testable without any problems on the depleted bulk.

Considering all tests on fully depleted production wafers from both vendors, the curves remain linear up to voltage differences distributed as (11.2 ± 2.9) V. The tests on main series wafers exhibit slopes within this linear region covering a wide range of resistivity values with a majority of results distributed at several 100 M Ω as well as a group of outliers yielding considerably higher results. For vendor A main production wafers the main group has resistivity values distributed as (370 ± 260) M Ω and a small outlying group with resistivities around (203 ± 14) G Ω . The correspondent distributions for vendor B main production wafers are (200 ± 130) M Ω for the main group and (2.32 ± 0.89) G Ω for the less dramatic outliers. These results approximately represent the parallel resistivity of four standard size inter pixel gaps and hence can be taken as a lower bound for the mean resistivity of inter pixel gaps scaled by a factor of 4. Especially the absence of very low resistivity values in the samples from both vendors confirms the good isolation qualities of the design and the competent implementation by the two manufacturers with the help of feedback and information from earlier device physics studies.

To realistically assess the worst possible impact of radiation damage on the inter pixel isolation, samples from a problematic vendor B pre-series wafer have been irradiated with high energy protons to the full design fluence of 10^{15} (1 MeV neutron equivalents)/cm² at the CERN irradiation facility. The resulting inter pixel current sweeps done at room temperature show a considerable contribution of constant leakage current if performed on a depleted bulk, which has been corrected against (see figure 4.39). At low ΔV_{pix} , a steep current increase apparently dependent of U_{bias} and absent on undepleted samples can be observed, leveling out into a much shallower linear part of the curve. The former increase could be an effect of the altered field geometry near the test pixel, redistributing the bulk leakage current into pixels with a more positive potential, but appears to be no inter pixel current proper. The approximate length of the linear interval going up to potential differences ranging between (8 – 12) V seems independent of applied bias, as does the slope in the linear area indicating a resistivity around (5 ± 3) M Ω or better for all bias values. The slope of the initial rise, effectively pointing towards a resistivity of (50 ± 20) k Ω , can not be considered a value representing the inter pixel resistivity, but could be a measure of the maximum influence of potential differences on noise variations caused by bulk leakage current to be expected after high fluence irradiation. Whether or not the implemented threshold adjustment of the front-end electronics can reliably cope with effects of this magnitude remains to be shown, but concerning isolation between the pixel cells themselves, these tests show a considerable effectiveness of the moderated p-spray technology even under extremely unfavourable conditions and are compatible with prototype tests on irradiated

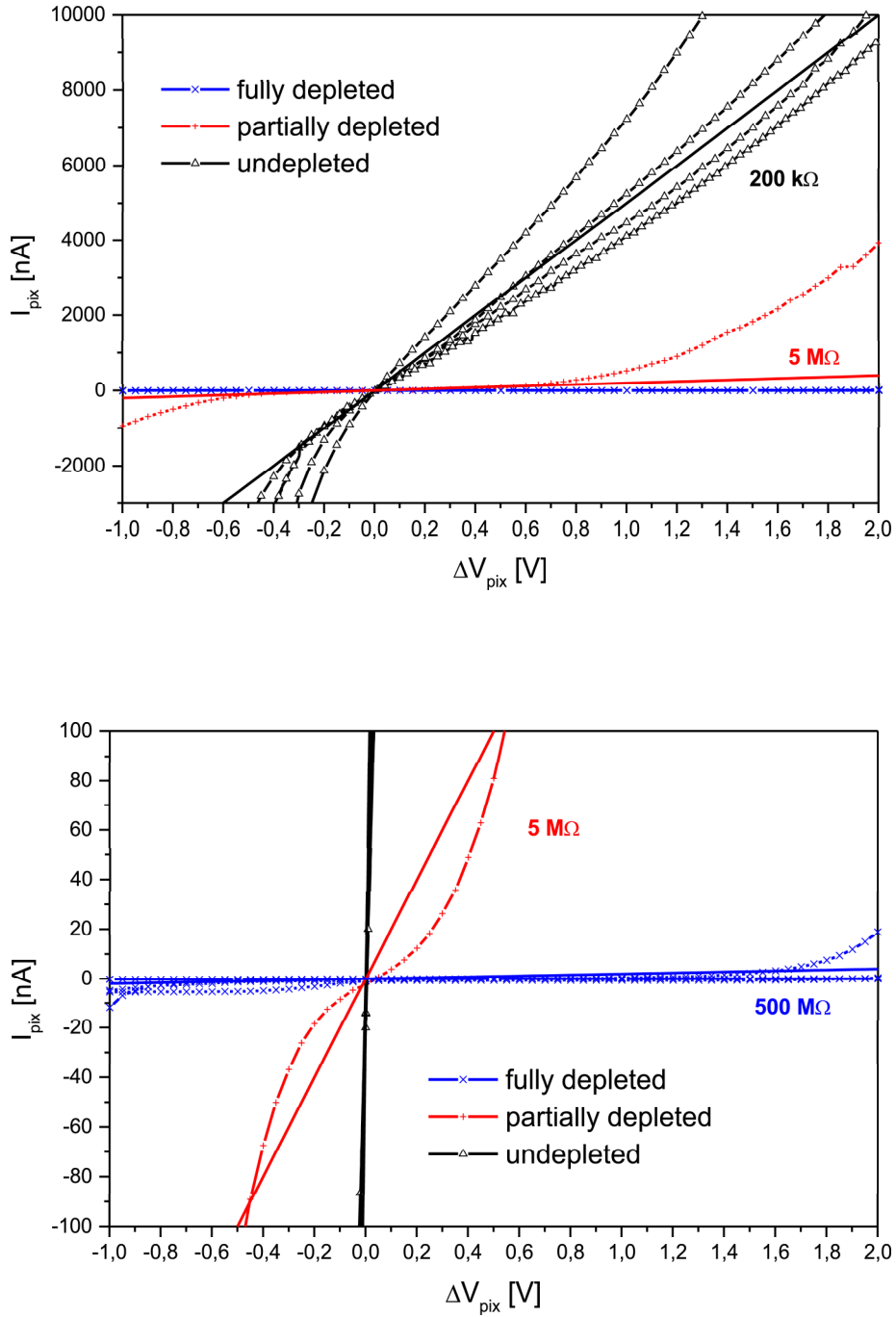


Figure 4.38: Current sweeps between two grounded double pixels and a central one biased with ΔV_{pix} on an undepleted, partially depleted ($U_{bias} = 50$ V) and fully depleted ($U_{bias} = 150$ V) bulk compared to typical slopes for the region of linear rise at a current scale a) up to $10 \mu\text{A}$ (top) and b) up to 100nA (bottom)

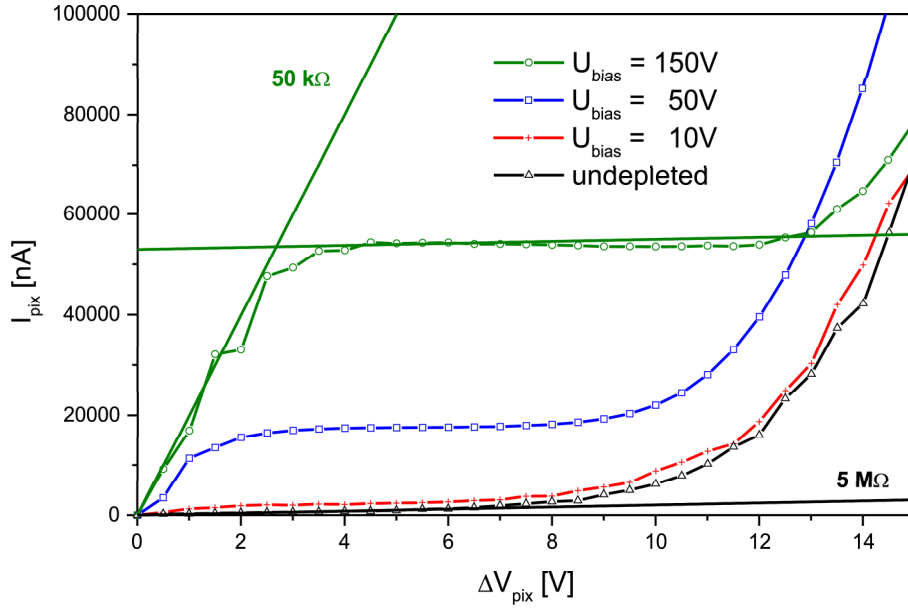


Figure 4.39: Current sweeps between two grounded double pixels and a central one biased with ΔV_{pix} on an undepleted or partially depleted bulk after proton irradiation, corrected for constant leakage current and compared to typical slopes for the region of linear rise

devices.

Inter pixel capacitance measured on the same test structures as the IVP tests has proven very sensitive to set-up calibration, so results influenced by calibration artifacts can not easily be ruled out. As repeated tests with different grounding of the n-side bulk have been carried out without any noticeable systematic effect on the capacitance, the exact scheme used for inter pixel currents could be used again. The test results from a sample of production wafers performed on fully depleted bulk yield an inter pixel capacitance distribution of (2.5 ± 1.7) pF without significant differences concerning vendor or production run.

A single device irradiated to full fluence with high energy protons shows a very unstable inter pixel capacitance in dynamic measurements on a depleted bulk, probably reconstruction artifacts due to changes in sensed leakage current dependent on the applied alternating test potential. A time resolved measurement on the test device without bias shows a rather stable C_{pix} value of (0.47 ± 0.07) pF. Similar measurements under bias yield mean values up to 5 pF, but exhibit so strong artificial fluctuations as to render the quality of the results suspect. In any case, no dramatic increase in inter pixel capacitance has been observed due to irradiation, which could have posed a problem due to increased capacitive noise during operation.

Measurements of sheet resistivity for implantations and metallizations have been performed on the narrower 1/16 geometry test structures on a grounded, but undepleted bulk. The tests on vendor A wafers yield a distribution of sheet resistance values of (160 ± 17) Ω/\square for n^+ -implantations and (144 ± 14) Ω/\square for p^+ -implantations. From the data from vendor B wafers, which are sparser due to time constraints of the production schedule, no implantation type dependent trend can be inferred, but an overall higher sheet resistance can be observed, the combined vendor B data distribution being (191 ± 22) Ω/\square . From these results, which are apparently typical for the processing at the respective manufacturer and only slightly varying between production runs, the implantation area density of the dopants could be derived, if the majority charge carrier mobility was known. For assumed mobilities typical for very high doping concentrations like $\mu_e \approx 100 \text{ cm}^2(\text{Vs})^{-1}$ and

$\mu_h \approx 50 \text{ cm}^2(\text{Vs})^{-1}$ [SZE85] and charge carriers from all doping atoms present at room temperature, the resulting formulae for the implantation area densities [HUG01] for n-type doping

$$N_{ni} = \frac{1}{e \cdot \mu_e \cdot R_s} \quad (4.7)$$

and p-type doping

$$N_{pi} = \frac{1}{e \cdot \mu_h \cdot R_s} \quad (4.8)$$

yield results of $N_{ni} \approx (3.9 \pm 0.4) \cdot 10^{14} \text{ cm}^{-2}$ and $N_{pi} \approx (8.7 \pm 0.8) \cdot 10^{14} \text{ cm}^{-2}$ for vendor A wafers and $N_{ni} \approx (3.3 \pm 0.4) \cdot 10^{14} \text{ cm}^{-2}$ and $N_{pi} \approx (6.5 \pm 0.8) \cdot 10^{14} \text{ cm}^{-2}$ for vendor B wafers. These values are close enough to each other to be all compatible with an implantation depth $\leq 500 \text{ nm}$ and a doping concentration $\geq 10^{19} \text{ cm}^{-3}$, and — at least for vendor A — consistent enough throughout the main series to indicate a well controlled implantation process.

In the case of metallization sheet resistors with a 1/16 geometry, differences between sheet resistance values from both wafer sides and both vendors are not significant, yielding an overall distribution of $(0.47 \pm 0.14) \Omega/\square$. Besides an unsurprisingly sufficient quality of the used metal concerning contact and conductivity, these values imply a continuously satisfactory standard of mask steps involving deposition and etching of the metal layers.

4.5 Logistics issues

Besides the main topics of direct quality control of the sensors and their production processes, more pedestrian tasks had to be organized and assessed. Their impact on sensor quality and the effectiveness of the quality plan deserves quick mention.

4.5.1 Transport and handling problems

The steps taken to minimize damage caused by handling procedures have been shown as adequate by visual inspections before shipping and at the bump vendors. Nevertheless, several mishaps did occur during handling and shipping of production wafers, which have shed some light on the potential threats to wafers and ways to avoid them.

The first such occurrence was a shipment damaged during a shipping accident, crushing the outer package, deforming the multi wafer box and destroying all contained wafers. Although no reasonable amount of packaging could prevent the wafers from being damaged by severe force like a collision of the parcel with a forklift, this incident motivated attempts to find the limits of shock tolerance and ways to improve the resilience of the packages, to be prepared for less dramatic shipping accidents. For this reason, parcels filled with a multi wafer box containing defect wafers and shock absorbing filling material were dropped from a considerable height under controlled conditions. The drop was performed from up to 13 m elevation onto a flat stone surface. A smaller 8 l parcel used for this test — while having survived lower drops from approximately 4 m without effects — did not show any outward signs of serious damage after having been dropped from the full height, but the resulting internal shock proofed forceful enough to shatter the wafers. When using a more voluminous box of 48 l, the filling material absorbed the shock considerably better, with the wafers not showing any visible mechanical damage afterwards. This series of events and tests has led to an increase in standard parcel size for shipping ATLAS pixel sensor wafers.

Another unfortunate but interesting incident was the dropping of a multi wafer transport box with eight measured wafers on their way to packaging — approximately 1.5 m onto an elastic laboratory floor. Of the eight wafers, two were shattered by the impact, two showed no outward damage, but have suffered from micro cracks leading to much earlier breakdowns and higher leakage current levels, rendering the wafers unfit for further assembly. For the remaining four wafers no significant deterioration of sensor quality has been indicated in repeated tests on the sensor tiles. Although the statistics yielded by this accident are low and are for obvious reasons not intended to be increased, the results point out the dangers of carelessness during routine tasks and of overestimating the protection provided by standard wafer boxes. On the other hand they indicate the real possibility of assembly and use of sensors affected by mechanical shock after a thorough examination for adverse effects.

4.5.2 Data management

Data from all measurements had to be gathered and stored during quality testing at all the participating ATLAS laboratories. In this task, the production data base (PDB) integrated into the SCT data base framework has proven valuable, but has created several specific requirements for the collaboration, too. To define not only the tests and compliance criteria, as needed for specifications, contracts and laboratory work anyway, but also to agree on the specific values and data structures to be put into the PDB did become a set of crucial decisions, and one not easily changed afterwards, as this would have required the change of the data base set-up itself. Discussions on these points had to be included into the planning process from the very start to create a sufficiently flexible data framework to incorporate later minor changes and additions to the measurement procedures and the assessment of results. As can be seen in the table of tests and criteria, a broad spectrum of possibly helpful parameters has been included from the start, as well as have raw or normalized test data as far as possible. The latter serves not only as an easy way for other institutes participating in sensor testing and module assembly and tuning to compare their own data with earlier or similar tests, but also as an off site back up for crucial test data in cases of computer crashes or other disasters at one of the testing laboratories. Only the raw data from the PLA tests — 160000 data

points for each test in the case of Dortmund measurements — have been deemed too expansive to be included in PDB uploads.

After laying down the conceptual framework in collaboration with the data base administrators, the remaining tasks included implementing a system for organizing the data at the institutes to facilitate easy uploading and exchange of test results. As the exact testing software at each participating laboratory varies, the primary test files will be different in syntax, and enforcement of changing the upload format of the whole data in the consensual setting of a scientific collaboration would be an undue demand on the participating institutes and would require considerable energy wasted on political maneuvering and pressuring. Therefore, only a common header has been agreed upon, containing all necessary information for data base insertion, after which a raw data field of any format, but marked as data not to be interpreted by the upload applications could be appended. As the upload applications are sufficiently selective to reject incomplete files and are set up to require any necessary quantity either to be present within the header or to be derived from the analysis of present data, they are enforcing the agreed upon data format by themselves without calling for any external kind of enforcement. In the case of the Dortmund laboratory, a set of programs based on the CERN ROOT software package has been developed, automatically generating headers from measurement output files, performing basic analysis tasks, appending raw data and organizing upload files and data base insertion scripts. To avoid multiple uploads and faulty analysis occurring with test data behaving in a non-standard way, an operator has to open and confirm each upload file, providing an opportunity to check any anomalies not already noticed during measurements.

Within a measurement setting mostly built from scratch with using only a minimum of existing instruments and measuring software, designing measurement and analysis tools already incorporating all necessary formatting and uploading features would be desirable, as has been done for module testing, using custom built hard- and software. But in the case of sensor tests the utility of a quick start of tests using already existing laboratory set-ups has outweighed problems with differing systematics and data formats, which have been harmonized to a degree necessary to produce relevant and comparable data on the produced sensors.

4 Results of quality testing

5 Assessment of relevance

The production of ATLAS sensors has been monitored step by step by quality tests from the initial prototyping to the end of the main production period and into extended purchase options to gain an additional stock of spare modules or to replace sensors lost because of handling and assembly problems or used for irradiation or electronics tests. As already discussed in the introductory chapters, the tests have a threefold aim, each aspect distinct, but interdependent to some degree with the other two.

The first aspect is the domain of quality control proper, testing the quality and likely operability of the product — in this case the pixel sensor — in terms of adherence to known specifications, building on the advance planning towards reliability and testability done during and before prototyping. The specifications have to be refined and the intensity of testing for a specific quality has to be directed continually according to knowledge about limitations of the testing procedures, problems of the manufacturing process and potential dangers for sensor operation, like it is illustrated by a succession of quality assurance steps similar to the FMEA process described in chapter 3.1. These successive steps of adaptation of the quality tests to problems at hand are informed by the other two aims, the gain of information on unknown or so far untested properties of the sensors as produced and delivered, and on the change of sensor properties by long term operation under conditions similar to those in the ATLAS experiment — most significantly on the tolerance of the sensors to radiation.

5.1 Quality assurance

The quality plan presented and supervised in the course of work on this thesis has proven both manageable for series tests at all sensor laboratories and sufficiently indicative to later sensor operation to catch close to all occurring production problems without excluding too many sensors which actually could be used in the experiment. This direct practical application of test results has set apart the testing regime under the quality plan from earlier, similar tasks during prototyping. The overall results of all measurement procedures have allowed for the gathering of a wide variety of information on functional parameters of the sensor as well as on details of the material and the production steps.

The time consumption of the testing process has allowed for a throughput of at least 5-10 wafers per week and participating laboratory, sensibly keeping up with the manufacturer output (see figures 5.1a-c for throughput data from the ATLAS laboratories). More important, the exact volume of tests, whether performed once per structure, per wafer or per batch could be fine-tuned according to the current indications of problems regarding specific parameters. The ability to respond to new problems appearing in the measurement data or in later test steps is illustrated in the assessment of surface currents across the guard rings on vendor A early main series wafers and the bias dot currents on vendor B pre-series wafers. In the latter case even a new test procedure has been introduced in response to insufficient information yielded by established tests. The peculiarities of the established testing procedures and their implementations at the individual laboratories have been studied especially in cases where a significant influence of method and laboratory are suspected. Even in the case of planarity tests, where radically different approaches have been used by the laboratories, the existing systematic effects could be identified and compared to a degree rendering the resulting data of relevance for conformity decisions and feedback to the vendors, both aspects integral to the quality plan.

In many cases the intended successive refinement of the production process by feedback from the ATLAS pixel institutes to the vendors could be realized. In the case of the vendor B pre-series

5 Assessment of relevance

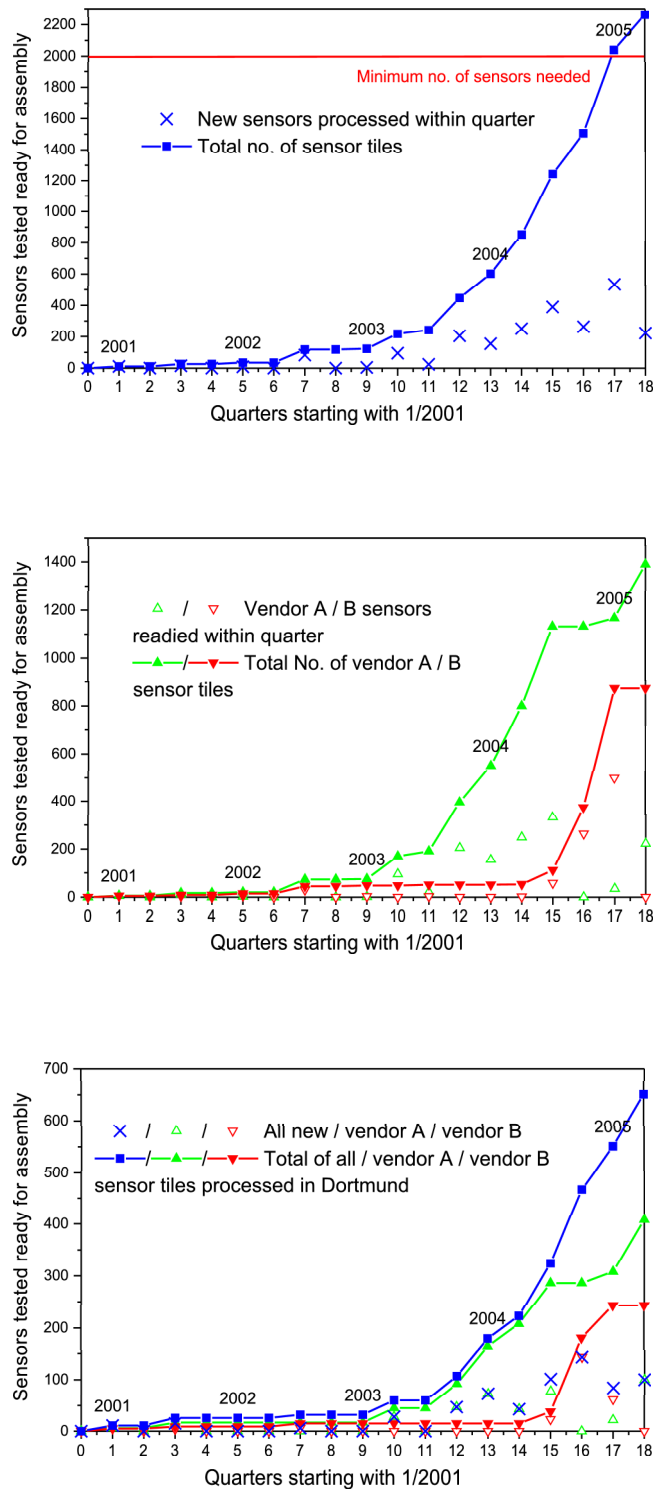


Figure 5.1: Sensor tile output in sum and per quarter a) for all ATLAS pixel laboratories in total (top), b) sorted by vendor (middle) and c) for testing efforts in Dortmund only (bottom)

this has led to the elimination of several initial problems severely limiting sensor operability and production yield, bringing the production up to a quality standard still not completely without problems, but financially and technically acceptable to both the ATLAS pixel collaboration and the vendor. For both vendors new causes for problems regarding conformity and operation — newly arising e.g. after changes in the production chain — have been caught during regular testing and have been discussed with the manufacturer and corrected for the following production run, sometimes even for late batches of the same run.

5.2 Sensor characteristics

The characterization of the wafer and sensor qualities does not only inform the decisions to be taken for quality control, but also leads to a better understanding of later detector behaviour and the manufacture process. This includes information on typical current levels after depletion as well as the exact depletion voltage within the allowed interval, both providing information on the substrate material and yielding data handy to choose operation settings after integration. Similarly, characteristics not critical for specification compliance like oxide capacitance and interface generation current have provided information for a better understanding of differences in the production processes, especially the distribution of interface characteristics dependent on used substrate and deposition process and the control of deposition parameters within this process.

Effectively testing possible problems of, solutions for and possibilities of sensor designs in a small series mass production as done in the run-up to this work, is of significant importance for the planning of later, similar pixel detectors, exemplified by several other collaborations inquiring on the layout of the already tested ATLAS sensor and experience gained with double sided processing by commercial vendors. Besides electrical properties, this information covers mechanical properties like planarity and surface quality crucial for detector assembly.

Another aspect of sensor testing of interest beyond quality control of the wafers at hand has been the opportunity to test several systematic influences at length, both applying known relations of e.g. temperature scaling as well as looking for interdependencies seldom considered, as they are specific to the tested devices and the testing set-up or hard to parameterize. Among those latter influences are the effects of humidity and bias stepping intervals on test results and overall curve shapes. Information like this might prove crucial for the planning and quality assurance of future sensor projects.

Another advantage of the quality plan from the point of view of pure device physics is the provision of test devices allowing for more detailed tests on the properties of p-spray isolated gaps. The comparison of the same p-spray layer as an under gate implantation in a MOSFET and as isolation in a punch through device working similar to a JFET has offered the opportunity to test aspects of isolation functionality on a set of different production runs from different vendors. From those results an assessment of the specific characteristics of the production runs has been possible, as well as first implications on the interdependence of different p-spray related phenomena.

Not to be neglected regarding the gain of information in device physics are the logistic advantages for dedicated research and development projects not directly concerned with pixel sensors. The availability of test devices for a wide array of material qualities and process parameters can be exploited to study those properties and test existing models or parameterizations without having to design or produce new test structures. This has already proven true for some studies cited or presented in this thesis, and, as the outer wafer sectors are not thrown out after dicing, can still prove helpful for later device research, with or without irradiation, for the preparation of future pixel detectors as well as general investigations of device parameters.

5.3 Radiation tolerance

Changes in behaviour due to irradiation effects has been a topic of intensive studies during the prototyping phase. Building on those results the irradiation tests on devices from production wafers presented here have verified the expected functionality of sensors built according to the

5 *Assessment of relevance*

ATLAS pixel design in a high radiation environment. Additionally there have been inquiries into aspects of sensor behaviour after irradiation not directly possible to extrapolate from existing data.

In the first category the development of leakage current and effective charge density induced in the bulk by hadronic radiation as well as the changes in interface generation current and flat band voltage induced by ionization of oxide and interface are well understood, and measurements taken on production samples agree with the expected behaviour. The radiation hardness of the p-spray layer in MOSFET structures and the inter pixel isolation after irradiation have only been studied in a small set of samples and have now been inspected slightly more in depth and especially using more samples differing in production parameters.

New insights have been gained in areas like current stability after irradiation and effects of incremental ionizing interface damage over long annealing periods, in both cases creating confidence in the consistent operation of irradiated sensors over long periods. Again, work on p-spray devices has had a central role among the newly considered topics, besides confirming the intrinsic radiation hardness of moderated p-spray demonstrating the functionality of the p-spray bias dot for all but the most outlandish production parameters. To assess radiation effects on sensor bulk and interface selectively and under different degrees of realism, the abundance of existing samples after wafer dicing has been used and the DEBE electron source and the proton irradiation facility at the CERN PS chosen to provide radically different irradiation scenarios. This combination of approaches to yield a more complete picture has proven very valuable and can be recommended for similar global studies of radiation tolerance in sensor devices.

6 Summary

The main focus of this thesis has been the verification of usability of sensors produced according to the ATLAS pixel sensor design by the chosen vendors and the question, in how far the implemented quality plan has yielded relevant results regarding quality control and device physics. Having reached the final stages of the pixel sensor production by spring 2005, successfully testing all regularly scheduled sensor wafers from both manufacturers and moving well into the testing of produced spares and replacements, an assessment of the suitability of the sensor design and the production process is possible, as well as of the positive impact of the quality plan in rejecting faulty sensors and identifying and understanding systematic production problems. This can confidently be considered a success in every aspect of quality assurance. Using the quality control data, the actual usability of produced sensors has successfully been assessed, new problems been identified and workable information for the solving of those problems provided to the manufacturers. Moreover, the test data offer a good overview of changes in the production process and information helpful for module assembly and detector operation.

Thus, the use of a quality plan specifically designed for a experimental physics collaboration and implemented during the work on this thesis has proven a viable and adequate approach, obviously applicable to similar task in other experiments. To realize this for a detector component, a high level of understanding of the device function and potential problems to be guarded against has to exist from the start and people sufficiently informed to assess new data have to be on call at all stages of the production, to spot unexpected behaviour and decide on refining the quality testing. Other crucial conditions for the successful implementation of a quality plan have been the good communication between the collaboration and the manufacturers and the ability to make quick and competent decisions. This stresses for future similar projects the need for a vendor able and willing to react quickly and to cooperate readily and the possibility of a wide variety of in house tests by the collaborators — including access to irradiation facilities — for cross checks and time critical in depth tests, even if mass testing were outsourced to the vendor. Especially, working with new, innovative technologies or making radical use of existing ones a high information accessibility and volume of data and the possibility to alter and repeat crucial tests to confirm newly observed behaviour and test it under a different aspect is of tremendous value.

Regarding the test of the designs and production processes chosen after sensor prototyping have been tested as fully adequate for permanent function in the ATLAS experiment according to the planned operation parameters. In particular, sufficient radiation tolerance of the sensor for long term operation in a high fluence hadronic radiation environment has been demonstrated, including sufficient depletion depth after full irradiation and current levels and current stability manageable for electronics and cooling systems. The full functionality and intrinsic radiation hardness of the moderated p-spray pixel isolation has also been confirmed as has the utility of the bias grid not only for initial testing but also as a sufficiently high impedance protective connection between the pixel cells before and after irradiation. All these results can become a basis of extrapolation for planning future pixel detectors as those for colliders with similar or even higher luminosity.

As the planning and realization of the quality plan has been the primary scope of work on this thesis, the positive results regarding confirmed sensor quality within the ATLAS project already can be considered sufficient justification for the efforts made, but are not all there is. Above and beyond any tests directly regarding sensor design and operation, the implementation of the quality plan allowed for data gathering on typical material properties and additional measurements elaborating on studies done during prototyping and earlier research and development projects. Just like these supplementary analyses have been informed by earlier results, they could serve as inspiration or source material for later research. E.g. the data gathered and considered on punch-through and switching behaviour in and below p-spray layers before and after irradiation have already allowed

6 Summary

for considerable elaboration on existing sources, but still falls short of a rigorous parameterization of the involved factors, which could be attempted later in a dedicated project. In this regard, quality assurance efforts can prove not only of interest for planning, engineering and controlling complex experimental set-ups, but of independent value for device physics.

A Appendix A: Physical constants

ΔE_G	band gap width in silicon	1.21 eV
e	electron charge	$1.602 \cdot 10^{-19}$ C
ϵ_0	permittivity of vacuum	$8.854 \cdot 10^{-12} \frac{\text{As}}{\text{Vm}}$
ϵ_{Si}	permittivity of silicon	11.75
ϵ_{SiO}	permittivity of dry silicon dioxide	3.4
k	Boltzmann constant	$8.61734 \cdot 10^{-5} \frac{\text{eV}}{\text{K}}$
μ_e	electron mobility in intrinsic Si (room temperature and low electric field)	$1450 \frac{\text{cm}^2}{\text{Vs}}$
μ_h	hole mobility in intrinsic Si (room temperature and low electric field)	$505 \frac{\text{cm}^2}{\text{Vs}}$
T_0	room temperature	$20^\circ\text{C} = 293.15$ K

Table A.1: Physical constants used within this thesis [PDB00] [DIN82] [LUT99]

A Appendix A: Physical constants

B Appendix B: Abbreviations

AC	alternating current
ALICE	a large ion collider experiment
ATLAS	a toroidal LHC apparatus
BOX	breakdown test on oxide
CAP	capacitance test between pixels
CCD	charge coupled device
CERN	centre/conseil européen pour la recherche nucléaire
CMS	compact muon solenoid
COX	capacitance vs. bias test on oxide
CP	combination of parity transformation and matter-antimatter conjugation in particle physics
CSC	cathode strip chamber
CVD	capacitance vs. bias test on diode
DB	data base
DC	direct current
DEBE	Dortmunder Elektronen-Bestrahlungseinrichtung
DEPFET	depleted field effect transistor
DORIC	digital opto-receiver integrated circuit
FE	front-end electronic chip
FMEA	failure mode and effect analysis
FZ	float zone silicon
GCD	gate controlled diode
GPIB	general purpose interface bus
IEEE	institute of electrical and electronics engineers
ITS	current time stability test
IVD	current vs. bias test on diode
IVG	current vs. bias test on GCD
IVP	current vs. bias test between pixels
IVS	current vs. bias test on sensor
JFET	junction field effect transistor
laser	light amplification by stimulated emission of radiation
LBNL	Lawrence Berkeley national laboratory
LCR	inductivity, capacitance and resistivity
Lemo	connector company named after Léon Mouttet
LEP	large electron-positron storage ring
LHC	large hadron collider
LHCb	LHC beauty experiment
MCC	module control chip
MFE	MOSFET threshold test
MIP	minimum ionizing particle
MOS	metal-oxide-semiconductor device
MOSFET	MOS field effect transistor
MPI-HLL	Max-Planck-Institut Halbleiterlabor
MDT	monitored drift tube
neq.	neutron equivalents
NIEL	non-ionizing energy loss

B Appendix B: Abbreviations

PDB	production data base
pixel	picture element
PLA	planarity measurement
PS	proton synchrotron
PSI	Paul-Scherrer-Institut
PUT	punch through test
RDxx	research and development project no.xx at CERN
ROOT	not an abbreviation, although anecdotal René's object oriented tool
ROSE	research and development on silicon for future experiments
RPC	resistive plate chamber
RPN	risk priority number
SCR	scratch pattern and vendor data inspection
SCT	ATLAS semiconductor tracker (using microstrips)
SRE	sheet resistance test
TGC	thin gap chamber
THI	thickness measurement
TQM	total quality management
TRT	transition radiation tracker
VCD	VCSEL driver chip
VCSEL	vertical cavity surface emitting laser
VIS	visual inspection

Table B.1: Abbreviations used within this thesis besides standard physics and chemistry nomenclature

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Figure T.1: Less serious achievements documented during the work on this thesis in collaboration with some of the people mentioned below.

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