Dissertation
zur Erlangung des akademischen Grades eines Doktors der Naturwissenschaften in der Fakultät Physik der Technischen Universität Dortmund

Commissioning of the ATLAS Insertable B-Layer and first operation experience

vorgelegt von
Dipl.-Phys. Karola Dette
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"Happiness can be found, even in the darkest of times, if one only remembers to turn on the light."

- Albus Percival Wulfric Brian Dumbledore

Abstract

Todays research in particle physics offers a wide field of opportunities for scientists from a variety of different subjects. Discoveries can only be made, with hundreds up to thousands of people working together in collaborations. Designing high precision detectors that can be up to several stories tall, followed by production, construction, commissioning and successful operation is only achievable with the combined effort of skilled and experienced detector physicists and engineers, while the vast amount of data recorded with those detectors calls for specialists in data analysis which are able to find the needle in a haystack or in other words the higgs in a sea of underground events.

One of the biggest science collaborations worldwide is the ATLAS collaboration with more than 5000 members from around 180 institutes. ATLAS is one of four big particle physics experiments at the LHC. Its tracking system has been upgraded with a new innermost layer, referred to as Insertable B-Layer (IBL), in 2014.

This thesis will focus on the construction, commissioning and first year of operation of the IBL detector and give a brief outlook on upgrade plans for the tracking system. The performance of the IBL and its services was observed before and after each step of its construction. Quality assurance measurements were performed to select the best working staves for the IBL construction. A system test was performed to verify the correct functionality of the final setup were the IBL was built on. A thorough commissioning testing the supply chain, the readout and the performance of complete detector was carried out in a clean room and repeated after installation in ATLAS. Several steps of re-testing took place after the IBL was exposed to thermal stress. The results of each commissioning step will be presented and discussed.

During the first year of operating the IBL, an increase of the low voltage currents in the readout chips was observed. A model to understand this increase will be introduced as well as measurements that were used to develop an operation guideline to protect the detector while continuing to take data.

The last part of this thesis will give a brief introduction to an alternative method for module hybridisation that was investigated as a possible option for the next upgrade of the ATLAS tracking system.

Contents

Chapter 1

High Energy Physics at the Large Hadron Collider

1.1 The LHC complex

Located at the Swiss-French border near Geneva, CERN[1] houses the facilities for a variety of particle physics research experiments. Several experiments make use of the pre-accelerator chain and four large detectors are placed around the LHC[2]. An overview of the complex structure of CERN's accelerator chain is shown in Figure 1.1.

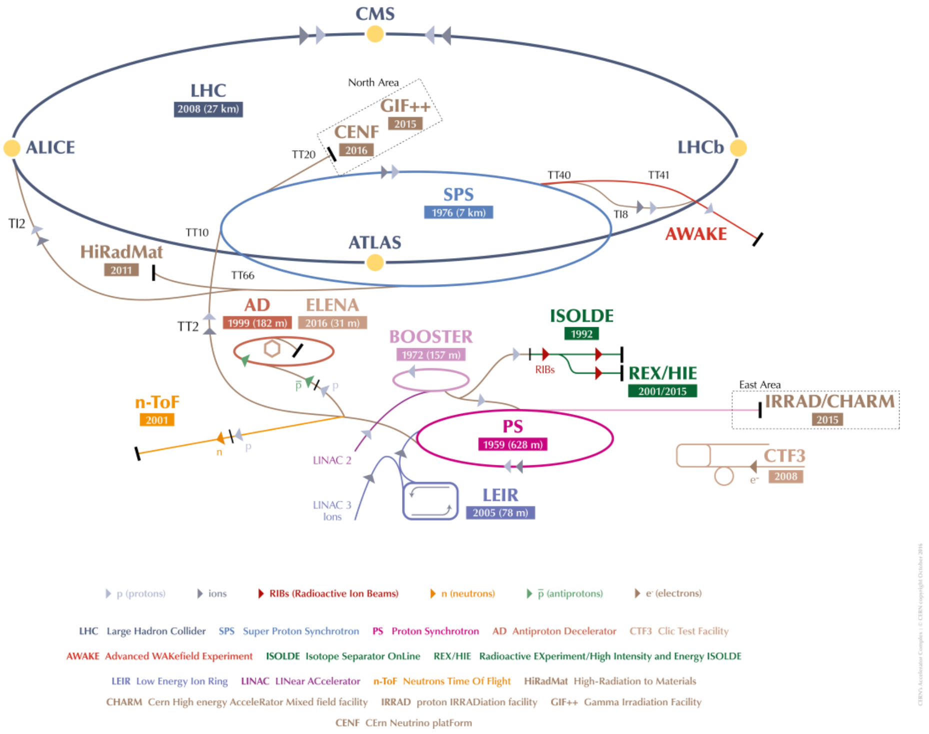

Figure 1.1: Overview of the CERN accelerator complex [1].

The purpose of the research done at CERN is to understand and explain the fundamental structure of the universe. Therefore, scientists perform high precision measurements on the basic constituents of matter. A profound understanding of how fundamental particles are produced

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[1] **C**onseil **E**uropéen pour la **R**echerche **N**ucléaire

[2] **L**arge **H**adron **C**ollider

and interact with each other is crucial in understanding the processes in nature.

The LHC collides particles at nearly the speed of light with a design centre of mass energy of 14 TeV and records the output of those collisions with complex detector systems. The accelerator consists of a 27 km ring built up of superconducting magnets and RF[3] cavities. The magnets used in the LHC are 1232 dipoles to bend the beam and 392 quadrupoles for focussing. In addition, there are magnets of higher order for smaller orbit corrections and for example to squeeze the beam prior to collisions. This results in a total number of more than 9000 magnets. The RF cavities oscillate at a frequency of 400 MHz and are used for acceleration as well as for keeping the proton bunches compact. An important parameter of an accelerator is its luminosity which describes the number of interactions per time. The instantaneous luminosity can be written as:

$$L = \gamma \frac{n_b N^2 f_{\mathrm{rev}}}{4\pi\beta^* \varepsilon_{\mathrm{n}}} R \; ; \tag{1.1}$$

$$R = 1/\sqrt{1 + \frac{\theta_c \sigma_z}{2\sigma}} \tag{1.2}$$

with γ = proton beam energy; n_b = number of bunches per beam; N = bunch population; f_{rev} = revolution frequency; β^* = beam beta function (focal length) at the collision point; ε_{n} = transverse normalized emittance; R = luminosity geometrical reduction factor; θ_c = full crossing angle between colliding beams; and σ, σ_z = transverse and longitudinal r.m.s. sizes [2]. In 2016 the LHC reached a peak luminosity of 1.37 x $10^{34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$ as shown in Figure 1.2.

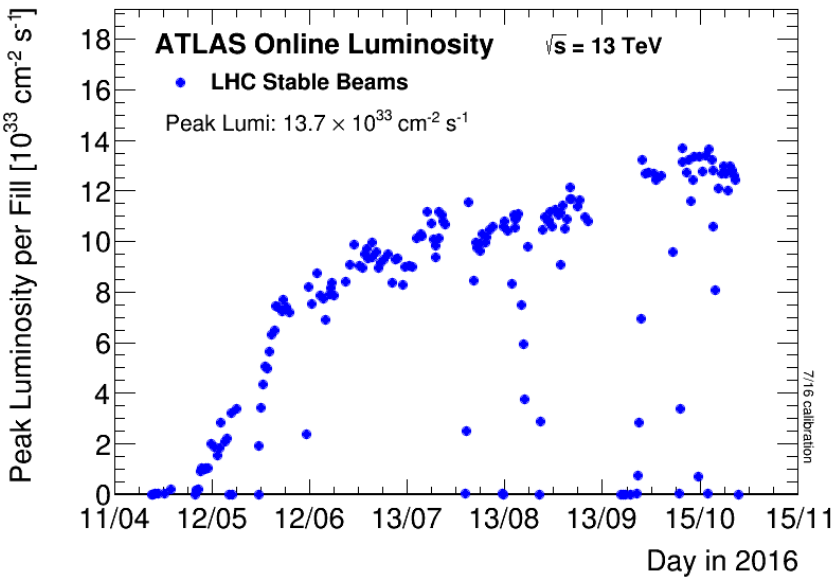

Figure 1.2: The peak instantaneous luminosity delivered to ATLAS during stable beams for pp collisions at 13 TeV centre-of-mass energy is shown for each LHC fill as a function of time in 2016. The luminosity is determined using counting rates measured by the luminosity detectors, and is based on a preliminary analysis of van-der-Meer beam-separation scans during 2016 [3].

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[3] **R**adio**f**requency

1.2 Planned upgrades of the LHC

In 2016, the LHC showed that with the current setup a luminosity of 1 x $10^{34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$ is achievable at a centre-of-mass energy of 13 TeV. This results in an integrated luminosity of around 40 fb^{-1} per year. To accumulate even more data, a two step upgrade will follow in the coming years. During the so-called LS2[4] the phase-I upgrade will take place. This upgrade aims for an increase of luminosity to 2.2 x $10^{34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$. One major change will be the start of the accelerator chain. Instead of the current linear accelerator LINAC 2[5], which can accelerate protons up to 50 MeV, a new linear accelerator called LINAC 4[6], which can accelerate protons up to 160 MeV, will be used. Linac 4 hit its design energy for the first time during commissioning tests in October 2016. The LS3[7] will aim for setting up the LHC in the so called High Luminosity configuration. A design study has been performed to determine a set of beam parameters and hardware configuration that will enable the LHC to reach a peak luminosity of 5 x $10^{34}\,\mathrm{cm}^{-2}$ which should result in an integrated luminosity of 250 fb^{-1} per year [2]. After a preliminary HL-LHC design report had been published in 2015, it had been announced that this number might even be increased and a luminosity of 7.5 x $10^{34}\,\mathrm{cm}^{-2}$ could be achievable [4]. At the same time the detectors will undergo the phase II upgrade to cope with the increased requirements with respect to radiation hardness, readout speed and precision. An overview of the estimated timeline is shown in Figure 1.3.

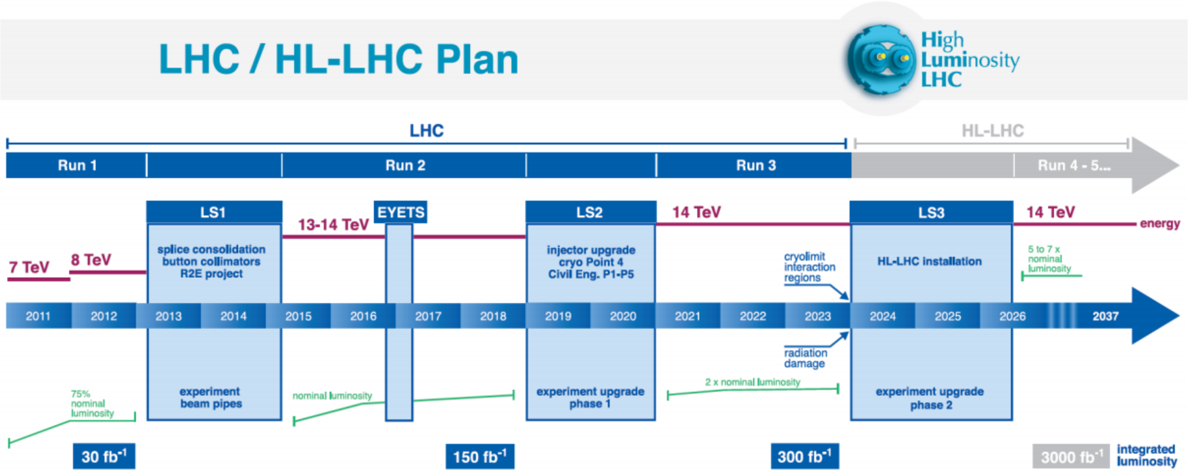

Figure 1.3: LHC baseline plan for the coming years. Shown in red is the collision energy, shown in green the luminosity increase. The blue boxes mark shutdown times of the LHC where upgrades will take place [4].

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[4] Second **L**ong **S**hutdown

[5] **Lin**ear **ac**celerator **2**

[6] **Lin**ear **ac**celerator **4**

[7] Third **L**ong **S**hutdown

Chapter 2

The LHC experiments

Collisions occur at four spots around the LHC and are recorded by four experiments located at those collision points: ALICE[1], ATLAS[2], CMS[3] and LHCb[4]. The four experiments can be subdivided in two groups. ATLAS and CMS are multipurpose detectors which are able to measure particles that propagate in all spatial directions, except those that move along the beam axis. They are designed to explore new physics, as for example the search for new particles which are predicted by theories of supersymmetry and to gather more statistics about the Higgs-mechanism. Therefore, they are operated at the maximum LHC luminosity.

ALICE and LHCb are specialised detectors. ALICE focusses on the study of the so called quark-gluon plasma to understand the origin of confinement, a mechanism that binds quarks and gluons in composite particles, and the generation of the mass of those composite particles.

LHCb is a forward detector which is designed to make precision measurements especially on b-quarks and their counterpart the anti-b quarks. The study of slight differences in the decay channels between those two particles can help to explain the matter-antimatter asymmetry, observed in the universe.

2.1 The ATLAS Detector

2.1.1 Overview

The LHC provides an environment with respect to energy and luminosity that extends the region of discoverable physics investigated at every other accelerator experiment that has been built so far. The ATLAS detector was designed and optimised to provide a maximal discovery potential for new physics beyond the standard model as well as the option to perform high precision measurements of known physics. To provide physicists with the data for those measurements, several requirements need to be fulfilled. The tracking system needs to provide efficient tracking data up to high luminosities to enable the measurement of high-p_T[5] lepton momentums, identification of electron, photon, τ-lepton and heavy-flavour particles as well as a full event reconstruction at lower luminosities. To cover events with particle tracks in all directions, a large acceptance in pseudorapidity $|\eta|$ with a coverage of nearly the full azimuthal angle ϕ is necessary. The coordinate system used in ATLAS is a right-handed system using cylindrical coordinates r and ϕ (= azimuthal angle around the z-axis) in the transverse plane, its centre point being located at the interaction point in the middle of the detector and the z-axis along the beam pipe. For

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[1] **A** **L**arge **I**on **C**ollider **E**xperiment

[2] **A** **T**oroidal **L**HC **A**pparatu**S**

[3] **C**ompact **M**uon **S**olenoid

[4] **L**arge **H**adron **C**ollider **b**eauty

[5] Transverse momentum

the x- and y-axis the LHC is taken as frame of reference, where the x-axis points towards the centre of the LHC and the y-axis points from the ring towards the surface. The pseudorapidity is defined as:

$$\eta = -\ln \tan\frac{\theta}{2} \tag{2.1}$$

with θ = polar angle with respect to the beam direction [5]. The calorimeter system needs to be optimised for electron and photon identification as well as for precise measurements of jets and missing transverse energy, while the muon system has to provide high-precision measurements of muon momentums. In addition, a high trigger efficiency at low-p_{T} di-muon events is required since this is crucial for the detection of events that contain b-quarks which are of high interest for most physics processes investigated at ATLAS.

2.1.2 Subsystems

ATLAS is the largest detector at the LHC with a diameter of 25 m, a length of 46 m and a weight of roughly 7000 t [6]. Four different subsystems provide the data for the event reconstruction. Those subsystems are:

- inner detector
- electromagnetic calorimeter
- hadronic calorimeter
- muon chambers

A sketch of the detector is shown in Figure 2.1. The inner detector is placed in a cylinder with a length of 7 m and a radius of 1.15 m and consists of three different systems, each optimised for

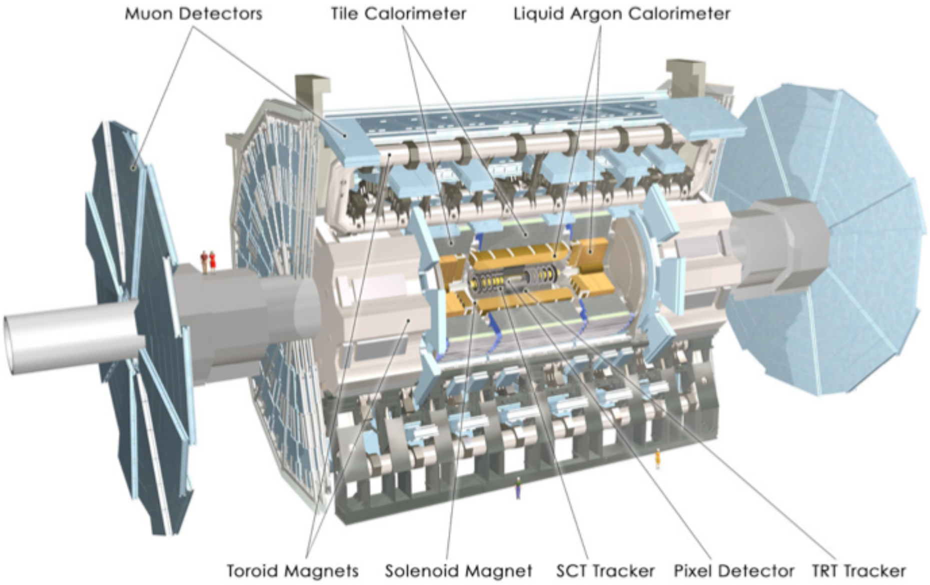

Figure 2.1: ATLAS overview [7]

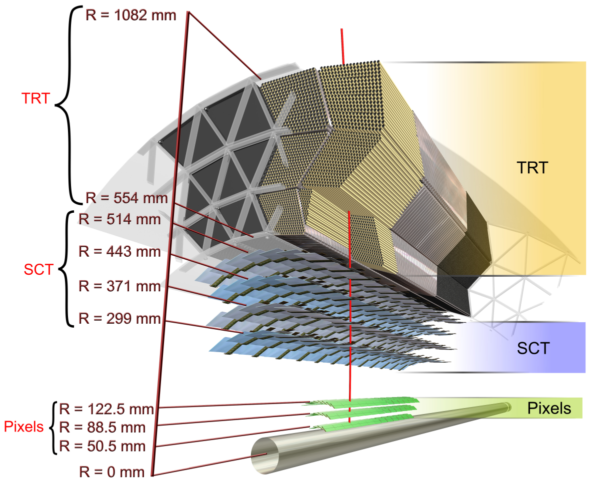

Figure 2.2: Schematic view of the ATLAS tracking system before installation of the IBL [8].

the requirements with respect to the distance of the interaction point. Closest to the interaction point are two silicon-based systems, namely the pixel detector and the SCT[6] detector. Since this thesis focusses on a part of the pixel detector, this system will be described in more detail in chapter 5. The SCT consists of silicon strip modules where each module contains two sensor layers rotated against each other by a 40 mrad stereo angle to increase the space resolution. Next to the SCT a continuous straw-tube detector called TRT[7] is located as the outermost part of the tracking system. It consists of straw tubes with a diameter of 4 mm, holding a thin wire in their centre. Xenon gas is used as a filler that gets ionised when traversed by charged particles. The TRT can be used to distinguish between electrons and hadrons by measuring transition radiation.

To receive information about the particle momentum in addition to the vertex information, the tracking system is surrounded by a solenoid magnet with a field intensity of 2T that bends the trajectories of charged particles. Schematics of all three subsystems are shown in Figure 2.2.

In the electromagnetic and hadronic calorimeter particles are stopped to measure their energy. For the electromagnetic calorimetry a liquid-argon sampling calorimeter is used which is built out of passive absorbers and active detection material. In ATLAS the absorber material is lead and the detection material is liquid argon. The calorimeter is contained in a cylinder of 6.8 m length at an outer radius of 2.25 m and covers the pseudorapidity range of $|\eta| < 3.2$. The hadronic calorimeter also uses liquid-argon for the end-caps with copper as passive medium while in the barrel region a scintillator-tile calorimeter made of scintillating tiles as active medium and iron plates as absorbers is placed. It is divided into a long barrel of 5.56 m and two extended

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[6] **S**emi**C**onductor **T**racker

[7] **T**ransition **R**adiation **T**racker

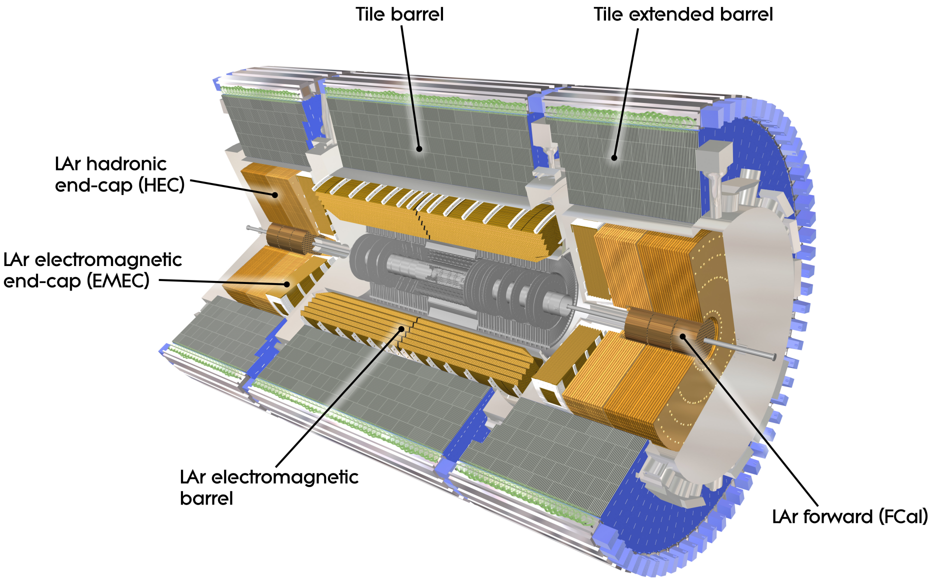

Figure 2.3: Schematic view of the ATLAS calorimeter system [9]

barrels of 2.91 m at an outer radius of 4.25 m. A schematic of the complete calorimeter system is shown in Figure 2.3. Nearly all particles are stopped inside the calorimeter system with two exceptions.

Due to their small interaction probability with matter, muons and neutrinos pass through the calorimeter system. While the only possibility for neutrino detection is the calculation of missing energy, muons can be measured in dedicated muon systems. The muon spectrometer is the outermost system of the ATLAS detector and located at an outer radius of about 11 m. A toroidal magnetic field of 4 T bends the muon trajectories to allow momentum measurements. Four different systems are used for the muon detection: TGC[8], RPC[9], MDT[10] and CSC[11]. Figure 2.4 shows the location of each system.

ATLAS showed an exceptional performance in 2016 where it recorded 92.54% of the delivered luminosity of $38.9\,\mathrm{fb}^{-1}$ [3]. The evolution of the luminosity over the year and the data recorded by ATLAS is shown in Figure 2.5.

2.1.3 Tracking and b-tagging

This thesis documents the installation, commissioning and operation of the new innermost layer of the ATLAS pixel detector that has been designed to improve the track and vertex reconstruction performance of the ATLAS tracking system. How is the tracking data used and why is the improvement of the tracking performance so important? A majority of physic searches at the

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[8] **T**hin-**G**ab **C**hambers

[9] **R**esistive-**P**late **C**hambers

[10] **M**onitored **D**rift **T**ubes

[11] **C**athode **S**trip **C**hambers

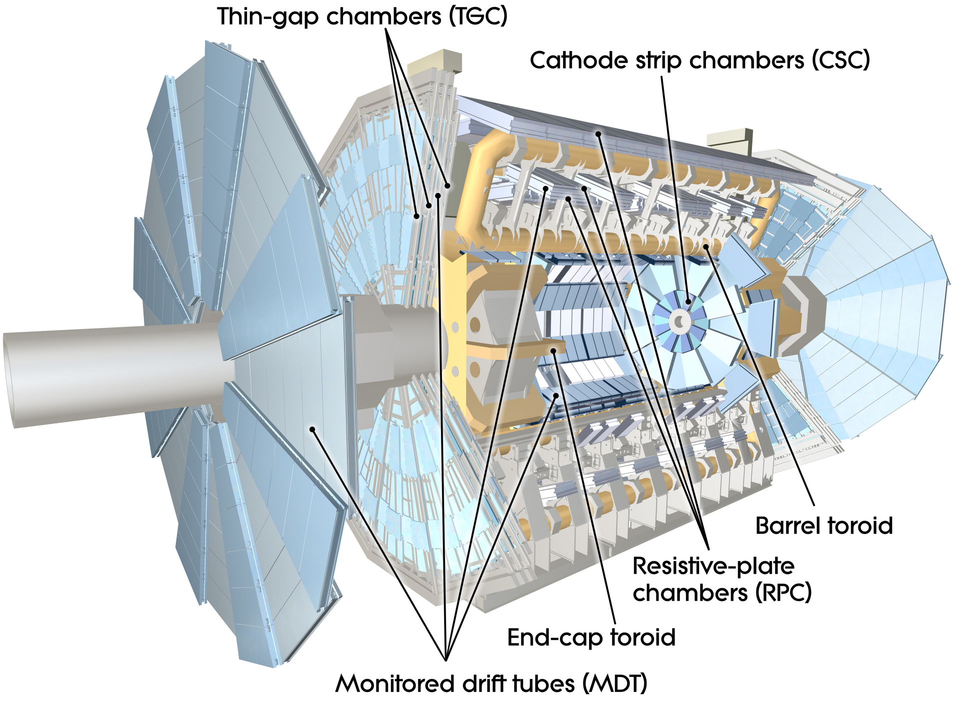

Figure 2.4: Schematic view of the ATLAS muon system [10]

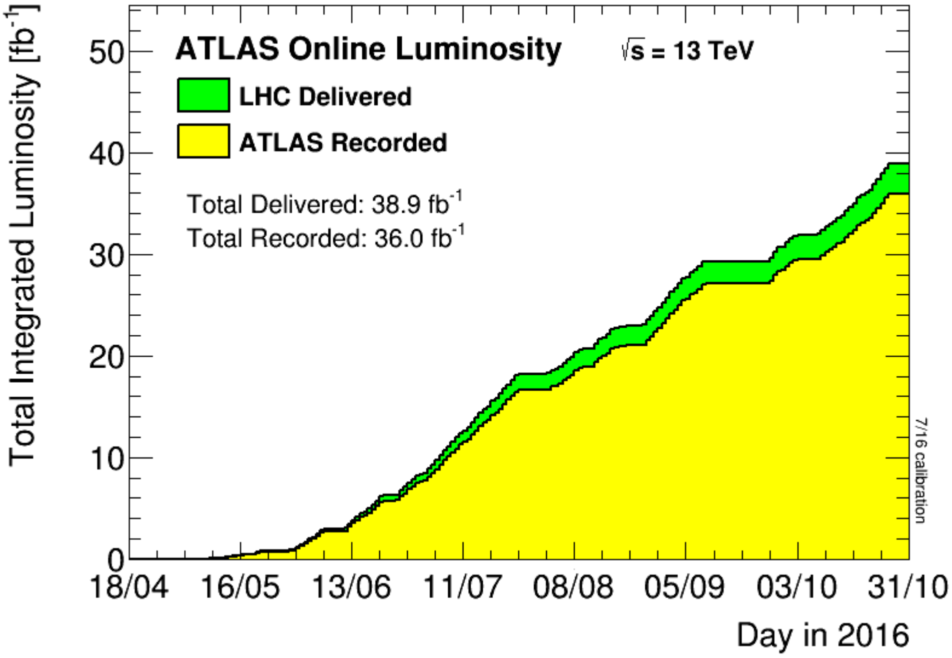

Figure 2.5: Cumulative luminosity versus time delivered by the LHC to ATLAS (in green) and recorded by ATLAS (in yellow) during stable beams for pp collisions at 13 TeV centre-of-mass energy in 2016 [3].

LHC experiments require precise information about hadron-jets containing b-quarks, so called b-jets. Tracking does not only give information about the trajectories of particles produced in collisions and their subsequent decay products but also information about a particle's charge and momentum. Those informations are used as inputs to so called b-tagging algorithms which are able to identify b-jets. Identifying events that include high p_{T} b-jets in their final state is essential for analyses that aim for precision measurements in the top-quark sector, searches for the Higgs boson and also searches for new physics signatures [11, 12]. An improved tracking performance enhances the quality of the b-tagging and is therefore directly beneficial for those analyses.

Chapter 3

Interaction of particles with matter

The aim of a tracking system is to provide high precision track measurements of particles. To measure those particles, their interaction with matter has to be well known. In tracking systems as used in high energy experiments, charged particles need to be measured while keeping the distraction of their trajectory to a minimum. Therefore, their energy deposit in the system should be minimised. If the energy loss in the insensitive material of the tracking system is too high, this would also affect the accuracy of the energy measurement in the calorimeter system and in addition would make track reconstruction more difficult.

Particles can interact with matter over a variety of processes. While traversing a detector, a combination of more than one kind of interaction can take place. Interactions that are used for particle detection are amongst others:

- ionisation by charged particles
- photon absorption/scattering
- transition radiation
- bremsstrahlung
- cherenkov-radiation

An important physical quantity that needs to be taken into account is the interaction probability expressed by the cross section σ which can be described as:

$$\sigma = \frac{\dot{N}_{\mathrm{R}}}{\dot{N}_{\mathrm{in}}} \frac{1}{nl} \tag{3.1}$$

with $\dot{N}_{\mathrm{R}}$ = reaction rate, $\dot{N}_{\mathrm{in}}$ = rate of incoming particles, n = number density of the target particles, l = length of the target [13]. This is true for thin targets which show only negligible interactions with the traversing particles. For thicker targets an exponential decrease of the number of incoming particles has to be assumed:

$$N(x) = N_0 e^{-\mu x} \tag{3.2}$$

with N_0 = number of incoming particles before interaction and μ = absorption coefficient. This formula was already found to be true in 1760 for the weakening of radiation intensity when radiation traverses an absorbing substance [14]. If a charged particle traverses matter it looses energy via ionisation and excitation. The amount of energy lost per distance is described by the Bethe-Bloch formula [15, 16, 17].

The mean energy loss in matter is a stochastic process and dependent on the properties of the traversed matter A, the mass M and the particle velocity β:

$$-\left\langle \frac{dE}{dx} \right\rangle = n \int_{T_{max}}^{T_{min}} T \, \frac{d\sigma_A}{dT} \, (M, \beta, T) \; dT \tag{3.3}$$

with n = target particle density, $\frac{d\sigma_A}{dT}$ = differential cross-section for the loss of kinetic energy T in a collision.

For the following calculations a charged traversing particle is assumed that gets scattered at orbital electrons, while the velocity and energy of the incoming particle is high compared to the orbital electrons. The target density is given as the electron density of the orbital electrons:

$$n_e = Z \, \frac{\rho}{A} \, N_A \tag{3.4}$$

If the minimal energy loss is further assumed as

$$T_{min} = \frac{I^2}{2 m_e c^2 \beta^2 \gamma^2} \tag{3.5}$$

one gets the Bethe-Bloch formula in the following form:

$$-\left\langle \frac{dE}{dx} \right\rangle = 4\pi N_A r_e^2 m_e c^2 \, \frac{Z}{A} \, \rho \, \frac{z^2}{\beta^2} \left[\frac{1}{2} \ln \frac{2 m_e c^2 \beta^2 \gamma^2 T_{max}}{I^2} - \beta^2 - \frac{\delta(\beta\gamma)}{2} - \frac{C(\beta\gamma, I)}{Z} \right] \tag{3.6}$$

with

- N_A = Avogadro's number : 6.022 x 10^{23} mol^{-1}
- r_e = electron radius : 2.8 fm
- m_e = electron mass : 511 $\frac{\mathrm{keV}}{\mathrm{c}}$
- z, β = charge in units of e and velocity of the traversing particle
- Z, A = atomic number and weight of the traversed medium
- T_max = maximal energy transfer to an orbital electron
- ρ = density correction, needed for calculations at high energies
- I^2 = mean excitation potential (= mean energy needed for ionising the material)
- C/Z = orbital correction, needed for small β values

A more detailed derivation of this formula can be found in Ref. [13]. Since the energy loss is dependent on the kinematic variables of a particle, it can be plotted for example as a function of $\beta\gamma$. Figure 3.1 shows an example plot for muons in copper. The first vertical black line (labeled

"Minimum ionization") marks the region of so called MIPs[1]. Near $\beta\gamma > 3$ the energy deposit reaches a local minimum with only a marginal increase at higher energies. For the energy deposit in thin silicon sensors a non-gaussian distribution can be observed since secondary electrons contribute to the ionisation at higher energies. Those electrons are called δ-electrons. Due to this effect, the energy loss of charged particles will follow a Landau distribution as displayed as an example for a 500 MeV pion in Figure 3.2.

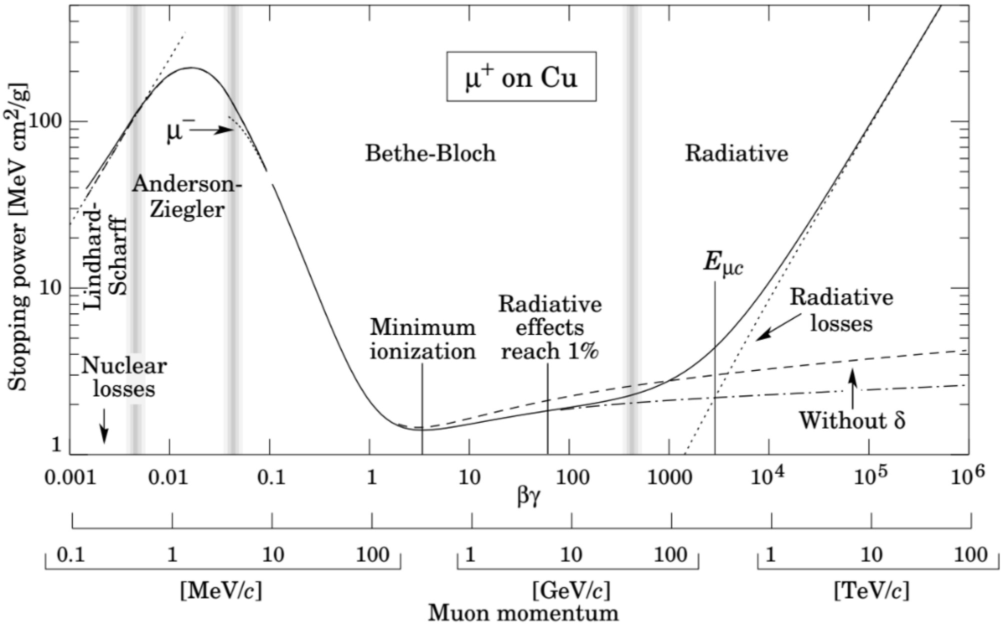

Figure 3.1: Stopping power ($= \langle -dE/dx \rangle$) for muons in copper as a function of $\beta\gamma = p/Mc$. First vertical black line indicates the region were MIPs are expected [18].

Photons also play an important role in the testing and operation of silicon trackers. As they are not charged, they interact differently with matter than the above described charged particles. Photons interact with matter in three different ways:

- photoelectric effect
- compton effect
- pair production

The first two processes do not play a major role in collider experiments, but are useful for laboratory tests of silicon detectors. The photoelectric effect describes a photon that is absorbed by an orbital electron. In case the energy of the photon exceeds the binding energy of the electron, the electron carries away the energy difference. If the photon is not absorbed but interacts with the orbital electron via inelastic scattering processes while loosing part of its kinetic energy, the effect is called Compton effect or Compton scattering.

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[1] **M**inimum **I**onising **P**article

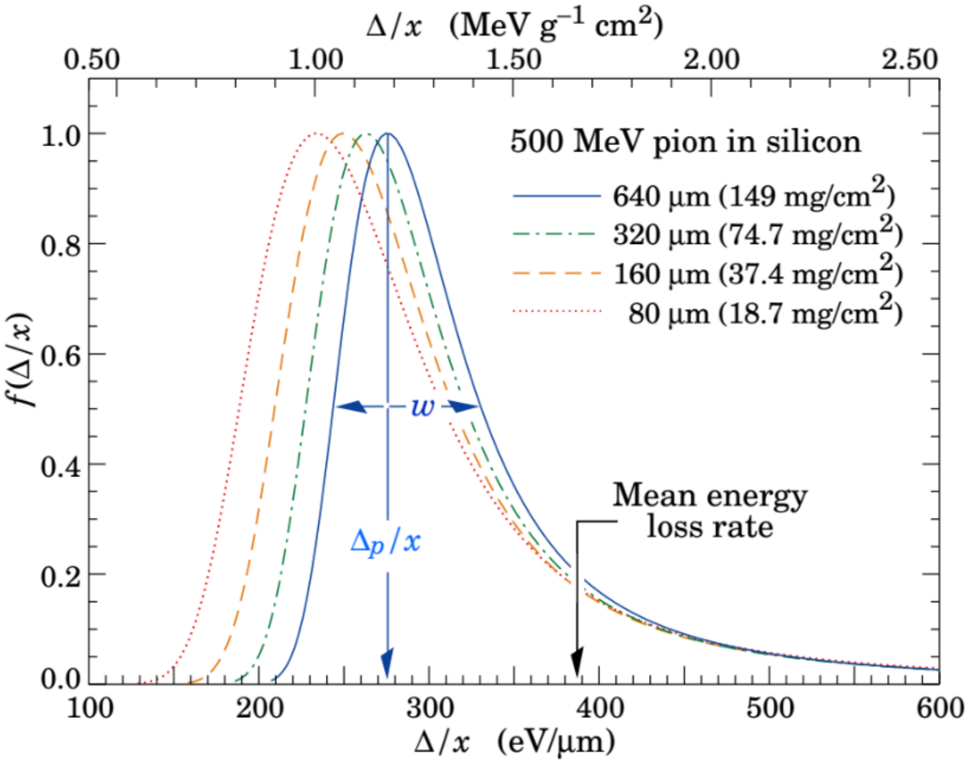

Figure 3.2: Straggling functions in silicon for 500 MeV pions, normalized to unity at the most probable value $\delta p/x$. The width w is the full width at half maximum. [18].

The third effect, called pair production, is the effect that is important for high energy experiments. Hereby an incoming photon interacts with the electromagnetic field of a nucleus and creates an electron-positron pair. The energy of the photon needs to be at least two to four times the energy of a resting electron for this effect to take place [19]. For tracking detectors this process is challenging since the reconstruction of photons via the tracks of the electron-positron pairs is difficult and the mean free path due to the pair production is dependent on X_0, a material property referred to as radiation length. From this, the free path can be written as: $\lambda = \frac{9}{7}X_0$ [20]. In order to keep the probability for pair creation in the tracking system low, this value needs to be kept as small as possible.

Chapter 4

Hybrid silicon detectors

Tracking systems as the one used in the ATLAS detector need to provide high precision measurements in a challenging environment. They have to offer a fast read-out with high granularity while not adding too much material and need to withstand high radiation doses due to their close proximity to the interaction point. The ATLAS Pixel Detector, which will be described more detailed in chapter 5, uses hybrid silicon detectors to fulfil those requirements. They consist of a silicon sensor in which a signal is created when a particle traverses the sensor and a silicon read-out chip for signal processing and transfer. The sensor and the read-out chip are connected via so called bump bonds, small solder bumps, which connect each sensor pixel with a pixel of the read-out chip. Underneath the bump balls, a layer of UBM[1] is applied to the sensor and front end chip. This metal layer is used to ensure a good electrical and mechanical contact of the bumps and is applied onto the passivation openings of sensor and chip. A reflow step is performed at 260 C° to establish the connection. A sketch of this process, referred to as flip chip process, is shown in Figure 4.1.

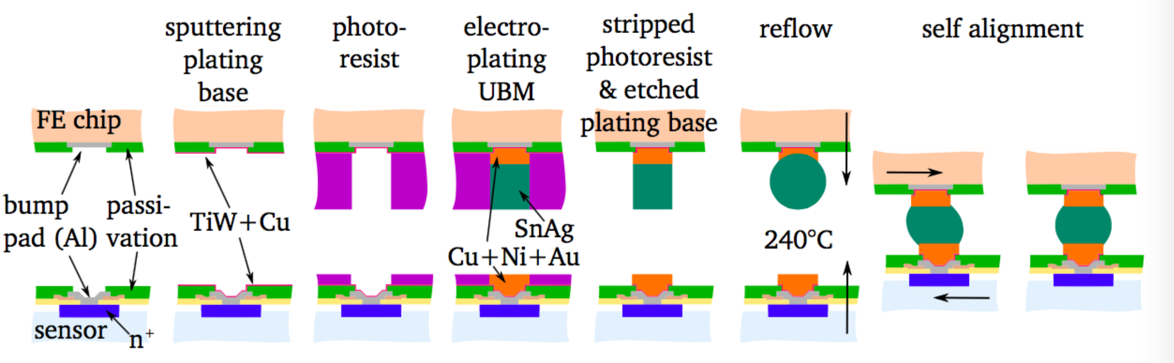

Figure 4.1: Schematic picture of a bump bonding process [21]

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[1] Under Bump Metal

4.1 Layout and working principle of silicon sensors

When an ionising particle traverses the silicon of the sensor, it creates mobile electron-hole pairs as displayed in Figure 4.2. To create those pairs, an energy bigger than the band gap energy of silicon of 1.12 eV [22] is needed. Since additional lattice excitations which consume part of the energy need to be taken into account, the required energy to create a pair is 3.62 V on average [19]. Silicon is a semiconductor and belongs to the fourth main group of the periodic table. It crystallises in a diamond lattice structure with two face-centred cubic crystal lattices. As one can see from Figure 4.3, each silicon atom has four equidistant neighbours. To introduce additional charge carriers, a technique called doping is used where elements from the third and fifth main group are introduced into the silicon.

For the so called p-doping, elements from the third group with three valence electrons are added. The introduction of those so called acceptors results in an excess of positive charge carriers since they create a deficit of electrons in the material. For the so called n-doping, elements from the fifth main group as, for example, arsenic or phosphor are used. They are called donors and have five valence electrons while only four are used for the binding with the silicon atom. This creates an excess of electrons and thereby negative charge carriers. Examples of different doping styles and their influence on the band structure of silicon are shown in Figures 4.3 and 4.4.

A planar silicon sensor can be treated as a semiconductor diode where the introduction of an n-doped and p-doped region creates a pn-junction. A so called depletion zone forms at the junction due to charge carrier recombination. Reverse biasing of the sensor increases the volume of this zone which is free of charge carriers and prevents the recombination of the electron-hole pairs. When a traversing particle creates electron-hole pairs, the electrical field separates them as they start drifting to the opposite sites of the sensor. The direction of the growth of the depletion zone depends on the type of silicon used, as shown in Figure 4.5 for silicon with a p- and n-type bulk.

The voltage needed to extend the depletion zone over the complete bulk volume of the sensor is called depletion voltage V_{depl} and depends mainly on the thickness of the bulk and the bulk resistivity ρ. It can be described as:

$$V_{\mathrm{depl}} = \frac{d^2}{2\rho \cdot \mu_{\mathrm{e}} \cdot \epsilon_{\mathrm{Si}} \cdot \epsilon_0} \tag{4.1}$$

with μ_e = electron mobility : 1427 $\frac{\mathrm{cm}^2}{V_s}$, ϵ_{Si} = dielectric constant of silicon : 11.75 and ϵ_0 = permittivity constant : $8.85 \cdot 10^{-6} \frac{\mathrm{pF}}{\mu\mathrm{m}}$ [21]. The influence of radiation on the depletion voltage will be described in section 4.2.

The reverse biasing also causes the creation of leakage current. One has to distinguish between bulk generation current and surface current. Bulk generation current and an avalanche breakdown are intrinsic properties of every silicon sensor. In addition, impurities and defects

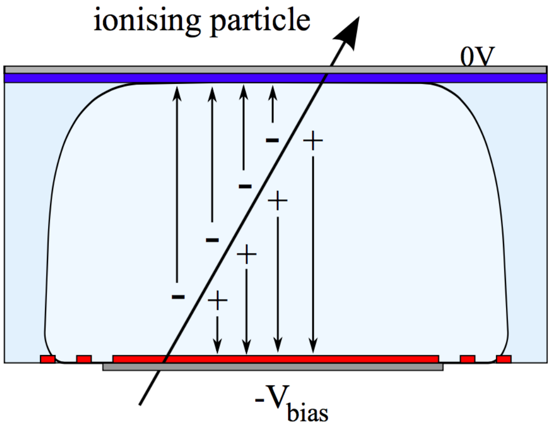


Figure 4.2: Cross section through a silicon sensor. The depletion zone is pictured in light blue in the middle, the p^+ implantation in red at the bottom and the n^+ implantation in dark blue at the top [21].

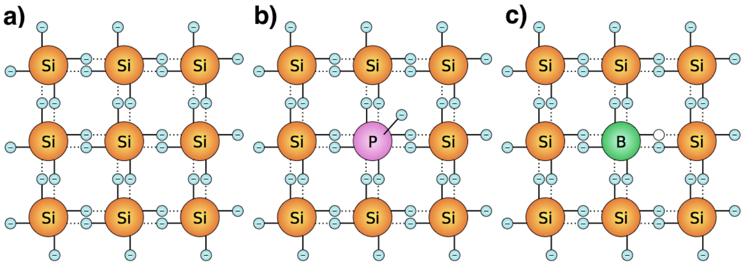


Figure 4.3: Silicon lattice cells: a) undoped b) n-doped c) p-doped [23]

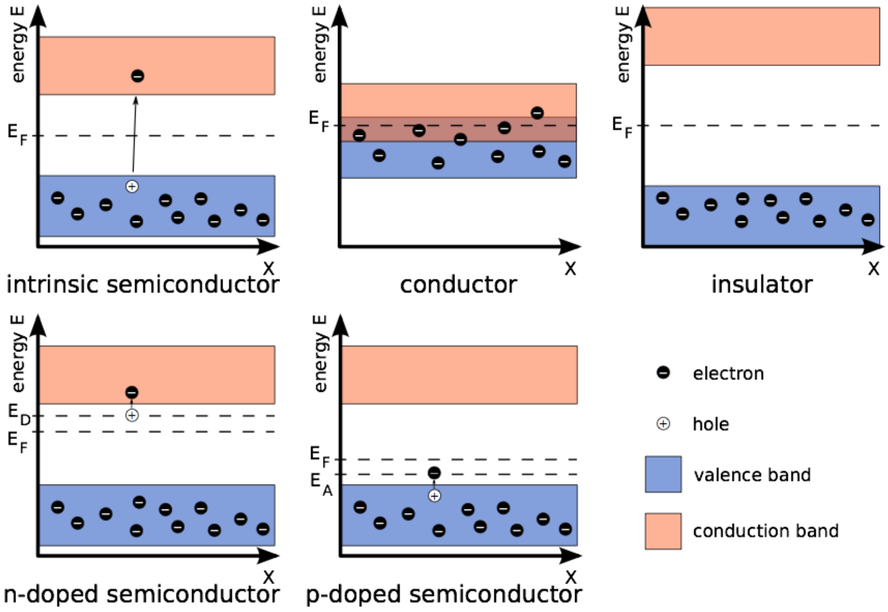
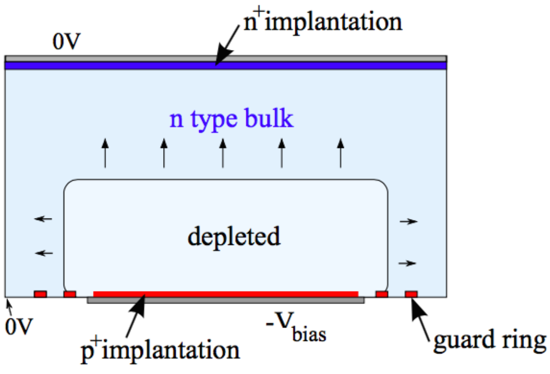


Figure 4.4: Band model structures for different materials [23]



(a) (b)

Figure 4.5: Growth of depletion zone in silicon sensors with n-type bulk (a) and p-type bulk (b) [21]

introduced in the production process can generate an interface generation current as well as ohmic currents. The bulk generation current depends highly on temperature. For comparison of current measurements taken at different temperatures one has to scale the current values with temperature as described in [22]:

$$I(T) = I(T_{\mathrm{ref}}) \left(\frac{T}{T_{\mathrm{ref}}} \right)^2 \exp \left(-\frac{E_{\mathrm{g}}}{2k_{\mathrm{B}}} \left[\frac{1}{T} - \frac{1}{T_{\mathrm{ref}}} \right] \right) \tag{4.2}$$

with $I(T_{\mathrm{ref}})$ = the current measured at a reference temperature, E_{g} = band gap energy of silicon and k_{B} = Boltzmann constant. A doubling of the leakage current is expected roughly every 7 degree.

Another important property of a silicon sensor is its spatial resolution. To achieve a good resolution, the sensors are pixelated, meaning that the n-implant is divided in separated segments, the so called pixel. The spatial resolution depends on the fineness of the segmentation, the pixel cell size, as well as on the charge collection efficiency, the amount of charge sharing by neighbouring pixel and the set threshold of the read-out chip (see section 4.3). The charge sharing is depending on intrinsic sensor properties as for example the inter pixel capacitance, the read-out settings and the operational parameters, for example bias voltage and degree of radiation damage. The width of the pixel cells is referred to as the pitch. To get a first estimation of the resolution, one can neglect the charge collection efficiency and read-out effects and take only the segmentation width into account. In addition it is assumed that a hit is only registered by one pixel in the region of half the pitch (p) around its centre (referred to as single hit cluster), while no charge sharing takes place and the particle distribution $f(x_{\mathrm{hit}})$ is homogenously one over the entire pixel [24]. In this case one can calculate the difference of the hit position x_{hit} to the measured position x_{meas} using:

$$\sigma^2_{\text{pos}} = \frac{\int_{-p/2}^{p/2}(x_{\text{hit}} - x_{\text{meas}})^2 f(x_{\text{hit}})dx_{\text{hit}}}{\int_{-p/2}^{p/2} f(x_{\text{hit}})dx_{\text{hit}}} \tag{4.3}$$

$$= \frac{\int_{-p/2}^{p/2} x^2_{\text{hit}} dx_{\text{hit}}}{\int_{-p/2}^{p/2} 1 dx_{\text{hit}}} = \frac{p^2}{12}$$

$$\Rightarrow$$

$$\sigma_{\text{pos}} = \frac{p}{\sqrt{12}} \tag{4.4}$$

4.2 Radiation damage in silicon sensors

To describe radiation damage in silicon sensors one has to differentiate between two main categories of defects: crystal defects by displacement of lattice atoms and surface defects caused by ionisation. For the first category the incoming particle needs to transfer a high amount of its energy to a lattice atom, to kick it out of its position in the lattice and leave a vacancy in this spot. This atom is then referred to as PKA[2]. In silicon the energy needed to remove an atom needs to be on average bigger than $E_{\text{d}} = 25\,\text{eV}$ while already $E_{\text{R}} \approx 15\,\text{eV}$ can be sufficient for single displacements [25]. If the PKA has enough energy, it will continue to travel through the silicon, creating more displacements in form of vacancies or interstitials while loosing its kinetic energy through ionisation and energy transfer to the material. A schematic of different crystal defects is shown in Figure 4.6. Primary defects as vacancies and interstitials can recombine if their distance is sufficiently small. When silicon atoms loose the last 5 - 10 keV of kinetic energy, their effective cross-section for elastic scatterings increases by several orders of magnitude, making it more likely that it will cause cluster- instead of point defects [26]. Charged particles loose their energy in silicon mainly through ionisation. Since this is a reversible process, it does not create lasting defects in the silicon bulk. Part of the energy of charged particles is lost via NIEL[3] processes, mainly due to Rutherford scattering which can lead to non-reversible defects. To make a comparison between radiation damage caused by different kinds of radiation possible, a normalisation needs to be applied. A hardness factor κ is introduced which is normalised to 1 MeV neutrons:

$$\kappa = \frac{\int_{E_{\text{min}}}^{E_{\text{max}}} \phi(E)D(E)dE}{D_n(1MeV)\int_{E_{\text{min}}}^{E_{\text{max}}} \phi(E)dE} \tag{4.5}$$

with $D_n(1\text{MeV}) = 2.04\text{keV}\frac{\text{cm}^2}{\text{g}}$ and the damage function $D(E)$ [27]. With this formula the hardness factor can be calculated for different types of particles at their average or most probable energies. A table with typical values can be found in Ref. [25].

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[2] **P**rimary **K**nock-on **A**tom

[3] **N**on **I**onising **E**nergy **L**oss

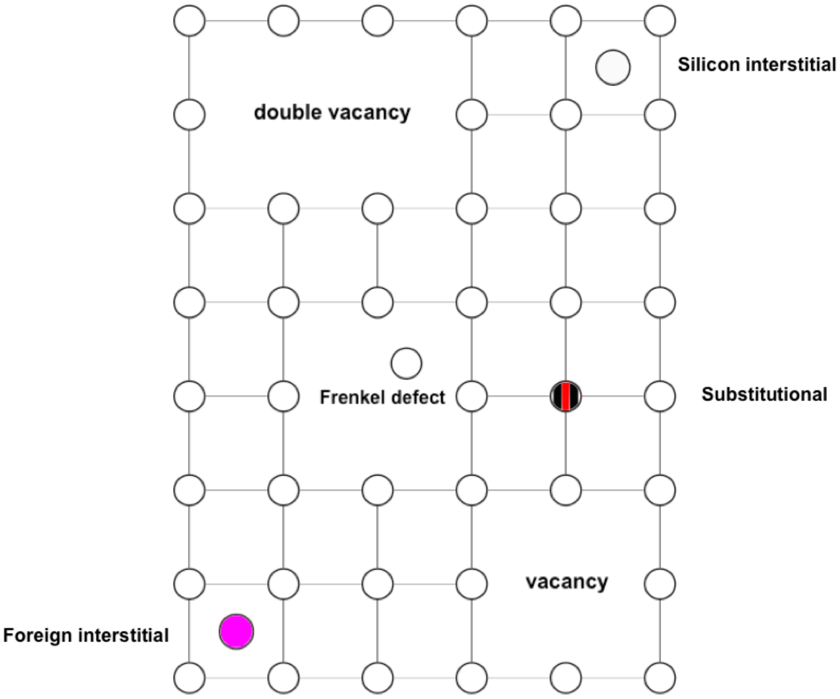

Figure 4.6: 2D schematic of different crystal defects in silicon.

The equivalent fluence ϕ_{eq} is scaled to the damage caused by a fluence of 1 MeV neutrons and its unit is given as neutron-equivalent per cm^2: $[\phi_{\mathrm{eq}}] = \frac{n_{\mathrm{eq}}}{\mathrm{cm}^2}$. It is the result of multiplying the actual fluence received during irradiation ϕ_{irr} with the hardness factor κ:

$$\phi_{\mathrm{eq}} = \kappa \cdot \phi_{\mathrm{irr}} \tag{4.6}$$

Radiation damage effects the sensor properties in several ways. One effect that directly influences the particle tracking is the so called trapping, where a charge carrier is trapped in the sensor but can also get released again after some time, causing delayed signals. Another effect is the change of the doping concentration by compensation of donors/acceptors. Donors can be removed due to defects in the lattice and additional acceptors can be introduced by displacement defects. Therefore, with increasing fluence the donor concentration N_{D} is decreasing while the acceptor concentration N_{A} increases. After a certain fluence which depends on the initial doping concentration this results in a so called type inversion where the former n-type bulk is getting p-type-like. At this point the effective doping concentration $N_{\mathrm{eff}} = N_{\mathrm{D}} - N_{\mathrm{A}}$ reaches a minimum. To describe the effect of this on the depletion voltage one has to include the effective doping concentration in the calculation [21]:

$$V_{\mathrm{depl}} = \frac{e_0 |N_{\mathrm{eff}}|}{\epsilon_{\mathrm{Si}} \epsilon_0} \frac{d^2}{2} \tag{4.7}$$

As one can see from this relation, the depletion voltage increases with increasing fluence after the sensor underwent type inversion. To counteract the radiation-induced lattice defects standard FZ[4] silicon can be enriched with oxygen during the production process. A detailed study about the effects is presented in Ref. [28]. The silicon produced this way is called DOFZ[5] material and its doping concentration increases less with fluence in addition to improved annealing properties. Annealing describes the effect that the doping concentration changes not only with fluence but, depending on temperature, also changes with time.
Following the *Hamburg model* [28, 29, 30] it can be separated into three different parts:

$$\Delta N_{\mathrm{eff}}(\phi_{\mathrm{eq}}, t(T_{\mathrm{a}})) = N_{\mathrm{a}}(\phi_{eq}, t(T_{\mathrm{a}})) + N_{\mathrm{c}}(\phi_{\mathrm{eq}}) + N_{\mathrm{y}}(\phi_{\mathrm{eq}}, t(T_{\mathrm{a}})) \tag{4.8}$$

with N_{a} = *short term annealing* or *beneficial annealing.* This type of annealing causes an increased N_{eff} and decreases with time. N_{c} is a damage constant only dependent on the fluence. N_{y} is referred to as *anti-annealing* or *reverse-annealing.* It causes a decrease of N_{eff} and counteracts the beneficial annealing, surpassing it on a long time scale. The temperature dependence of the annealing is partially caused by the fact that defects have a higher mobility at higher temperatures, making recombinations more likely.
Radiation damage also increases the leakage current which leads to increased noise and power consumption. To cope with this effect, the detector is cooled down which decreases the current and thereby noise and power consumption. One can parametrise the leakage current as a function of fluence ϕ_{eq} and depleted volume V:

$$I = \alpha \cdot \phi_{\mathrm{eq}} \cdot V \tag{4.9}$$

with α = proportionality factor (current related damage rate). This proportionality factor depends on time and can be determined for long term annealing and annealing at high temperatures using [30]:

$$\alpha(t) = \alpha_I \exp\left(-\frac{t}{\tau_I}\right) + \alpha_0 - \beta \cdot ln\left(\frac{t}{t_0}\right) \tag{4.10}$$

with t_0 set to 1min. α_I is temperature independent and describes the rapidly annealing part. It was found to be:

$$\alpha_I = (1.23 \pm 0.06) \cdot 10^{-17} \frac{\mathrm{A}}{\mathrm{cm}} \tag{4.11}$$

The temperature dependence $\frac{1}{\tau_I}$ is described by

$$\frac{1}{\tau_I} = k_{0I} \cdot \exp\left(-\frac{E_I}{k_{\mathrm{B}} T_{\mathrm{a}}}\right) \tag{4.12}$$

---

[4] **F**loat **Z**one

[5] **D**iffusion **O**xygenated **F**loat **Z**one

with k_B = Boltzmann constant, $k_{0I} = 1.2^{+5.3}_{-1.0} \cdot 10^{13} s^{-1}$, $E_I = (1.11 \pm 0.05)\text{eV}$.

The parameters α_0 and β are given by:

$$\alpha_0 = -(8.9 \pm 1.3) \cdot 10^{-17} \frac{\text{A}}{\text{cm}} + (4.6 \pm 0.4) \cdot 10^{-14} \frac{\text{AK}}{\text{cm}} \cdot \frac{1}{T_a} \tag{4.13}$$

$$\beta = (3.07 \pm 0.18) \cdot 10^{-18} \frac{\text{A}}{\text{cm}} \tag{4.14}$$

4.3 Working principle of the read-out chip

As described before, the signal generated in the sensor is transferred via bump bonds from a pixel of the sensor to a pixel of the read-out chip. The specifications of the chip used for the construction of the IBL modules will be described in chapter 2.1, while this section will give a general overview of the working principle. The chip contains an analogue and a digital part. In the analogue block the signal gets amplified by a charge sensitive amplifier connected to a feedback circuitry and is then compared to a threshold by a discriminator. Figure 4.7 shows a simplified schematic and the evolution of the signal shape.

The digital part contains the logic for data processing. It digitises the signal coming from the amplifier by converting it to an amplitude information called ToT[6] and transfers this information together with the pixel address of a hit and its time stamp. The ToT is the result of the comparison of the measured signal to the set threshold and is in first order proportional to the charge before amplification. The data is stored temporarily in buffers at the chip periphery and gets transmitted in case a hit correlates with a trigger signal of the experiment and gets deleted in case no trigger arrives after a trigger system dependent latency.

The threshold as well as the ToT can be set to different target values by tuning the chip which ensures a uniform response of all pixels. The ToT can be adjusted by tuning the feedback current of the preamplifier and is measured in units of bunch crossing. The threshold is used to distinguish between signal and noise and is normally set to a value of a few thousand electrons. To determine the threshold and the noise one can plot the discriminator activation curve as a function of the internally injected charge. In an ideal case the system would show no response up to the threshold value and then jump to a 100% response after that value, resulting in a step function. In the real case scenario the charge response is smeared by the amplifier noise and coupling capacitances introduced by the connected sensor. The latter case can be shown by measuring the noise of a single chip and comparing the result to a noise measurement after flip chipping. The interaction of those effects results in a convolution of a step function and a gaussian distribution as presented in Figure 4.8 referred to as s-curve fit. The threshold corresponds to the 50% point of this fit and the 30% and 70% points are used for defining the

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[6] **T**ime **o**ver **T**hreshold

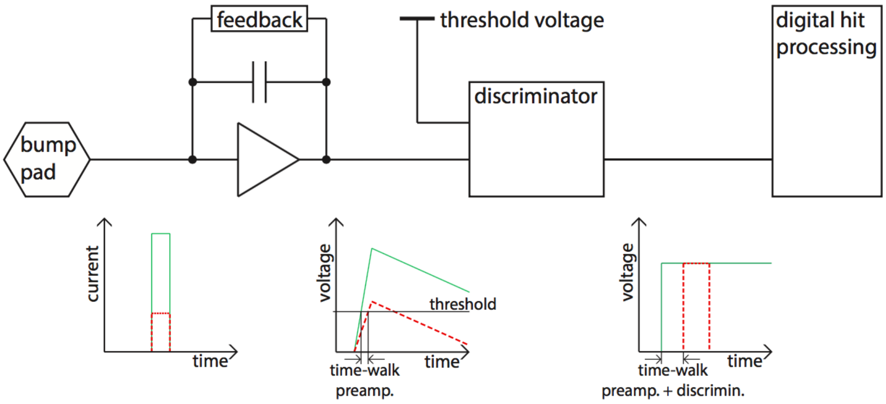


Figure 4.7: Typical analogue read-out chain as used in hybrid pixel detectors. The signal shape is shown for a large input charge (illustrated with a solid green line) and for a small input charge (illustrated with a dashed red line) after each building block [31].

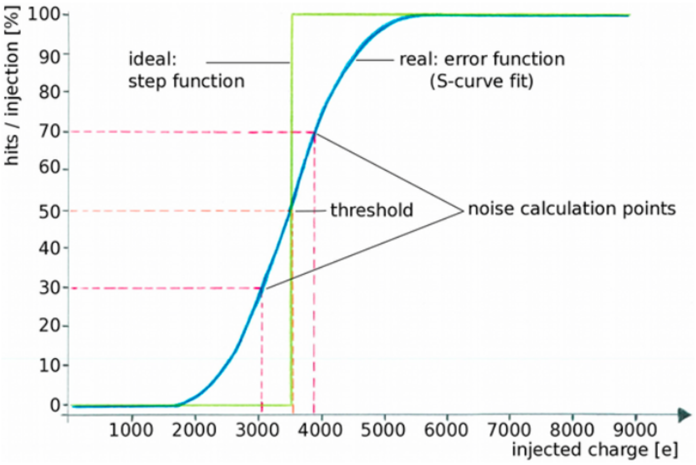


Figure 4.8: S-curve fit with marked points for threshold and noise determination [32].

noise. The fit function can be written as [33]:

$$
\begin{aligned}
P_{\text{hit}}(Q) &= \Theta(Q - Q_{\text{thr}}) \otimes e^{\left(-\frac{Q^2}{2\sigma_{\text{noise}}}\right)} \\
&= \frac{1}{2}\text{erf}\left(\frac{Q_{\text{thr}} - Q}{\sqrt{2}\sigma_{\text{noise}}}\right) \qquad (4.15)\\
&\text{with} \\
\text{erf} &= \frac{2}{\sqrt{\pi}} \cdot \int_x^\infty e^{-t^2} dt \qquad (4.16)
\end{aligned}
$$

Results of threshold and ToT measurements will be presented in chapter 6.

4.4 Radiation damage in transistors

Each of the IBL read-out chips contains millions of so called n-channel MOSFETs[7], in the following referred to as NMOS transistors. NMOS transistors have a p-type silicon bulk in which an inversion layer is created, referred to as n-channel. To create this channel, voltage needs to be applied to the gate (G), which opens the ability of the n-channel to conduct charges between source (S) and drain (D). To prevent a current flow between neighbouring components, the transistor is embedded in an STI[8] made of silicon dioxide (SiO_2). A simplified schematic of an NMOS transistor is shown in Figure 4.9.

The main effect of radiation damage in NMOS transistors investigated in this thesis is the increase of the transistor's leakage current in dependence of the accumulated TID[9]. The leakage current increase in NMOS transistors is a known phenomenon [35, 36] and several techniques have been developed to suppress this effect. The drawback of those techniques however, is their need of dedicated libraries for design as well as increased space requirements, as for example enclosed transistors require more space than non-enclosed ones. Since this would increase production cost and does not match with the design requirements for the ATLAS read-out chips, not all safety measurements could be implemented in the FE-I4[10] chip used for the IBL detector. Therefore, the behaviour of the leakage current in dependence of dose rate and temperature needs to be well understood, to prevent the detector from damage during operation.

As described in section 4.1, ionising radiation generates electron-hole pairs which can then either recombine or travel trough the material. Electrons have a high mobility in SiO_2 and will be collected by the gate electrode in the order of picoseconds. The mobility of holes on the other hand is very low in SiO_2. It is around 10^6 times smaller than the mobility of electrons [13]. In response to any present electric fields, the holes will move to the Si-SiO_2 interface by an anomalous stochastic process called trap-hopping before they are ultimately trapped as they approach the interface in long-term trapping centres. An overview of the radiation-induced

---

[7] **M**etal-**O**xide-**S**emiconductor **F**ield-**E**ffect **T**ransistor

[8] **S**hallow **T**rench **I**solation

[9] **T**otal **I**onising **D**ose

[10] **F**ront **E**nd chip, **I**BM version 4

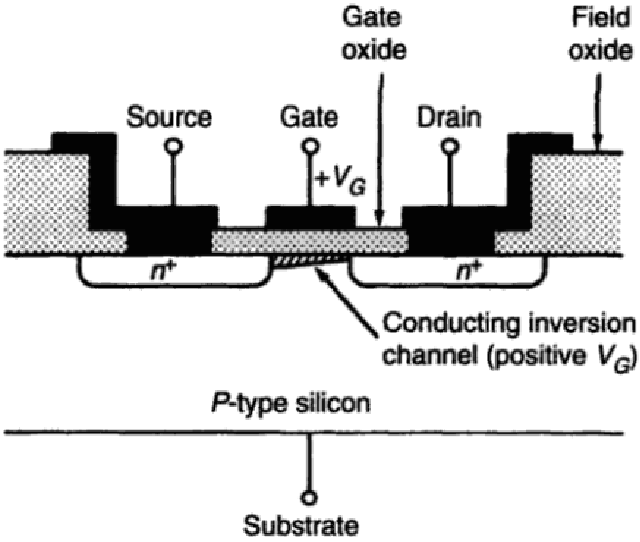


Figure 4.9: Cross-sectional view of a simplified n-channel MOSFET [34]

charge generation processes is presented in Figure 4.10. However, the holes are not permanently captured in the long-term trapping centres but can get annealed through thermal emission where holes leave the silicon oxide. This process is irreversible and results in permanent annealing. A reversible annealing can appear through electron compensation induced by tunnelling of an electron from the Si substrate. The electron has the ability to tunnel back and therefore this effect is not permanent. Both effects are dependent on temperature and the applied electric field [37]. The accumulation of trapped positive charges at the STI interface gradually builds an internal space charge field. This field creates an artificial inversion layer that results in a leakage current path flowing from source to drain as indicated in yellow in Figure 4.11.

Another effect of radiation on the Si-SiO$_2$ interface is the buildup of interface traps. These are electronic energy levels within the semiconductor band gab that are generated due to the lattice mismatch of the amorphous oxide and the crystalline silicon, disconnected chemical bonds or impurities [39]. A two-stage model to describe the creation of the interface traps was proposed by McLean [40, 41]. The first stage of this model describes the production of positive H$^+$ ions by interaction of holes that are moving towards the interface with the oxide lattice. Similar to the holes, those ions then travel to the interface via hopping transport. At arrival they react with the silicon and create dangling bonds by breaking the Si-H bonds forming H$_2$ and a free dangling bond which then acts as a trapping centre. The creation and transport of the H$^+$ ions is shown in Figure 4.10.

In NMOS transistors electrons are trapped by the interface states. Since the trapping of electrons at the interface deteriorates the performance of the transistor, hydrogen is often used during the manufacturing of the silicon to deactivate pre-existing dangling bonds. When exposed

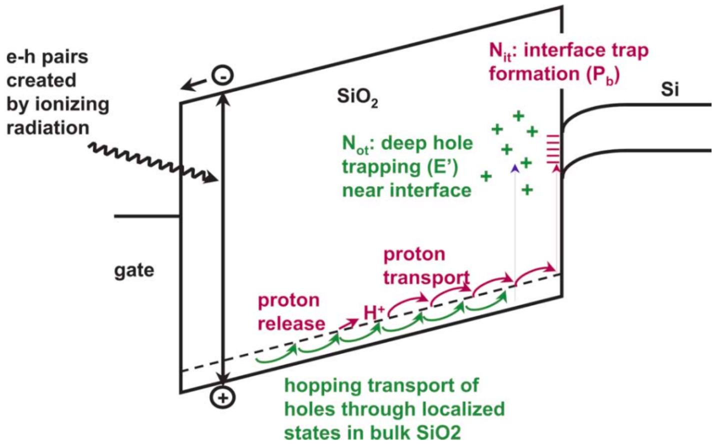
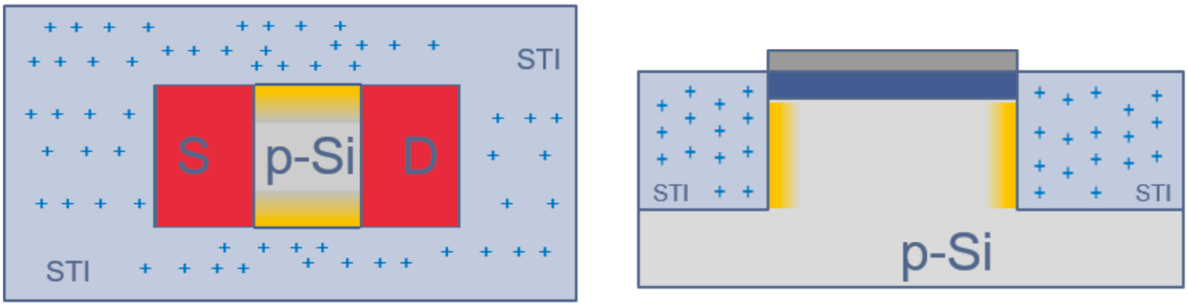


Figure 4.10: Overview of the radiation-induced charge generation processes in MOS structures [38].



(a)

(b)

Figure 4.11: Cross section of an NMOS transistor in top (a) and side view (b). The channel of the parasitic transistor along the STI is indicated in yellow [42].

to ionising radiation, those dangling bonds get reactivated or new ones are created. The trapping of electrons builds up an electrical field which counteracts the field of the oxide charges and therefore leads to a decrease of the leakage current. The development of interface traps is a slower process than the fast accumulation of positive oxide charges. Therefore, the interface traps only start compensating the electrical field induced by the oxide charges with some delay after the start of an irradiation, resulting in the so called rebound effect [35, 37] which describes the decrease of the current when the interface trapping dominates.

The following description of a model to quantify the behaviour of the leakage current in dependency of TID is based on Ref. [42] where a more detailed derivation of formulas (4.17) to (4.24) can be found and has partially also been published in Ref. [43].

The behaviour of the LV current increase can be described using the transfer characteristics of a parasitic transistor, where no current is flowing as long as the gate voltage V_{G} is smaller than the threshold voltage V_{thr}. In saturation mode, the drain current I_{D} can be described as a quadratic function with a constant factor K':

$$I_{\mathrm{D}} \approx K' \cdot (V_{\mathrm{G}} - V_{\mathrm{thr}})^2 \tag{4.17}$$

The main change of the leakage current in NMOS transistors during irradiation is driven by the number of oxide charges accumulated in the STI and by interface traps activated at the Si-SiO$_2$ interface along the STI. For p-type silicon the STI oxide charges form a conduction channel between source and drain which increases the leakage current. Contrary to that, the interface traps lead to a decrease of leakage current due to the accumulation of fixed negative charges which compensate the positive charges. The gate voltage of parasitic transistors can be described by the effective number of charges N_{eff} (see Eq. (4.23)) and the threshold voltage by the threshold number of charges N_{thr}. Based on this, the leakage current can be described for the case of $N_{\mathrm{eff}} > N_{\mathrm{thr}}$ as:

$$I_{\mathrm{leak}} = I_{\mathrm{leak}}^0 + K \cdot (N_{\mathrm{eff}} - N_{\mathrm{thr}})^2 \tag{4.18}$$

with I_{leak}^0 describing the current consumption before irradiation and a proportionality constant K.

The number of positive charges N_{ox} that get trapped in the STI during irradiation with a constant dose rate D is proportional to the time duration of the irradiation t with a proportionality constant $k_{\mathrm{ox}}D$. Hereby, k_{ox} describes the number of holes that get trapped per dose unit. Since the holes have the ability to leave to STI again after being trapped, a lifetime τ_{ox} has to be defined in addition. This results in a differential equation describing the number of trapped holes as:

$$\frac{d}{dt} N_{\mathrm{ox}}(t) = k_{\mathrm{ox}} D - \frac{1}{\tau_{\mathrm{ox}}} N_{\mathrm{ox}}(t) \tag{4.19}$$

which is solved by:

$$N_{\mathrm{ox}}(t) = k_{\mathrm{ox}} D \cdot \tau_{\mathrm{ox}} \cdot \left(1 - e^{-\frac{t}{\tau_{\mathrm{ox}}}}\right) \tag{4.20}$$

When the irradiation is stopped after a time t_1, the number of holes trapped in the STI decreases exponentially. This effect, referred to as annealing, can be described by

$$N_{\mathrm{ox}}(t) = N_{\mathrm{trap}} + (N_{\mathrm{ox}}(t_1) - N_{\mathrm{trap}}) \cdot e^{-\frac{t-t_1}{\tau_{\mathrm{ox}}}} \tag{4.21}$$

with N_{trap} describing the number of holes captured in deep traps of the oxide which will not be set free at a low temperature and remain in the oxide.

The negative charges get activated by the accumulated positive charges at the interface along the STI. The number of interface traps N_{if} is technology dependent and limited. Due to this, the number of available trapping centres decreases with time and the probability that holes activate new interface traps decreases exponentially. This can be described with:

$$N_{\mathrm{if}}(t) = k_{\mathrm{if}} D \cdot \tau_{\mathrm{if}} \left(1 - e^{-\frac{t}{\tau_{\mathrm{if}}}}\right) \tag{4.22}$$

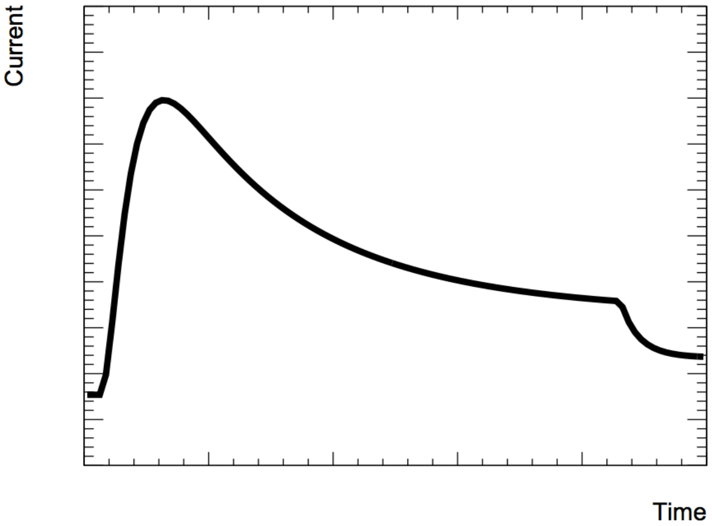


Figure 4.12: Leakage current parametrisation in arbitrary units as a function of the time following equation 4.24 [42].

with k_{if} describing the number of holes available to activate interface traps per dose unit and their lifetime τ_{if}. The interface traps will not anneal at the operation temperatures of the FE-I4 chips. The needed temperature for annealing is technology dependent and was found to be in the range of 100°C to 300°C.

Since the negative interface traps counteract the electric field induced by the positive oxide charges, the effective number of charges can be derived from the difference of equations 4.20 and 4.22:

$$N_{\text{eff}} = N_{\text{ox}} - N_{\text{if}} \tag{4.23}$$

For the resulting leakage current of the front-end chip one has to sum up the current consumption before irradiation and the current increase:

$$I_{\text{leak}} = I^0_{\text{leak}} + K \cdot \left[k_{\text{ox}} D \cdot \tau_{\text{ox}} \cdot \left(1 - e^{-\frac{t}{\tau_{\text{ox}}}}\right) - k_{\text{if}} D \cdot \tau_{if} \cdot \left(1 - e^{-\frac{t}{t_{\text{if}}}}\right) - N_{\text{thr}} \right]^2 \tag{4.24}$$

When no irradiation is ongoing, N_{ox} is replaced with equation (4.21) instead of (4.20).

The expected current trend should therefore be stable at the beginning of an irradiation, followed by a continuous increase until the number of interface traps exceeds the number of oxide charges, which will then lead to a decrease of the current until it reaches a plateau where no further change is expected. In case the irradiation is stopped before the plateau is reached, a steeper decrease of the current due to annealing is expected. The current trend vs. time as predicted by this equation is presented in Figure 4.12.

Chapter 5

The Pixel Detector

5.1 Layout

Located closest to the interaction point, the ATLAS pixel detector [44] has to cope with a specifically harsh environment. It has to withstand high radiation doses while still providing precise tracking information at a high rate. The detector was designed to be functional at least up to a fluence of 1 x 10^{15} MeV $\frac{n_{\mathrm{eq}}}{\mathrm{cm}^{-2}}$ which calculates to 50 Mrad of dose. Due to its close proximity to the collisions, it is very important for the identification of secondary vertices and b-tagging. Originally built as a three-layer detector, the pixel detector was upgraded in 2014 with a fourth layer that will be described more detailed in the next section. The pixel detector, as shown in Figure 5.1, covers a pseudorapidity of $|\eta| < 2.5$ and can provide three or more space points for track reconstruction.

The three barrel layers are located at average radii of 5 cm, 9 cm and 12 cm. They are populated with 1456 modules glued to support structures called staves. In addition, the detector is covered in forward and backward direction with three disks at radii between 9 cm and 15 cm equipped with 288 modules, resulting in a total number of 1744 modules [45]. The pixel modules are arranged in an overlapping way for hermetic coverage to avoid loosing track information. Each pixel module consists of a 250 μm thick n^+-in-n silicon sensor of 2 x 6.3 cm^2 bump bonded to 16 so called FE-I3[1] readout chips which contain the communication and control circuitry. The bulk substrate of the sensors is made of lightly n-doped silicon, with 50 x 400 $\mu\mathrm{m}^2$ pixel implantations. For those implantations, a highly n^+-doped substrate is used on the front side and highly p^+-doped implantations are placed at the back side. To avoid loosing tracking information in the gaps between the 16 readout chips, a row of long pixels with a size of 50 x 600 μm and ganged pixels that connect two sensor pixels to one read out pixel have been implemented. The module is then connected to a flex hybrid equipped with an MCC[2], passive SMD[3] components, a radiation hard 10 kΩ NTC[4] sensor and a pigtail used for routing the signals to an accessible location where a so called type 0 cable can be connected. A carbon bi-stave support structure holds 13 pixel modules in place. The staves are equipped with evaporative $\mathrm{C_3F_8}$ cooling, enabling to operate the modules at a set temperature of -20°C, resulting in a module temperature of about -13°C. Via the type 0 cable, an LVDS[5] is transferred at a rate of 40 or 80 Mbit/s to the PP0[6] [46]. A schematic of one pixel module is shown in Figure 5.2.

The PP0 is part of eight SQPs[7] that are installed on both sides of the detector and channel

---

[1] **F**ront **E**nd chip - **I**BM version 3

[2] **M**odule **C**ontroller **C**hip

[3] **S**ervice **M**ounted **D**evice

[4] **N**egative **T**emperature **C**oefficient

[5] **L**ow **V**oltage **D**ifferential **S**ignal

[6] **P**atch **P**anel 0

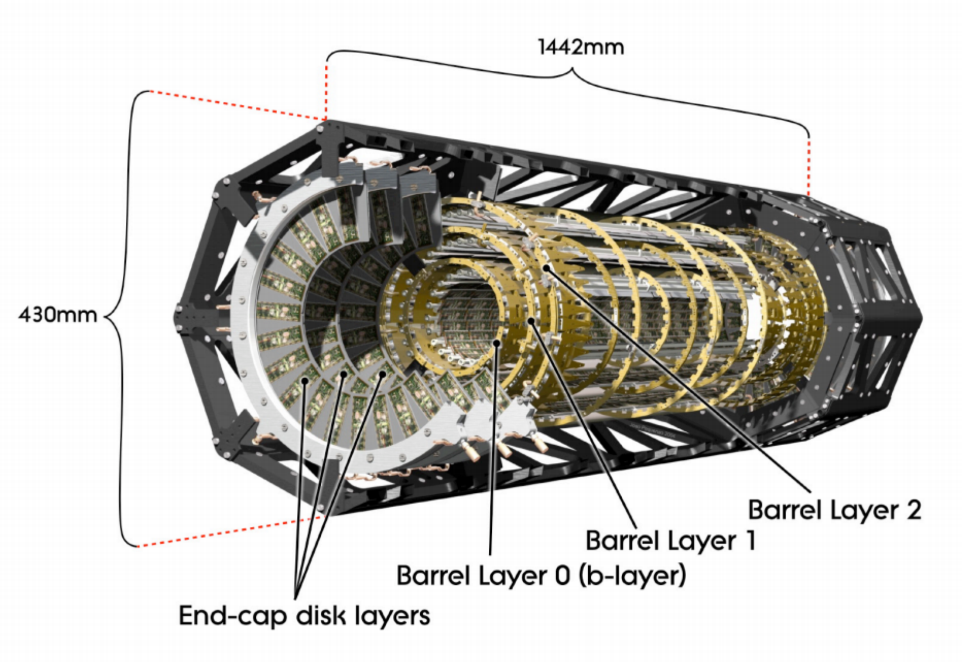


Figure 5.1: Schematic view of the active region of the pixel detector consisting of barrel and end-cap layers [45]

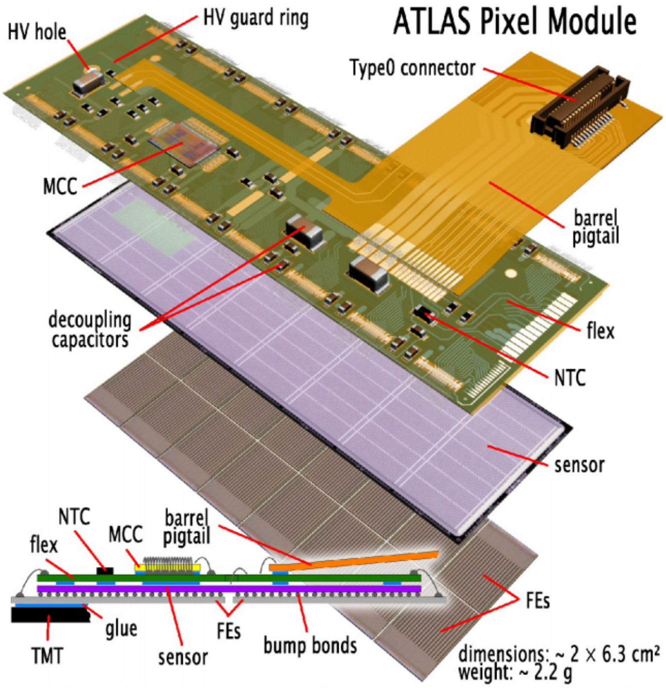


Figure 5.2: Cross-sectional view of the ATLAS Pixel Module [47]

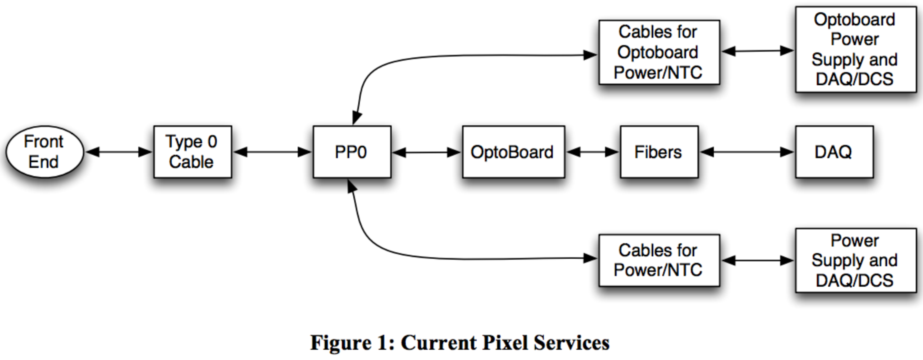


Figure 5.3: Pixel Services before upgrade to nSQP [46]

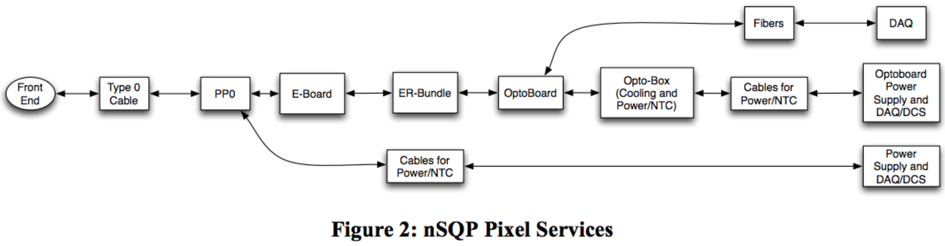


Figure 5.4: nSQP Pixel Services [46]

electrical power as well as cooling and optical power out of the detector. In their first version they also included electro-optical inverters, so called optoboards to translate the electrical signal coming from the detector into an optical signal that can be transferred via 80 m long cables to readout systems in the service cavern and vice versa. An overview of the chain from front-end chip to the readout system is shown in Figure 5.3. The translation from electrical to optical signals is realised with a system of laser arrays and a PIN diode is used for the conversion from optical to electrical signals. Due to their location within the SQPs, the lasers are not accessible without opening the detector. Since opening the detector is a risky and slow process, a new system called nSQP[8] was designed, allowing easier access and repair of the optoboards [46]. The updated chain layout and a picture of one of the nSQP panels are shown in Figures 5.4 and 5.5.

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[7] **S**ervice **Q**uarter **P**anels

[8] **n**ew **S**ervice **Q**uarter **P**anels

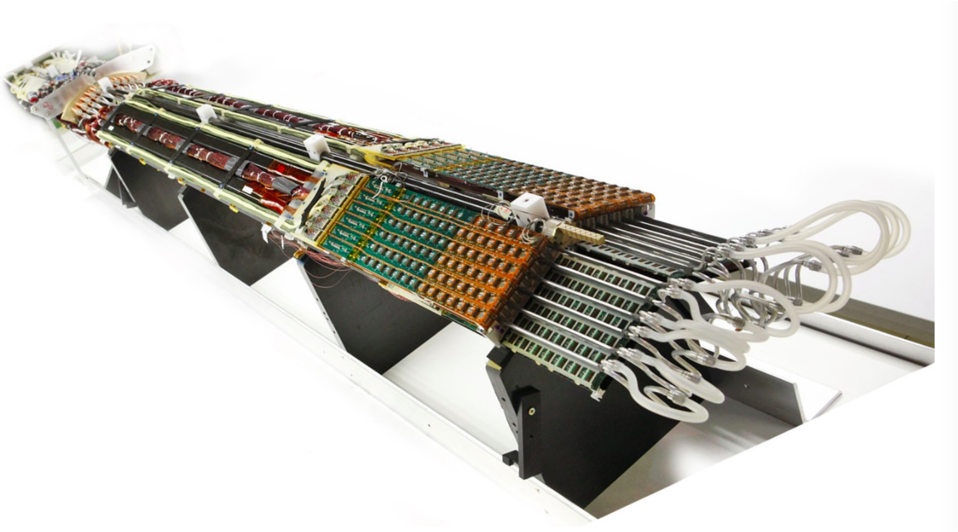

Figure 5.5: Photograph of one out of eight ATLAS Pixel nSQPs located in a test stand in the CERN Bat. 180 clean room [32].

5.2 The Insertable B-Layer

During the LS1 in 2013 - 2014, the pixel detector was upgraded with a forth layer, the so called IBL[9] [45]. The aim of this upgrade was to improve the tracking performance, in especially the impact parameter resolution, while dealing with increased occupancy, pile-up and bandwidth requirements as well as to serve as a partial backup solution in case the modules of the former innermost layer, the B-layer, begin to show inefficiencies due to radiation damage. A decrease of efficiency is expected when the instantaneous luminosity surpasses 2 x $10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$. To gather free space for the IBL installation, the former beam pipe was removed and replaced by a new one with a smaller radius. Before the replacement of the beam pipe, the radial free space was 8.5 mm. Reducing the beam pipe diameter to 47 mm resulted in a free space of 12.5 mm. A comparison of the layout with and without IBL is shown in Figure 5.6.

Going radially from the inside to the outside the layout of IBL comprises of three parts. The IPT[10] is attached to the beam pipe, followed by the staves and services which are enclosed by the IST[11]. The IST was fixed inside the pixel detector structure when it was refurbished during the shutdown and therefore was brought to the surface.

The IBL consists of a single cylindrical layer with sensors at an average radius of 33 mm. It covers a pseudorapidity of $|\eta| < 3.0$ and is made up of 14 staves which serve as support structures for modules and cooling. The staves are made of a low density carbon-foam which provide stability at a low material budget. Each stave is tilted by 14 degrees with respect to the normal incident angle so their active area overlaps to provide full azimuthal coverage. The

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[9] **I**nsertable **B**-**L**ayer

[10] **I**nner **P**ositioning **T**ube

[11] **I**nner **S**upport **T**ube

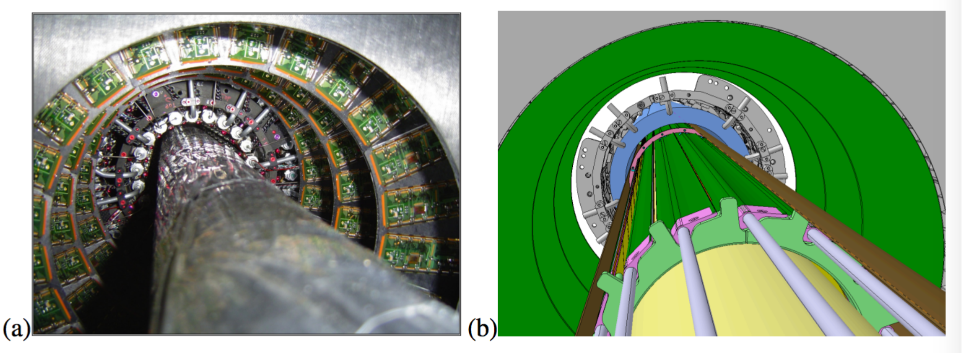

Figure 5.6: Photo of the Pixel detector with the inserted beam pipe (a) and rendering of the planned insertion of the IBL with a new smaller beam pipe (b) [45].

schematics of the positioning of the detector around the beam pipe are displayed in Figure 5.7 and Figure 5.8 shows a longitudinal view of the IBL.

Two different types of modules are installed on the staves, 12 double chip assemblies with planar sensors (see section 5.2.1) and 8 single chip assemblies with 3D sensors (see section 5.2.2) adding up to 20 modules per stave. Both sensor technologies had to fulfil the same requirements. Due to the limited space, the modules are placed with no overlap in z but instead are placed next to each other with the smallest possible gap of $200\,\mu$m and therefore the inactive edge of the sensors needed to be minimised. It was stated that the inactive region cannot be larger than $450\,\mu$m.

The sensors need to be operational at temperatures down to $-25°$C and must not dissipate not more than $200\,\frac{\mathrm{mW}}{\mathrm{cm}^2}$ at the foreseen operation temperature of $-15°$C to not interfere with the cooling requirements. As described before, the depletion voltage increases with fluence. For the IBL modules it was requested that the required voltage would not exceed 1000 V up to a fluence of $5 \cdot 10^{15}\,\frac{\mathrm{n_{eq}}}{\mathrm{cm}^2}$ or a total ionising dose of 250 Mrad and also the charge collection should stay sufficient up to that fluence. For readout, each stave is divided into two half staves with 4 module groups consisting of either two double chips or four single chips. The two sides are referred to as A and C side in conformity with the ATLAS naming scheme. Both sensor technologies are bump bonded to the so called FE-I4B chip, described in section 5.2.3. The bonding process for the IBL modules was developed by IZM[12] and uses SnAg solder bumps.

The staves are connected at each of their ends to 3 m long extensions which are connected to the inner detector end-plate which holds the connections to the external services. Two systems are used for operation and read out of the detector. The power distribution to the modules as well as the electrical and environmental monitoring is controlled by the DCS[13], while the data transfer is controlled by the DAQ[14] system. Each stave is electrically connected via the stave flex to a so called end of stave card at the PP0. The connection from the PP0 to the opto-boards

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[12] Fraunhofer-Institut für Zuverlässigkeit und Mikrointegration (Berlin, Germany)

[13] **D**etector **C**ontrol **S**ystem

[14] **D**ata **Acq**uisition

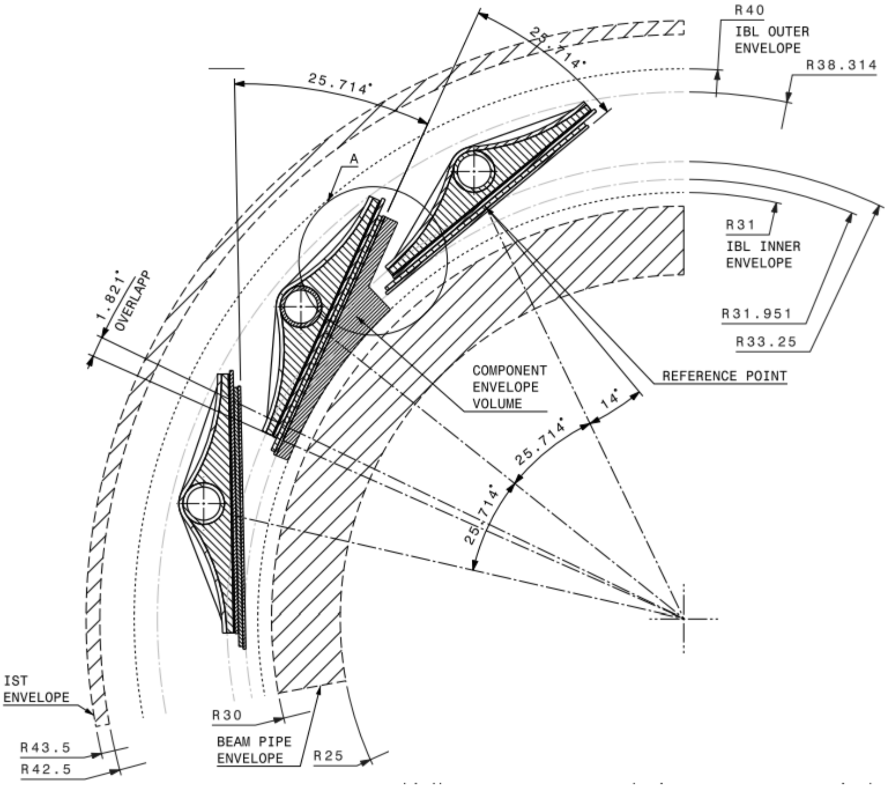

Figure 5.7: IBL layout: rϕ view [45]

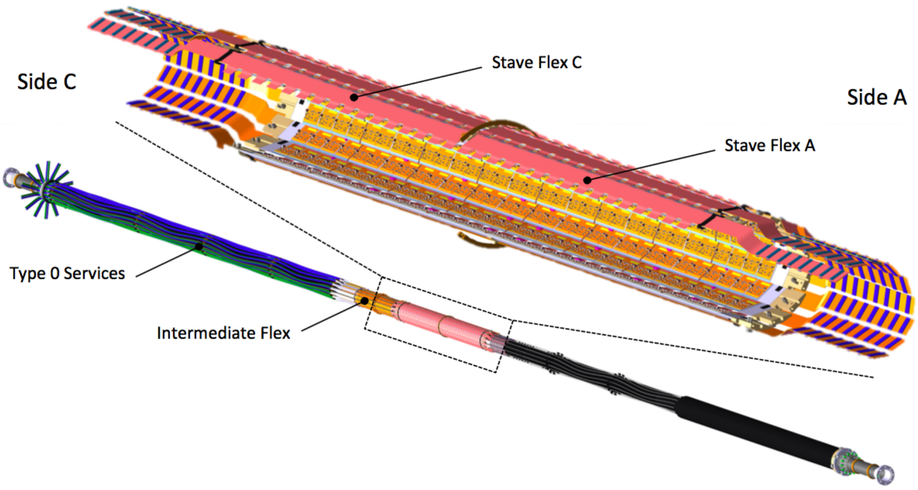

Figure 5.8: IBL layout: longitudinal view [48]

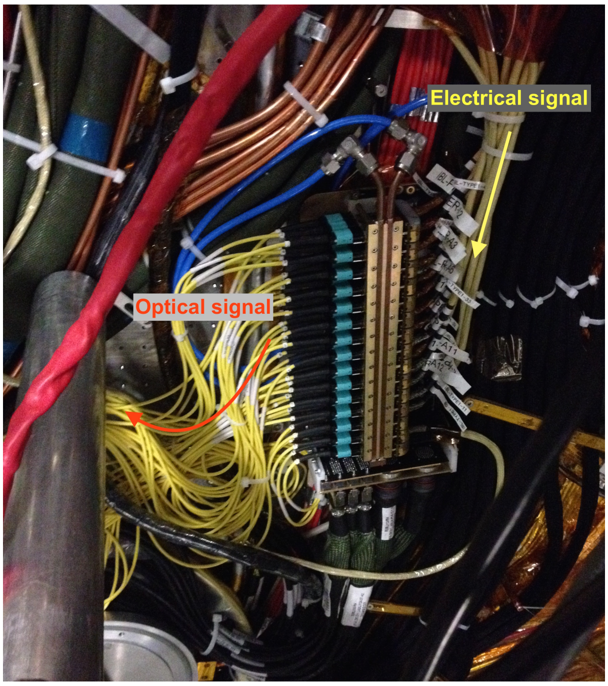

Figure 5.9: Picture of the IBL opto-board after installation in the pit

is made by a bundle of thin electrical wires, so called type 1 cables. Comparable to the nSQP approach for the pixel services, the IBL opto-boards were designed in a way that makes easier access possible as it can be seen in Figure 5.9.

The IBL was installed in May 2013. Pictures of the transport and installation are shown in Figure 5.10.

5.2.1 Planar sensors

The planar sensors used for the IBL module construction are made in n^+-in-n technology. They consist of a 200 μm thick slightly n-doped bulk with highly n^+-doped pixel implants on the front side and highly p^+-doped implantation on the back side of the sensor. This technology was already used for the sensors of the pixel detector and proved to be reliable during run 1. A cross section of an ATLAS pixel sensor is shown as an example for this technology in Figure 5.11.

Since the IBL is located closer to the collision point and hence a finer segmentation is required to guarantee a good track separation ability, the size of the n^+ pixel implantations for the IBL sensors was decreased compared to the former pixel sensors. In addition, this results in a lower hit occupancy per pixel and a better z-resolution. While the pixel sensors have pixel implantations of the size of 400 μm x 50 μm, this was reduced to 250 μm x 50 μm for the IBL sensors.

To decrease the inactive space on the sensor edges and to allow closer placement of sensors next to each other, a new design approach was proposed, referred to as slim-edge design. This design implements two main changes, connected to the so called guard rings. Guard rings are

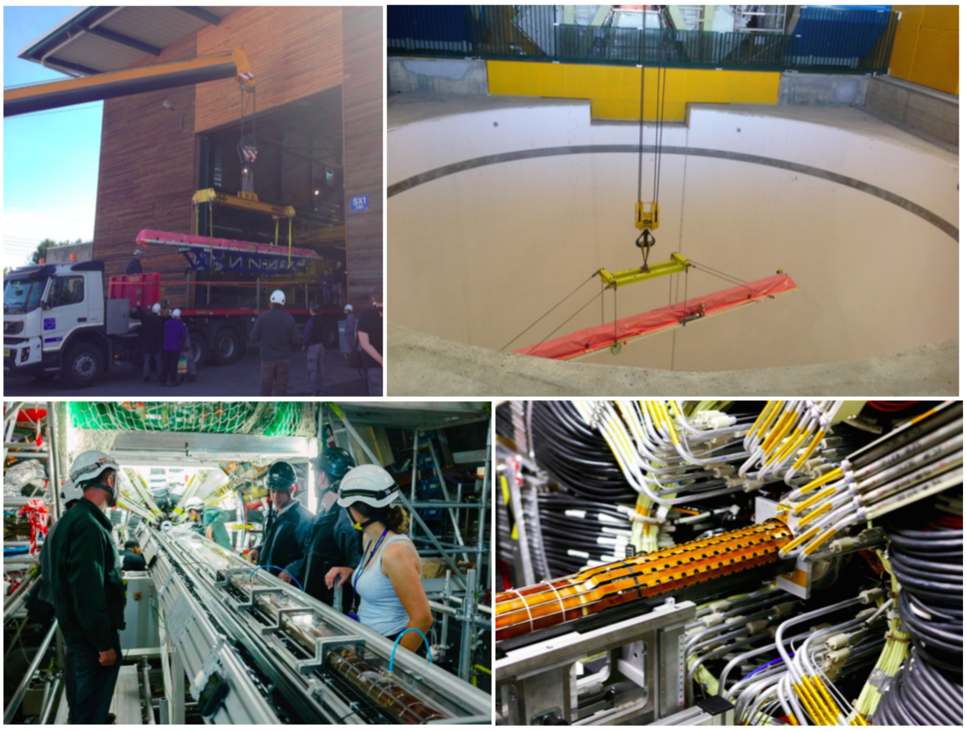

Figure 5.10: Pictures of the IBL transport to the experimental cavern and installation

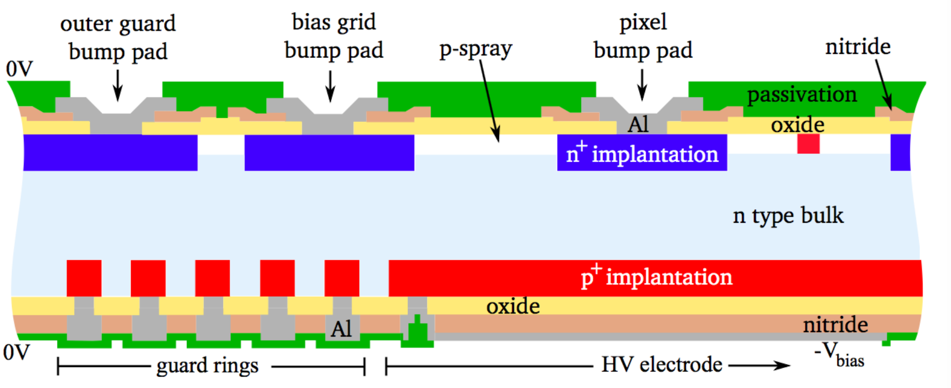

Figure 5.11: Cross section of a planar ATLAS pixel sensor [21].

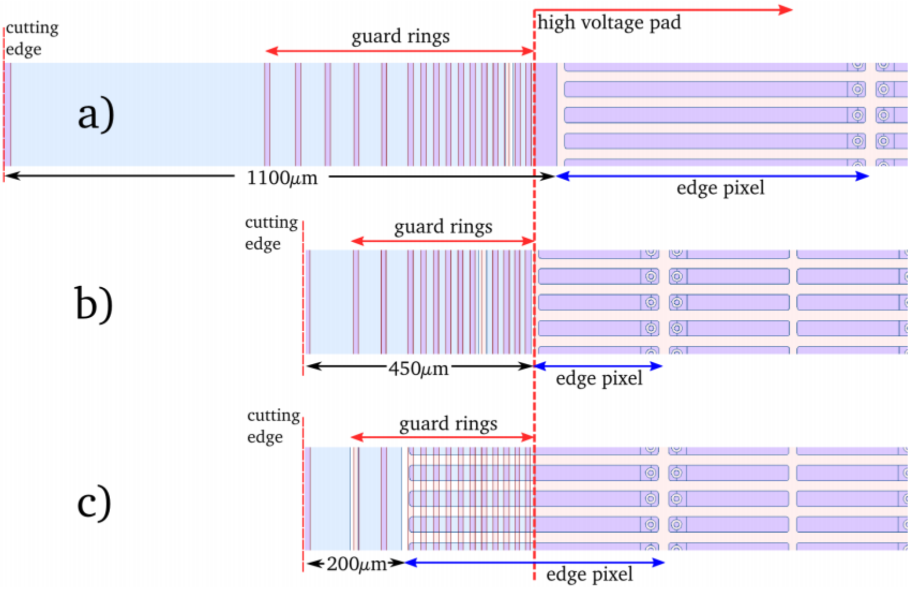

Figure 5.12: Top view of the sensor edge region of the ATLAS pixel sensor design (a) as well as the conservative (b) and the slim edge (c) IBL design. The n^+ implantation is seen in blue, the p^+ implantation in red. The inactive edge could be reduced from 1100μm for the ATLAS pixel design to 200μm for the slim edge IBL design [49].

ring shaped implants that ensure a controlled potential drop from the HV structure to the cutting edge, which is connected to ground. The new design reduces the number of those rings from 16 to 13 and in addition reduces the inactive edge area by shifting the 500 μm long edge pixel underneath the guard rings. A comparison of the old and new design is shown in Figure 5.12.

It was decided to use 200 μm thick material, since it proved to offer the best yield for the stated requirements. Even though in general production of wafers down to 175 μm showed a good yield, one needed to take into account that for hybridisation the sensors need to be equipped with UBM. Adding those to wafers thinner than 200 μm requires a handling wafer and thus would increase production cost [21]. The matrix of the sensor is organised in 80 columns and 336 rows to match the layout of the readout chip. A p^+ implant is located at the back side of the sensor, serving as a HV pad. A bias grid network, where each pixel is connected to the bias grid via a bias dot, is used to supply the HV via the so called punch-through effect. A picture showing the location of the bias dot and the bump bonding dot is presented in Figure 5.13. In addition to the HV supply, this network allows for easier characterisation of the sensor and prevents floating potentials in case of open bump connections. A 90 μm wide bias grid ring surrounds each pixel. It was already found for the old pixel design, that the charge collection efficiency suffers in the region of the bias-dot with increasing irradiation, but the before mentioned advantages lead to the decision to keep this structure. Each planar IBL module consists of a 18.8 x 41.3 mm^2 sized double chip sensor, read out by two front-end chips [45]. To bridge the gap between the two

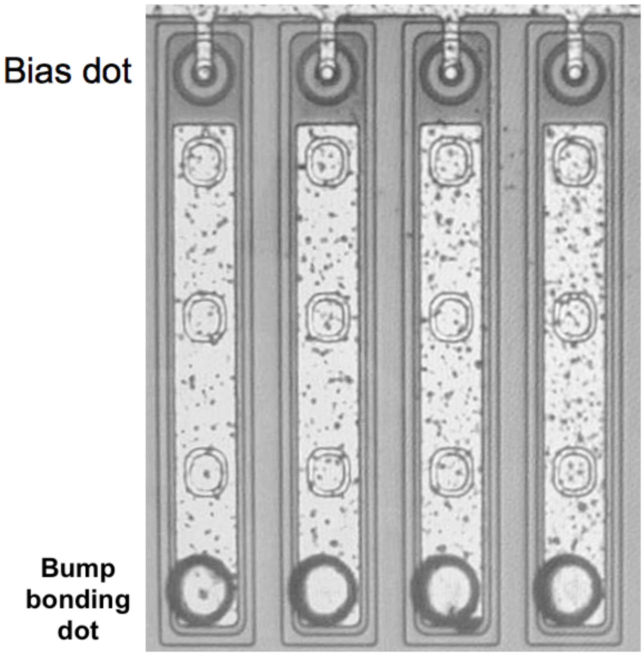

Figure 5.13: Location of the bias dots and bump bonding dots for a planar IBL sensor.

readout chips, 450 μm long pixel are used.

5.2.2 3D sensors

25% of the IBL modules use 3D instead of planar sensors and single chip instead of double chip assemblies. Those modules populate both ends of a stave whereas the planar modules are mounted in the middle region. While planar sensors use implants introduced at the wafer surface, 3D sensors make use of electrodes that are fabricated inside the bulk of the sensor [50]. Different industrial technologies can be used for production of 3D sensors like MEMS[15] and VLSI[16] [51, 52]. The electrodes in the silicon bulk are produced using the DRIE[17] technology, where holes get etched into the substrate which are afterwards filled with polysilicon using a high temperature thermal diffusion process. The distance between the electrodes is small compared to the planar technology, resulting in a shorter drifting distance which decreases the required bias voltage and increases the radiation hardness.

The IBL sensors are produced on 4" p-type FZ wafers with a thickness of 230 μm and were processed by two vendors, CNM[18] and FBK[19]. Both vendors produced sensors in a double sided 3D design with a slim fence. The two types of sensors differ mainly in depth of the implants. The CNM sensors use implants which do not penetrate the whole substrate but end shortly before

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[15] **M**icro-**E**lectro-**M**echanical **S**ystems

[16] **V**ery-**l**arge-**s**cale **i**ntegration

[17] **D**eep **R**eactive **I**on **E**tching

[18] **C**entro **N**acional de **M**icroelectronica (Barcelona, Spain).

[19] **F**ondazione **B**runo **K**essler (Trento, Italy)

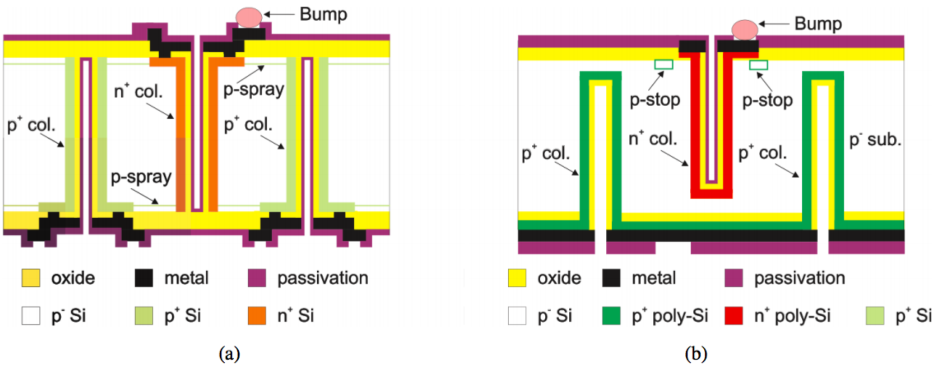

Figure 5.14: Comparison of 3D sensors produced by FBK (a) and CNM (b)

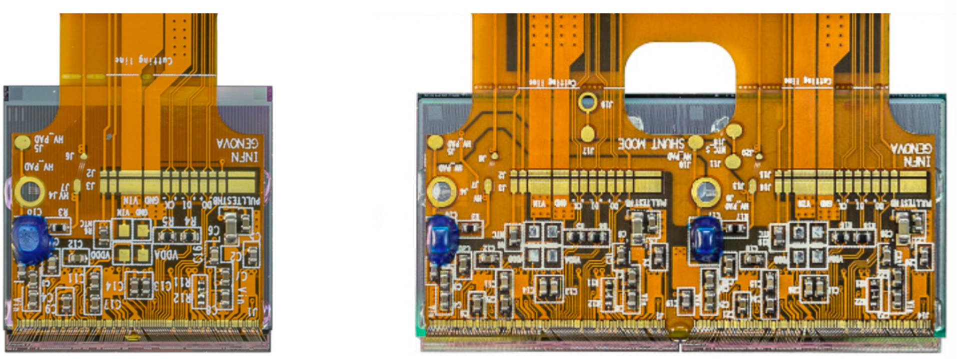

Figure 5.15: Pictures of an assembled single 3D module (left) and planar double chip module (right) [31].

they reach the surface while the FBK sensors use columns that penetrate the complete bulk material. The isolation of the n^+ columns to the surface is also different for both technologies. The CNM sensors use p-stop implants on the front side and FBK sensors use p-spray implants on the front and back side. Lastly, the implementation of the slim fence differs as well. The slim fence is used to gradually reduce the potential towards the cutting edge (comparable to the guard rings for planar sensors). For CNM sensors, this reduction of the potential is realised using a slim edge guard ring structure that connects biased fences with a grounded n^+ ring while the FBK sensors hold several rows of ohmic columns which shield the cutting edge from the active area. A comparison between both technologies is shown in Figure 5.14.

Modules with both technologies, planar and 3D, are after hybridisation glued to a 130 μm thick double-sided flexible PCB[20], the so called module-flex. Mounted on the module-flex are passive components used for decoupling, filtering and terminating the signal traces. Pictures of the assembled single chip and double chip modules are shown in Figure 5.15.

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[20] **P**rinted **C**ircuit **B**oard

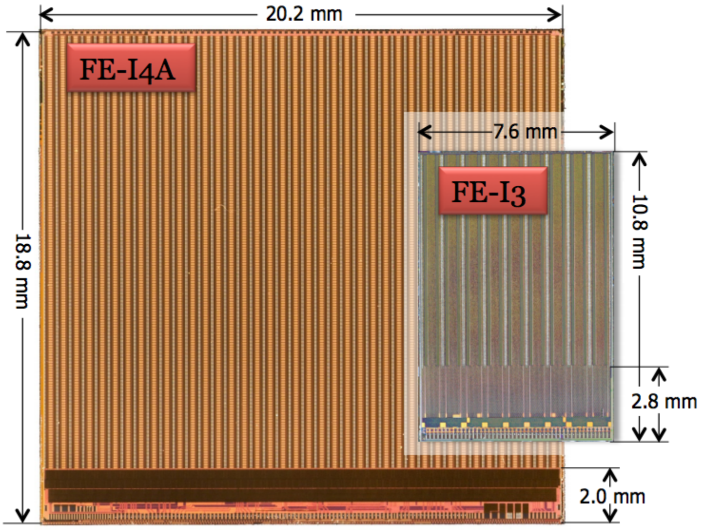

Figure 5.16: Picture of an IBL FE-I4 chip and the to-scale pixel FE-I3 chip for comparison [51]

5.2.3 FE-I4 readout chip

The FE-I4 readout chip is the successor of the FE-I3 chip that has been used for the pixel detector modules. The matrix of the chip contains 80 columns and 336 rows, resulting in a total number of 26 880 pixels. Each pixel is 250 μm long and 50 μm wide. A size comparison of the FE-I3 chip and the FE-I4 chip is shown in Figure 5.16. For the design of the FE-I4 one had to take into account the increased amount of radiation the chip would have to withstand, the increased number of pile-up events requiring precise and fast readout and the limitations due to the material budget. The latter point lead to especially strict requirements as to power dissipation and current flow since cooling capabilities are limited inside the IBL volume as well as the material budget for cables.

The chip is designed in 130 nm CMOS IBM technology and holds around 80 million linear transistors. Enclosed transistors would require more space and were therefore not used for most parts of the chip. The FE-I4 chip records the time of a hit and the ToT information with a 4-bit resolution in counts of an externally supplied clock running at a nominal frequency of 40 MHz. The information provided by the discriminator can be stored in the chip for up to 255 cycles of the external clock. If a trigger arrives during this interval, the data gets processed further and is deleted otherwise. The chip uses a serial data output with an 8b/10b encoded primary output mode at a rate of 160 Mb/s. Hereby, the first 8 b contain the actual data while the other 2 b are used to perform a parity check to detect transmission errors. To ensure safe operation of the chip, a system to reduce and control transient currents which are introduced by load fluctuations, needs to be implemented. Those fluctuations can appear during configuration of the chip as well as by accidental loss of the configuration. To keep the transient currents

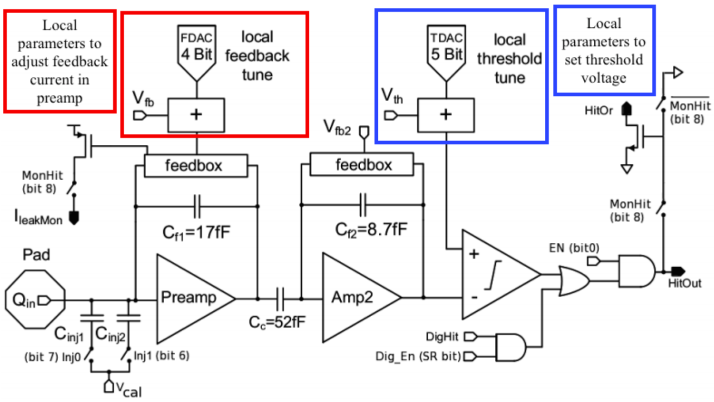

Figure 5.17: Schematic view of the analog part of the FE-I4 readout chip. Modified version of [51].

under control the chip uses LDO[21] regulators in partial shunt mode. In this mode an additional current is shunted to ground by the regulators in case the current consumption of the chip drops below an adjustable threshold. Each chip contains two on-chip LDO regulators which convert a common input voltage into two separate voltages for analog and digital supply [53]. The LDOs are linear regulators which keep the output voltage at a constant value independent of the input voltage and the load current and use on-chip generated reference voltages for operation.

As explained in section 4.3, each pixel includes a charge sensitiv amplifier with adjustable shaping capabilities, followed by a discriminator which compares the signal to a manually set threshold. The amplification is done in two stages, optimised for low noise and power operation with fast rise time. The first amplifier, referred to as preamplifier, as well as the second stage amplifier are AC coupled with an adjustable feedback current. DACs[22] are used for adjusting the response of each pixel. The preamplifier feedback can be adjusted by using a 4-bit DAC to fine tune the ToT response while the threshold value used for the discriminator can be adjusted by using a 5-bit DAC. A detailed schematic of the analog part including the specific DACs for tuning of the chip is shown in Figure 5.17. To allow testing of the chip, additional injection circuitries are implemented, labeled V_{cal} and $C_{inj1/2}$ in Figure 5.17.

Since the FE-I4 was designed to cope with increased hit rates, the digital activity was reduced compared to its predecessor chip. The FE-I3 uses a column drain architecture which results in a pixel being busy in case of a hit until the double column bus is available to transfer the information to the end of column logic. The FE-4 chip on the other hand divides the column pairs further in blocks of two pixels by two pixels, where four independently working analog pixels share one memory and digital logic block. A schematic of this is shown in Figure 5.18.

The outputs of each of the four discriminators are processed in four separate hit processing units which compute the ToT and store the time stamp of a hit. Up to five events can be stored

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[21] **L**ow **D**rop-**O**ut
[22] **D**igital to **A**nalog **C**onverters

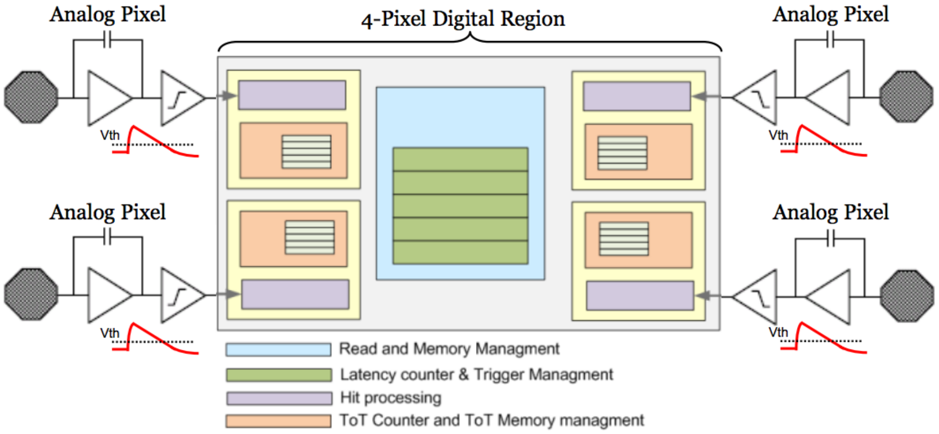

Figure 5.18: Schematic view of the 4-pixel digital region of the FE-I4 chip [51].

together with their timing information. A counter keeps track of the time that passed since the hit was registered. The resolution is given by the external clock period which is nominally 25 ns and is also used as unit for the ToT value, in the following referred to as BC[23], in dedicated scans used for characterising the chip as well as validating the tuning parameters for operation. A specific trigger latency can be programmed and is compared to the time counters of the five stored events in case an external trigger arrives. When a hit is registered but no trigger arrives in this latency interval, the data is deleted. If a hit gets selected by the trigger it is processed further and send off chip via serial LVDS[24] output. Using a common digital block for four pixels makes sense for usage in a detector since hits will mostly be clustered and therefore resource sharing for such hits is useful. In addition, the power consumption is lowered since only triggered hits are transferred while un-triggered hits can be deleted without further processing. This also eliminates the main source of inefficiency at the estimated hit occupancies for IBL which was found out to be the data transfer to the periphery.

Another effect, where this structure provides an advantage, is the time-walk compensation. Time-walk describes the effect that hits with a low deposited charge arrive later than those with a high charge and thus during an LHC run a hit can be assigned to the wrong bunch. Hits below a certain ToT, which is programmable between 1 and 3 clock periods, are referred to as small hits, while those above it are referred to as large hits. A time counter is started as soon as a large hit is registered, while small hits do not start a counter. When a counter is started, the ToT value of each of the four pixel belonging to one block is stored in a local buffer. In case a discriminator did not fire, a 0 is stored as ToT information. This ensures that small hits are stored in the same time bin as the large hits which belong to the same cluster and therefore they are associated with the correct bunch due to the geographical proximity to large hits instead of being sorted into the wrong bunch due to their discriminator time stamp.

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[23] **B**unch **C**rossings

[24] **L**ow-**V**oltage **D**ifferential **S**ignaling

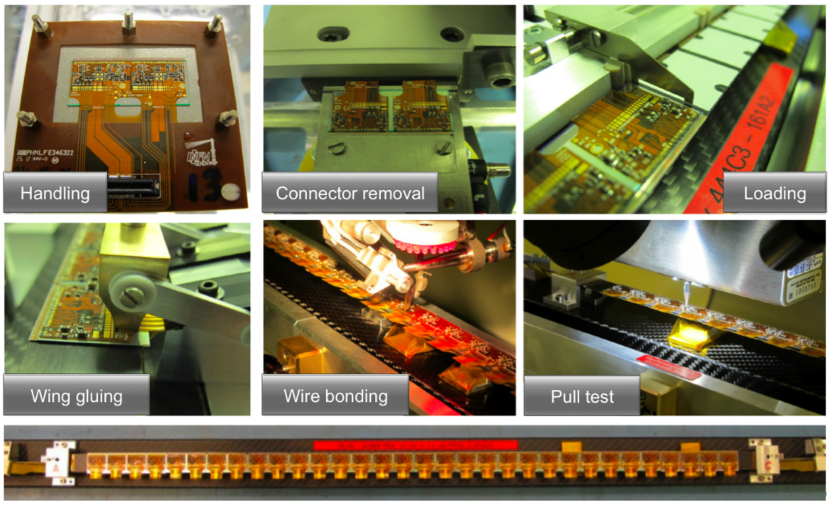

Figure 5.19: Overview of the stave loading process for IBL staves [54].

5.2.4 Stave construction

All IBL bare staves and flexes were glued at CERN, optically and electrically inspected and sent to the University of Geneva for loading of the modules. After their arrival, the staves and flexes were again visually inspected to verify that no damage occurred during transport, underwent metrology measurements to ensure their planarity and were thermally cycled to verify their mechanical stability under temperature variations as they will occur after installation since the detector will be operated at cold temperatures. Results of these tests can be found in Ref. [48].

The modules used for the assembly of IBL staves were tested in parallel at two sites: INFN[25] in Italy and the University of Bonn in Germany. First the FE and sensor functionality was verified by electrical tests, checking their powering and biasing behaviour and their digital registers. Modules that passed this tests then underwent ten thermal cycles from -40 C° to +40 $C°$ and were retested to exclude modules that develop problems under thermal mechanical stress. Modules that also passed the thermo-cycling without damage were tested more extensively with calibrations, module functionality tests and tunings. Only modules with a total number of bad pixels smaller than 1% were chosen for the loading on staves. Figure 5.19 shows an overview of the stave loading process. More detailed information about this procedure can be found in References [48] and [54]. After the loading procedure, the staves were sent back to CERN for their final inspection and installation. The procedure and results will be described in chapter 6.

5.3 Performance improvement after installation of IBL

The IBL detector has shown an impressive performance during the first phase of run 2, operating at about 98% track-cluster association efficiency as a function of track p_{T}. Figure 5.20 shows

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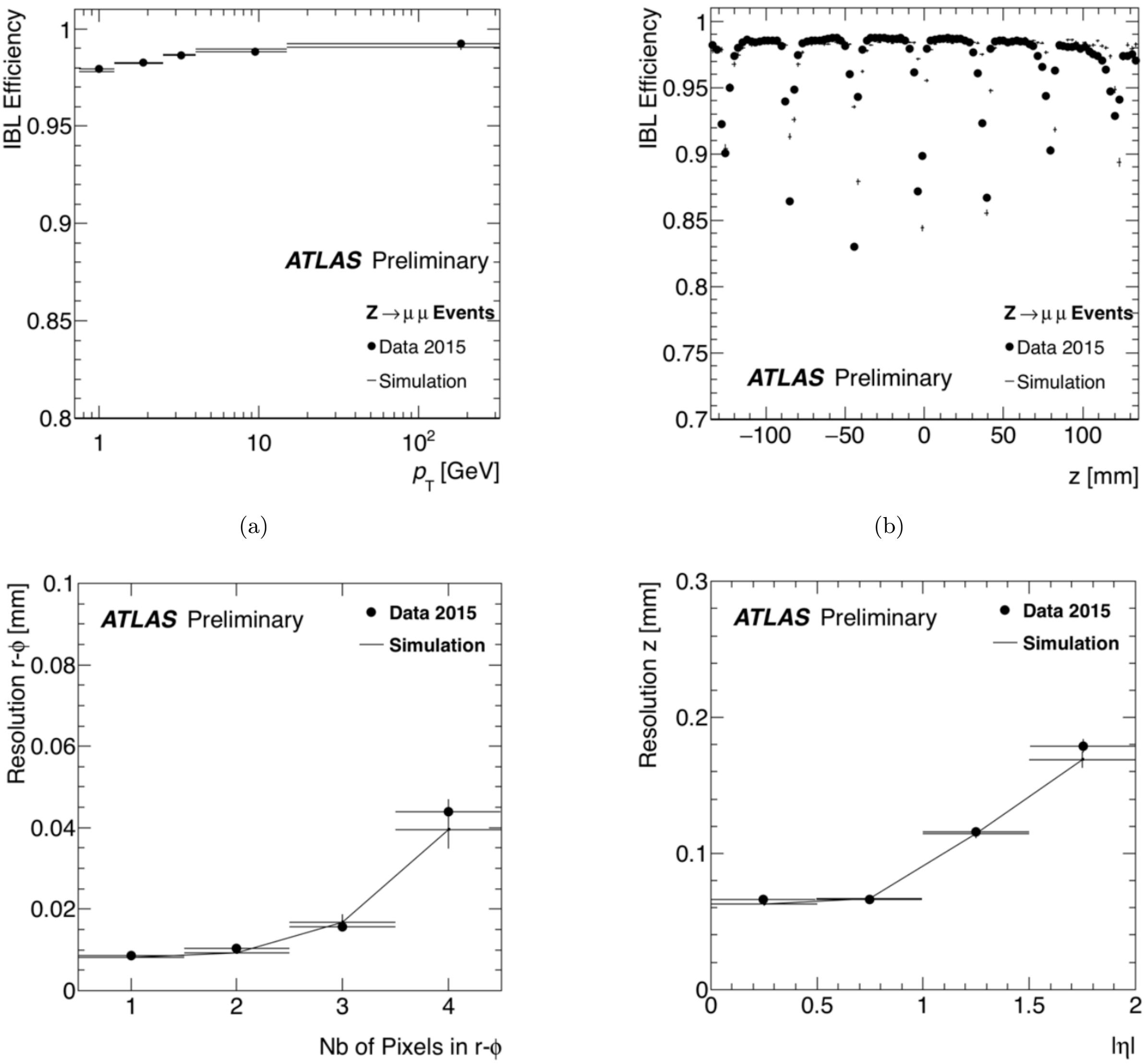
[25] **I**stituto **N**azionale di **F**isica **N**ucleare Sezione di Genova

the performance of IBL as measured from a sample of Z → $\mu\mu$ events in data taken in 2015. To determine the intrinsic detector resolution, a measurement on a sample of reconstructed particle tracks was performed. The tracks were required to traverse the active region of neighbouring IBL modules overlapping in ϕ and that two IBL hits are associated to them. The intrinsic detector resolution was then obtained from the distribution of the distance between the two IBL clusters extrapolated to the same distance from the beam line.The resolution was found to be $10.0 \pm 0.1\,\mu$m in r-ϕ and $66.5 \pm 0.8\,\mu$m in z [55].

Apart from the IBL standalone efficiency, the improvement of the combined pixel tracking system is of great interest. It can be stated that the overall performance was improved significantly over the whole acceptance. A comparison of the impact parameter resolution with and without IBL clearly shows this enhancement and is presented in Figure 5.21. For data analysis this improvements are especially beneficial since a better track reconstruction performance also leads to advanced b-tagging capabilities and for example score an average 10% increase in efficiency for similar light-jet rejection. The impact parameter measuring improvement is also beneficial for the identification of secondary vertices. B-hadrons have a relatively long lifetime of about 1.5 ps, leading to a flight length of a few millimetres before they decay. The point of this decay is referred to as a secondary vertex and can be identified by measuring the impact parameters of tracks belonging to the particles that are the resulting products of the decay. More detailed informations about the improvements of the ATLAS b-tagging performance in 2016 can be found in Ref. [57]. Until the end of 2016, the four-layer pixel detector proved the ability to take data at nearly 99% efficiency with a maximum dead time of around 2% for rates up to 85 kHz.



(a)

(b)

(c)

(d)

Figure 5.20: (a) Track-cluster association efficiency as a function of track p_T, (b) track-cluster association efficiency as a function of longitudinal coordinate z, (c) intrinsic detector resolution in r - ϕ as a function of cluster size, (d) intrinsic detector resolution in z as a function of η [56].

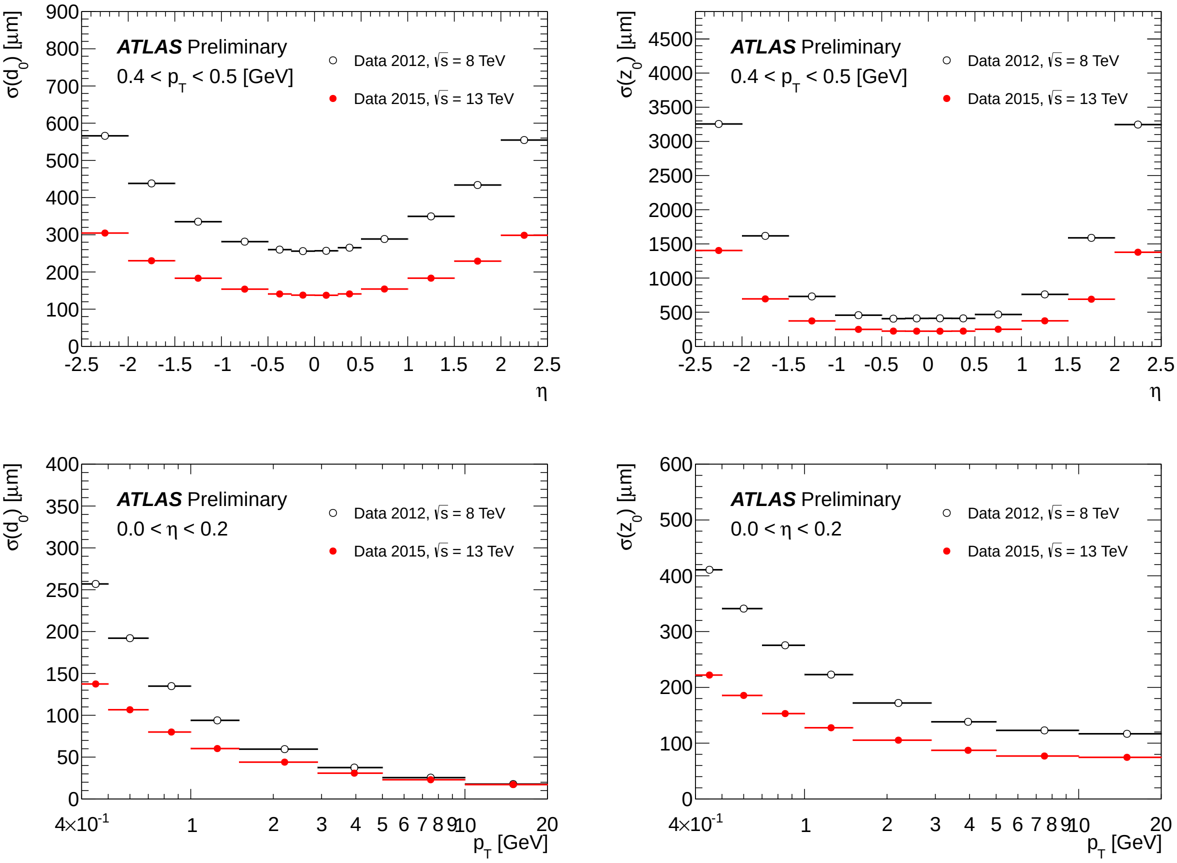


Figure 5.21: Unfolded transverse (left plots) and longitudinal (right plots) impact parameter resolution measured from data in 2015, $\sqrt{s} = 13$ TeV, with the inner detector including the IBL, as a function of $\mathrm{p_T}$, for values of $0.0 < \eta < 0.2$, (top plots) and η and for values of $0.4 < p_T < 0.5$, (bottom plots) compared to that measured from data in 2012, $\sqrt{s} = 8$ TeV. [58].

Chapter 6

Commissioning and operation of the IBL

6.1 Quality assurance measurements in SR1

The loaded IBL staves underwent a detailed test procedure at CERN to ensure their functionality and to rank them depending on their quality. Detailed results of those tests can be found in Ref. [54] and [59]. This ranking, which is presented in Table 6.1, was later taken as a reference to decide which staves are to use for the final construction of the IBL detector. The qualification test setup is shown in Figure 6.1. It consists of a 2 x 1 x 1 m^3 environmentally controlled aluminum box to allow measurements at operation temperatures. The setup was designed to offer an environment as close as possible to the situation after installation of the IBL detector in ATLAS with respect to supply devices, monitoring and for example cable lengths.
After arrival at CERN, high resolution pictures were taken of the staves for an optical inspection. When a stave passed this inspection it was installed in the environmental box for further testing. First the electrical and logical functionality of the modules was tested, followed by a calibration of all chips to ensure a uniform response after which scans were performed to qualify the calibration. Source scans were performed with a radioactive ^{90}Sr source where each chip was illuminated for 400 s to identify disconnected and inoperable bumps and to check the module's functionality. The initial tests were performed at +20 °C with a threshold value of 3000 e and a ToT of 10 bunch crossings (BC) at a reference charge of 16000 e, which is the most probable signal created by a MIP in 200 μm thick silicon. To achieve calibration results that are comparable to the conditions during operation, a retuning was performed at −12 °C to a threshold target value of 1500 e and a ToT of 10 BC @ 16000 e. With this configuration three thermal cycles were performed in a temperature range from −20 °C to +20 °C . After each cycle a reduced set of scans consisting of an analog, digital, threshold and ToT scan was performed to check for failures developed due to the thermal mechanical stress. All staves proved to be unaffected by those thermal cycles.

Two staves (numbers 7 and 8) were damaged during the quality assurance when they were accidentally exposed to high humidity. Due to this, they are not included in Table 6.1. Since the damage was not affecting the whole stave, they were later used for the system test which will be reported in section 6.2.

Based on the ranking of the staves, the best 14 were chosen for the construction of the IBL. A major criterium for the ranking was the number of working channels, the stave planarity and the sensor's leakage current stability. All 18 staves passed the QA criteria and no stave contained more than 0.3% bad pixels. With the 14 best working staves, the number of operational channels of the IBL could be confirmed to be 99.9% [54].

Table 6.1: "Ranking and loading order of the 14 IBL staves. The cooling pipe of the stave in position 01 is at $\phi = -6.1°$, subsequent staves are displaced by 25.7° in ϕ. The score is determined by the number of bad pixels, each of which is weighted according to the position on a stave. A lower score thus translates into a higher quality stave. The planarity shows the difference between the minimum and maximum height of a stave." [59]

Position	stave	Number of bad pixels	Score	Planarity [μm]	Reworked
#01	ST17	1052	1.01	114	no
#02	ST02	579	0.44	205	yes
#03	ST19	971	1.13	266	no
#04	ST09	1110	1.00	229	yes
#05	ST18	1266	0.94	336	no
#06	ST04	799	0.69	235	yes
#07	ST13	718	0.56	224	no
#08	ST10	646	0.62	243	yes
#09	ST11	565	0.58	298	no
#10	ST12	542	0.62	314	yes
#11	ST16	879	0.82	329	no
#12	ST06	734	0.79	290	yes
#13	ST15	864	0.84	325	no
#14	ST05	601	0.68	189	yes
n/a	ST01	1011	1.04	224	yes
n/a	ST03	1235	2.48	223	yes
n/a	ST14	1877	1.11	218	no
n/a	ST20	2139	2.01	237	no

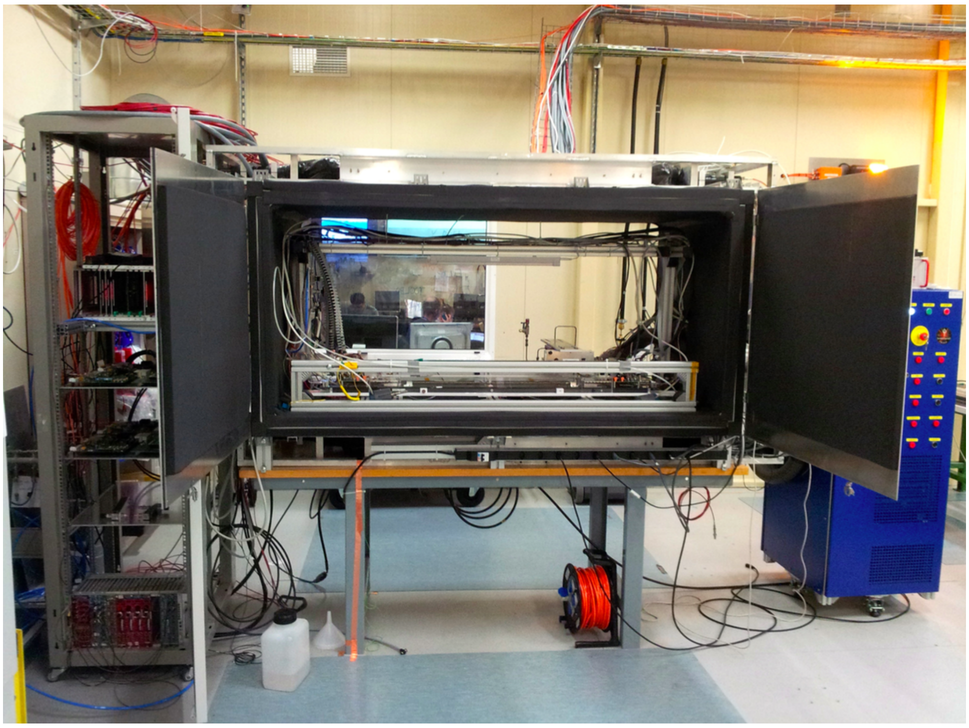


Figure 6.1: Photo of the test setup for the ATLAS IBL stave quality assurance tests at CERN [59]

6.2 Final test before assembling the IBL detector

The two staves (number 7 and 8) that had been rejected due to the damage that occurred when they were subjected to high humidity, were mounted on the IPT to perform a system test, in the following referred to as final test. The preparations for the final test started when components and cables arrived at CERN in September 2013. The setup was prepared in the following months followed by the installation of stave 7 and 8 on the IPT in December 2013. The final test itself only took one month to allow for a more extensive and detailed testing of the actual detector after the installation of the chosen 14 IBL staves. The goal of this test was to provide a realistic test environment with respect to the operation of the detector. Therefore, only production parts were used for the services in order to be as close as possible to the final system as it would be in ATLAS. The powering and readout chain was verified and the staves were tested by running calibration scans, source scans and taking cosmic data. Every measurement was compared to the quality assurance measurements as reference. The final test was an important basis for the development of a protocol that was used for the commissioning of the services for the on-surface commissioning as well as for the final detector commissioning after installation in the experiment.

The first part of the commissioning of the setup was to test and map all electrical services.

The mapping for the low voltage powering as well as the mapping of the temperature sensors was checked using a dummy load that simulated the staves. The dummy load is a test board to mimic the stave power consumption without endangering or damaging the actual staves while at the same time it provides easy access to measure the inputs and outputs. When provided with low voltage one could cross-check the displayed voltage in the control panel for the staves, the so called FSM[1] panel [60], and the voltage measured with a multimeter on the dummy load. If the module group where the voltage was displayed and the one where it was measured differed, the mapping was corrected. The dummy load was used to compare the displayed and measured values of the low voltage and its corresponding current as well as the values for the high voltage and its current. It was found that one HV PP2 board needed some rework due to bad soldering quality and was therefore temporarily replaced. After rework no more problems occurred with the HV supply chain.

After verification of the powering chain, the dummy load was disconnected and staves 7 and 8 were connected instead. Tuning configurations from the QA were loaded and threshold and ToT scans were performed to test the functionality of the staves after installation around the IPT. The tests were performed using a full 2-stave RCE[2] [32] system with optical readout. Since the optoboards that were produced to be used in the final setup in ATLAS were not yet available, pixel optoboxes were used as a temporary solution.

For the scan results it has to be noted, that on stave 7 module A2-1 was not working due to a short between reset and GND[3] pads and on stave 8 A8-1 and C5-2 were not working due to broken regulators. Therefore, they were disabled and only QA data is shown for them in Figure 6.2. Figure 6.2 (a) - (b) shows the threshold and ToT values for both staves in comparison to the results obtained during the QA. One can see that the results are showing no significant difference between both tests and therefore it could be stated, that the chips were not damaged or influenced in a negative way by the installation of the staves around the IPT. Only three chips show worse results than during the QA, namely on stave 8 chip C5-1 which failed the threshold scan and on stave 7 chip A2-2 which showed very high noise. Both chips are part of double chip modules of which one chip was broken during the QA, therefore problems when operating them were expected and should not be taken as indicators for problems that might have occurred during installation. Overall the results obtained for different tunings showed excellent performance with a slightly lower and more homogeneous noise level compared to the QA.

The next step was to ensure that a stave can be operated without influencing its neighbour. Therefore noise scans were performed first after tuning the stave, then repeated after several steps of noisy pixel masking and lastly while running a threshold scan simultaneously on the other stave. The result is displayed in Figure 6.3. It could be proven that the noise is not increased on any chip of one stave while operating the neighbour stave simultaneously.

The last part of the final test was to test the actual functionality of the staves by running source scans and taking cosmic data. Source scans were performed with ^{241}Am and ^{90}Sr sources placed above the staves in two different configurations. Data was taken for one hour, the result

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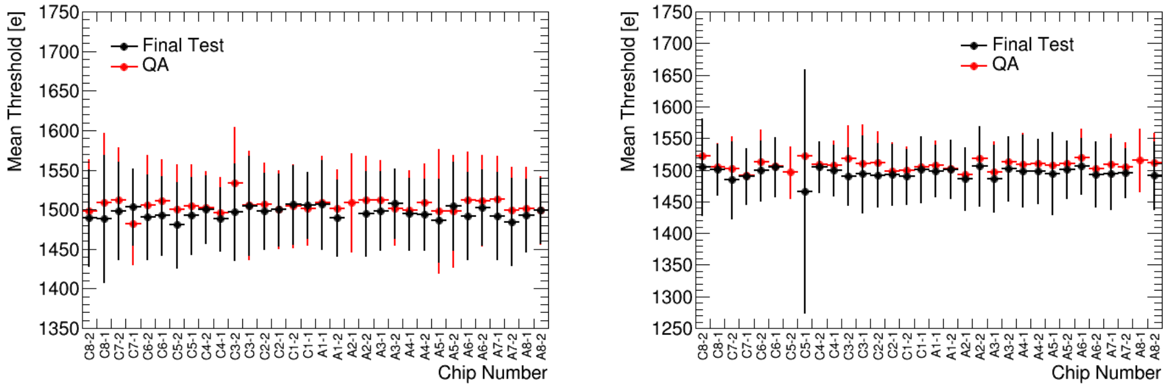
[1] **F**inite **S**tate **M**achine

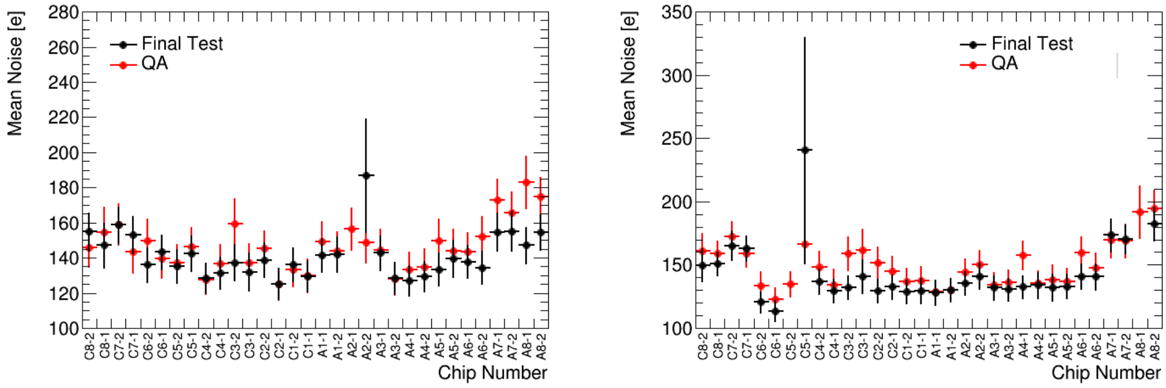
[2] **R**econfigurable **C**luster **E**lement

[3] **Ground**



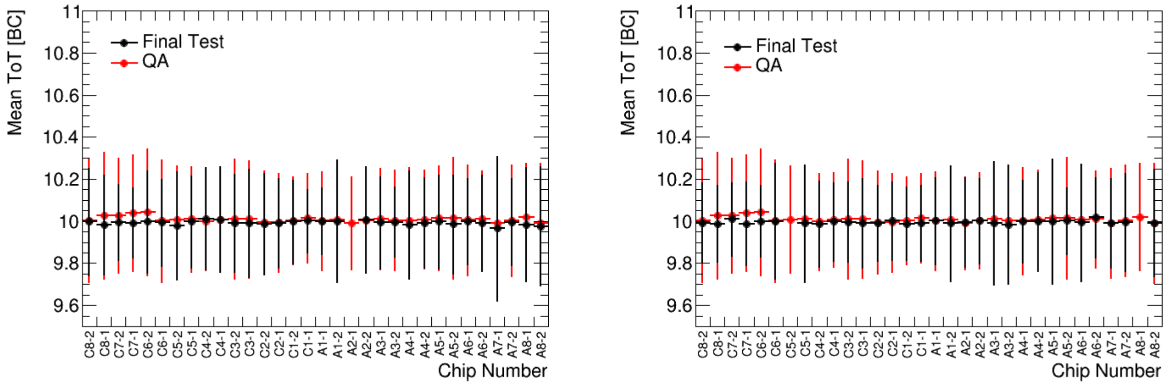
(a) Stave 7, Threshold scan

(b) Stave 8, Threshold scan



(c) Stave 7, Threshold noise

(d) Stave 8, Threshold noise



(e) Stave 7, ToT scan

(f) Stave 8, ToT scan

Figure 6.2: Stave 7 (left) and stave 8 (right) Threshold (a,b), Noise (c,d) and ToT (e,f) results. It should be noted that on ST07 the front-end chip A2-1 was not working due to a short and on stave 8 the front-end chips A8-1 and C5-2 were not working due to broken power regulators. Therefore, they were disabled during the final test and only QA data is shown for them in the comparison plots.

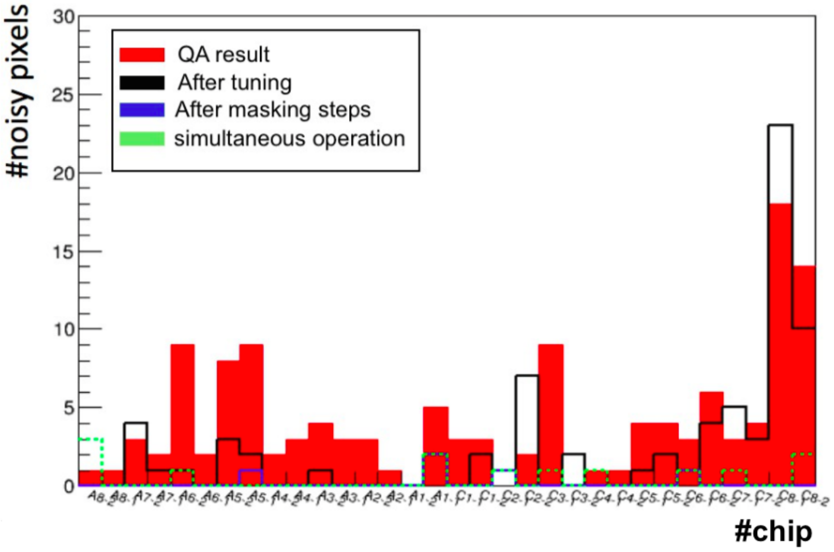
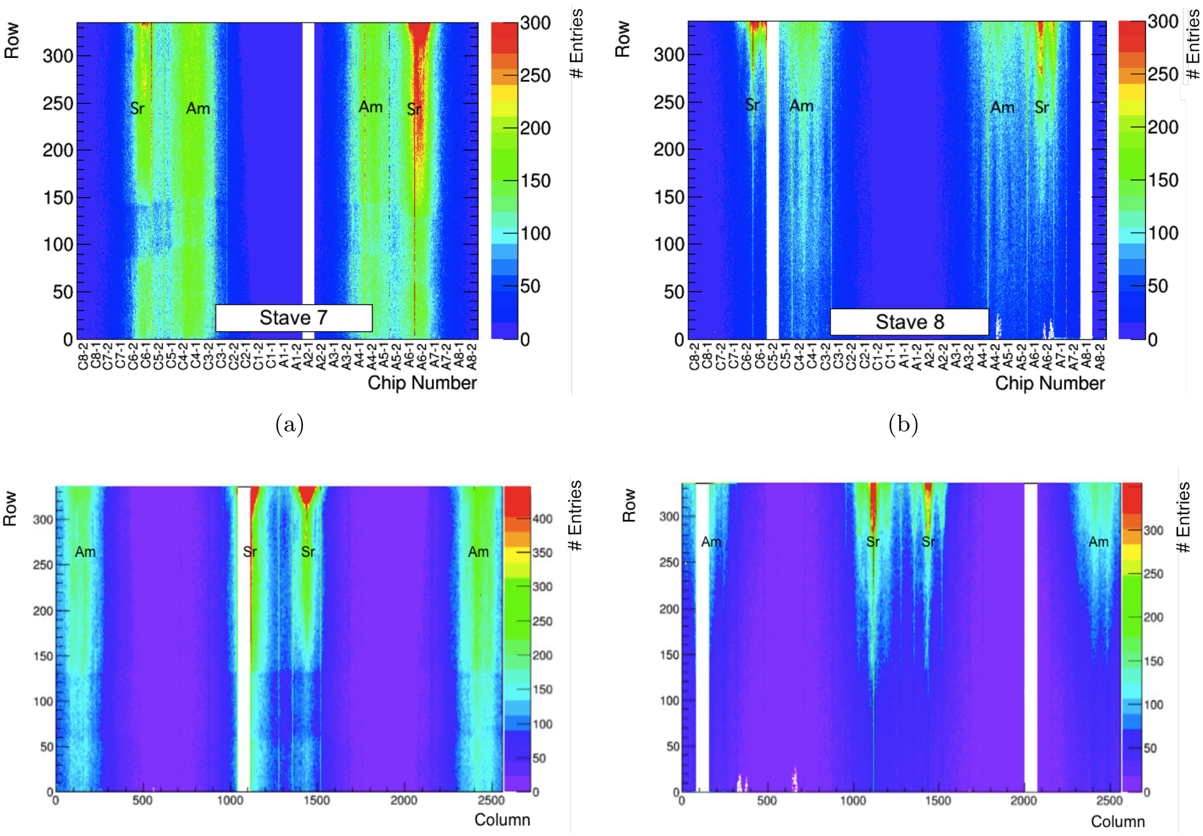


Figure 6.3: Number of noisy pixels per front-end readout chip as obtained by noise scans during QA (in red), after re-tuning (in black), after masking noisy pixels (in blue) and when running scans on the neighbouring stave in parallel (in green). No increased noised is visible when two neighbouring staves are operated simultaneously.

is shown in Figure 6.10 (a) - (d). The white stripes are due to the disables modules and the blue horizontal shade visible in the lower region of stave 7 can be identified as the cooling tube. The setup and the placement of the sources for both measurements is shown in Figure 6.5. A one hour cosmic data run also showed no problems and an example of a cosmic track traversing one full front end chip is presented in Figure 6.6.

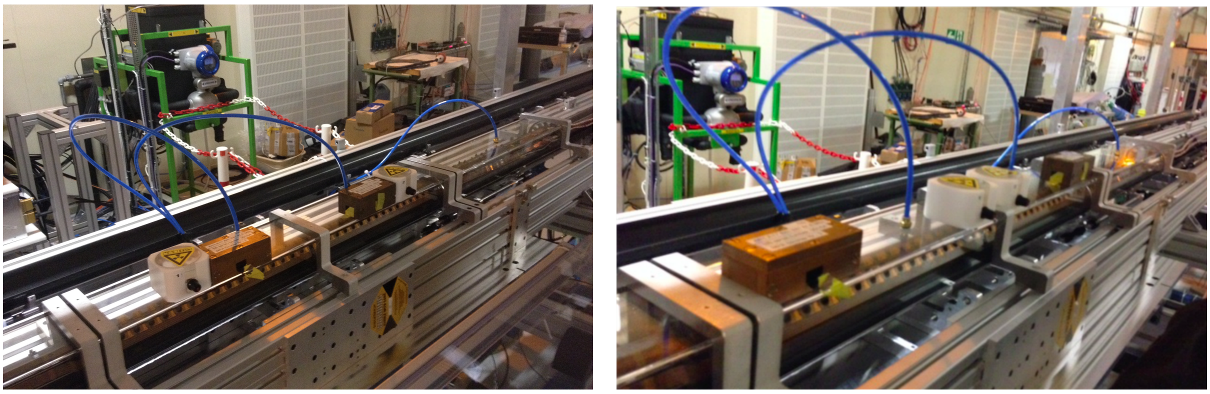
The final test was also used to confirm the stable operation of the CO_2 cooling system and the functionality of the interlock system. The module temperatures were kept stable below 20°C for different supply voltages and module configurations and no problem with either of the two systems was observed during the duration of the tests. To avoid condensation, the staves were sealed in a plastic box which was flushed with dry air as shown in Figure 6.7. In conclusion it can be stated that the full functionality of the setup was verified by the final test, faulty components got replaced or re-worked, the connectivity of the whole setup was understood and corrected on many levels and thus the installation of the IBL detector could be carried out subsequent to this tests.



(a) (b)

(c) (d)

Figure 6.4: Source Scan results for stave 7 (left) and stave 8 (right) in two different configurations. Top: configuration 1, bottom: configuration 2. Data was taken with ^{241}Am and ^{90}Sr for one hour.



(a) (b)

Figure 6.5: Placement of the ^{241}Am and ^{90}Sr sources for source scan data marked with configuration 1 (a) and configuration 2 (b).

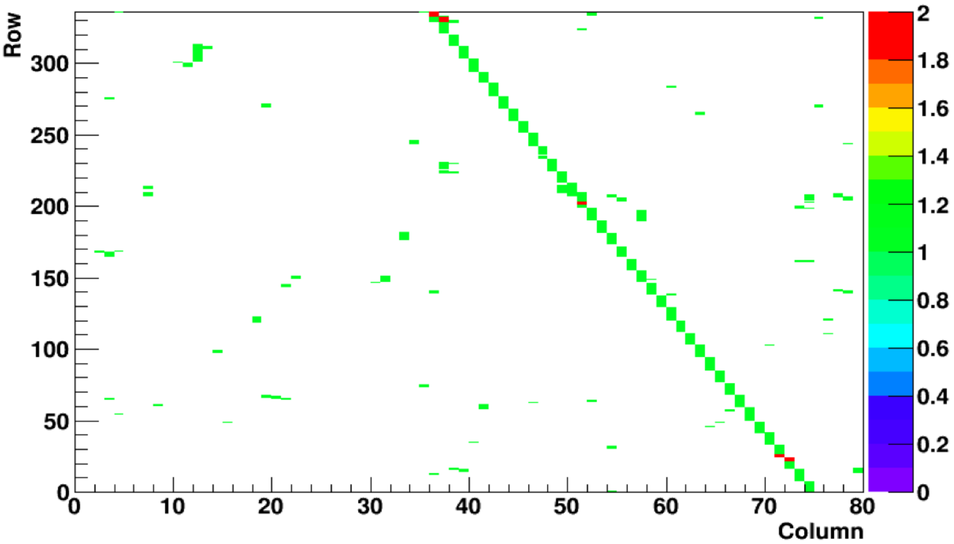


Figure 6.6: Example of a cosmic track along the 3D single chip module A8-2 of stave 7. The green colour corresponds to one hit being registered in a pixel.

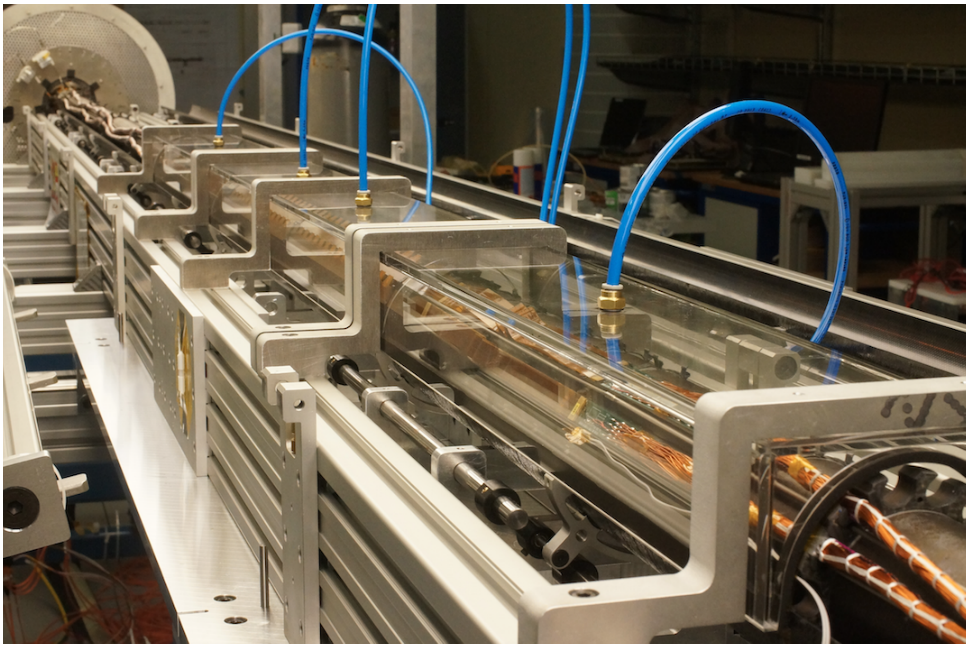


Figure 6.7: Final test setup with stave 7 and 8 installed, covered with a plastic box that is equipped with hoses (in blue) for dry air supply.

6.3 Commissioning before installation in ATLAS

Before the 14 staves were installed, each of them underwent a procedure called brazing to extend the embedded stave cooling pipe and connect it to an extension to avoid using fittings which would have added to the material budget [48]. Afterwards, the staves were integrated around the IPT. To align them while avoiding neighbouring staves to touch, micrometer screws were used, leaving a clearance of 0.8 mm between the staves. After alignment, the staves were fixed to rings on the IPT. To maintain a fixed distance in azimuthal direction, a central pin is used which bonds the staves to a central ring. A sketch of the procedure is shown in Figure 6.8.

The staves were integrated one by one, each followed by the installation of their powering and read-out services. A model of the services in presented in Figure 6.9. For the tests presented in section 6.4, only the outermost connectors of the type-1 bundles could be used for testing as they are the only part of the IBL services that are accessible after the IBL installation in ATLAS. Therefore the services had to be tested thoroughly while all parts were still accessible. Each stave was tested twice, after installation and after installation of its neighbour. This was done to make sure no damage was caused on a stave due to the installation of its neighbouring stave. Since the IBL is a closed cylinder, the first stave was tested three times, as it also had to be retested after the installation of the last stave.

A mobile test system, referred to as connectivity setup, was developed to test the functionality of the IBL staves after each integration step. Due to its mobility the setup was used on surface as well as for checks after installation in ATLAS. The readout was done via an RCE system which enabled tests in a very short time due to simultaneous readout of 16 front end chips. This was necessary since no active cooling was available during the connectivity tests and the modules would reach the interlock temperature after roughly 10 seconds. Figure 6.10 presents a summary of the results of the connectivity test. The scan results on their own as well as a comparison to the QA results show a very uniform outcome and no unexpected deviations.

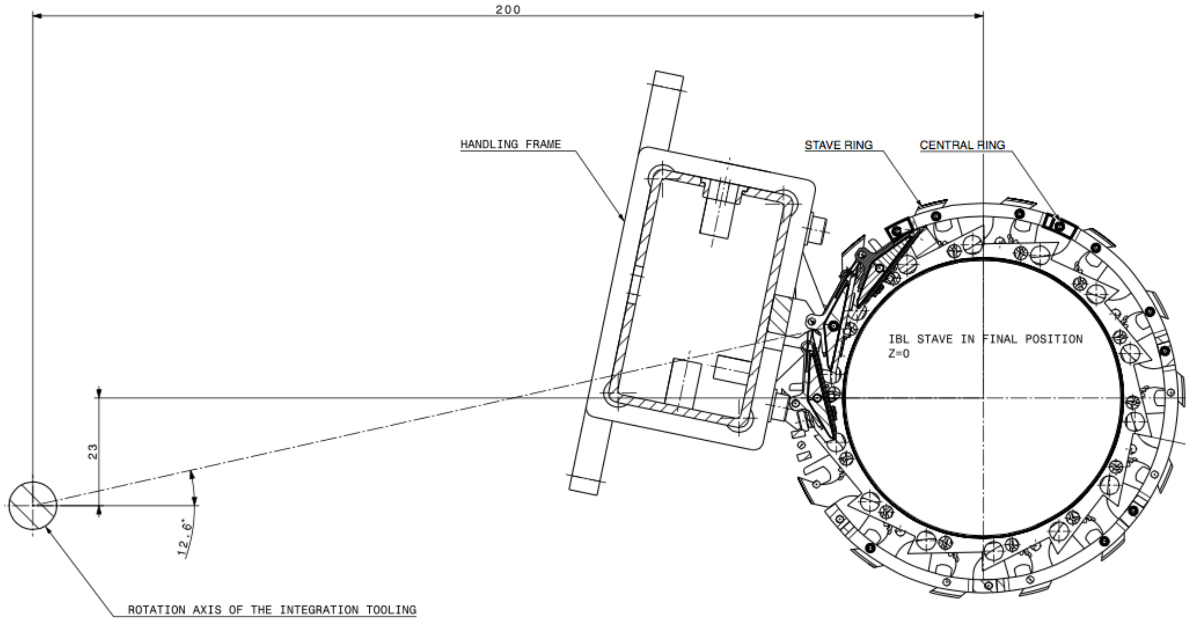


Figure 6.8: Transversal view of the stave integration around the IPT. On the left side the handling-frame is depicted [48].

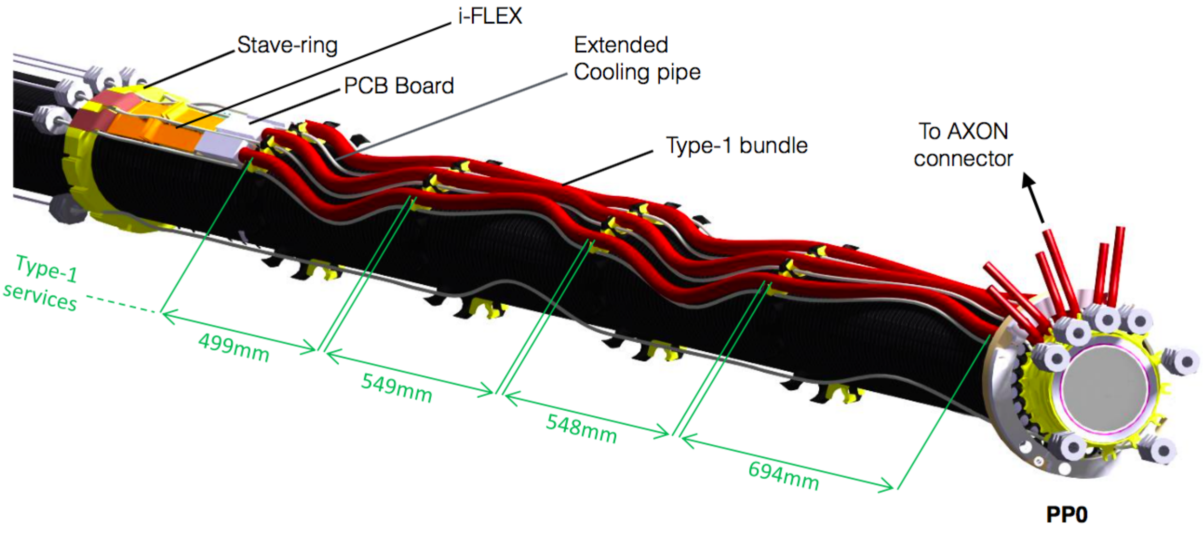


Figure 6.9: Model of the IBL services. Type-1 cable bundles are connected to i-flexes via PCBs at the end of each stave [48].

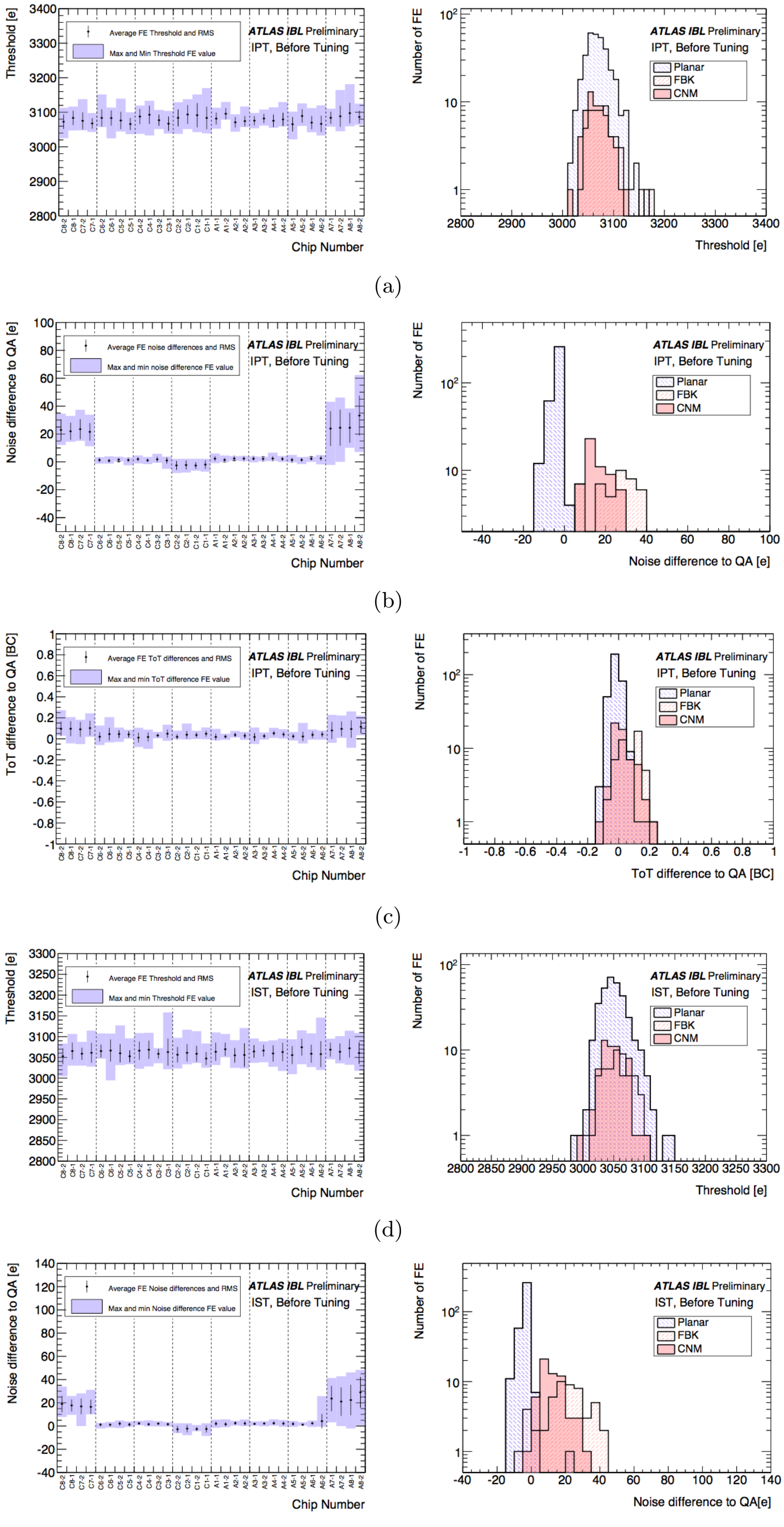


Figure 6.10: Result of Threshold and ToT scans after installation around the IPT (a)-(c) and after closing the IST (d) and (e). Data Taking was performed using the QA configuration targeted to 3000 e and 10 ToT [48].

6.4 Commissioning after installation in ATLAS

After the verification of the full functionality of all 14 IBL staves, the detector was inserted in ATLAS in May 2014 and the commissioning in the cavern started in June. After insertion all tests performed during the connectivity test had to be repeated, to ensure that no damage occurred during transport or insertion of the detector. For this final commissioning, the staves were powered via the ATLAS DCS[4] infrastructure while the read-out was still carried out by parts of the connectivity test setup described in the previous section.

One critical parameter of the IBL operation, which will also be an important point in chapter 7, is the LV supply. One has to ensure that no over-voltage can occur in case of failures in the service chain. To test the output voltage for different scenarios, the voltages at the PP1 were measured in dependence of different sense line failures. In order to prevent damage to the staves, a dummy load was used again. The LV was measured for the nominal case, in case of an open high-sense line, an open return-sense line and for the case of both sense lines being open. The result is presented in Figure 6.11. The test was performed with the operation voltage for IBL of 2.1 V. The outcome showed that in case of a sense line failure, the voltage that would be applied to the IBL modules exceeds the maximum value that was stated for the safe FE-I4 operation of 2.5 V. Therefore, additional powering procedures with carefully set safety limits were devised, to ensure a safe operation of the detector. A dedicated test however found no problematic sense lines, but since a sudden failure cannot be ruled out, the safe powering scheme will be used each time the detector needs to be switched on. In normal operation switching on the detector will not be done often, since there is no need to switch off the LV while cooling is in place. But as the first year of operation showed, one has to take into account the possibility of power cuts caused for example by unexpected marten attacks [61]. When the detector gets switched on, each module group is tested with a low supply voltage first to check the functionality of the LV sense line and only after it passes this test the nominal voltage is applied. After finishing the LV testing, the HV behaviour and the full service chain was tested and could be verified to be fully functional as well.

For the commissioning of the IBL staves a set of tests was performed stave by stave consisting of scans to test the chip performance as well as the measurement of IV curves and a full retuning of all staves. The cooling was stable at +15°C, resulting in module temperatures of about +17°C. For the readout an adjusted version of the RCE readout from the connectivity test was used. As a starting point, configurations from the QA were loaded that had been obtained at +22°C, with target values of 3000 e for the threshold and a ToT of 10 BC at a reference charge of 16000 e. It took about 1.5 hours to test one stave with this programme, including fibre swapping and power-up. During the tests it was found that two modules on stave 13 did not send any data, which would impact data taking noticeable. After a dedicated investigation the problem could be traced back to a faulty optoboard. As explained in chapter 5, the optoboards have been

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[4] **D**etector **C**ontrol **S**ystem

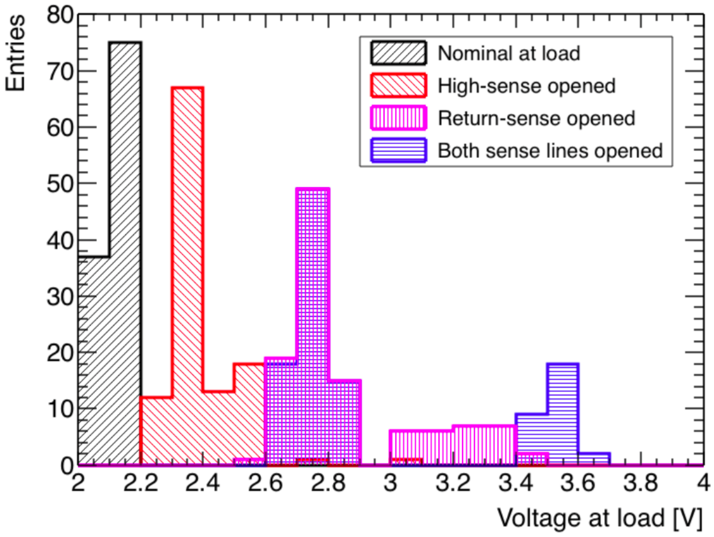
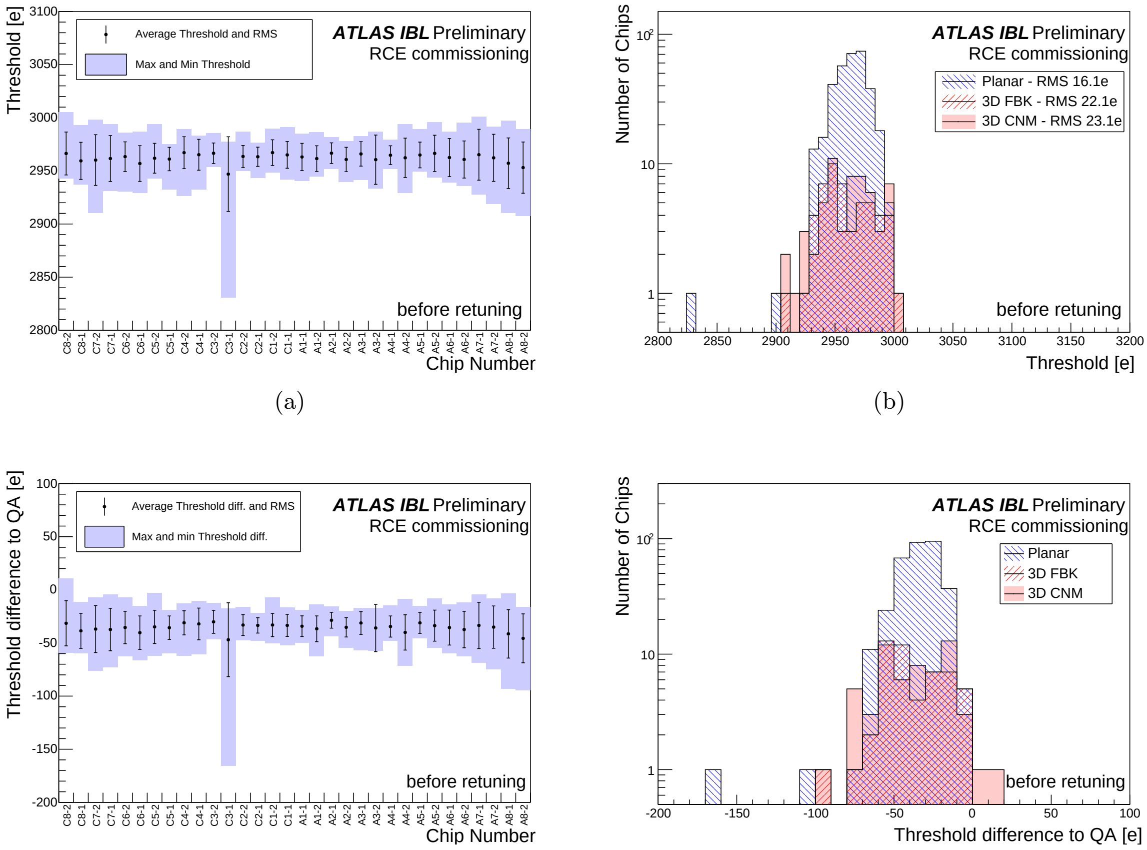


Figure 6.11: Measured voltages at PP1 during the service testing for a set voltage of 2.1 V under different sense open lines scenarios. A dummy load was connected at PP1 simulating the type-1 bundle resistance. [48].

designed in a way to be accessible even after installation of the IBL. Therefore the non-working optoboard could be replaced without problems.

After these initial difficulties were solved, threshold and ToT scans were performed and the results were plotted as standalone data as well as in comparison to the QA results to see if the trend is uniform and to check if any major changes can be spotted, which would be a hint for damage that might have occurred during transport or installation. The results, presented in Figures 6.12 to 6.14, show the measured values summed up over all modules on the left side and separated for each technology on the right side. It can be stated that no unexpected deviations were found except for one module which failed the threshold scan and one module which had a bad response during the ToT scan. After retuning however, the response of both modules was good again. The overall threshold is slightly lower than it had been during the QA, which is caused by the temperature difference. With lower temperatures the threshold decreases and therefore the results obtained after installation in ATLAS at +17°C were expected to be slightly lower than the results obtained during the QA at +22°C. On the A-side of all staves a lower noise has been observed. This observation can be explained by a small noise on the HV line of the QA setup which was a known factor. On the A-side more FBK modules are loaded which are more sensitive to this kind of noise and therefore an increased noise was observed during the QA but not after installation in ATLAS.

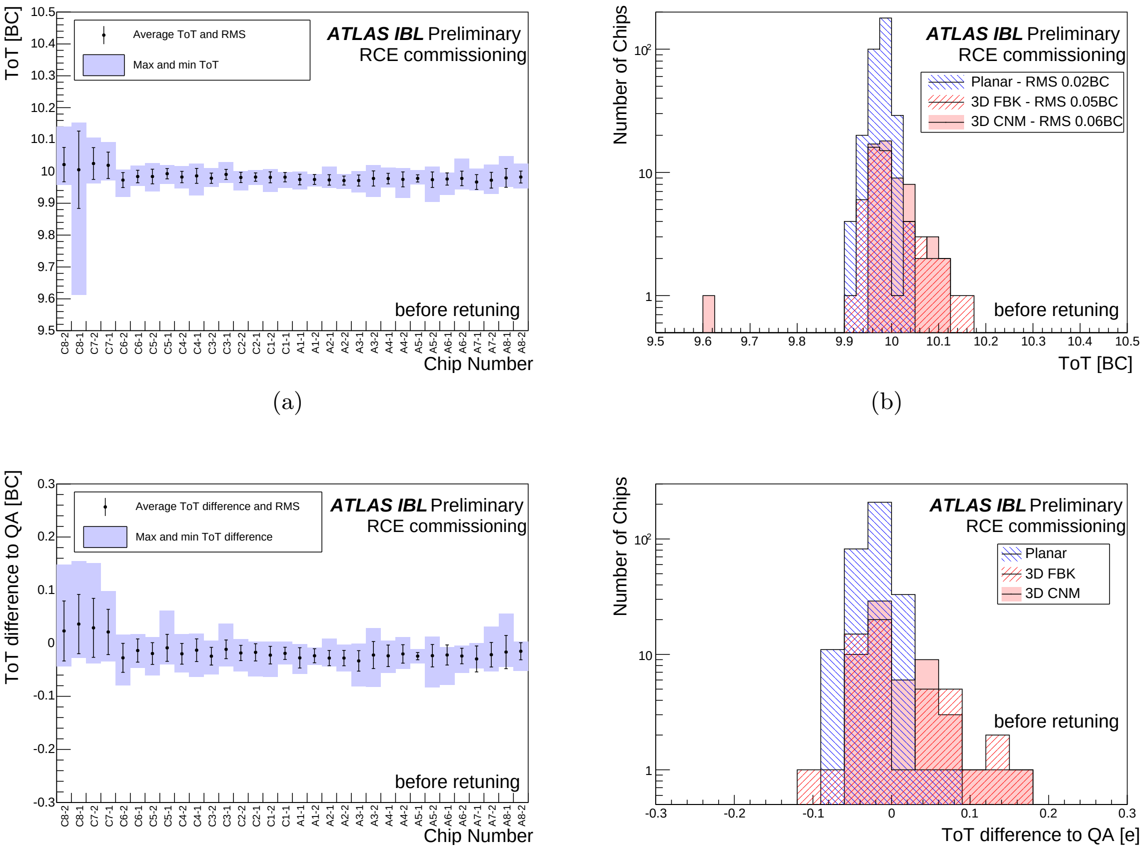
After the successful testing of all staves with the QA configurations, a full retuning was performed and the scans were repeated. The outcome of the retuned scans is presented in Figures 6.15 to 6.17. Also after retuning no unexpected deviations were observed and a more even and uniform distribution had been achieved. The full functionality of the detector was verified and the initial part of the commissioning was successfully concluded.



(a) (b)

(c) (d)

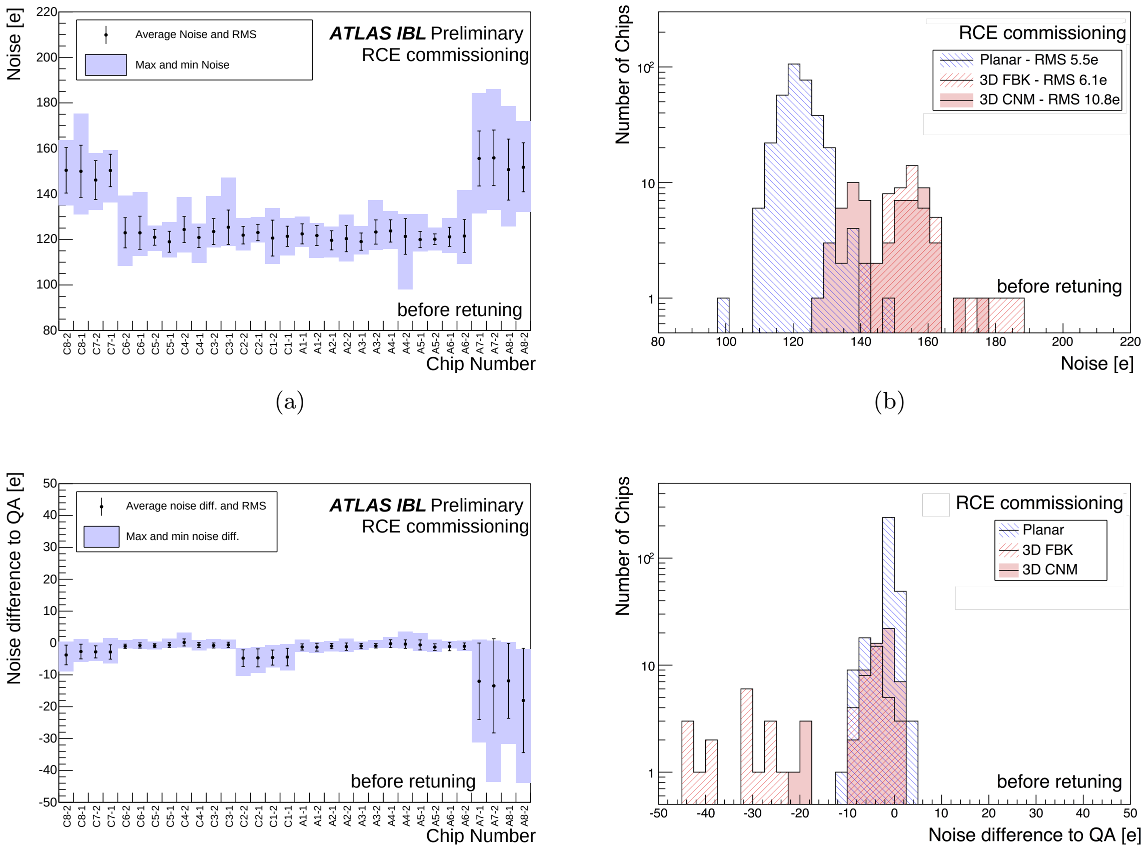
Figure 6.12: (a) Threshold chip-to-chip variation among the 14 IBL production staves. Data was taken with a configuration targeting 3000 e and a 10 ToT target response for 16000 e that was obtained during the QA at 20°C. The individual pixel data have first been averaged over each chip. The plots show, for each chip position on the stave, the mean and scatter of the 14 data points (one from each stave). The error bars show the RMS spread, while the solid boxes show the minimum and maximum values. (b) Correspondent FE threshold mean values distribution for each technology. (c) and (d) show the difference of the values obtained in the RCE measurements and the QA. The shift to lower thresholds is caused by the lower module temperature compared to the temperature when the tuning was done [62].



(a) (b)

(c) (d)

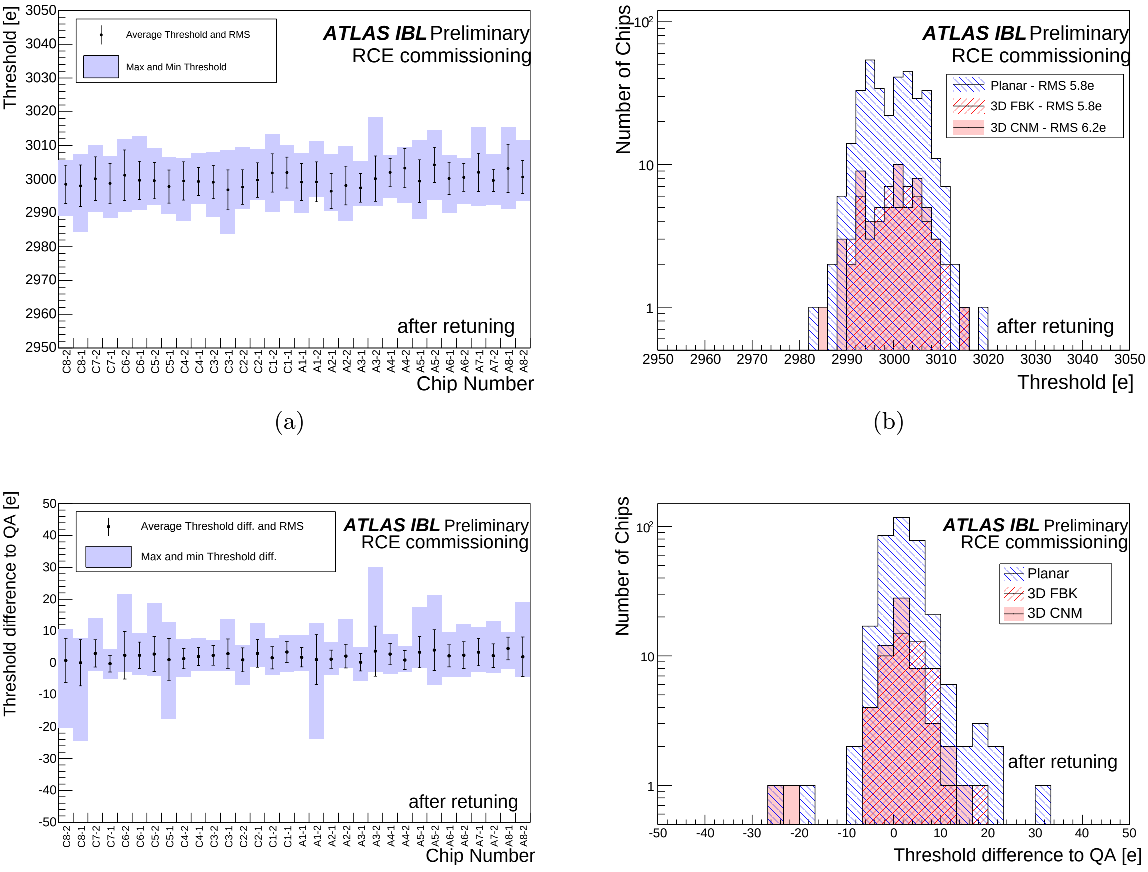
Figure 6.13: (a) Chip-to-chip variation of average Time over Threshold (ToT) in each pixel from injections of a 16000 e charge. ToT is measured in in units of bunch crossings, each of which represents 25 ns. Data was taken with a configuration targeting 3000 e and a 10 ToT target response for 16000 e that was obtained during the QA at 20°C. The plots show, for each chip position on the stave, the mean and scatter of the 14 data points (one from each stave). The error bars show the RMS spread, while the solid boxes show the minimum and maximum values. (b) Correspondent ToT mean values distribution for each technology. (c) and (d) show the difference of the values obtained in the RCE measurements and the QA [62].



(a) (b)

(c) (d)

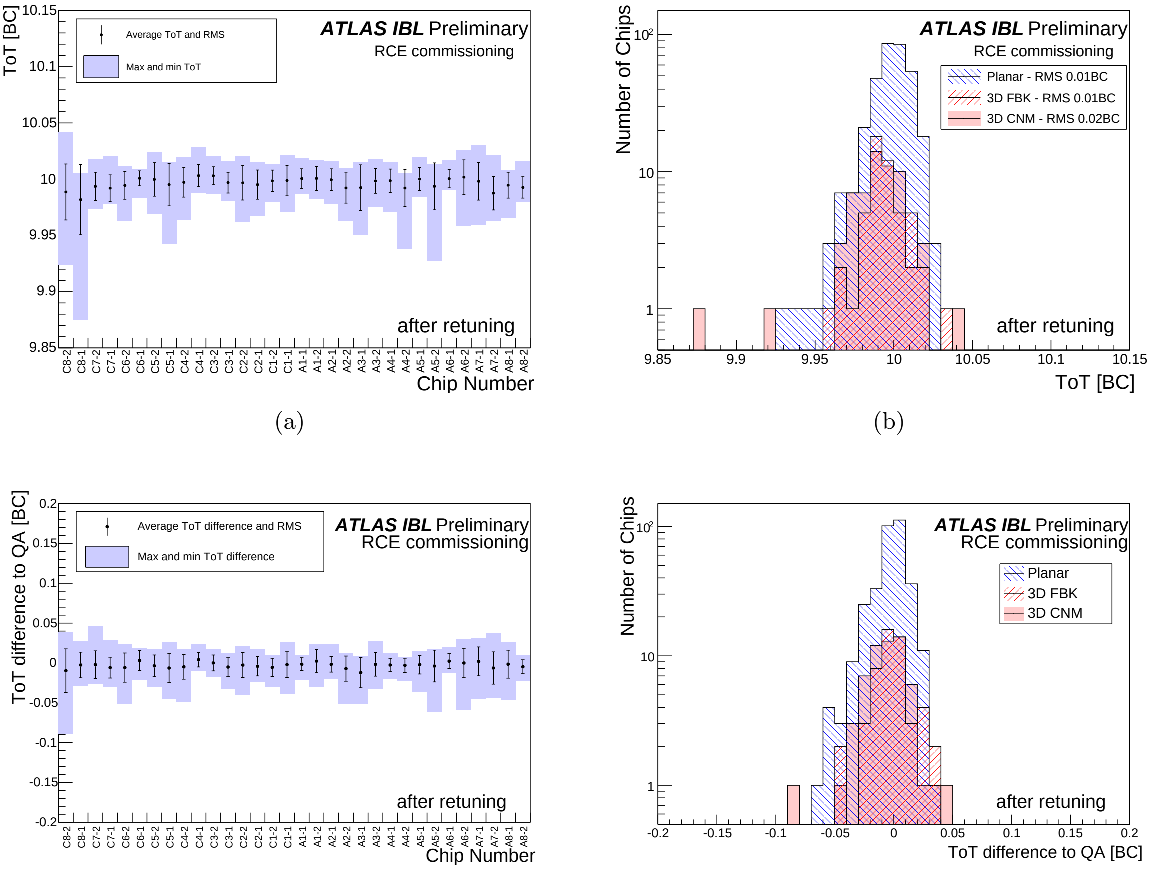
Figure 6.14: (a) Noise chip-to-chip variation among the 14 IBL production staves. Data was taken with a configuration targeting 3000 e and a 10 ToT target response for 16000 e that was obtained during the QA at 20°C. The individual pixel data have first been averaged over each chip. The plots show, for each chip position on the stave, the mean and scatter of the 14 data points (one from each stave). The error bars show the RMS spread, while the solid boxes show the minimum and maximum values [62]. (b) Correspondent noise mean values distribution for each technology. (c) shows the difference of the values obtained in the RCE measurements and the QA. The higher noise on the A-side in the QA measurements was caused by a small noise on the HV line of the setup and the sensitivity of FBK modules, which were more frequently chosen for loading on A-side, to such noise. The noise on the outer 3D modules is generally higher than on the planar modules [62]. (d) shows the noise difference distribution for each technology.



(a) (b)

(c) (d)

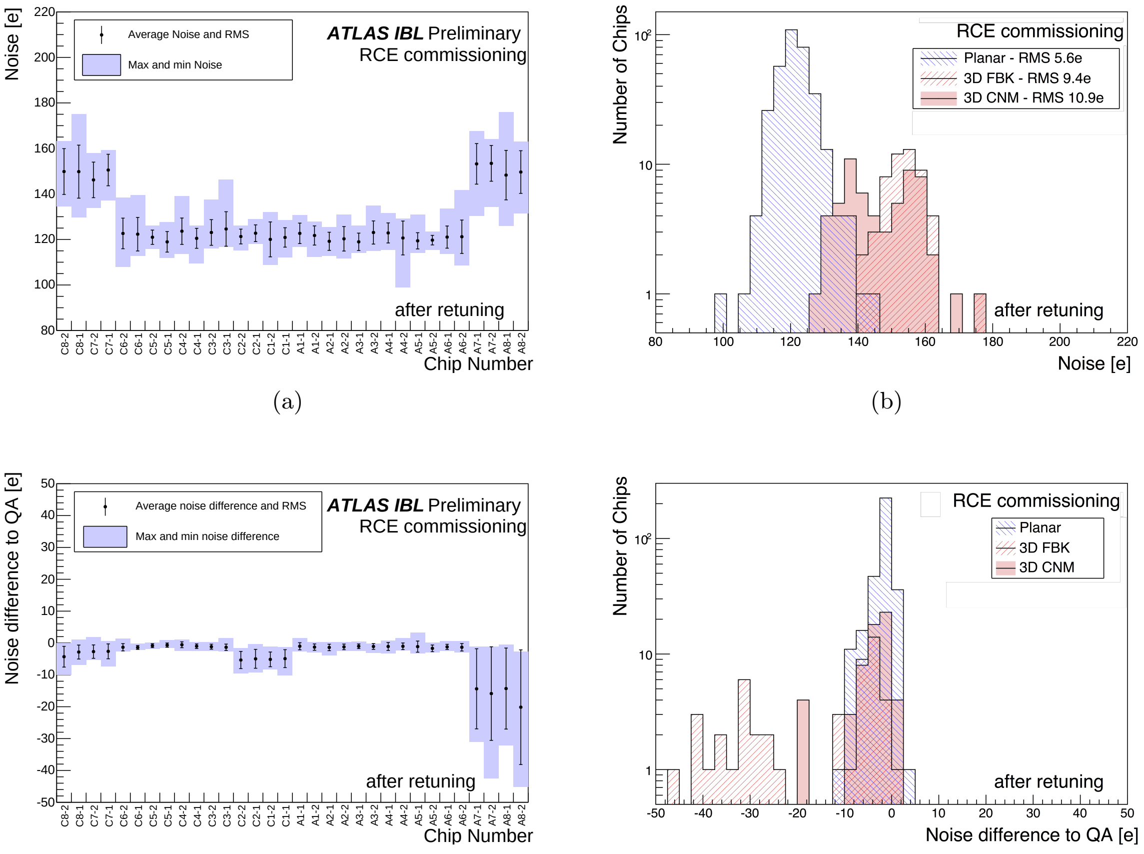
Figure 6.15: (a) Threshold chip-to-chip variation among the 14 IBL production staves after retuning all pixels to a target threshold of 3000 e and to a 10 ToT target response for 16000 e. The individual pixel data have first been averaged over each chip. The plots show, for each chip position on the stave, the mean and scatter of the 14 data points (one from each stave). The error bars show the RMS spread, while the solid boxes show the minimum and maximum values. (b) Correspondent threshold mean values distribution for each technology. (c) and (d) show the difference of the values obtained in the RCE measurements and the QA [62].



(a) (b)

(c) (d)

Figure 6.16: (a) Chip-to-chip variation of average Time over Threshold (ToT) in each pixel from injections of a 16000 e charge. ToT is measured in in units of bunch crossings, each of which represents 25 ns. The pixels were retuned to 3000 e target threshold and to a 10 ToT target response for 16000 e. The plots show, for each chip position on the stave, the mean and scatter of the 14 data points (one from each stave). The error bars show the RMS spread, while the solid boxes show the minimum and maximum values. (b) Correspondent ToT mean values distribution for each technology. (c) and (d) show the difference of the values obtained in the RCE measurements and the QA [62].



(a) (b)

(c) (d)

Figure 6.17: (a) Noise chip-to-chip variation among the 14 IBL production staves after retuning all pixels to a target threshold of 3000 e and to a 10 ToT target response for 16000 e. The individual pixel data have first been averaged over each chip. The plots show, for each chip position on the stave, the mean and scatter of the 14 data points (one from each stave). The error bars show the RMS spread, while the solid boxes show the minimum and maximum values [62]. (b) Correspondent noise mean values distribution for each technology. (c) shows the difference of the values obtained in the RCE measurements and the QA. The higher noise on the A-side in the QA measurements was caused by a small noise on the HV line of the setup and the sensitivity of FBK modules, which were more frequently chosen for loading on A-side, to such noise. The noise on the outer 3D modules is generally higher than on the planar modules [62]. (d) shows the noise difference distribution for each technology.

6.5 Sanity checks after thermal stress

After the initial commissioning was finished, the cooling system was planned to undergo an emergency test. The cooling of IBL is organised by two cooling plants, while only one is needed to cool the detector. The emergency test was set up to check if the second plant would instantly take over in case of a failure in the first plant. In case both plants fail to work, an emergency blow of system consisting of gas bottles should step in and this case was also tested. The test worked out as planned until it was stopped. After the test a slug of liquid re-entered the warming up detector, causing the temperature to went down to −35°C in less than a minute. The temperature trend with some added explanations is presented in Figure 6.18. It was discovered that the plant's safety by-pass can inject liquid from the closed-off plant into the liquid line from the detector. A safety by-pass at plant level was found as a solution to solve this problem and prevent incidents like this in the future.

All staves got retested after this incident to ensure that the modules were not damaged due to thermo-mechanical stress. To avoid unnecessary cable swapping, 12 staves got tested with the DAQ system, which is the designated readout system used during operation. Only two staves, namely 1 and 3, got retested with the RCE system since they were more affected due to multiple liquid injections and therefore got a more detailed inspection than the other 12. In principle the DAQ system is capable of running the same tests as the RCE system, but since the detector and especially the readout was still in its commissioning phase, not all possible applications were available at that time. The retesting consisted of:

- Taking IV curves
- Comparing threshold and ToT scans to RCE commissioning results
- Completely retest two staves with the RCE system
- Comparing the noise of scans with HV on and off

Figure 6.19 presents the IV curves of all sensors taken at −2°C, temperature corrected to +20°C. The correction was applied to get comparable results to the IV curves taken in earlier measurements. Figure 6.20 shows the IV results obtained during the QA at +20°C for comparison. The retesting showed no problematic sensors with respect to their leakage current. Some sensors showed a slight increase compared to the QA results, but all stayed in the limits which are considered safe for operation.

After verifying the leakage current trend, scans were performed to check the functionality of the front end chips and to check for bigger areas of defect or disconnected pixels. No problematic chip was found by this investigation. Figure 6.21 shows the result of the threshold and noise scan compared to the result obtained during the RCE commissioning. The scans were taken at −2°C with the configurations obtained at +17°C during the commissioning. The temperature difference caused the threshold to decrease by 200-300 e, but apart from this expected difference

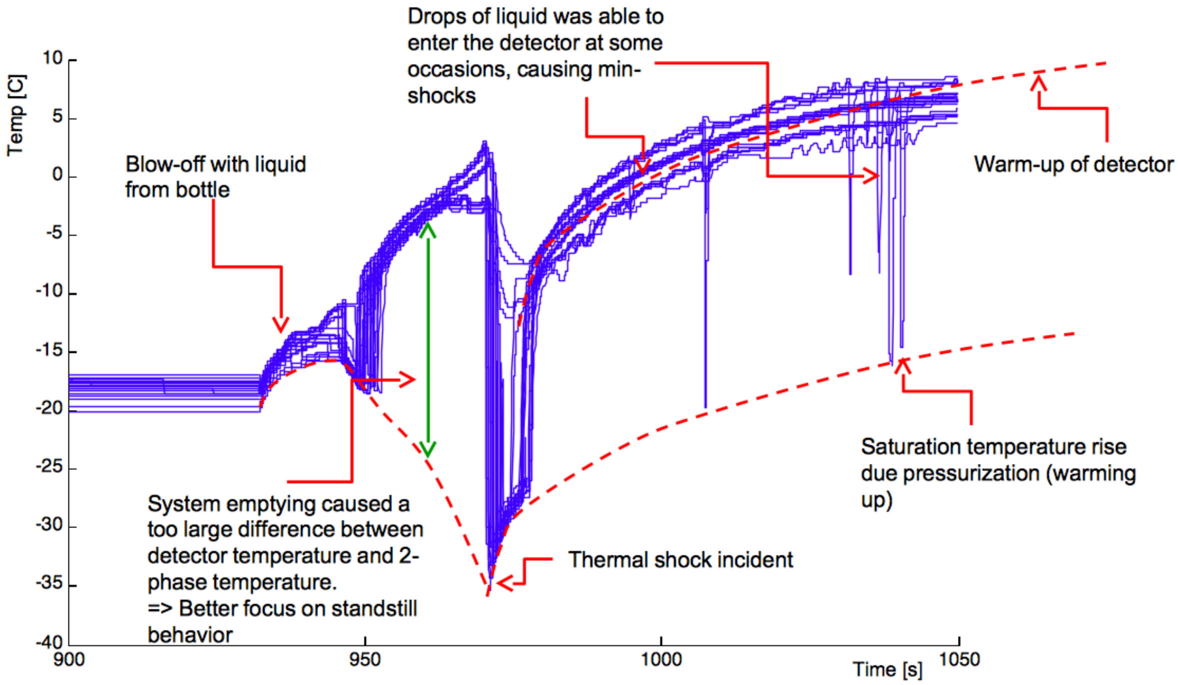
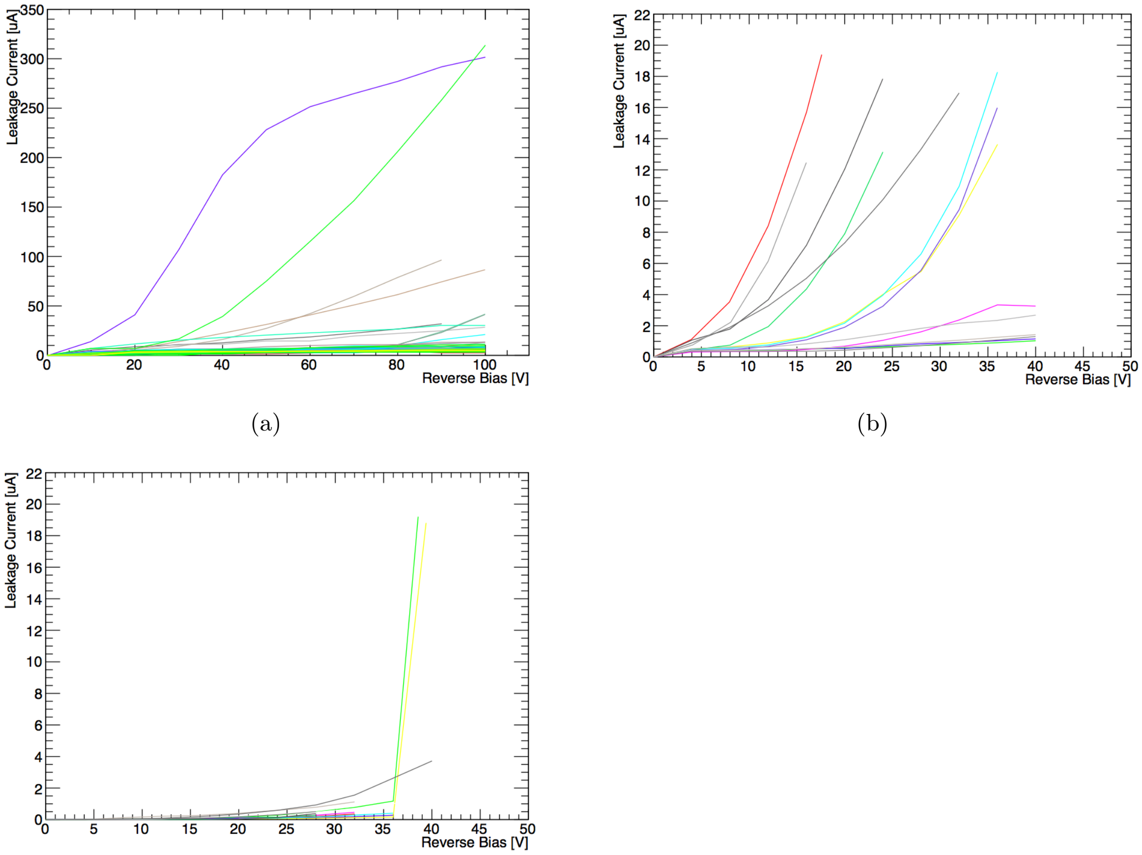


Figure 6.18: Temperature trend vs. time after an emergency cooling test performed on the IBL cooling system [63].

no deviation of the threshold values was found.

The overall noise behaviour showed a very uniform result as well. Only a small number of single chips showed bigger deviations. To make sure that this was not caused by a defect of the chip, a 2D noise map for the affected chips was checked. It was found that no cluster of non-responding pixels was present but a symmetric pattern which hinted at a readout instead of a chip problem. A second scan was performed using the RCE system and the 2D map was checked again. The second scan showed no problem and verified the full functionality of the chip. A more detailed investigation found a timing problem in the readout software and the problem did not show up again after debugging. The result of both scans is presented in Figure 6.22.

A second test was performed especially to search for defect and disconnected pixel. The aim was to make sure that no bump connections were damaged due to the temperature shock on a smaller scale. Noise scans were performed with HV on and off and the noise difference between the two scans was compared. A pixel is considered defect if the absolute value of the on/off difference is less than 15 e. This value was determined during the QA by comparing the results of source scans, which offer a reliable number of non-responding pixels, with the results of calculating the HV on/off difference. Since a source scan is not an option after installation in ATLAS, this method gives the most accurate results. This method is only applicable for planar sensors, since the noise difference for 3D sensors is too small to give reliable results. To illustrate this difficulty, Figure 6.23 shows the noise difference in electrons for scans with HV on and off for planar and 3D sensors. It can be seen that the difference for 3D sensors is close to 0 while planar



(a)

(b)

(c)

Figure 6.19: IV curves taken of all IBL modules after temperature drop for planar sensors (a), CNM sensors (b) and FBK sensors (c).

sensors show a difference of more that 200 electrons on average. Figure 6.24 shows the result of comparing the number of defect pixels from 133 planar modules to the numbers obtained during QA. Only 133 modules could be compared since some modules were needed at the same time to debugged the readout problems described before. No considerable difference was found and therefore it was stated that the shock-cooling of the IBL detector did not damage the staves and the detector was still 100% functional.

In September 2014 the first IBL stave was included in a cosmic run and could be tested successfully. Nine staves were included in October before the beam pipe bakeout took place. During this bakeout, the beam pipe was heated up to a temperature of 230°C to activate the NEG[5] coating which is used to maintain the required ultra-high vacuum levels during operation of the LHC [64]. The IBL cooling system kept the sensors at a maximum temperature of -8°C during the whole bakeout to prevent them from overheating. After the bakeout was finished, all 14 staves got retested a last time to finish the commissioning and verify the full functionality of the detector towards operation. The same set of tests was performed as after the cooling incident.

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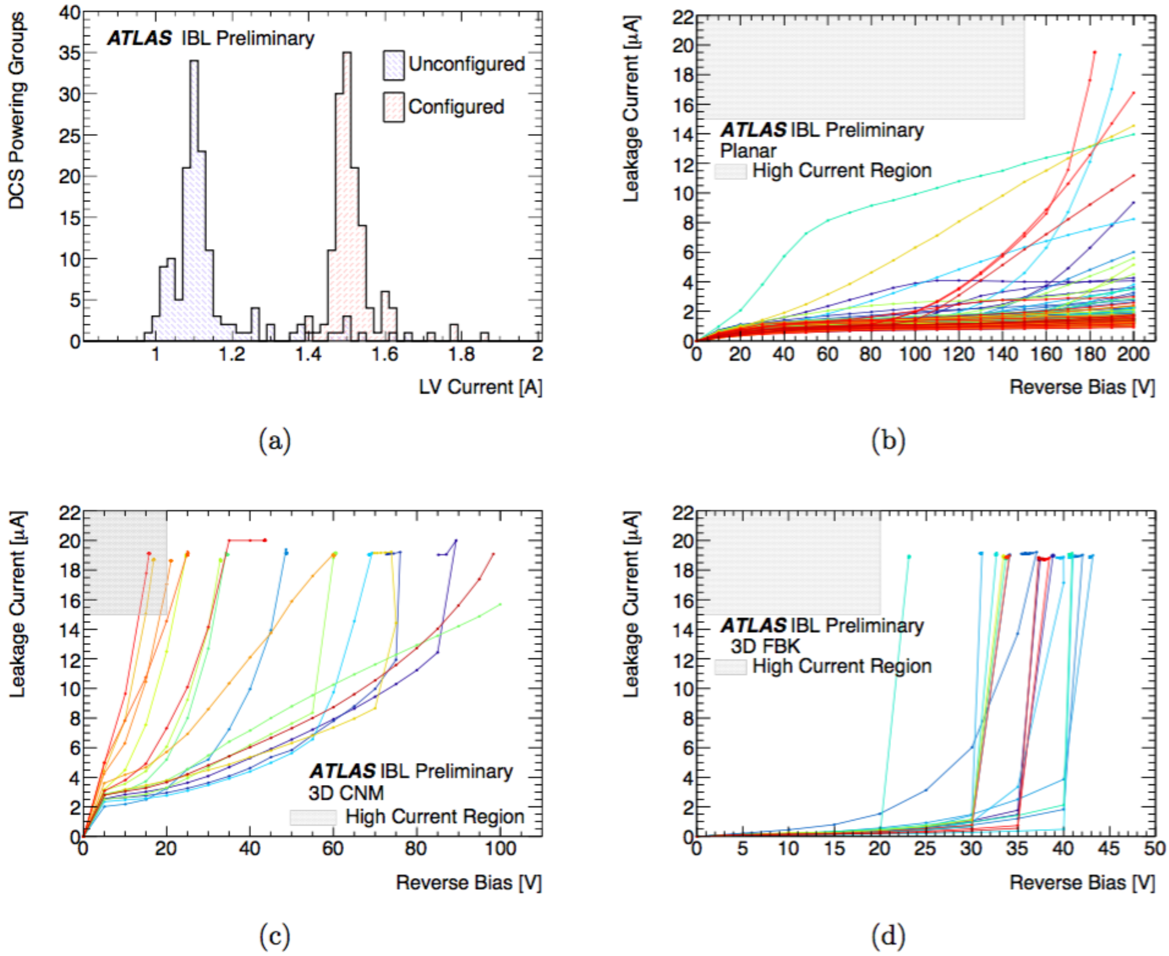
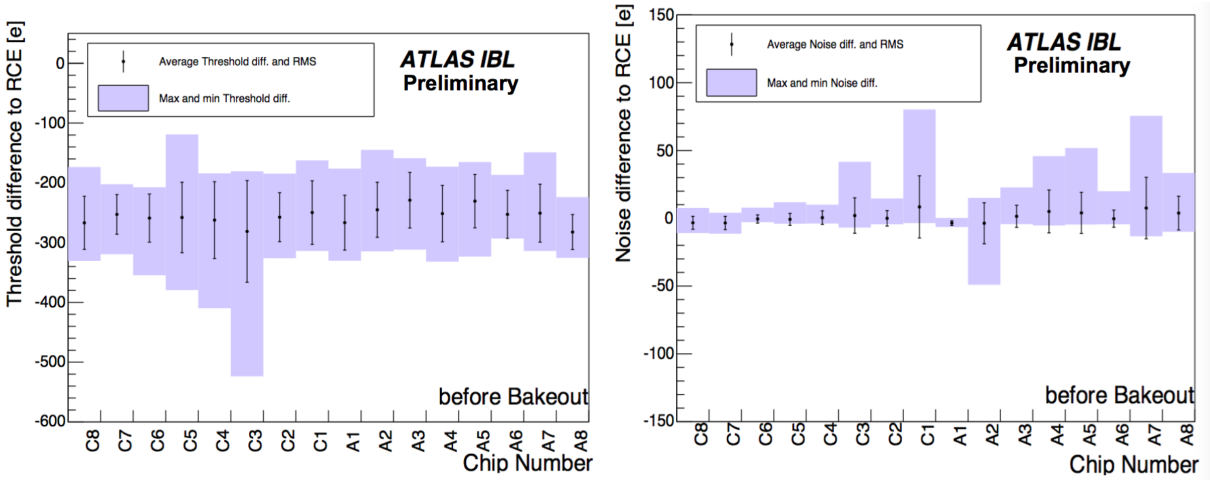
[5] **n**on **e**vaporable **g**etter



(a) (b)

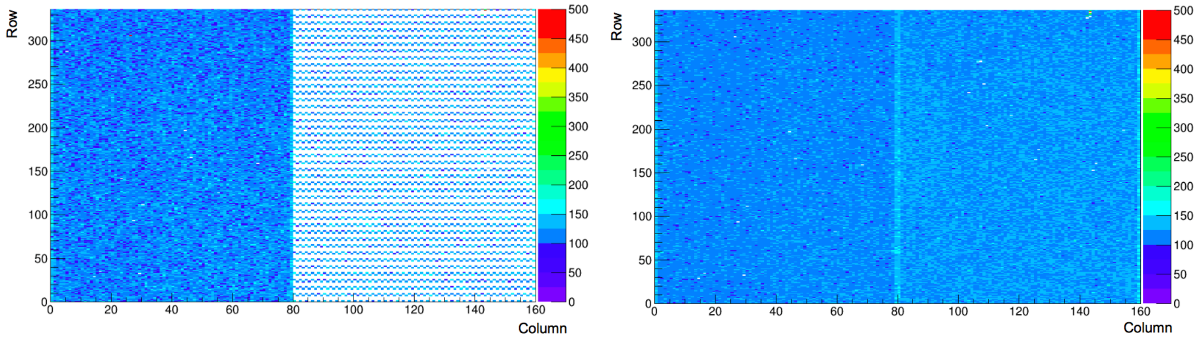
(c) (d)

Figure 6.20: (a) DCS groups' LV current consumption of all 18 staves and IV characteristics of (b) planar, (c) CNM and (d) FBK sensors of 17 staves at a module temperature of +20°C. The data set from Stave 20 is missing due to a recording failure [32].



(a) (b)

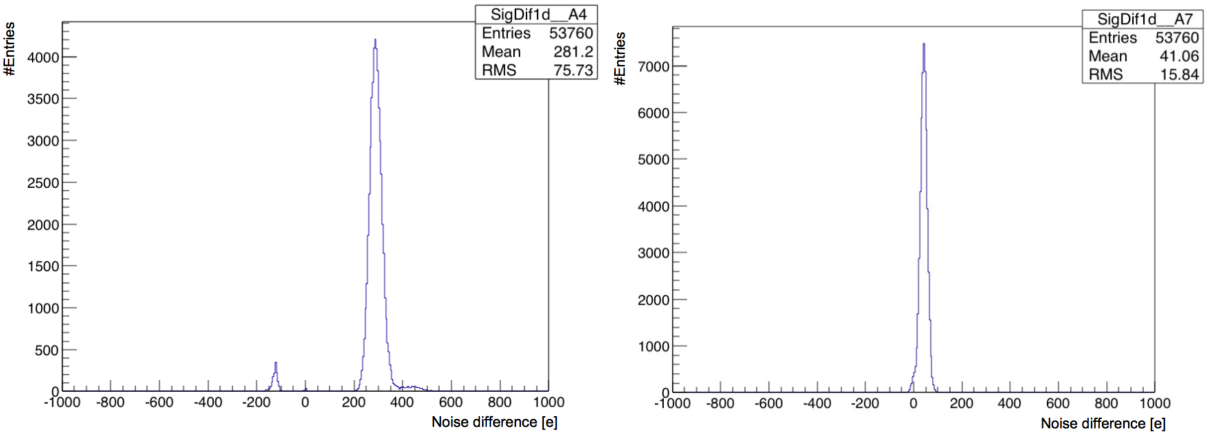
Figure 6.21: Chip-to-chip Threshold (a) and noise (b) variation as difference to the RCE commissioning results among the 14 IBL production staves after loading a configuration with a target threshold of 3000 e and to a 10 ToT target response for 16000 e. The individual pixel data have first been averaged over each chip. The plots show, for each chip position on the stave, the mean and scatter of the 14 data points (one from each stave). The error bars show the RMS spread, while the solid boxes show the minimum and maximum values.



(a) (b)

Figure 6.22: 2D noise map for stave 3, A-side, chip M1-A2. Scan result obtained with the DAQ readout system (a) and the RCE system (b).

The result of the IV curves, taken at -20°C and temperature corrected to +20°C, is presented in Figure 6.25, the threshold and noise comparison is shown in Figure 6.26 and the difference of defect pixels is displayed in Figure 6.27. Due to the lower temperature the threshold decreased again as expected. Since the readout system was successfully debugged, all 168 planar modules could be tested for defect pixels and no increase was found. Overall no deviations from the results obtained during the RCE commissioning were found and the detector was verified to be ready for operation.



(a)

(b)

Figure 6.23: Noise difference obtained in Threshold scans performed with HV on and off for planar (a) and 3D (b) sensors.

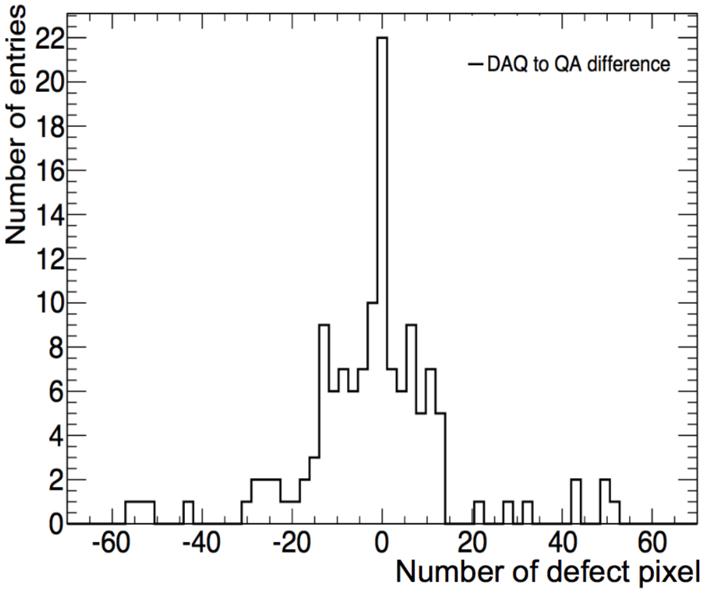
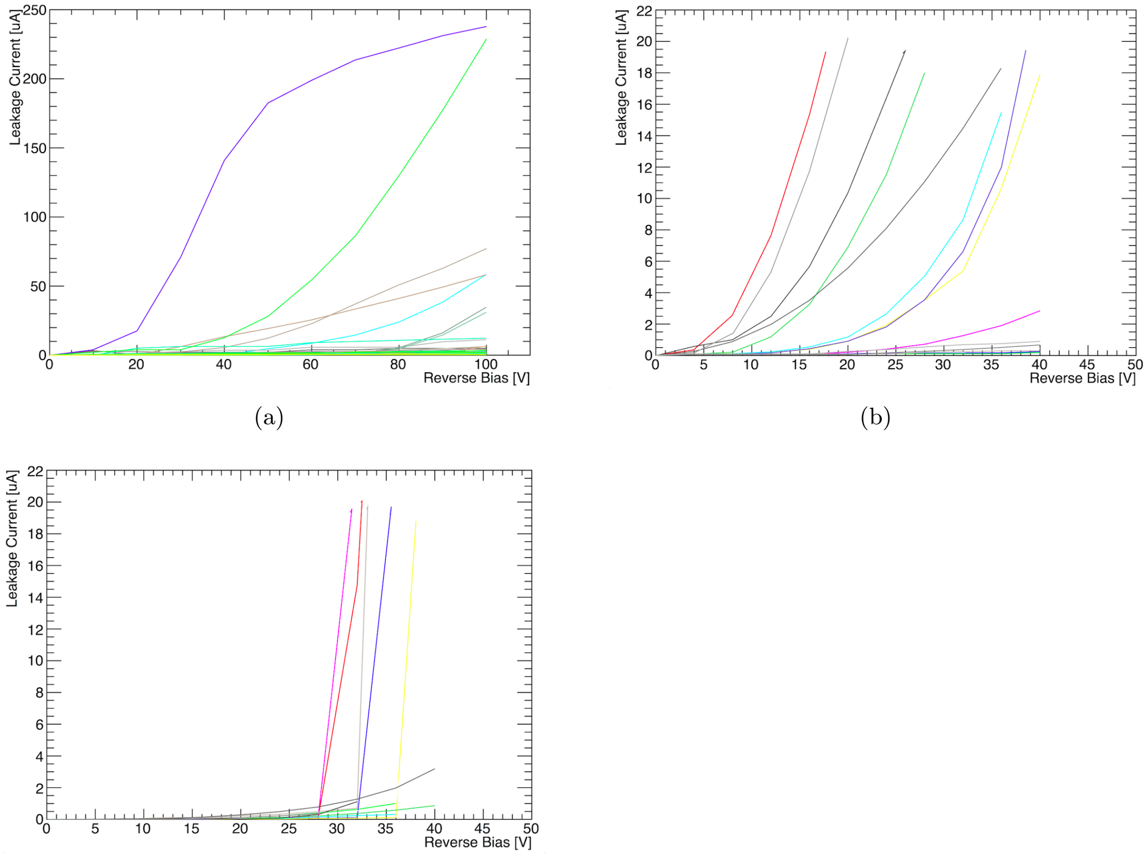


Figure 6.24: Difference in the number of defect pixels as obtained through threshold scans performed with HV on and off during QA and DAQ measurements.

All 14 IBL staves were first included in an ATLAS cosmic run in November 2014. An event display of a cosmic ray event that has been tracked by the IBL during this cosmic run is shown in Figure 6.28. Data taking with stable proton beams started in June 2015 at a collision energy of 13 TeV. Figure 6.29 shows a collision event recorded during the first stable beams run.

In conclusion it can be stated that the qualification and commissioning of the IBL detector was extremely successful, proving a fully functional detector during all steps from construction to operation.

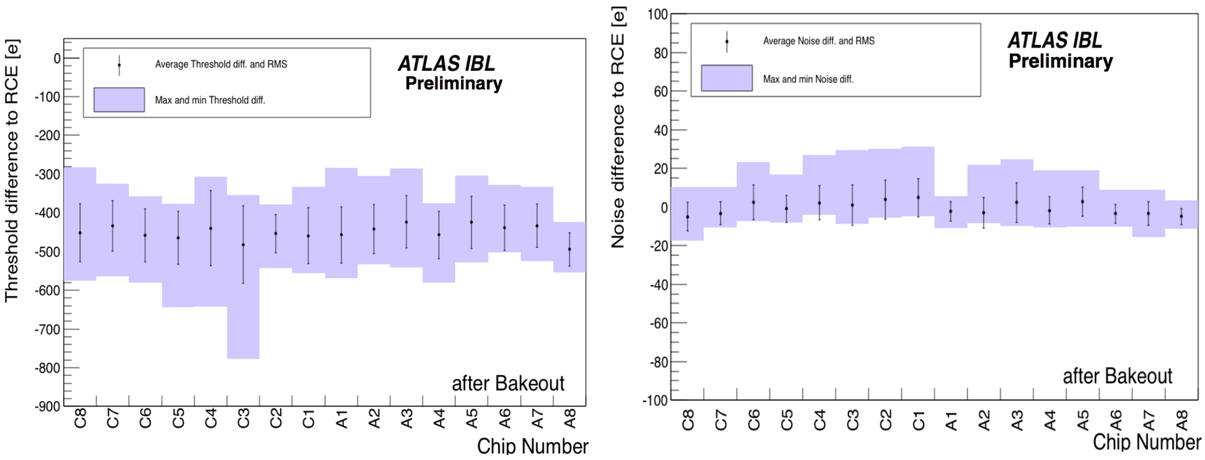


(a)

(b)

(c)

Figure 6.25: IV curves taken of all IBL modules after temperature drop for planar sensors (a), CNM sensors (b) and FBK sensors (c) after the beam pipe bake-out took place.



(a) (b)

Figure 6.26: Chip-to-chip Threshold (a) and noise (b) variation as difference to the RCE commissioning results among the 14 IBL production staves after loading a configuration with a target threshold of 3000 e and to a 10 ToT target response for 16000 e. The individual pixel data have first been averaged over each chip. The plots show, for each chip position on the stave, the mean and scatter of the 14 data points (one from each stave). The error bars show the RMS spread, while the solid boxes show the minimum and maximum values.

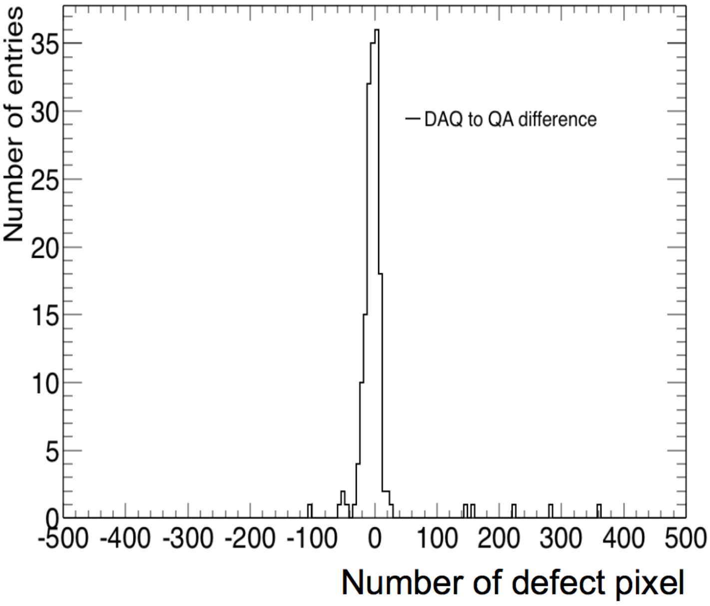


Figure 6.27: Difference in the number of defect pixels as obtained through threshold scans performed with HV on and off during QA and DAQ measurements after the beam pipe bakeout took place.

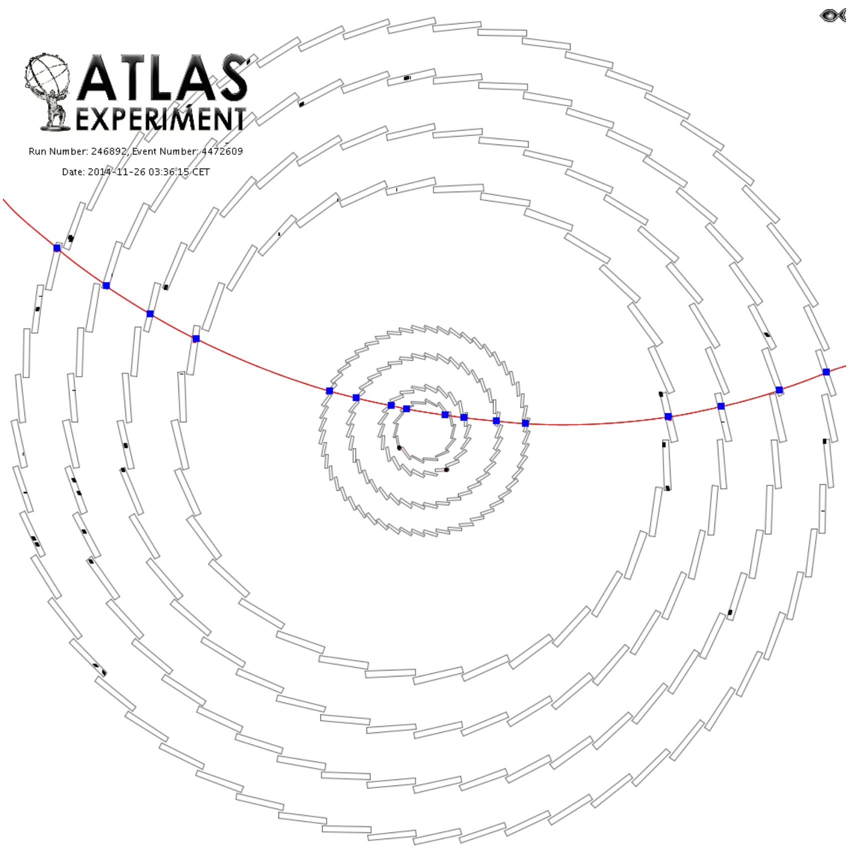


Figure 6.28: Atlantis event display of a cosmic ray event (number 4472609 from run 246892) with a cosmic ray passing through the newly installed IBL, the three layers of the pixel detector and four layers of the SCT detector. Modified version of [65].

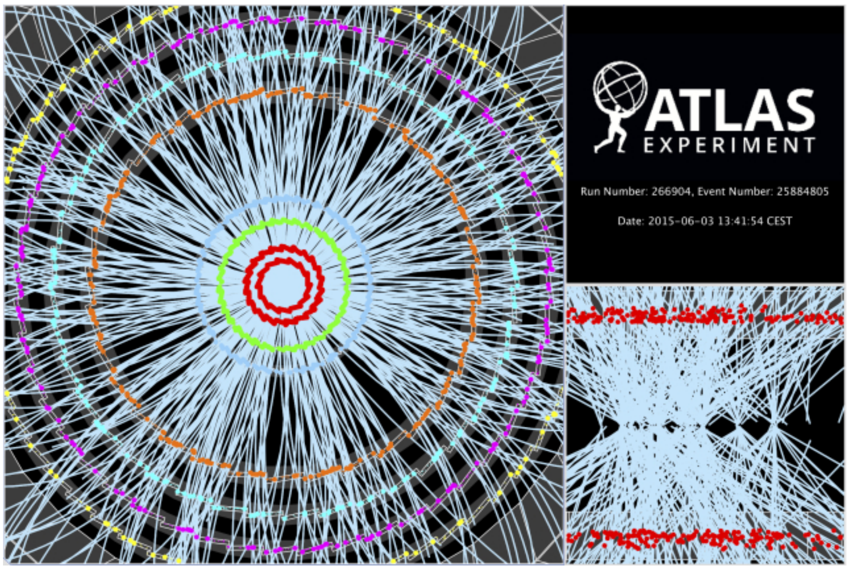


Figure 6.29: Event display of a collision event recorded by ATLAS on 3 June 2015 during the first run with stable proton-proton beams at a collision energy of 13 TeV [66].

Chapter 7

Low voltage leakage currents in FE-I4 read-out chips

The FE-I4 read-out chip of an IBL module contains around 80 million transistors that produce a leakage current which is dependent on the accumulated dose. During operation, the IBL read-out chips get irradiated when there is beam in the LHC and especially during collisions with high instantaneous luminosity. This chapter will describe the observations made during operation and present measurements which were performed in a laboratory to understand the observed behaviour. Parts of this chapter have also been published in Ref. [43].

7.1 Observations during operation

After the first months of IBL data-taking in the 2015 pp collision run at $\sqrt{s} = 13\,\text{TeV}$, a significant increase of the LV currents and a shift of the calibration parameters threshold and ToT was measured. The LV currents are read out for a module group of four front-end chips, meaning that the current of four single chips is summed up. Before exposure to beam, the LV current of a module group was around 1.6-1.7 A. The low voltage current for one module group and the calibration parameter shift are shown in Figures 7.1 and 7.2. To cope with the calibration parameter shift, the detector was re-tuned regularly in between fills to stay close to the target values. To protect the detector from damage due to the increasing currents, modules were switched off in case they reached a safety limit of 2.8 A. The complete IBL detector was switched off during one LHC fill due to safety concerns regarding the voltage transients on the supplying services. As it can be seen from Figure 7.1, switching off the detector and absence of beam resulted in a recovery of the current values due to annealing.

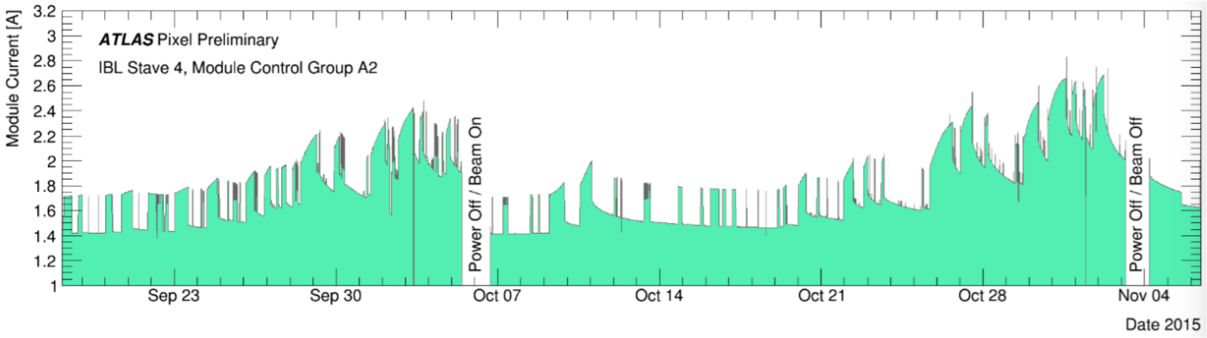
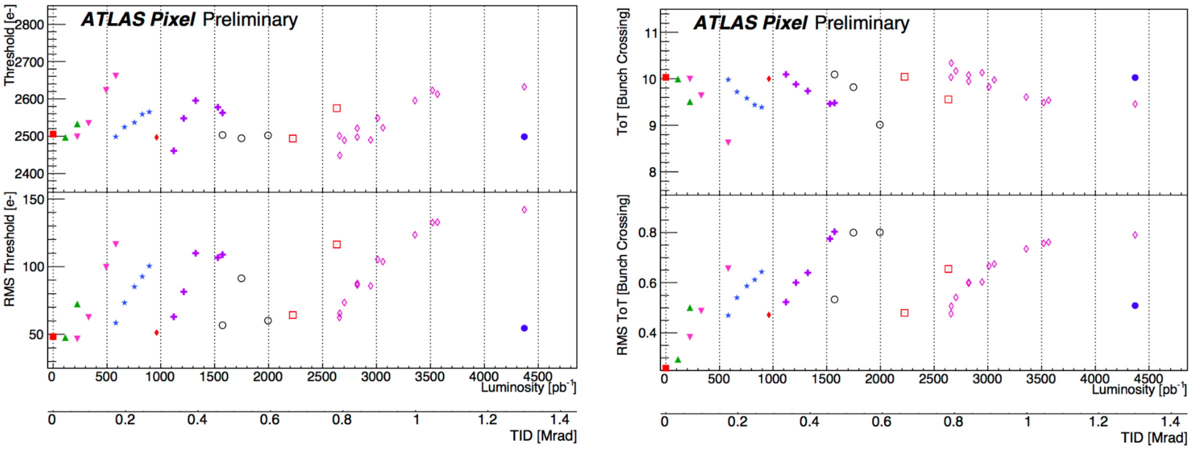


Figure 7.1: "An example of the low-voltage current drift of IBL modules from the middle of September until the beginning of November 2015. The module control group of Stave 4, A2 (4 front-ends) is shown for illustration. There are two levels of the current depending on the configuration of the front-end modules: STANDBY (lower level, not for data taking) and READY (higher level, for data taking). There are two long power-off periods on October 5-6 and November 3-4, plus a short power-off on October 3 and November 1." Figure and caption taken from [67].



(a)

(b)

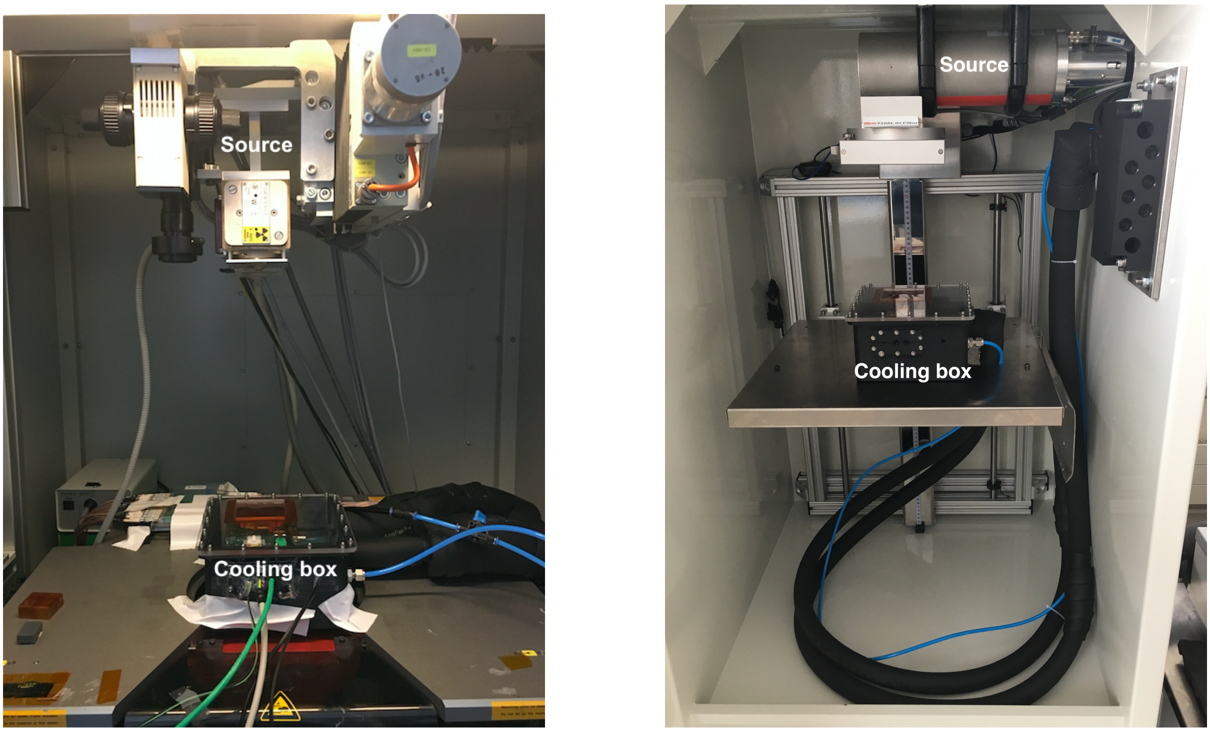
Figure 7.2: Evolution of the mean and RMS of the measured threshold (a) and ToT (b) values as a function of the integrated luminosity and the corresponding total ionising dose (TID) in 2015, as measured in calibration scans. The target values were 2500 electrons for the threshold and a ToT of 10 BC at 16k electrons. Each colour/symbol series corresponds to measurements taken after a re-tuning of the detector [68].

7.2 Setup of laboratory measurements

To quantify the dependency of the current increase on dose rate and temperature, several irradiation and electrical tests were performed. Since the temperature is the only parameter that can be controlled in the operation of the IBL, the main goal was to find a safe operation temperature that would not induce a current increase near the safety limit. For all measurements presented in this chapter, two different setups have been used. The first set of measurements has been carried out using a Seifert RP149 X-ray tube [69]. This X-ray tube is equipped with a tungsten target, sealed by a beryllium window of 0.25 mm thickness and can provide a peak energy of 10 keV. In addition, an aluminium filter of 0.15 mm is used to ensure a uniform dose rate in the front-end chip. The distance between the tube and the chip was set to 36 cm to achieve a dose rate of 120 krad/h and to 20 cm for a rate of 420 krad/h. The X-ray machine is periodically calibrated with a pre-calibrated diode. Occasionally, this calibration is cross-checked by using dosimetric films to verify the results. It was found that the dose rate can be given with an accuracy better than 20% [70].

A second set of measurements has been performed using an XRAD-iR-160 machine [71]. The machine has an adjustable shelf allowing a distance of source to shelf from 10 to 100 cm. The maximum applicable voltage is 160 kV and the maximum current 45 mA. For a dose rate of 120 krad/h the settings were 30 kV and 30 mA at a source to chip distance of 29.4 cm and for 10 krad/h the settings were 30 kV and 10 mA at a distance of 50 cm. An aluminium filter of 0.15 mm thickness is used in addition to a 0.8 mm beryllium window. A calibration of the machine was performed using the same diode as it has been used for calibrating the Seifert RP149 X-ray tube. Pictures of both setups are presented in Figure 7.3.

A sealed cooling box was designed to ensure a stable temperature during the measurements. A computer generated image of the design is presented in Figure 7.4. The box was flushed with dry air to prevent the formation of an ice layer on the chip. The front-end chip was powered using two Keithley 2410 devices.



(a) (b)

Figure 7.3: Seifert RP149 setup (a) and X-Rad iR160 setup (b).

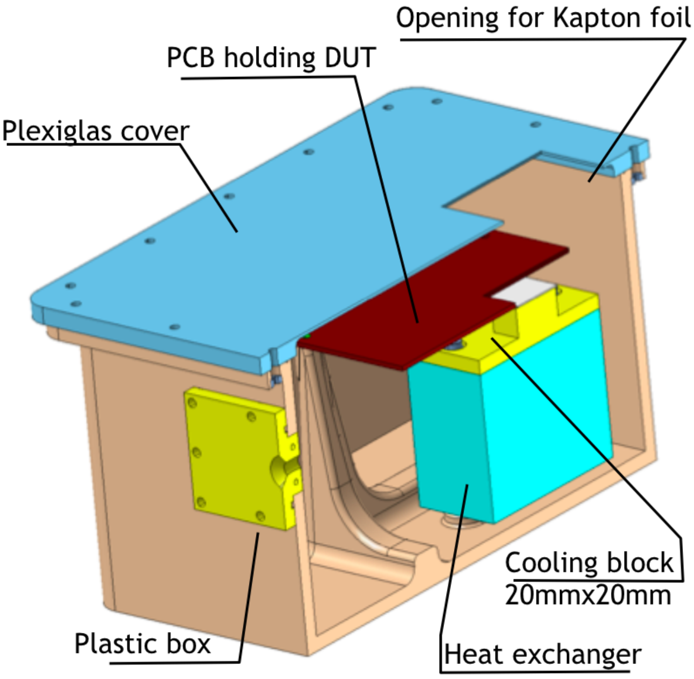
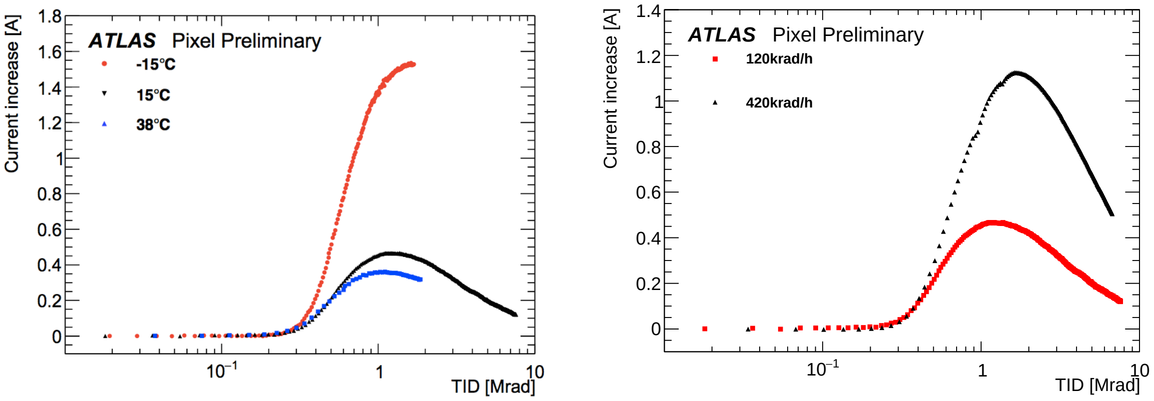


Figure 7.4: Computer generated image of a cooling box designed for temperature controlled measurements at different X-ray setups.

7.3 Measurement results

A first set of measurements was performed at a fixed dose rate of 120 krad/h for different temperatures to investigate the dependency of the current trend on temperature. The result is shown in Figure 7.5 (a). It can be observed that a higher temperature results in a lower current increase.



(a) (b)

Figure 7.5: LV current increase of single front-end chips in data taking mode as a function of the total ionising dose (TID) with a logarithmic x-axis scale. (a) Lab measurements carried out at 38°C (in blue), at +15°C (in black) and at −15°C (in red) with a dose rate of 120 krad/h. The LV current of a single front-end chip before irradiation was 400 mA (at 38°C), 360 mA (at 15°C) and 380 mA (at −15°C). (b) Lab measurements carried out at +15°C with a dose rate of 120 krad/h (in red) and 420/,krad/h (black). The LV current of a single front-end chip before irradiation was 380 mA (420 krad/h) and 360 mA (120 krad/h) [72].

The increase in the current trend can be explained by the quick trapping of positive charges in the STI oxide, opening a current path which results in an increased LV leakage current. The accumulation of interface traps along the STI partially compensates for the positive space charge in the thin silicon dioxide and therefore leads to a decrease of the current. Due to the fact that this is a slower process, the decrease only becomes visible after accumulating a certain amount of dose. The observation that a higher temperature results in a lower LV current increase, can be attributed to the faster formation of STI interface traps at higher temperatures. It was therefore decided to increase the IBL operation temperature from −5°C to +15°C, to get a resulting current increase which should stay well below the safety limits.

A second set of measurements was performed at a fixed temperature of +15°C with two different dose rates of 120 krad/h and 420 krad/h. It can be seen that a higher dose rate also results in a higher current increase.

In addition to measurements at different conditions, two irradiations were performed at the same dose rate and temperature to compare the behaviour of different chips under the same irradiation condition. The result, as presented in Figure 7.6, shows that both chips have a comparable current increase with a maximum current that only deviates by ∼6%.

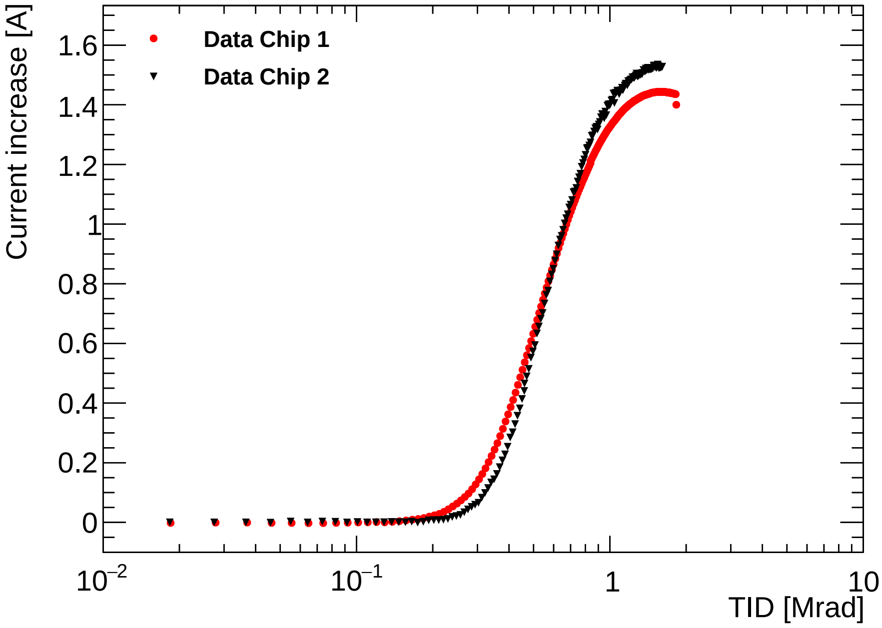


Figure 7.6: LV current increase of two single front-end chips in data taking mode as a function of the total ionising dose (TID) with a logarithmic x-axis scale. Laboratory measurements carried out at −15°C with a dose rate of 120 krad/h. The LV current of a single front-end chip before irradiation was 376 mA (Chip 1) and 380 mA (Chip 2).

In 2016, the IBL was expected to receive a higher dose rate due to increased luminosity while at the same time the module temperatures were raised by 20°C to cope with the increasing currents as explained before. To mimic the influence of these changes to the LV current increase, a two step measurement was performed where the dose rate was raised from 120 krad/h to 420 krad/h and the temperature was increased from −15°C to +5°C. The result presented in Figure 7.7 shows that with the expected higher luminosity and increased temperature, the current increase in 2016 is expected to be lower than in 2015 and should therefore not exceed the safety limit.

Due to the fact that a colder temperature is beneficial for the sensor performance, the feasibility of operating the IBL at a lower temperature had to be tested. Compared to the LHC dose rate of 10 krad/h expected to be received during operation in 2016/17, the dose rate of 120 krad/h was too high to give realistic results for the expected current increase of the IBL front-end chips. Therefore, a second set of measurements was performed at 10 krad/h and +5°C as well as 0°C. It is found that an operation temperature of +5°C results in a current increase of about 0.25 A, as shown in Figure 7.8. This would multiply to a current increase of 1 A for one IBL module group of four front-end chips, not exceeding the limits for safe operation. The

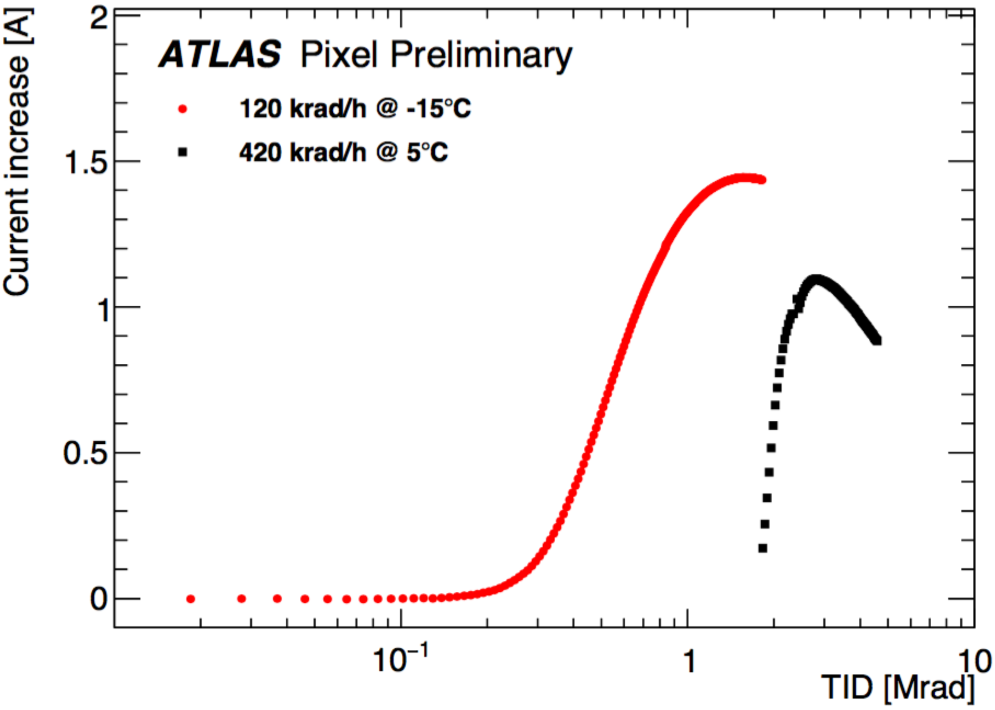


Figure 7.7: LV current increase of a single front-end chip in data taking mode as a function of the total ionising dose (TID) with a logarithmic x-axis scale. Laboratory measurements carried out at −15°C with a dose rate of 420 krad/h (in red) and at +5°C with a dose rate of 120 krad/h (in black) . The LV current of a single front-end chip before irradiation was 380 mA.

measurement at 0°C showed a current increase of up to 0.4 A, which would not fulfil the safety requirements. The result of this measurement is presented in Figure 7.9.

While for the temperature and dose rate comparisons the irradiation was made in one step, the irradiations presented in Figures 7.8 and 7.9 were performed stepwise to check the annealing behaviour at low temperatures and the impact of the rebound effect on consecutive current peaks. The LV current in both measurements reaches its first peak at around 1 Mrad. At this point the irradiation was stopped and the chips were annealed at the respective temperatures they were kept in during irradiation. For the +5°C measurement the annealing phase was 4.5 h with the beam being kept on and the chip powered off. For the 0°C measurement the chip was annealed for 27.3 h with beam switched off but chip powered, followed by the second annealing phase in the same configuration for 37.95 h. The results clearly show that annealing with beam on and the chip being powered off is faster. This coincides with the observations made during operation of the IBL, where a faster annealing was observed when the modules were powered off while there was beam in the LHC. It could also be observed that the maximum of each consecutive peak decreases as expected, since more interface traps are present in the silicon.

The last part of the current investigation was a study of the annealing at higher temperatures. One chip that had been irradiated with 420 krad/h at +15°C was annealed at +120°C for 120 h

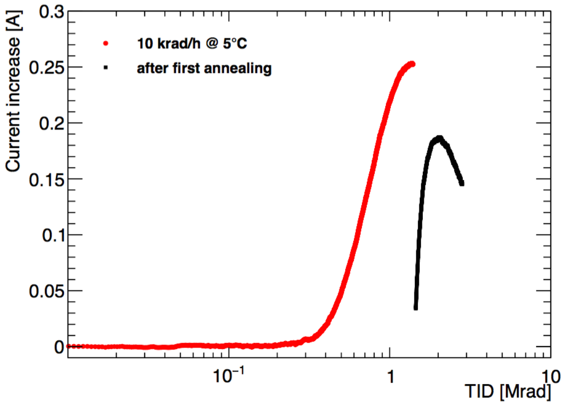


Figure 7.8: LV current increase of a single front-end chip in data taking mode as a function of the total ionising dose (TID) with a logarithmic x-axis scale during two consecutive irradiation campaigns. The temperature of the chip was kept at +5°C and the dose rate was 10 krad/h. Between the irradiation steps was a several hour annealing period, resulting in the observed recovery. The LV current of the front-end chip before irradiation was 376 mA.

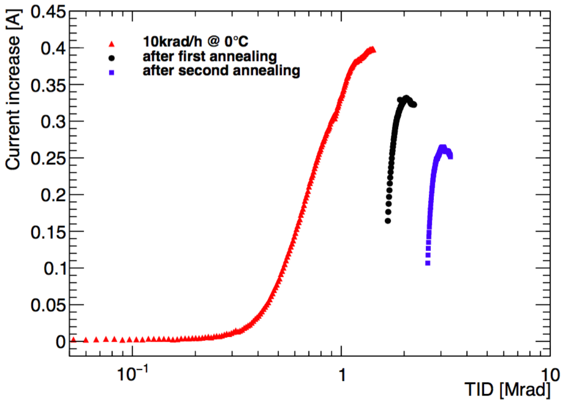


Figure 7.9: LV current increase of a single front-end chip in data taking mode as a function of the total ionising dose (TID) with a logarithmic x-axis scale during two consecutive irradiation campaigns. The temperature of the chip was kept at 0°C and the dose rate was 10 krad/h. Between the irradiation steps was a several hour annealing period, resulting in the observed recovery. The LV current of the front-end chip before irradiation was 385 mA.

and afterwards irradiated under the same conditions again. The result is presented in Figure 7.10. Even though the current went back to its pre-irradiation value, a complete annealing did not take place and the maximum current is lower than in the first irradiation. It is therefore assumed that the temperature and time was not sufficient to anneal all interface traps. To check if consecutive annealing steps result in comparable start parameters, a chip was annealed two times at +120°C for 120 h and afterwards irradiated at 0°C with 120 krad/h. As it can be seen in Figure 7.11, the current trend after both annealing steps is comparable with just small fluctuations.

In addition, the shift of the calibration parameters was investigated. In comparison to the current measurements, this turned out to be more difficult. The results obtained at 420 krad/h and 120 krad/h could not be used to find reliable conclusions about the tuning behaviour. During the irradiation, an increasing number of pixels showed failures in the analogue part, resulting in inconclusive scan results. To see how much percent of the chip is affected by this, the number of pixels showing deviating results from the expected value was plotted as obtained in analogue and digital scans. After consulting with the operations coordinator it was decided that a pixel is considered to be bad if the number it returns in a scan deviates more than 5% from the tuning value. As it can be seen from Figure 7.12, the number of analogue pixels that deviate from the tuning value increases significantly up to 2-3 Mrad and decreases again afterwards while the digital part seems not affected at all. It is assumed that this arises from a shift of the operation point of the amplifier chain. The analogue readout chain uses a charge sensitive

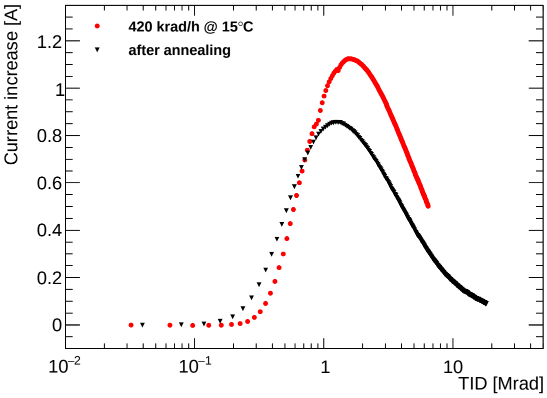


Figure 7.10: LV current increase of a single front-end chip in data taking mode as a function of the total ionising dose (TID) with a logarithmic x-axis scale. Laboratory measurements carried out at +15°C with a dose rate of 120 krad/h with a 120 h annealing period at +120°C in between. The LV current of the single front-end chip before irradiation was 376 mA (in red) and 380 mA (in black).

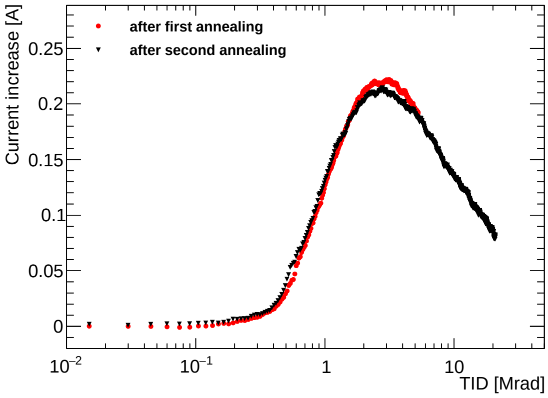
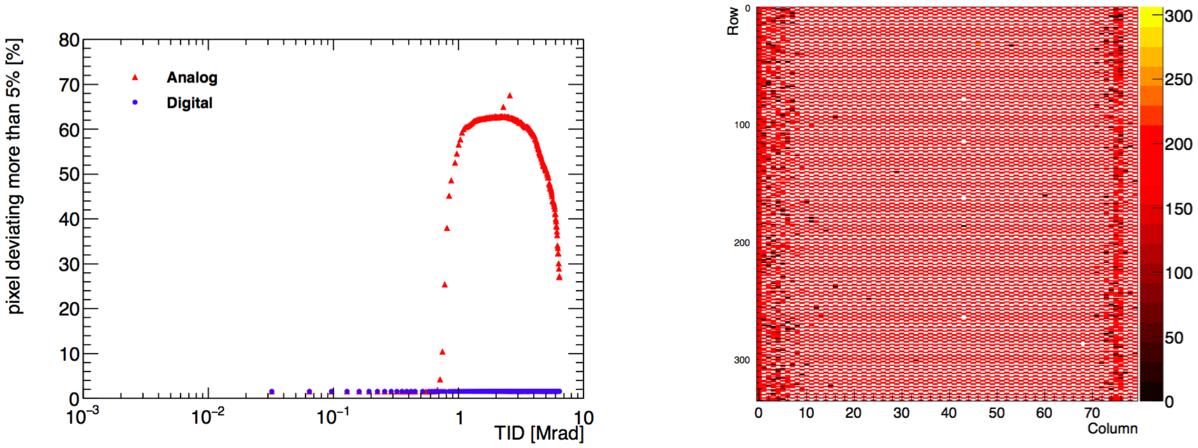


Figure 7.11: LV current increase of a single front-end chip in data taking mode as a function of the total ionising dose (TID) with a logarithmic x-axis scale. Laboratory measurements carried out at 0°C with a dose rate of 120 krad/h after a 120 h annealing period at +120°C before and in between. The LV current of the single front-end chip before irradiation and after annealing was 418 mA.

amplifier with a feedback circuitry as explained in chapter 5. In general, the analogue test tends to be less stable as it is more sensitive to different error sources [31]. With decreasing current, the operation point shifts back which could explain the decrease in the number of pixels failing the scan. When running the same test at a dose rate of 10 krad/h, this behaviour could not be observed since the current increase is too small. A failure of pixels was only observed after a current increase of more than 500 mA. Before irradiation around 1.5% of the pixels show a slight deviation from the expected value of 200 responses and as it can be seen in Figure 7.13, this percentage only increases by up to 0.03% which can be considered a normal fluctuation during operation.



(a) (b)

Figure 7.12: Percentage of pixels deviating by more than 5% of the expected 200 responses when performing an analogue and digital scan (a). Example of an occupancy map obtained in an analogue scan after irradiation with 120 krad/h to 2 Mrad (b).

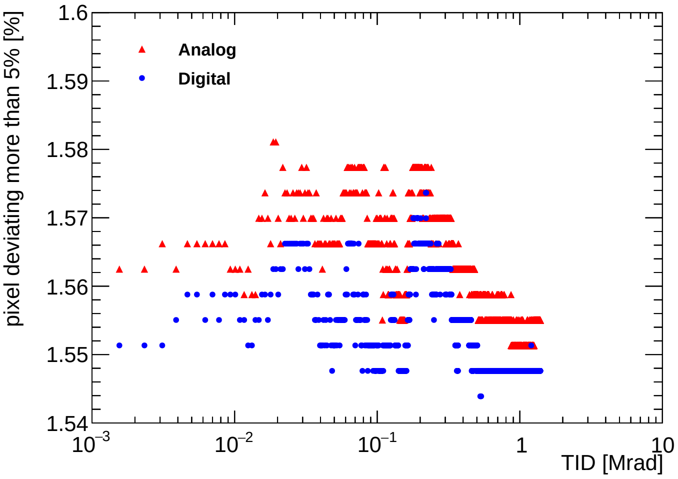
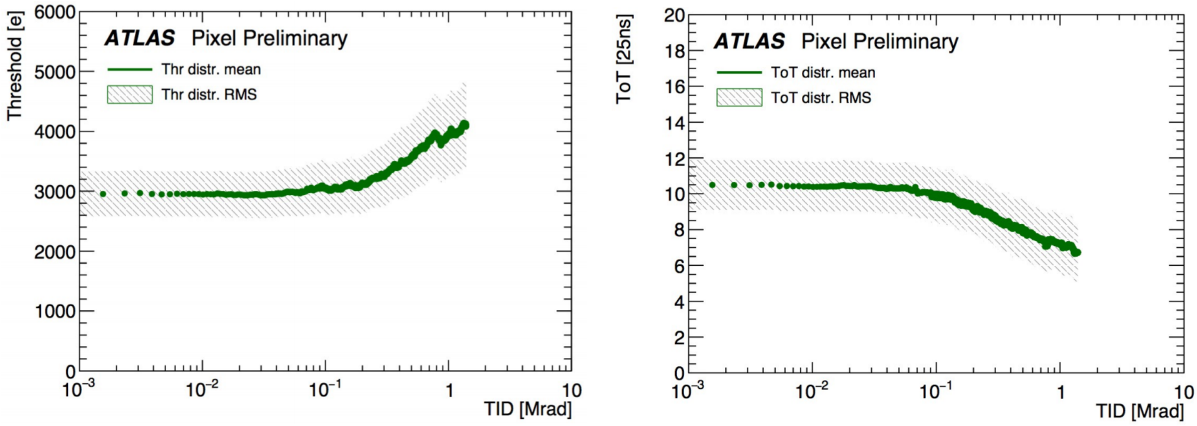


Figure 7.13: Percentage of pixels deviating by more than 5% of the expected 200 responses when performing an analogue and digital scan.

Since the chip behaviour at a low doserate seemed to be more reliable, the results of the threshold and ToT scan from the measurements at 10 krad/h were taken to check if the trend is comparable to what was seen during operation. A direct comparison of the shift was not possible, since the irradiations were carried out without retuning in between, while the IBL detector underwent regular retunings. The result of the measurement at 0°C is shown in Figure 7.14. The measured parameters follow the same trend as it was seen during operation and show continuous shifting. Due to this result a frequent retuning of the detector even after longer radiation exposure is recommended.



(a) (b)

Figure 7.14: Trend of the Threshold (a) and ToT (b) parameter shift of a single front-end chip in data taking condition as a function of the total ionising dose (TID). The temperature of the chip was 0°C and the dose rate was 10 krad/h [72].

7.4 Operation guidelines based on the measurement results

During the second half of 2015, an increase of the LV currents of the IBL modules was observed. This observation was of serious concern for the operation of the detector in 2016 due to the expected increase in peak luminosity. To ensure the safe operation of the IBL detector, the dependency of the current on TID and temperature was investigated in X-ray irradiations. The measurements confirm the hypothesis that the driving factor of the current increase is the radiation induced NMOS transistor leakage current. First measurements indicated, that a higher operation temperature would result in a lower current increase. It was therefore decided to raise the operation temperature from −5°C to +15°C. Further measurement performed at the expected maximum dose rate the LHC would deliver in 2016 indicated that safe operation of the IBL would be possible at a temperature of +5°C. During the next technical stop of the LHC, the IBL operation temperature was decreased to +5°C, following this results.

By mid 2016 the front-end chips of IBL accumulated around 9 Mrad of total dose and no further increase of the current is expected. It was therefore decided to operate the detector at a setpoint temperature of −20°C in 2017, which will result in module temperatures of around the design temperature of −15°C.

Chapter 8

New concepts for the ATLAS tracking system upgrade

When the LHC will be upgraded for its high luminosity operation, the complete tracking system of ATLAS will be replaced with a new tracker, referred to as ITk detector. This detector will consist only of silicon sensors. Especially for the outer layers, the price of producing modules is an important factor due to the large area that needs to be covered. The hybridisation via bump bonding is a costly procedure which makes up around 50% of production cost [73]. In addition, it introduces challenges when considering thinner sensors as they experience thermal bowing during the reflow process.

An idea to avoid the high temperatures needed for bump bonding and to provide a cheaper alternative is the connection of sensor and chip with a thin glue layer. The advantages of this method would be the easy and cheap availability of commercial epoxy glues, which have proven to be radiation hard and are curable at low temperatures which would avoid bowing of the modules. The signal transfer in that case would be realised by capacitive coupling through the glue. Since the signal in passive sensors is not artificially amplified, a very thin glue layer in the order of $10\,\mu$m needs to be applied. In addition, the alignment needs to be very precise with a placement accuracy in the order of a few micrometer. Another technology which makes use of glued assemblies is called HV-CMOS[1] [74]. This technology contains amplifiers that are embedded in the sensor and amplify the signal before it is transferred to the glue layer.

A study with glass plates used as dummies was carried out to find the best working glue and glue amount. After deciding for a glue, several flip chip machines were tested to achieve the best alignment precision possible. Dummy modules were produced with non-functional production sensors and front-end chips from the IBL production which were afterwards cut open to inspect the glue layer thickness and uniformity. Later on, a functional module was produced with the same procedure to check the feasibility of reading out the signal via capacitive coupling in source scans.

8.1 Gluing studies

One of the first ideas for applying a glue layer to the chip was tested for HV-CMOS prototypes, where epoxy-based lamination glue sheets were used. It was found that those sheets could not be bought in thicknesses that were sufficient and in addition the handling was rather difficult. It was therefore not considered as an option for the tests on planar sensors.

Instead, three different two-component epoxy glues were used for testing:

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[1] **H**igh **V**oltage CMOS

- Uhu Endfest 300
- Araldite 2011
- Araldite 2020

The first two glues were chosen because Araldite 2011 is already in use for the IBL detector and proved to be radiation hard and reliable [75] and Uhu Endfest 300 has very similar properties and was expected to show the same performance. Araldite 2020 was chosen due to its very low viscosity of 0.15 Pas compared to the higher viscosity of 30-45 Pas of Araldite 2011 [76] and Uhu Endfest 300 [77].

The tests were performed using 2x2 cm^2 glass sheets to mimic the sensor and chip and the glue was applied using a manual dispenser.

A simple setup was used where the glass sheets were aligned with a pick and place machine and pressure was applied by putting 3.16 kg of weight on top of the placer in form of lead blocks. A picture of the setup is presented in Figure 8.1.

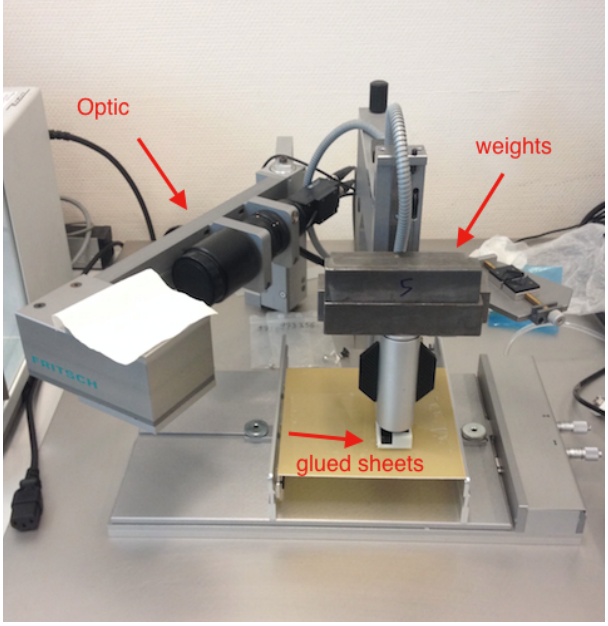
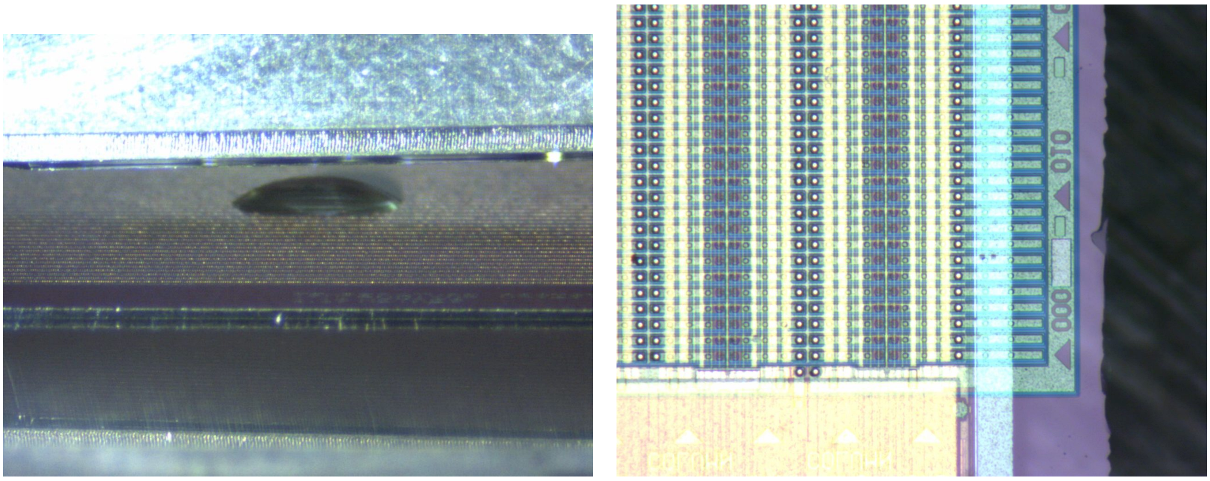


Figure 8.1: Setup used for gluing studies. Glass sheets were picked up using vacuum.

The tests with Araldite 2011 and Uhu Endfest 300 turned out to be not satisfying. Due to the higher viscosity, air bubbles got trapped inside the glue during the mixing of both components. This could be avoided using a vacuum chamber, but this was not tested since also the achievable thickness was not sufficient. In tests with different numbers of glue dots being applied to the glass sheet a minimal thickness of around 30 μm was reached. The best results were obtained when applying the glue in five parallel lines. Thereby, the glue layer thickness could be reduced to 20 μm, which was still thicker than the requirements demanded.



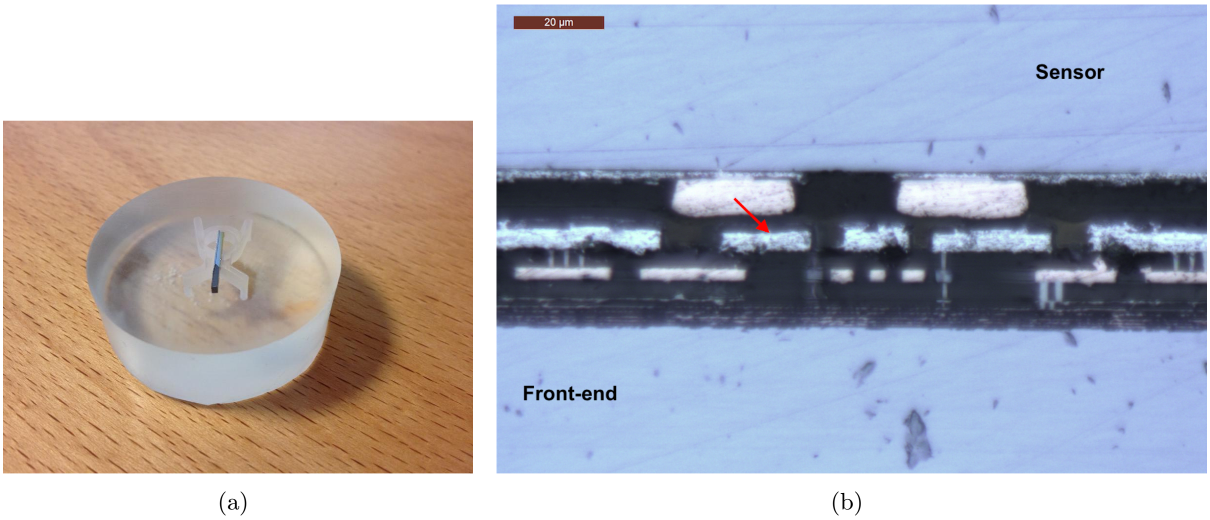
(a) (b)

Figure 8.2: Placement of a sensor on top of a front-end chip using a Fineplacer Pico machine.

Since most of the difficulties arose from the glue's viscosity, tests with Araldite 2020 were carried out. No air bubbles got entrapped when mixing the two components and due to the more liquid consistency of this glue, it was possible to apply just one glue dot to the middle of the glass sheet, put the second sheet on top and wait for the glue to spread due to capillary force. This way the glue distributed evenly over the whole surface, leading to good reproducibility of the results and a glue layer thickness of less than 10 μm. Different amounts of glue were tested to see down to which amount the glue would still spread over the complete area to achieve the thinnest layer. It was found that 2 mg of Araldite 2020 is the smallest amount of glue with which a complete coverage of the surface could be realised.

After deciding for a glue, different flip chip machines were tried out for assembling modules since they offer the possibility of having a precise alignment and controlled curing of the glue due to heaters. An initial test run was performed with a Fineplacer Pico [78]. Due to a limitation in the availability of sensors without UBM, this test was carried out with sensors that had UBM on them. Therefore, mainly the alignment was checked since the UBM acted as a kind of spacer which made it difficult to make reliable statements about the glue layer thickness. For later tests only sensors without UBM were used. The sensor and front-end chip was aligned optically by overlaying images of both parts and adjusting their position with micrometer screws. A picture of this is shown in Figure 8.2.

The glued assembly was afterwards brought to CERN were a cross-section was done. The assembly was cut into four pieces and each piece was embedded in a resin as shown in Figure 8.3(a). The surface got polished so pictures of the cross-section could be taken and the glue layer thickness and the alignment could be measured. The cross-section is presented in Figure 8.3(b). As it can be seen, the alignment precision reached is better than 10 μm. The data sheets of other commercially available flip-chip machines however, stated that an even better alignment precision



(a) (b)

Figure 8.3: Cut piece of a glued sensor/front-end assembly embedded in resin (a) and result of the cross-seciton (b). Misalignment indicated with red arrow.

should be feasible. A list of requirements was compiled and different vendors were approached to test their machines and check which one met the most of them. The requirements were:

- alignment precision as good as possible (preferably better than 10 μm)
- high zoom capabilities with good resolution as well as large field of view in minimum zoom
- possibility to move along x and y axis to check alignment over the whole surface
- possibility to use high force of up to 100 N for bigger modules and low force of less than 5 N for smaller prototypes
- controlled heating

Six different setups were tested and the best results were obtained with an Accura 100 machine [79]. Hereby, a uniform glue layer of about 5μm thickness could be achieved with an alignment precision better than 3μm.

As a next step a working module was assembled and tested at CERN. First IV curves were taken and compared to IV measurements done at the production site to see if the glue has a negative impact on the leakage current behaviour. The result is presented in Figure 8.4. No deterioration of the leakage current performance was found. A challenge for supplying the sensor with HV was given by the fact that no electrical contact to the bias grid was given due to the missing bump bonds. Therefore, the bias grid needed to be contacted from the backside of the sensor as it was the only reachable area. This was realised by placing a wirebond on a metal implant at the edge of the sensor which is connected to the cutting edge and therefore enabled a transfer of the HV via a punch through to the bias ring.

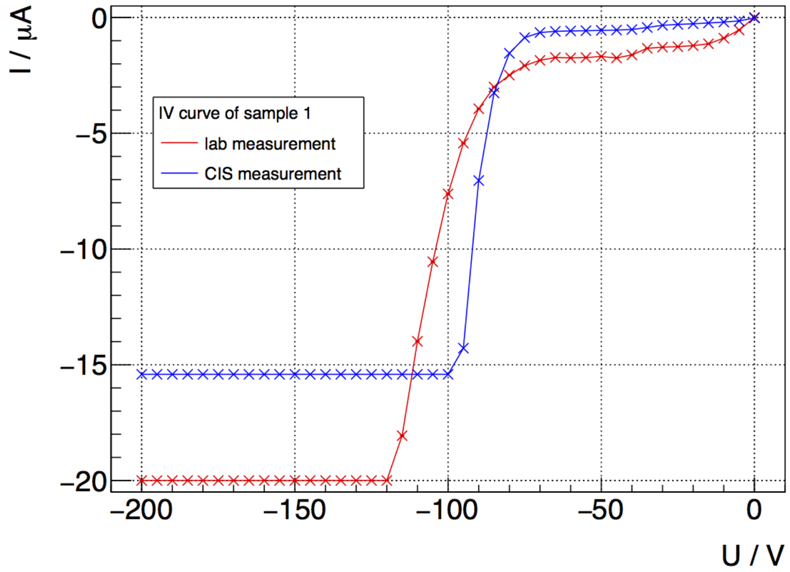


Figure 8.4: Comparison of IV curves taken at CIS (in blue) with the single sensor and after gluing the sensor to a front-end chip (in red).

After verifying the electrical functionality of the assembly, several tunings to different threshold values were performed, followed by source scans. Starting at 1500 e, each consecutive tuning aimed for a threshold of 100 e less. The lowest obtainable threshold was 600 e. The FE-I4 chip was designed to be operated at a threshold of 1500 e and reliable operation could be proven down to a threshold of 1000 e. This explains the wider distribution and less Gaussian shaped result of the threshold scan at 600 e. It should be noted, that the middle part of the chip contains more pixels with a higher threshold than the targeted value of 600 e.

To exclude the possibility of mistaking noise for actual hits, a 30h source scan was done beforehand with no source attached. The result of this scan is presented in Figure 8.6 (a). Only single hits were recorded during that time which could be identified as cosmic hits. It is therefore assumed, that all hits recorded with a ^{90}Sr source are actual hits. The result of an 11 h source scan with a threshold setting of 600 e is presented in Figure 8.6 (b).

Source scans obtained with tunings to thresholds higher than 600 e returned no or just very few hits, while a threshold of 600 e resulted in higher numbers of hits being measured, but only in a restricted area. It is assumed that the circular shape of the area where hits were recorded can be traced back to incomplete spreading of the glue. The result of the source scan indicates that the glue only covers part of the module and in addition did not spread homogeneously. It can be assumed that the glue layer thickness is thinner in the ring shaped area at the outer part of the connected region where thus more hits were recorded. In addition the threshold scan showed an increased number of pixels with higher threshold values especially in the middle part of the chip, which would also result in less hits being recorded in this region.

With the FE-I4 chips, reliable operation is possible down to thresholds of around 1000 e

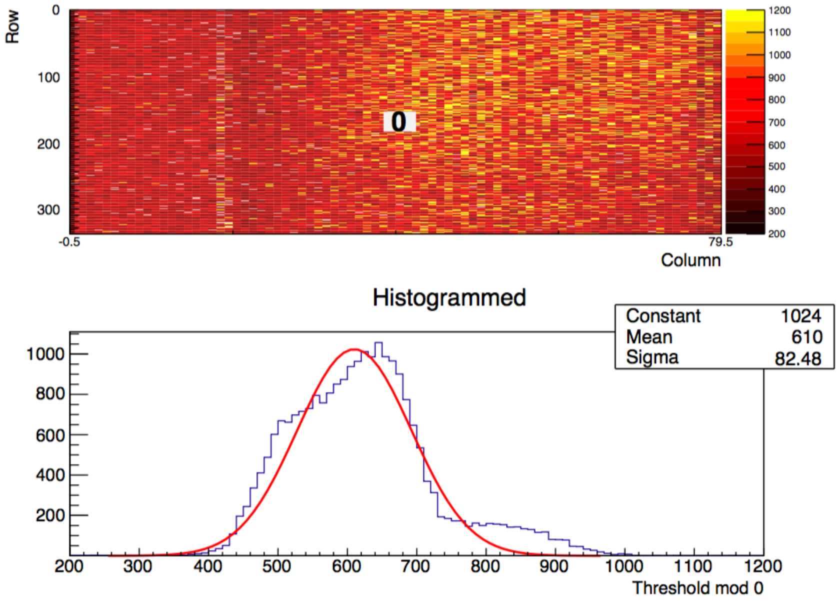
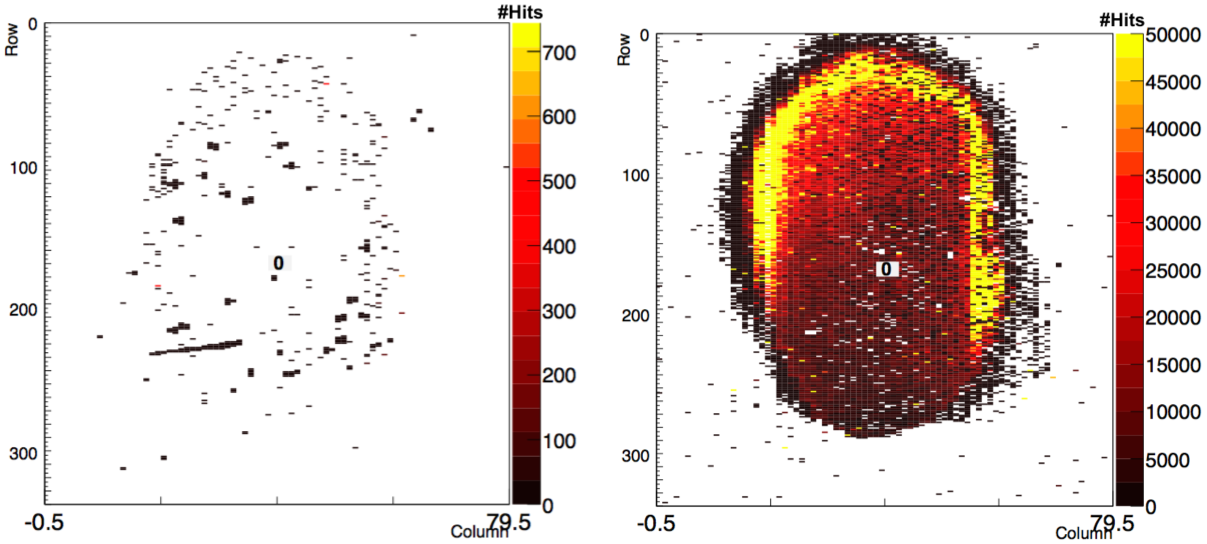


Figure 8.5: Threshold scan after attempted tuning to 600 e.

while operation down to a lower threshold of 600 e is under investigation with prototypes of a new read-out chip [4]. Since the results of the source scan showed however, that it would be inevitable to achieve this lower threshold uniformly for the full chip to be able to detect any hits, it was decided that at this point no further testing will be spend on passive planar sensors in combination with the FE-I4 chip, as their signal strength turned out to be not sufficient for the proper usage of capacitive coupling as a transfer technique for this case. However, the experience gathered with respect to gluing of larger areas in the order of 4 cm^2 will still be used to assemble modules with sensors containing amplifiers as the before mentioned HV-CMOS technology.



(a)

(b)

Figure 8.6: Result of source scans with a threshold setting of 600 e. Scan taken for 30 h w/o a source (a) and for 11 h w/ a ^{90}Sr source (b).

Chapter 9

Conclusions

The innermost part of the ATLAS tracking system, the pixel detector, has been upgraded with a new fourth layer during the long shutdown 1 of the LHC. This new layer, the Insertable B-Layer, consists of 14 staves that have been selected after quality assurance measurements performed on 20 produced staves. The IBL was installed in ATLAS in 2014 and is providing an extra space point for tracking since the LHC started operation again with 6.5 TeV proton-proton collisions in 2015.

This thesis presented the selection process of the IBL staves which was followed by a system test performed on two staves to verify the functionality of the setup for the final IBL construction. For the system test, the setup's electrical functionality was tested first with a dummy load to prevent damage to the staves. After verifying the functionality of the service chain, two staves were mounted and tested with respect to their calibration capability and readout performance. Only production components were used as well as the designated cooling system to achieve results as close as possible to the operation conditions. It could be proven that the setup was fully functional, which was essential to know before the construction of the IBL detector could take place.

Each stave was tested after installation around the inner positioning tube and retested after its neighbour got installed. All staves were successfully tested and it was verified that the entire detector was performing as expected. It could therefore be stated that no damage occurred to the staves during the construction of the IBL.

In May 2014 the IBL was installed in ATLAS. A thorough commissioning took place after installation to ensure that no damage was caused by the transport from the clean room to the ATLAS access shaft or during installation in the experiment. The measurements used to verify the electrical integrity as well as calibration measurements to check the performance of the modules were repeated two times after the detector had been exposed to thermal stress, namely a sudden temperature drop to -35°C and the beam pipe bake-out.

It could be shown that all modules were performing as expected as well as the service and readout chain. The commissioning of the detector successfully proved the full functionality of IBL and gave important reference data for the operation of the detector.

During the first year of operation an increase of the LV currents of the IBL modules was observed. This was a serious issue for operation and data efficiency, as modules had to be switched off when their current approached a safety limit and the whole detector was switched off for one LHC fill due to safety concerns.

The dependency of the LV current on TID and temperature was investigated in dedicated measurements and it could be shown that the increase arose from an increase of leakage current in the NMOS transistors of the readout chip.

Measurements under conditions comparable to the expected conditions during operation showed that safe operation of the IBL detector would be possible at a temperature of +5°C. It could also be shown that after accumulating a TID of around 10 Mrad, no further significant increase is expected which lead to the decision of operating the IBL at its design temperature of −15°C from 2017 on.

The complete tracking system of ATLAS will be replaced during the long shutdown 3. The new tracker will be made up completely of silicon modules. Since hybridisation accounts for up to 50% of the module production cost, a new hybridisation technique was investigated. The last part of this thesis summarised the results obtained with glued assemblies consisting of a passiv planar sensor and a FE-I4 readout chip. It was shown that a readout via capacitive coupling is not feasible with this technology but that the techniques investigated for achieving glue layers in the order of a few μm over larger areas could successfully be developed and will be used for technologies as for example HV-CMOS sensors in the future.

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