Single-Trap Phenomena in Nanowire Biosensors

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Dedicated to my beloved wife and family

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ABSTRACT

Single-trap phenomena (STP) in nanoscale transistor devices possess outstanding properties that are promising for many useful and important applications including information technologies and biosensing. In this thesis, a novel biosensing approach based on monitoring of STP parameters as a function of target biomolecules on the surface of liquid-gated (LG) silicon (Si) nanowire (NW) field-effect transistor (FET) biosensors was proposed and demonstrated. To enhance STP dynamics and improve the efficiency of the approach, unique two-layer (TL) NW FETs with NW channels consisting of two Si layers with different concentrations of dopants were designed and fabricated. A stable and leakage-free operation in liquid confirms the high quality of TL NW devices. At the same time, fabricated TL nanostructures are conceptually different from the conventional uniformly doped Si NWs and demonstrate more statistically pronounced STP with considerably stronger capture time dependencies on drain current compared to that predicted by classical Shockley-Read-Hall theory. A comprehensive analysis of the experimental data measured at low temperatures allowed the identification of the origin of single traps in TL NWs as a vacancy-boron complex. Several important effects enabling the advancement of sensing capabilities of STP-based devices were revealed using fabricated TL NW FET biosensors. First, a significant effect of channel doping on the quantum tunneling dynamics of charge carriers to/from a single trap was registered in TL nanostructures, analyzed, and explained within the framework of proposed analytical model. Second, a distinct fine-tuning effect of STP parameters by applying a back-gate potential to LG TL NW FETs was experimentally revealed and supported by numerical simulations. Such a unique feature of STP in TL NWs allows the sensitivity of STP-based biosensors to be enhanced in a well-controllable way. Furthermore, STP in NW FETs offer a great opportunity for the suppression of low-frequency noise. Considering a trap occupancy probability (g-factor) as a signal, a new method for the estimation of g-factor noise was proposed and utilized. As a result, the effective suppression of the low-frequency noise even beyond the thermal noise limit was experimentally and numerically demonstrated. The derived analytical model showed an excellent agreement with the obtained results underlining the importance of STP for biosensing applications. Utilizing the unique advantages of STP in fabricated TL NW FET biosensors, several proof-of-concept applications including high-sensitive detection of target chemical and biological analytes: mono- and divalent ions, ascorbate molecules, and amyloid-beta peptides were demonstrated. Thus, the performed experiments together with the developed analytical models represent a major advance in the field of biosensors and pave the way for the next generation of novel ultrasensitive bioelectronic sensors exploiting single-trap phenomena.

ZUSAMMENFASSUNG

Ein-Fallen-Phänomene (STP) in nanoskaligen Transistor-Bauelemente besitzen herausragende Eigenschaften, die für viele nützliche und wichtige Anwendungen, einschließlich der Informationstechnologien und Biosensorik, vielversprechend sind. In dieser Doktorarbeit wurde ein neuartiger Biosensor-Ansatz vorgeschlagen und demonstriert, der auf der Überwachung von STP-Parametern als Funktion von Ziel Biomolekülen auf der Oberfläche von flüssigkeitsgesteuerten (LG) Silizium (Si) Nanodraht (NW) Feldeffekttransistor (FET) Biosensoren basiert. Um die STP-Dynamik zu erhöhen und die Effizienz des vorgeschlagenen Ansatzes zu verbessern, wurden einzigartige zweischichtige (TL) NW FETs mit NW-Kanälen, die aus zwei Siliziumschichten mit unterschiedlichen Konzentrationen von Dotierstoffen bestehen, entworfen und hergestellt. Ein stabiler und leckfreier Betrieb in einer Flüssigkeit bestätigt die hohe Qualität der TL-NW-Bauelemente. Gleichzeitig unterscheiden sich die hergestellten TL Nanostrukturen konzeptionell von den konventionellen, gleichmäßig dotierten Si-NWs und zeigen, im Vergleich zur Vorhersage der klassische Shockley-Read-Hall-Theorie, statistisch ausgeprägtere STP mit wesentlich stärkeren Einfangzeitabhängigkeiten vom Drainstrom. Eine umfassende Analyse der experimentellen Daten, die bei tiefen Temperaturen aufgenommen/vermessen wurden, ermöglichte die Identifizierung des Ursprungs der einzelnen Fallen in den hergestellten TL NWs als einen Leerstellen-Bor-Komplex. Anhand der hergestellten TL NW FET Biosensoren wurden mehrere wichtige Effekte aufgedeckt, die eine Verbesserung der Sensorfähigkeiten von STP-basierten Bauelementen ermöglichen. Erstens wurde ein signifikanter Effekt der Kanaldotierung auf die Quantentunneldynamik von Ladungsträgern zu/von einer einzelnen Falle in TL-Nanostrukturen registriert, analysiert und im Rahmen des vorgeschlagenen analytischen Modells erklärt. Zweitens wurde ein ausgeprägter Feinabstimmungseffekt der STP-Parameter durch Anwendung eines Back-Gate-Potentials auf die LG TL NW FETs experimentell aufgedeckt und durch numerische Simulationen unterstützt. Diese einzigartige Eigenschaft von STP in TL NWs ermöglicht es, die Empfindlichkeit der STP-basierten Biosensoren auf eine gut kontrollierbare Weise zu verbessern. Darüber hinaus bieten STP in NW-FET-Bauelementen eine große Chance für die Unterdrückung des niederfrequenten Rauschens. Unter Berücksichtigung einer Trap Belegungswahrscheinlichkeit (g-Faktor) als Signal wurde eine neue Methode zur Abschätzung des g-Faktor-Rauschens vorgeschlagen und angewandt. Als Ergebnis wurde die effektive Unterdrückung des tieffrequenten Rauschens auch jenseits des thermischen Rauschgrenzpegels experimentell und numerisch nachgewiesen. Das abgeleitete analytische Modell zeigte eine hervorragende Übereinstimmung mit den Ergebnissen und unterstrich die Bedeutung von STP für Biosensorik-Anwendungen. Unter Ausnutzung der einzigartigen Vorteile von STP in den hergestellten TL-NW-FET-Biosensoren wurden mehrere Proof-of-Concept-Anwendungen einschließlich hochempfindlicher Detektion von chemischen und

biologischen Zielanalyten demonstriert: mono- und divalente Ionen, Ascorbatmoleküle und Amyloid-beta-Peptide. Somit stellen die durchgeführten Experimente zusammen mit den entwickelten analytischen Modellen einen großen Fortschritt auf dem Gebiet der Biosensoren dar und ebnen den Weg für die nächste Generation neuartiger, ultrasensitiver bioelektronischer Sensoren, die Ein-Fallen-Phänomene nutzen.

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INTRODUCTION

“When a sensory device approaches its sensitivity limit, one has to start thinking and care about noise.”

Prof. Dr. Peter Handel

“The game of science has different rules when you play at the nanoscale.”

Dr. Noushin Nasiri

Over the past few decades, significant research efforts have been devoted to developing new medicines and diagnostic tools that make patient’s diagnosis and treatment faster and more effective. In this regard, however, the early detection of a disease is probably the most efficient way to increase the chances of a successful recovery. Although research on new strategies for early diagnosis is still ongoing, it has been revealed that the detection and monitoring of some specific molecules known as biomarkers provide a unique opportunity to detect and identify disease at its early stages, which helps clinicians to make an early decision about a required therapy intervention. To better recognize a disease and thus increase confidence in treatment decisions, a mixture of biomarkers usually needs to be detected and analyzed with high accuracy and sensitivity.

The human body has a variety of molecules that can be used as biomarkers. Some of them indicate different biological processes that are normally happening in a healthy body. However, the presence of some definite biomarkers in body fluids indicates processes related to a certain disease. For instance, when heart cells are damaged, some specific proteins and enzymes are released into the bloodstream (see Figure 1.1). The key ones are cardiac troponin I (cTnI), cardiac troponin T (cTnT), and creatine kinase M and B [1]. These biomarkers are commonly used to detect and identify cardiovascular diseases [1–3]. Another example is C-reactive protein (CRP) molecules which are synthesized in a human body in response to inflammation. Interestingly, several reports also demonstrate that the elevated concentration of C-reactive protein (CRP) molecules in blood can be considered as an independent factor to evaluate the risk of developing heart problems [4–6]. Besides, biomarkers play a vital role in the detection of cancer and its treatment. In particular, the detection of mutations in genes of tumor cells helps doctors to identify a particular type of cancer and therefore target a specific way to defeat a severe cancer disease more effectively. Amyloid-beta ($A\beta$) plaques and tau tangle pathology are further examples of useful biomarkers. The presence of these molecular species is a direct and reliable hallmark of neurodegeneration processes leading to neurodegenerative disorders such as Parkinson's disease or Alzheimer's disease [7–9]. Therefore, the early detection and monitoring of various biomarkers under physiological conditions is of paramount importance to saving many lives of patients.

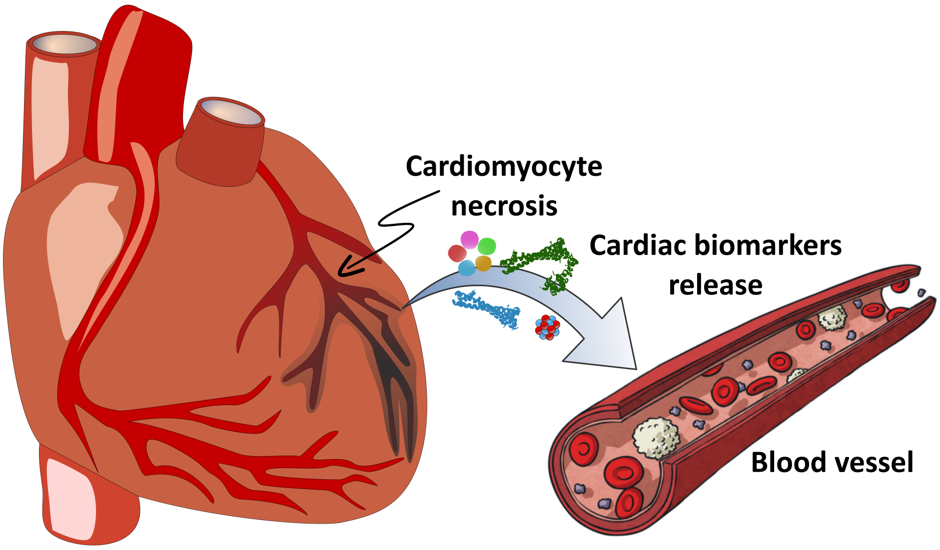

Figure 1.1: Release of cardiac biomarkers from damaged cardiac cells into a blood vessel after myocardial injury (schematically).

Up to now, many methods and techniques have been developed and tested for the detection and continuous monitoring of disease biomarkers. Among them, an enzyme-linked immunosorbent assay (ELISA) is the most commonly used technique. The assay provides both high sensitivity and selectivity to the target biomolecules. However, it still has several drawbacks and limitations which significantly impacts the effectiveness of such a tool for clinical practice and medical applications. In particular, ELISA is a sophisticated and expensive tool that is usually operated by a well-trained person. Furthermore, the assay involves biomarker labeling and preparation of reagents which makes the technique time-consuming and labor-dependent. Such requirements substantially challenge the use of the tool for medical applications, especially in case of emergencies. Therefore, the development of a high-efficient, compact, and high-performance diagnostic tool capable of real-time, high-speed, and highly sensitive detection and monitoring of disease biomarkers is of extreme importance. These devices are ones that have yet to be developed. In this perspective, biochemical sensors (biosensors) based on field-effect transistors (FETs) are widely considered promising devices to be employed as complete diagnostic tools that provide highly efficient healthcare monitoring and disease diagnosis even at early stages when biomarkers exist at very low concentrations. Typically, these devices are performed as classical ion-sensitive field-effect transistors (ISFETs) in which the active transducer element is covered with a functional bio-recognition layer to provide an exclusive selectivity and specificity to the biological analyte of interest [10].

Nowadays, researchers involve various materials and technologies to develop biosensors that could be high-speed, reliable, and extraordinarily sensitive. In particular, with the introduction of novel nanopatterning methods and discovery of new nanomaterials such as graphene, carbon nanotubes, and other low-dimensional materials, a new generation of high-sensitive nanoscale FET-based sensors has been established [11, 12]. Among them, silicon (Si) nanowires (NWs) configured as liquid-gated (LG) FETs demonstrate a tremendous potential to yield highly integrated state-of-the-art biosensors. Owing to their remarkable features such as tunable electrical properties, high surface-to-volume ratio, biocompatibility, and exceptional scalability, Si NWs are promising transducer elements that can effectively convert biological or chemical reactions into a detectable electrical signal. Also, what is more important, the sensing principle of such devices is based on the label-free approach which allows direct monitoring of biorecognition processes between receptors and target biomolecules. Furthermore, being a modern nanoscale version of classical metal-oxide-semiconductor FETs (MOSFETs) [10], Si NW FETs can be fabricated using the well-established complementary metal-oxide-semiconductor (CMOS)-compatible technology. This feature makes the Si NW devices cost-effective in production and allows them to be easily integrated into a complete diagnostic chip. Therefore, LG Si NW FETs are excellent candidates for the development of novel label-free, cost-efficient, and high-performance biosensors capable of rapid, precise, and highly sensitive detection of target bio-species such as disease biomarkers.

Although many promising results using transistor-based biosensors have been achieved so far, the sensing performance of such devices is still critically influenced by the noise quality of the transducer elements [12–14]. The electrical noise plays an important role in any type of sensors determining their capability to detect small signals coming from the target analyte. Therefore, careful consideration and understanding of noise in the aforementioned devices is a key approach to develop indeed reliable and highly sensitive biosensor platform. Typically, the physical sources of noise in large-area FETs originate from the fluctuations of microscopic entities, such as mobility or number of charge carriers due to their interactions with different traps randomly distributed in a gate insulator layer of underlying transistors [15]. However, such noise mechanisms and models become irrelevant for small devices in which the electrical noise becomes single-carrier phenomena. In particular, the number of electrically active traps substantially decreases as device dimensions shrink. In this perspective, if the trap number is reduced to a single trap, a strong modulation of a nanoscale transistor conductance appears as **single-trap phenomena (STP)**, resulting in two-level discretized electrical fluctuations known as random telegraph signal (RTS) noise. Such an RTS effect in nanoscale electronic devices is usually avoided as it increases the noise level affecting their performance and reliability. However, due to the discrete nature of the phenomenon and its outstanding properties, the use of STP is expected to contribute the real benefits and advancements to future ultimate nano- and biotechnologies.

In this thesis, we have intensively worked towards the understanding of STP in liquid-gated NW FETs as novel and extremely sensitive effects to be exploited for biosensing applications. In contrast to the traditional view of RTS noise as a result of STP in nanoscale devices, we propose and define here a new class of biosensors that use this effect as the information-carrying signal. Unlike usual transistor-based biosensors, where the shift of threshold voltage or drain current is the signal and voltage fluctuations are the noise, we suggest using STP in LG NW FETs as a novel transducer principle enabling to enhance the sensitivity and performance of nanoscale biosensors. Moreover, we reveal and demonstrate making the analogy with the stochastic resonance effect found in biological systems that the exploitation of STP in nanosensors allows the low-frequency (LF) noise in such devices to be suppressed even beyond the thermal limit level. The obtained experimental and analytical results confirm the advantages and efficiency of the proposed STP-based approach for biosensing applications.

This thesis is organized as follows. In **Chapter 2**, we present a brief overview of the main state-of-the-art biosensing techniques and approaches currently used for the sensing of different kinds of biomarkers. We focus more specifically on the detection and operation principles of transistor-based biosensors as ideal candidates to be exploited for point-of-care testing and other medical applications. We outline the main advantages and challenges of such devices and provide the necessary theoretical background on fluctuation phenomena with an emphasis on STP in nanoscale transistors as a unique opportunity to advance the performance of nanotransistor-based biosensors. Measurement setups and data analysis methods used in this thesis are described in **Chapter 3**. In **Chapter 4**, we describe a fabrication process of the specially designed two-layer nanowire FETs with different concentrations of dopants in the channel and investigate the transport and noise properties of the fabricated nanostructures. The registered RTS noise with enhanced capture dynamics in highly doped LG nanostructures is analyzed and considered for the application in biosensing. The effect of tuning of capture time by applying a back-gate potential to the TL NW structures is revealed and discussed also in this chapter. The potential of STP for noise suppression is shown in **Chapter 5**. We demonstrate experimentally, numerically, and analytically that the signal-to-noise ratio of the biosensors exploiting STP can be beyond that of trap-free devices. Finally, the full potential of the STP approach for biosensing is demonstrated in **Chapter 6** which presents the experimental results on real-time, label-free, and highly sensitive detection of ions and target biomarkers as a proof of concept. Relevant parameters and results achieved are briefly summarised after each chapter. The final remarks, conclusions, and outlook are presented at the end of this thesis. We believe that the novel biosensing strategy developed and defined in this thesis can revolutionize the current approach and push the limits of FET-based biosensors towards biomolecular detection even at a single-molecule sensitivity level that would make medical diagnoses and healthcare monitoring more reliable and efficient.

THEORETICAL BACKGROUND AND MAIN CONCEPTS

2.1 Biosensors for health applications: main challenges and parameters

A new era of biotechnology and personalized medicine is developing very quickly nowadays. Due to the progress in biomarker technology, it becomes possible to deliver personalized medical care to a patient based on his/her unique biomarker expression profile. Such an individual approach improves the quality of health care and thus maximizes the patient's benefit. Therefore, the research is focused now on developing biosensing platforms that allow the relevant biomarkers to be detected and identified in the best possible way to assist successful treatment and recovery of patients. In this perspective, various diagnostic techniques and strategies have been developed and adopted for the detection of biomarkers so far. This includes techniques based colorimetric, paramagnetic, fluorescence, electrochemical, and surface plasmon resonance approaches (see Figure 2.1). However, despite huge advancements and significant success in the detection of target biomarkers in the last decade, there remain many obstacles affecting the real practical application of the biosensors. In general, the ideal biosensing device is the right combination of sensitivity, selectivity, speed, and price. All these features need to be combined in the right balance to facilitate a disease treatment and consequent clinical benefit.

At present, most of the classical methods for the detection of biomarkers are based on an enzyme-linked immunosorbent assay (ELISA) technique. ELISA is a plate-based assay method developed for detecting and quantifying different bio-species such as peptides, proteins, antibodies, and hormones. The detection strategy of ELISA tests is based on a highly specific antibody-antigen interaction and employs the effect of enzyme-labeling of antigens or antibodies as a marker for the specific detection of target proteins. Spectrophotometer, fluorometer, or luminometer instrumentations are typically then used for signal detection. Several variations of ELISA have been developed nowadays allowing qualitative detection or quantitative measurement of either target antigen or antibody species. The main four of them are direct, indirect, sandwich, or competitive ELISAs (see Figure 2.2) depending on the antigen immobilization protocol, the detection method of the immobilized antigen, and the number of antibodies used. For example, the difference in a direct vs indirect ELISA comes from the detection method of the immobilized antigen on the microplate surface. The direct ELISA uses a conjugated primary antibody, while indirect ELISA additionally involves the secondary antibody to quantify the primary antibody. This allows better sensitivity and selectivity to be achieved, however, results in longer detection time due to the extra step and increases the risk of cross-reactivity.

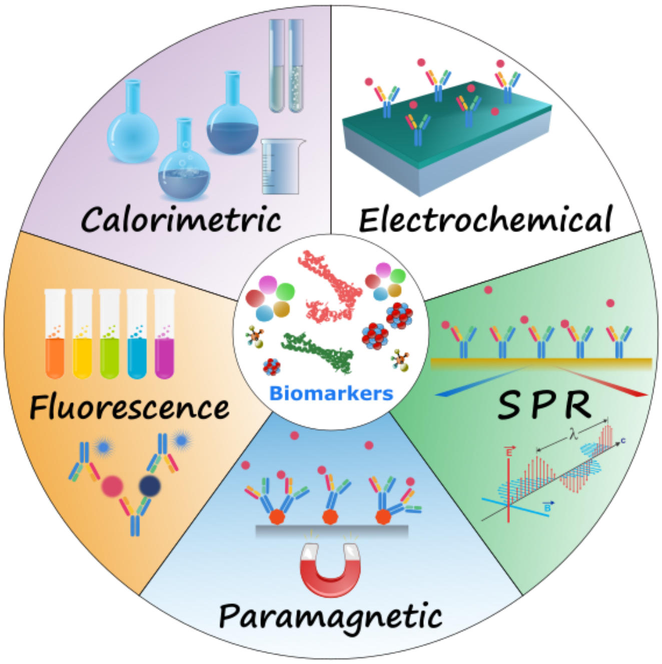

Figure 2.1: Various biosensing techniques and approaches developed and adopted for detecting different kinds of biomarkers.

In principle, ELISA assays tend to have high sensitivity, specificity, and accuracy which makes them preferred to be used in many cases. However, ELISA tests have also several drawbacks and limitations which significantly impact the effectiveness of such immunoassays for clinical practice and medical applications. In particular, ELISA assays are usually performed in central laboratories by well-trained and professional operators, and results are available only after several hours. Furthermore, ELISA testing requires sophisticated and expensive bulky equipment (incubator, reagents washing machine, optical detection system, etc.). All the pointed drawbacks make the ELISA technique not suitable for point-of-care (POC) use and applications in emergencies and remote non-clinical areas (at home, schools, offices, etc.). Therefore, there is an urgent need to develop more practical, simpler, and faster analytical devices for POC testing. Designing and prototyping of ideal biosensors for the detection of biomarkers have to be robust against the following challenges. First of all, healthcare devices have to be extraordinarily sensitive since target biomarkers are difficult to detect as they usually exist at a very small concentration in serum or other biological fluids. The second challenge is the speed of detection. Since some diseases progress very quickly, point-of-care tests have to be rapid and independent of centralized lab equipment. Typically, a combination of several biomarkers is required to diagnose one single disease. The detection of several biomarkers simultaneously allows the doctor to determine the disease stage and guide personalized therapy. Therefore, a capability to rapidly detect multiple targets in real-time with high selectivity and specificity is a mandatory feature of POC assay tools particularly aiding the decision-making in emergencies.

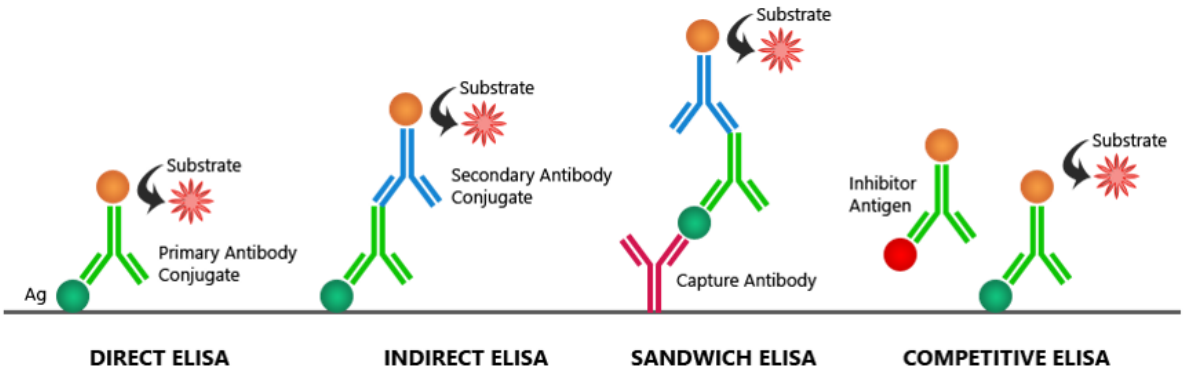

Figure 2.2: Enzyme-linked immunosorbent assay (ELISA) technique used to detect the presence and concentration of target biomarkers in the given sample. Several variations of ELISA tests have been developed, allowing qualitative detection or quantitative measurement of target biomolecules: direct, indirect, sandwich or competitive ELISAs. The figure is adopted from a web page*.

Moreover, periodic or serial measurements of biomarkers are usually required to evaluate their kinetics for monitoring an inflammatory disease progression. Therefore, POC biosensors have to be inexpensive or reusable. Economic factors also play an important role in the biosensors industry. Therefore, cost-efficient fabrication technology for POC devices production has to be developed and used. Furthermore, the POC biosensor has to be a simple and easy operation, so that nonprofessional user could perform testing practically everywhere. The results should be available within minutes and easily interpreted providing quantitative or qualitative information on patient's health depending on the purpose of the test. Some prototypes of biosensors with the potentials to achieve the abovementioned features have been already proposed in recent literature, however, no devices for continuous monitoring of biomarkers in biological fluids have been yet validated for real applications. To fulfill the requirements for POC devices, biotechnology still needs further development considering new transducer principles and device architectures [10].

Biosensors based on nanotransistor devices that are very similar to mass-production state-of-the-art semiconductor transistors appeared in recent years as potentially cheaper, faster, and more effective tools for clinical applications including personal healthcare and precision medicine. Such portable devices allowing "on-site" testing and analysis of multiple biomarkers in real-time with high speed, sensitivity, selectivity, and accuracy are ideal candidates to be used as analytical devices for point-of-care testing. In the following sections, we consider the working as well as sensing principles of nanotransistor-based biosensors and discuss the challenges that have to be met and tackled in such devices to fulfill the requirements of precision medicine and personal health care.

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[*] https://www.bosterbio.com/protocol-and-troubleshooting/elisa-principle

2.2 Nanotransistor biosensors: from metal to liquid gate

Biosensors based on liquid-gated (LG) field-effect transistors (FETs) attract much attention as miniaturized tools capable to perform biosensing of target analyte in real-time and with high sensitivity. The operation principle of such devices is very similar to that of metal-oxide-semiconductor FETs (MOSFETs) and the electrolyte solution is used as a liquid gate. For the comparison, a typical MOSFET device and its corresponding LG FET prototype are schematically shown in Figure 2.3(a) and 2.3(b), respectively. A conventional MOSFET consists of a conducting semiconductor channel formed between two highly-doped regions called source and drain. The current flowing through the channel is called drain current and it is proportional to the number of mobile charge carriers in the channel. This number of free carriers is precisely controlled by applying a voltage to a metallic gate in the case of MOSFET. In contrast, the LG FET is gated by applying a gate potential to a reference electrode immersed in the electrolyte solution. Additionally, the FET devices can be back-gated by applying a voltage to a substrate which serves as a back-gate electrode. A typical dependence of drain current on gate voltage applied to the FET structure is shown in Figure 2.3(c). The dependence is called transfer I-V characteristic and shows how effectively the conductive channel is controlled by the gate potential. To prevent a direct current flow between the gate electrode and conductive channel (i.e, leakage current), the latter is covered by an insulator layer (usually oxide). In the case of LG FET, the surface of the gate oxide is exposed to the solution and defines the sensing area of the LG FET device.

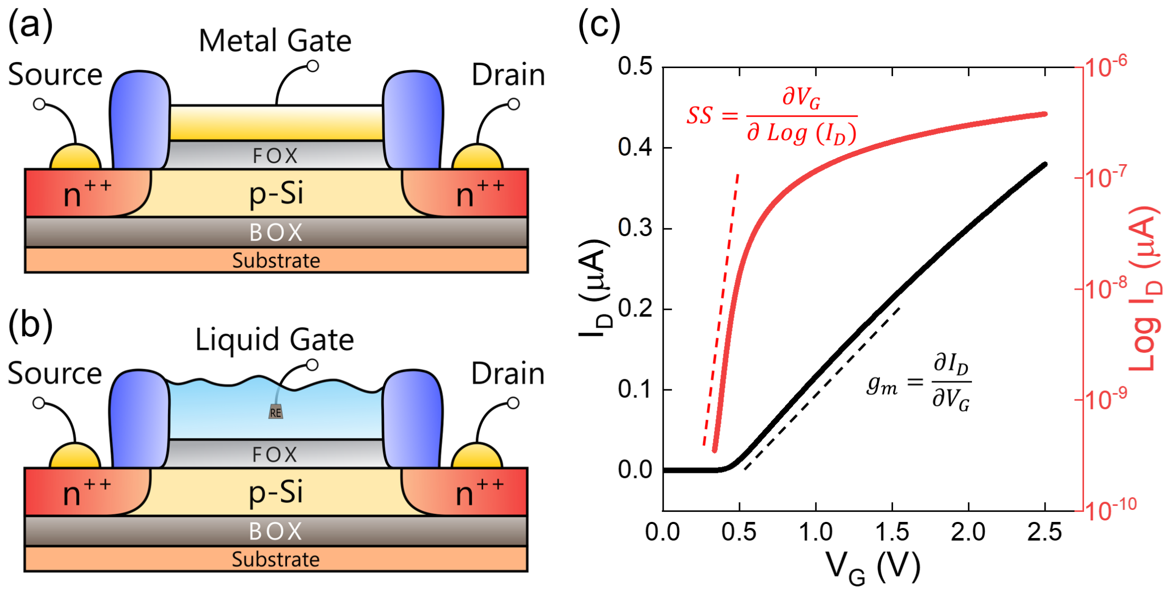


Figure 2.3: Schematic representation of (a) MOSFET and (b) ISFET devices; (c) Typical transfer I-V characteristic of a FET-based device plotted in linear (left axis) and semilogarithmic scales (right axis).

The non-metalized gate dielectric surface is typically covered with hydroxyl groups. When the surface is in contact with an electrolyte solution, the protonation/deprotonation of these groups occurs resulting in alterations of the surface charge [16]. Such processes lead to changes in the distribution of surface potential and hence have a direct effect on the charge-carrier flow through the channel. The phenomenon is known as the electrostatic gating field-effect and defines the working principle of any charge-sensitive FET-based device. The effect was discovered and explained in the 1970s by Piet Bergveld and co-workers [16]. Since that time, the ion-sensitive field-effect transistors (ISFETs) have emerged as one of the most promising classes of electronic sensors capable to convert chemical reactions into a measurable electrical signal via the above-explained electrostatic gating field effect.

Liquid-gated nanowire (NW) FETs are the modern version of the conventional ISFETs [17–19]. The high surface-to-volume ratio and nanoscale diameter of NWs allow fast accumulation/depletion of charge carriers enabling them to rapidly translate biochemical reactions occurring on their surface into a measurable electronic signal that can be further processed and analyzed. To make Si NW FETs selectively sensitive to the target biomolecules or chemical analytes, the surface of NWs have to be functionalized with the analyte-specific receptor molecules. A schematic illustration of a LG Si NW FET functionalized with receptors for the selective detection of target biomolecules is presented in Figure 2.4. Being dissolved in liquid, biomolecules like proteins or DNA possess a net positive or negative charge depending on the pH of the solution [20]. Therefore, when a charged analyte selectively binds to the receptors covalently anchored on the NW surface, the corresponding biomolecular recognition reactions (i.e. receptor-analyte interactions) induce changes in surface potential and thus modulate the charge-transport characteristics of the underlying NW FET. The induced changes can be then electrically measured and correlated with the analyte concentration. Such a concept defines the sensing principle of all biologically sensitive FET-based devices and allows direct detection of biorecognition processes between receptors and target biomolecules.

To date, Si NW FET-based biosensors have been exploited for various applications including pH [17, 21] and ion sensing [17, 18, 22] as well as for monitoring of different biological events such as protein-protein interactions [23, 24], antigen-antibody binding [11, 25, 26], enzyme-substrate reactions [23, 27], and genome sequencing [28]. However, operating and sensing in liquid are challenging tasks. In particular, the presence of ions and other charged bio-objects in most of the biofluids (e.g., blood, saliva, sweat) that electrically screen the charges of the target biomolecules considerably limits the response of the sensors to the analyte [25, 29, 30]. As a result, only biomolecules within the electrical double layer can be effectively detected by such devices. In this respect, receptor molecules responsible for the specific recognition and binding of target biomolecules should not exceed the Debye screening length to provide effective and sensitive biosensing [26]. Therefore, optimization of the bio-recognition layer by changing surface architecture and involving shorter receptor and linker molecules is a promising

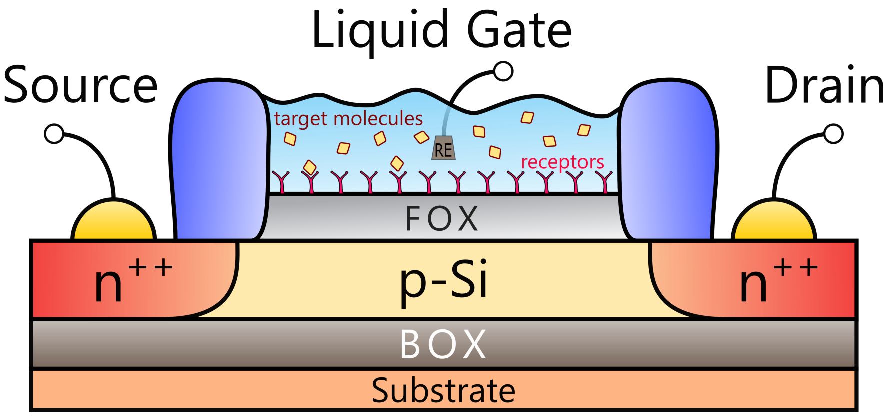


Figure 2.4: Schematic illustration of a biologically sensitive FET-based biosensor. The surface of the gate oxide is functionalized with receptors responsible for the selective binding of the analyte molecules.

way to increase the sensitivity of FET-based biosensors [10]. In this perspective, as described below in this thesis, we successfully designed and sensitized short ssDNA aptamers that are highly specific to the biomarkers of interest such as cTnI proteins and $A\beta40$ peptides to improve the specificity and sensitivity of fabricated NW biosensors. The corresponding chemical functionalization protocols enabling successful immobilization of aptamers on the SiO_2-covered surface of NWs were developed and used. Although a proper architecture of the biorecognition layer allows us to reduce non-specific binding and promote a charge transfer between transducer and analyte, which consequently improves the performance and sensitivity of FET-based biosensors, the latter is still critically dependent on the intrinsic electrical properties of the underlying FETs which are used as transducer elements. In particular, it has been traditionally considered that the LF noise of FETs determines the smallest change in analyte concentration that can be measured with such transistor-based biosensors. However, as we demonstrate later in this thesis, careful consideration of noise is an effective way to develop a highly sensitive and reliable biosensing device capable to detect the target analyte with the sub-elementary charge or even with the single-charge sensitivity in liquid. Such ability is required for biosensors aiming to be employed for practical early-diagnosis in clinical and healthcare applications.

2.3 Fundamentals of field-effect transistors (FETs)

Transistor-based biosensors are mass-fabrication-compatible electronic devices of interest for real-time, high-sensitive, and label-free biosensing. In this section, we give a general introduction to the electronic working principle of the LG FETs responsible for the transducing of biological signals in such liquid-gated transistor-based biosensors.

As noted above, the operation principle of the LG FETs can be described as similar to that of classical MOSFETs and explained based on the energy band diagrams shown in Figure 2.5(a-d). By the definition, the energy band diagram represents the plot of electron energy variation versus the position. The energy levels of interest are the bottom of the conduction band (E_C) and the top of the valence band (E_V). In between the conduction band and the valence band, there is a region called a forbidden gap (E_G) where there are no allowed states for the electrons. At absolute zero temperature, the electrons are all in the lowest energy states. The highest energy level that an electron can occupy at absolute zero temperature is known as the Fermi level (E_F). In the case of an intrinsic (undoped) semiconductor, $E_F = E_i$ and lies in the middle of the forbidden gap. At non-zero absolute temperature, there is a non-zero probability that electrons can move from the valence band to the conduction band due to the thermal random motion of atoms. Assuming that the material is homogeneous and ignoring metal-semiconductor work-function difference, the energy levels E_C and E_V are flat and the Fermi level is a constant within the system when no voltage is applied to the gate electrode. In this case, the surface potential that is a total voltage drop across the semiconductor equals to zero. This situation is called a "*flat-band voltage*" mode.

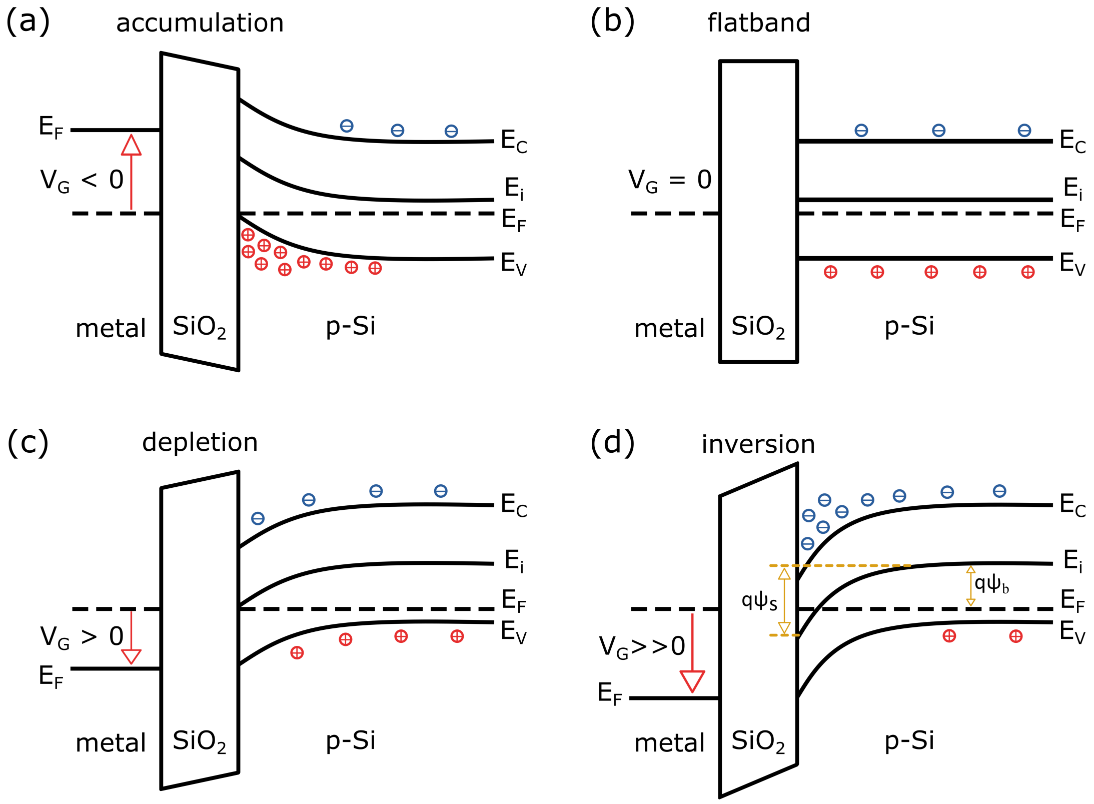


Figure 2.5: Energy band diagrams for a typical p-type MOS structure metal-gated at different V_G: (a) $V_G < 0$ - accumulation regime; (b) $V_G = 0$ - flat-band voltage mode (i.e., no "built-in" potential); $V_G > 0$ - depletion regime; $V_G >> 0$ - inversion regime.

In the case of p-type semiconductor material, a negative gate voltage accumulates holes as majority carriers close to the semiconductor/insulator interface. The concentration of holes increases exponentially near the Si/SiO_2 surface and pulls all the bend energies up relative to the Fermi level. Such a regime is called "*accumulation*" and explains the working principle of so-called accumulation mode transistors with p-type conductivity.

In the opposite case, if a positive voltage is applied to the gate, the mobile holes in the p-type semiconductor are pushed away from the interface, so that the area close to the interface becomes depleted of holes. In this case, the energy bands are pulled down and the space charge is mainly determined by the negatively charged acceptor impurities. However, if the energy bands go down, the concentration of electrons accumulated to the surface increases exponentially. And, if a positive gate voltage is further increased, the band bending becomes significant and as a result, a concentration of accumulated electrons will exceed the hole concentration near the interface. In this case, the inversion in conductivity type occurs. This means that the electrons become majority mobile carriers and therefore p-type material starts to behave as n-type. This regime is called "inversion" and correspondingly explains the working principle of so-called inversion mode transistors with n-type conductivity. The criteria for the inversion can be mathematically written as:

$$\psi_s = 2\psi_b \tag{2.1}$$

where ψ_b – is the difference between the intrinsic Fermi level (E_i) in the bulk and the actual Fermi level (E_F) of the doped semiconductor:

$$\psi_b = \frac{kT}{q} ln(\frac{N_A}{n_i}) \tag{2.2}$$

where k is a Boltzmann constant, T is absolute temperature, q is elementary charge, n_i is the intrinsic carrier density of semiconductor (for silicon, $n_i \simeq 10^{10}\ cm^{-3}$) and N_A is the acceptor density in p-type semiconductor. Therefore, by changing the doping level of the semiconductor one can change the condition for the inversion regime.

The surface concentrations of holes and electrons are determined by the surface potential as follows from the equilibrium statistics:

$$p_s = N_A \cdot e^{-\frac{q\psi_s}{kT}} \tag{2.3}$$

and

$$n_s = n_i^2/p_s = n_{p_0} \cdot e^{\frac{q\psi_s}{kT}} \tag{2.4}$$

where n_{p_0} is the equilibrium concentration of the minority carriers in the bulk, and ψ_s – is the surface potential related to the applied gate voltage in the following way:

$$V_G = \psi_s + V_{ox} \tag{2.5}$$

where V_{ox} is the potential drop across the oxide. Thus, the charge carrier concentrations and therefore the conductivity of the conduction channel strongly depend on the applied gate voltage. Considering the geometry of a simple planar MOSFET (see Figure 2.3(a)) one can derive equations for the drain current in different operation regimes determined by the gate voltage applied:

$$I_D = \begin{cases} 0, & V_G \leq V_{th}; \\ C_{ox}\mu\frac{W}{L}\left[(V_G - V_{th})V_{DS} - \frac{1}{2}V_{DS}^2\right], & V_G > V_{th},\ V_{DS} \leq V_G - V_{th}; \\ \frac{1}{2}\mu C_{ox}(V_G - V_{th})^2\left[1 + \lambda(V_{DS} - V_{DSsat})\right], & V_G > V_{th},\ V_{DS} > V_G - V_{th}. \end{cases} \tag{2.6}$$

where V_{th} is a threshold voltage (i.e., a gate voltage at which the current starts flowing through the transistor channel), W and L are width and length of the FET channel, respectively; μ is the electron mobility, V_G is the gate voltage, V_{DS} is the drain-source bias, λ is the channel-length modulation parameter, V_{DSsat} is the saturation drain-source voltage and C_{ox} is the capacitance of the MOS structure given by:

$$C_{ox} = \frac{\epsilon_0\epsilon_{ox}}{t_{ox}} \tag{2.7}$$

where ϵ_0 is the vacuum permittivity, ϵ_{ox} is the permittivity of the dielectric layer and t_{ox} is the thickness of the oxide layer.

A typical transfer curve of an n-type FET device is shown in Figure 2.3(c). A transfer characteristic is obtained when the source-drain current is measured as a function of the voltage applied to the gate. At small $V_G < V_{th}$, the conductive channel between source and drain has not formed yet, so there is no current flow and transistor can be considered in “off-state”. When the gate voltage is increased slightly above V_{th}, the conductive channel is forming and the sub-threshold drain current is increasing exponentially with V_G. The regime is called the *sub-threshold operation regime*. The slope of sub-threshold current in the semi-logarithmic scale is called sub-threshold swing (SS) that can be defined as the change in gate voltage which must be applied to the gate in order to create a one decade increase in the drain current:

$$SS = \frac{dV_G}{d(log(I_D))} \tag{2.8}$$

Usually, a smaller sub-threshold swing reflects a better channel control, which means a less leakage current and better performance of a device. A theoretically calculated SS minimum for silicon FETs at room temperature is about 60 mV/dec.

If the gate voltage is further increased ($V_G > V_{th}$), the transistor starts to behave like a simple resistor when the current is linearly proportional to the voltage applied. Such a regime is called a *linear operation mode*. When the gate voltage is increased even further ($V_G >> V_{th}$), the transfer curve starts to saturate due to the contact and high-field effects. In this case, a device can be considered in the "on-state" and its operation regime is known as a *saturation mode*.

The parameter showing how effectively gate voltage controls the drain current is called transconductance (g_m) and it is defined as:

$$g_m = \frac{\partial I_D}{\partial V_G} \tag{2.9}$$

The higher transconductance usually means a larger amplification that the FET device is capable to deliver. In terms of FET-based sensors, higher transconductance generally means a higher sensitivity when the drain current is monitored as a signal.

2.4 Fluctuation phenomena in FET-based devices

Spontaneous fluctuations of current or voltage are inherent for any electronic device due to the presence of electrical noise. While the physical mechanisms behind these random fluctuations may vary for different types of devices, noise is an important concern to be considered for the development of "all-electrical", compact and reliable biosensors capable to perform high-sensitive and high-efficient biosensing of target analyte in real-time. In this section, we give a brief introduction to noise fundamentals which includes basic noise theory and description of some fundamental noise mechanisms in the state-of-the-art electronic FETs as well as liquid-gated FETs which are used as transducers in such FET-based biosensors.

2.4.1 Basic noise theory and models

Electrical noise is the random fluctuations of the current (or voltage) inside any electrical device. The origin of such fluctuations comes from the physical processes inside a device material and is related to continuous motion of microscopic entities (electrons, atoms, etc.) at the micro-level. Interestingly, noise is nothing but a direct evidence of the discrete nature of electrical charges and might be generated by different internal physical mechanisms. Noise mechanisms caused by external sources such as disturbances from the power lines, external electromagnetic fields, or etc., are beyond the scope of this thesis. To prevent such parasitic external disturbances and minimize their impact on noise measurements, proper shielding and appropriate design of the measurement circuits must be applied.

Unlike other areas of physics that study the behavior of averaged characteristics of an object of interest, the physics of fluctuation phenomena studies random, spontaneous deviations (often local) of a deterministic signal from its average value. Therefore, due to the statistical nature of fluctuations, the noise measurements can be used as a diagnostic tool to gain information about device quality and reliability as well as to study the origin of physical processes governing the transport properties of a device. The ability to investigate the behavior of transport and noise in a device at the condition of thermodynamic equilibrium without significant influence of the measurement process on the measurement results makes noise spectroscopy technique to be an indispensable tool for study dynamic processes in nanoscale devices (e.g., nanosheets, nanowires, nanodots), where noise becomes basically a single carrier phenomenon. Therefore, noise spectroscopy is a powerful method allowing us to probe the transport properties of a device at the microscopic level in space and time.

The noise fluctuations of any electrical signal (e.g., current, voltage, conductance) are based on the random and spontaneous nature of the transition of electrons between different energy levels, which leads to corresponding local changes in the signal. In general, the fluctuating signal can be defined as:

$$X(t) = \langle X \rangle + x_n(t) \tag{2.10}$$

where $\langle X \rangle$ is the average value of the signal and $x_n(t)$ denotes noise fluctuations (the object of measurements). Figure 2.6 shows how an electrical signal $X(t)$ is perturbed from its given value due to the presence of stochastic noise. At the equilibrium, $\langle X \rangle$ is constant, while the value of $x_n(t)$ is random and different at any point in time. The dependence of $x_n(t)$ is difficult to analyze directly, therefore the study of noise phenomena involves a mathematical approach based on the power spectral density (PSD) concept.

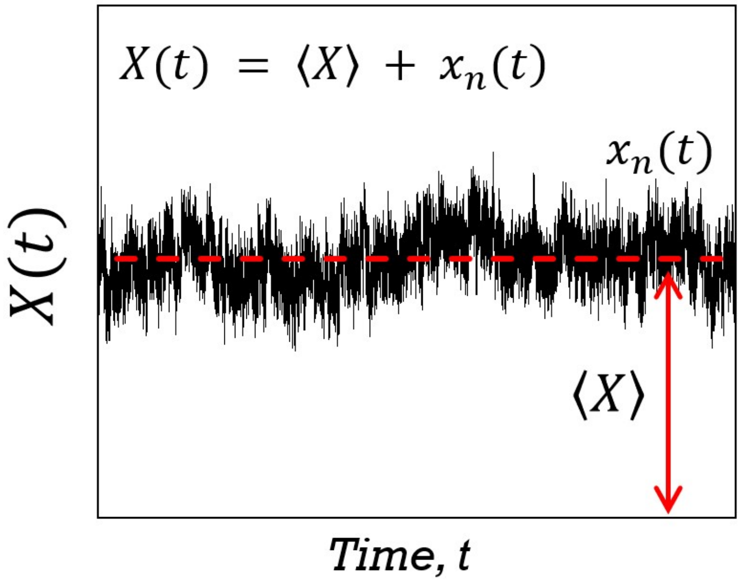


Figure 2.6: Typical electrical signal waveform perturbed by random noise.

Considering $X(t)$ as a random process that is observed in the infinitely long interval $[-\frac{T}{2},\frac{T}{2}]$, one can define the autocorrelation function $C(\tau)$ of the signal $x_n(t)$ as follows:

$$C(\tau) = \langle X(t)X(t+\tau)\rangle = \lim_{T\to\infty}\frac{1}{T}\int_{-\frac{T}{2}}^{\frac{T}{2}} X(t)X(t+\tau)dt \tag{2.11}$$

where the brackets denote a time averaging over an ensemble of realizations of the random fluctuations $X(t)$. Then, according to the Wiener-Khintchin theorem [31], PSD can be determined as:

$$S(\omega) = \lim_{T\to\infty} S_T(\omega) = \lim_{T\to\infty}\frac{1}{T}\langle|\hat{X}_T(\omega)|^2\rangle \tag{2.12}$$

where $\hat{X}_T(\omega)$ is the truncated Fourier transform of a realization of the random process $X(t)$ over an interval $[-\frac{T}{2},\frac{T}{2}]$ given by:

$$\hat{X}_T(\omega) = \int_{-\frac{T}{2}}^{\frac{T}{2}} dtX(t)e^{-i\omega t} \tag{2.13}$$

PSD of noise fluctuations provides valuable information about how noise power is distributed in the frequency domain. Therefore, the PSD-based approach is a powerful method to characterize and describe noise fluctuations happening in the electrical device. Typically, the PSD spectrum may consist of several superimposed components that are related to different noise mechanisms. Below, we will describe some potential sources of noise in FET-based devices in detail.

2.4.2 Origin of noise in nanoscaled transistors

The field-effect transistor is a complex device that typically has several noise sources with different spatial locations and different physical mechanisms. Figure 2.7 schematically shows the noise PSD as a function of the frequency for a device demonstrating different types of noise (thermal noise, shot noise, $1/f$ flicker noise, and generation-recombination noise). It is usually observed that different noise sources are non-correlated, therefore the PSD spectrum of noise fluctuations is a superposition of noise components.

Thermal noise. The origin of thermal noise comes from the thermodynamic fluctuations of thermally excited charge carriers in any electrically conductive material. A random thermal motion and scattering of charge carriers result in spontaneous changes in charge density leading to random fluctuations of voltage on the contact terminals of any electrical device. However, due to its fundamental nature, thermal noise is the only noise component that occurs regardless of whether a voltage bias is applied to the material. The existence of thermal noise was predicted by A. Einstein in 1906. Later in 1928, Einstein's theory was experimentally verified by

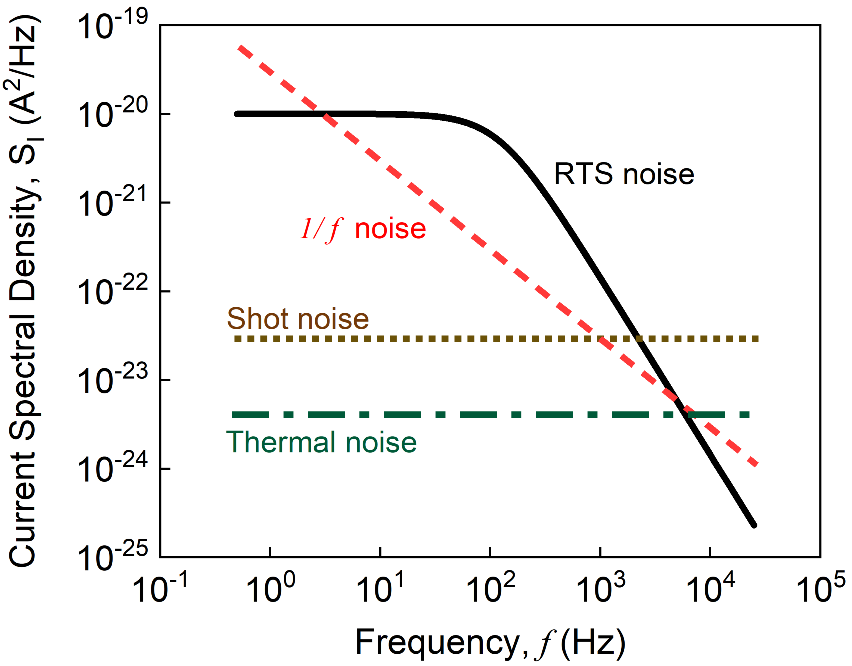


Figure 2.7: Schematic illustration of the current noise PSD of the main noise components presented in a typical FET-based device.

J.B. Jonson and theoretically confirmed by H. Nyquist. Therefore, the thermal noise is often called in the literature as the *Johnson-Nyquist noise*.

The current PSD of the thermal noise is given by:

$$S_I = 4kT/R \tag{2.14}$$

where k is the Boltzmann constant, and R is a resistance of material at non-zero temperature (T). The PSD of thermal noise is frequently independent in the relatively wide frequency range (up to a few GHz). Therefore, thermal noise is often considered as white noise (i.e., noise with a constant PSD for all frequencies). Due to the fundamental nature of the physical mechanisms behind the thermal noise, this type of noise cannot be eliminated for a given material with resistivity (R) at given temperature (T). Therefore, the thermal noise defines the lower limit of noise in any electrical device. Other noise components usually demonstrate a higher noise level and can de found on the top of the thermal noise.

Thermal dielectric-polarization noise. The concept of dielectric-polarization (DP) noise was initially introduced by the mesoscopic physics community to describe noise in elementary charge-sensitive electrometers whose origin was typically attributed to fluctuating charges in the substrate. Later, the biosensor community used the DP noise model to explain experimentally measured noise in the nanoscale silicon transistors [13, 18], carbon nanotubes [32], graphene FETs [33] and organic electrochemical transistor devices [34].

The origin of DP noise comes from the thermal fluctuations of dipoles in the gate dielectric layer of a transistor. If a non-ideal dissipative dielectric is considered, the PSD of voltage noise referred to the gate of the transistor can be defined as follows:

$$S_{V_G} = 4kTRe(Z) = \frac{2kT\tan(\delta)}{\pi f C_{ox}} \tag{2.15}$$

where $\tan(\delta) = \epsilon^{''}/\epsilon^{'}$ is the dielectric loss tangent with $\epsilon^{''}$ and $\epsilon^{'}$ as the real and imaginary dielectric permittivities of the gate dielectric material, respectively. The Equation 2.15 is derived from the fluctuation-dissipation theorem which extends Johnson–Nyquist noise equation to complex impedances and provides a good quantitative agreement with the experimental data [18]. Unlike the thermal noise, the PSD of the DP noise demonstrates $1/f$ behavior due to the complex impedance of the dielectric material. The DP noise together with the regular thermal noise creates a *fundamental thermal limit* in biosensing defining the detection limit of any FET-based sensor. One of the research aims of this thesis is to push the thermal limit due to the noise suppression with single-trap phenomena approach as will be shown below.

Shot noise. Shot noise is usually generated when the charge carriers cross a potential barrier (e.g., Schottky barrier, p-n junctions) independently and randomly in such a way that there is no continuous current flow through the barrier due to the discrete nature of the carriers. In this case, the PSD of the current fluctuations in an electrical device with a potential barrier can be calculated as:

$$S_I = 2qI \tag{2.16}$$

where q is the elementary charge, and I denotes the DC current across the barrier. Similarly to the thermal noise, the PSD of the shot noise is independent of the frequency, as shown in Figure 2.7.

Generation-recombination noise. Noise in transistor-based devices is highly sensitive to the quality of the device material determined by the fabrication technology. In particular, the presence of traps, lattice damage, and other defects are main noise sources which usually determine a noise level of a device. Generation-recombination (G-R) noise is a type of "*trapping*" noise in semiconductor devices originating from the individual traps or generation-recombination centers that randomly capture or emit charge carriers. The energy of such centers lies in the forbidden band gap usually within a few (kT) to the Fermi energy level. Random processes of electron capture and emission to/from centers result in current fluctuation with PSD given by:

$$S_I = I^2 \frac{N_t}{N^2} \frac{\tau}{1 + (2\pi f \tau)^2} \tag{2.17}$$

where N_t is a number of traps, N is a total number of free electrons in a device at given bias, I is transistor drain current and τ is the effective time constant of the capture/emission processes. According to Equation 2.17, the PSD of (G-R) noise with characteristic time constant τ has a Lorentzian shape (see Figure 2.7). Usually τ is a function of N and can be calculated as $\tau = 1/2\pi f_0$, where f_0 is a corner frequency of a Lorentzian-shaped spectrum. The PSD of G-R noise is proportional to N_t and inversely proportional to N^2. For the devices in which traps and free electrons are spatially separated, the τ may also depend on the distance between them. A special case of the G-R noise when $N_t = 1$ is a subject of the interest in this thesis. Therefore, it will be described in detail at the end of this section. The current fluctuations can be further converted (recalculated) into the voltage fluctuations referred to the transistor gate using equation:

$$S_{V_G} = \frac{S_I}{{g_m}^2} \tag{2.18}$$

where g_m is a device transconductance calculated using Equation 2.9.

Flicker noise. A flicker or so-called $1/f$ noise is a dominant type of noise fluctuations with PSD that is inversely proportional to frequency (f) on a logarithmic scale. Flicker noise has been found in many systems and becomes the subject of numerous studies on a large variety of semiconductor devices. In general, the PSD for $1/f$ noise is defined as follows:

$$S_I = \frac{KI^\beta}{f^\alpha} \tag{2.19}$$

where K is a constant, β stands for a current exponent and α is a positive number usually in the range $(0.7 - 1.3)$.

The origin of the flicker noise is still under debate among the scientific community since the $1/f$ noise mechanism is different in different devices and still not completely understood. Currently, two standard models dominate to explain flicker noise in semiconductor FET devices. The first model is known as a *number fluctuation model* due to the traps in the gate oxide, while the second one is a bulk *mobility fluctuation model*. Sometimes, deviations from the expected $1/f$ noise are experimentally observed, so that $1/f$ fluctuations cannot be described properly by any of the aforementioned models. In this case, the *correlated model* appears that accounts for both number fluctuation and mobility fluctuation effects simultaneously. Below, we will briefly discuss each of the standard $1/f$ noise models commonly used to describe low-frequency noise fluctuations in semiconductor devices.

2.4.3 $1/f$ noise fundamentals for transport characterization of FETs

Number fluctuation model. The number fluctuation or trapping-detrapping model is a state-of-the-art noise model aiming to explain $1/f$ fluctuations generated in the channel of the transistor-based devices. The model was proposed in 1957 by McWhorter and is based on tunneling capture/emission processes of charge carriers due to the traps presented at the Si/SiO_2 interface and in the gate oxide. Such dynamic random exchange of carriers between the traps and conductive channel results in fluctuations of surface potential which are further translated in the current or voltage noise of a device. Transitions of charge carriers to/from the traps are thermally activated tunneling processes that depend on the nature of the trap and the operation conditions.

As mentioned above, the interaction of charge carriers with a single trap induces a G-R noise component with a Lorentzian shape PSD. Therefore, assuming that a large-enough device might have several traps, the superposition of all Lorentzian components due to individual traps results in the total $1/f$ noise spectrum. Herewith, the interactions between traps are excluded. According to McWhorter's model, the PSD of $1/f$ voltage noise referred to the transistor gate is defined as:

$$S_{V_G} = \frac{q^2 N_t}{{C_{ox}}^2 A f} \sim \frac{1}{A} \tag{2.20}$$

where q is the elementary charge, N_t is the density of oxide traps (or other charge trapping sources), C_{ox} is the gate oxide capacitance per surface unit (see Equation 2.7), A is a gate area, and f is the frequency.

Therefore, the current transport in transistor-based structures is very sensitive to the traps presented in the gate oxide or at its interface with a conductive channel. The number fluctuation noise mechanism is discussed in detail for different types of devices elsewhere [12, 13, 35]. In general, as it has been widely demonstrated, the trapping noise model works better for the inversion-mode transistor devices in which the inversion conductive channel is confined directly under the gate oxide (so-called surface channel). In this case, the tunneling process of charge carrier from the channel to the traps and backward is likely to occur. So, the quality of the Si/SiO_2 interface basically determines the noise level in such transistor structures. The McWhorter model indeed shows an excellent agreement with experimental results obtained for inversion mode transistors with relatively large gate area ($A > 1\ \mu m^2$), however, the model fails in some other cases. For example, the trapping model doesn't work properly for accumulation mode transistors demonstrating so-called a volume conductivity. Also, a serious problem with the number fluctuation model appears for devices with very thin gate dielectrics ($1-2\ nm$) due to the fast tunneling time of charge carriers to the traps located even at the oxide/gate interface. To address such problems, different theories have been suggested and investigated. Below, we will briefly discuss some of them.

Mobility fluctuation model. In the frame of the mobility noise fluctuation model or so-called Hooge noise model, $1/f$ noise inside a conductive homogeneous bulk material is generated by fluctuations in the mobility of charge carriers due to different scattering processes (mainly due to phonon scattering). Such mobility fluctuations cause noise with PSD given by Hooge's empirical formula:

$$S_I = I^2 \, \frac{\alpha_H}{N f} \tag{2.21}$$

where N is the number of carriers and α_H is the dimensionless Hooge parameter, which is often used to quantitatively assess and compare the noise level in different materials and devices. Initially, the Hooge parameter was considered as a constant ($\sim 2\times10^{-3}$). However, considering that different scattering mechanisms depend on various parameters such as channel position and vertical electric field, Hooge proposed later to use the alpha Hooge as the parameter that depends not only on fabrication technology but also on the crystal quality and the bias applied to the sample. Typically, in the case of silicon-based devices, alpha Hooge varies in the range ($10^{-2} \div 10^{-6}$) depending on device operation regime and condition.

Usually, the Hooge model successfully describes $1/f$ noise fluctuations in accumulation mode p-type transistors [13, 36, 37] demonstrating rather a volume conductivity than surface conductivity. However, deviations from the expected noise behavior are often reported in the literature even for p-type devices operating, for instance, in the subthreshold regime [38, 39]. In such cases, the improvements in the mobility noise model are suggested. In particular, it was shown that the different scattering mechanisms contribute with different magnitude to the fluctuation in the mobility of charge carriers. Therefore, lower values of alpha Hooge parameters can be expected for the devices operating in the subthreshold regime, for instance due to the stronger impact of the Coulomb scattering mechanism [40, 41]. Also, it was shown in the literature that the variation of alpha Hooge is related to the phonon-phonon scattering rate [40]. A random scattering of phonons induces additional phonon-electron scattering giving rise to $1/f$ noise in the mobility. The importance of the surface roughness scattering on the mobility fluctuation is demonstrated in Ref. [42]. In particular, it was shown that similarly to the carrier number fluctuations, the mobility fluctuations are highly sensitive to the properties of the interface between the gate oxide and conductive channel (e.g., traps, G-R centers, defects). Although the exact origin of the mobility fluctuations is still not completely understood, the Hooge model plays an important role to explain noise in semiconductor and metal-based devices.

Correlated mobility fluctuation model. Studies on low-frequency noise in various semiconductor devices demonstrated that both mobility fluctuations and number fluctuations mechanisms play an important role in the generation of $1/f$ noise. Each mechanism (model) can be successfully applied to explain noise fluctuations in different types of devices. On the other hand, the Hooge model is more successful for instance in the accumulation mode devices, while the McWhorter model works better for the inversion mode transistor structures. Despite the success of each abovementioned model, there is a relatively large number of reports in the literature showing the practical situations when the deviations from the standard models in noise behavior occur. In this case, the so-called correlated mobility fluctuation model was suggested to account for both mobility and number fluctuations mechanisms [43–45]. It was demonstrated that trapping and detrapping of charge carriers by the traps lead to the fluctuations in charge density due to the both number and mobility fluctuations, simultaneously. In particular, it was shown that a trapped carrier, in fact, affects surface mobility through Coulomb interaction, therefore both noise sources contribute to the total $1/f$ noise and should be considered simultaneously. In this case, the PSD can be calculated as follows:

$$S_{V_G} = \frac{q^2 N_t}{{C_{ox}}^2 A f} \left(1 \pm \alpha_{sc} \mu C_{ox} (V_G - V_{Th})/q\right)^2 \sim \frac{1}{A} \tag{2.22}$$

where the first term is due to the fluctuating number of inversion charge carriers, while the second number accounts for the mobility fluctuations correlated to the number fluctuations. Parameter α_{sc} is the scattering parameter showing the impact of the oxide charge (charged traps) on the carrier mobility. The sign of α_{sc} depends on if the mobility increases or decreases due to trapping of charge carriers.

Quantum $1/f$ noise model. The quantum $1/f$ noise model was initially proposed by *Prof. Dr. Peter Handel* and co-workers to explain $1/f$ noise in a condensed matter as fluctuations in the electron scattering accompanied by the emission of the low-frequency (infrared) photons [46]. The photon emission transfers only negligible energy but it still modulates the current flowing in a system, which results in $1/f$ noise. The Handel's theory describes the infrared-divergent conventional $1/f$ fluctuations of quantum mechanical cross-sections and process rates considering fundamental quantum electrodynamics formulas. Furthermore, the theory derives also the coherent quantum $1/f$ effect [47] to explain $1/f$ noise in semiconductor materials, p-n junctions and quartz resonators providing optimal designing rules for such kinds of devices. However, despite the success and explicit results of quantum $1/f$ noise theory in describing $1/f$ noise in different materials, devices, and systems, the quantum $1/f$ noise model has provoked a huge debate between its opponents and supporters due to several objections and contradictions later discovered in the quantum $1/f$ noise theory [48, 49].

2.5 Single-Trap Phenomena (STP) in nanostructures

A great deal of attention among researchers and engineers has been paid to a special case of G-R noise appearing as random discrete switching events between two or more states in the time domain under constant bias conditions, so-called *random-telegraph-signal* (RTS) noise. The origin of such fluctuations has been attributed to trapping and detrapping of a single charge carrier by and from a single trap or defect state located at the Si/SiO_2 interface or in the gate oxide close to a conductive channel of a nanotransistor. In this respect, the RTS effect is often called ***single-trap phenomena*** (STP). The investigation of RTS noise in various devices operated at the room as well as cryo-temperatures has been the subject of the research during the last few decades. Until now, the RTS effect has been observed in many devices including bipolar junction transistors (BJTs), MOSFETs, graphene FETs, carbon nanotubes, quantum dots, and liquid-gated NW FETs. The RTS phenomenon in the latter devices is the subject of interest in this thesis. Interestingly, the RTS-like effect has been also found in biology when a current is flowing through single ionic channels [50, 51].

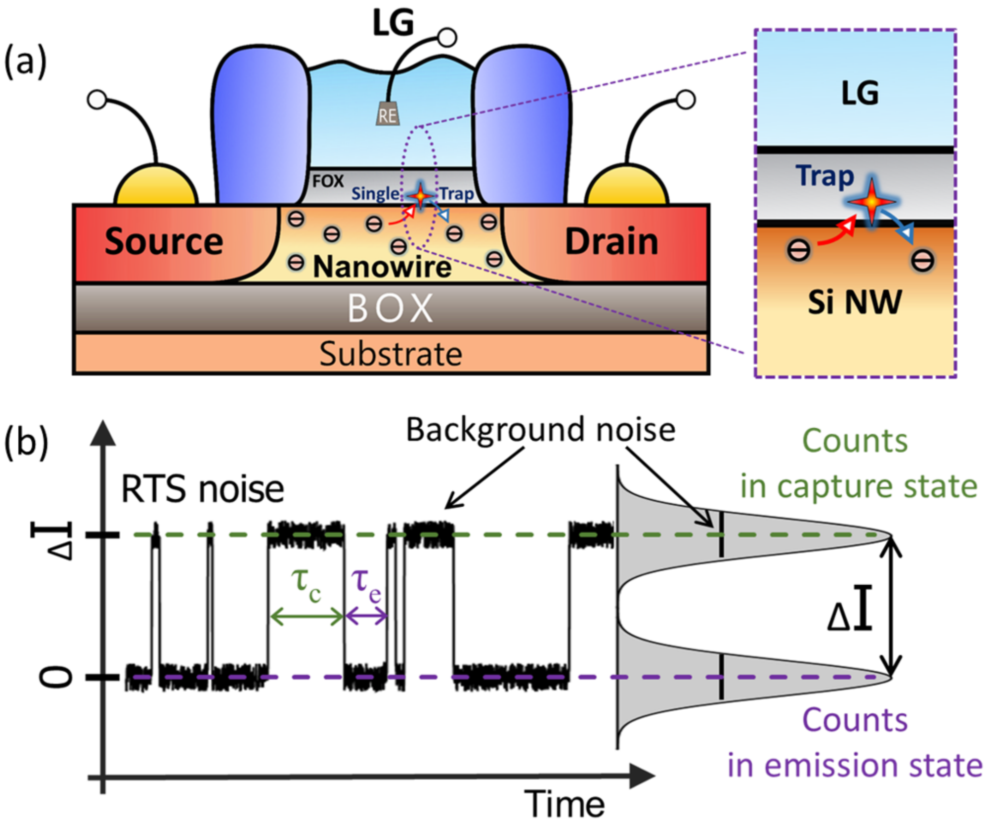


Figure 2.8: Single-trap phenomena in nanoscale transistor-based biosensors: (a) schematic illustration of a liquid-gated nanotransistor with a single trap that induces (b) two-level RTS fluctuations of the drain current.

A schematic representation of a nanoscale transistor with a single trap in the gate oxide layer is depicted in Figure 2.8(a). The trap exchanges charge carriers with a conductive channel which results in RTS fluctuations of the drain current between two distinct levels (see Figure 2.8(b)). The difference between levels is the RTS amplitude (ΔI) which reflects a change of the signal when transition event occurs. Considering a simple electrostatics [12] of the transistor structure, the RTS amplitude can be calculated as follows:

$$\Delta I = g_m \times \frac{q^*}{C_{ox} A} \tag{2.23}$$

where g_m is the transconductance and q^* is an effective charge of about $(0.5q)$ for SiO_2 that accounts for image charge effects [12, 52].

Fluctuating behavior of drain current is a fully stochastic process and therefore can be characterized by performing statistical analysis [53, 54]. The probability that a trap is occupied by a charge carrier is given by trap occupancy factor (g) defined as:

$$g = \frac{\tau_e}{\tau_e + \tau_c} \tag{2.24}$$

where τ_e is an average emission time of a charge carrier from the trap and τ_c is an average time for a random charge carrier to be captured by the trap. Both RTS characteristic time constants characterize a specific trap level at given bias condition and follow a Poisson distribution $P(t) \sim exp(-t/\langle t\rangle)$, where $\langle t\rangle$ denotes capture or emission time constant averaged over all states of an ensemble at a given time t. A probability of a transition from the captured carrier state to the free carrier state is given by $1/\tau_c$, while the probability of carrier to be released by the trap is $1/\tau_e$.

The identification of the switching direction to either emission or capture state is based on the gate-bias dependence of time constants in such a way that trap occupancy factor g (see Equation 2.24) increases with increasing carrier concentration in the conductive channel. The chemical nature of the traps responsible for the RTS effect is not yet completely clear. However, two different types of traps involved in the RTS processes in transistor devices have been recognized [55]: acceptor-type (repulsive) and donor-type (attractive) traps. The acceptor-type trap is neutral when empty and becomes charged after it captures a charge carrier from the conductive channel (i.e., becomes repulsive for other charge carriers in the channel). The donor-type trap is charged when empty (i.e., attracts charge carriers from the channel) and becomes neutral when it is occupied by a charge carrier.

Usually, the electrically active single trap located in the vicinity of a conductive channel results in a simple two-level RTS process. However, several reports can be found in the literature showing the complex RTS noise when the signal fluctuates between three and more levels [12, 56]. The physical origin of such complex RTS noise has not been fully understood yet. However, few assumptions have been proposed considering two and more metastable states [15] of a single trap as well as simultaneous multi-carrier trapping by the same trap [56].

The noise PSD of a single two-level RTS is given by a Lorentzian:

$$S_I = \frac{4\Delta I^2}{(\tau_c + \tau_e)\left[\left(\frac{1}{\tau_c} + \frac{1}{\tau_e}\right)^2 + (2\pi f)^2\right]} \tag{2.25}$$

where ΔI is the change in drain current of the nanotransistor caused by the single trap (i.e., the RTS amplitude), f is the frequency, and τ_c and τ_e are the trap capture and emission times, respectively. Both times characterize a specific trap level at a given bias condition and define a corner frequency, f_0 of Lorentzian-shaped PSD (see Figure 2.7) as follows:

$$f_0 = \frac{1}{2\pi\tau} = \frac{1}{2\pi} \times \left(\frac{1}{\tau_c} + \frac{1}{\tau_e}\right) \tag{2.26}$$

where τ is the effective time constant.

If $\tau_c = \tau_e$ and considering Equation 2.26, Equation 2.25 can be reduced to:

$$S_I = \frac{2\Delta I^2 \tau}{4 + (2\pi f \tau)^2} \tag{2.27}$$

At the same time, by considering Equations 2.25, 2.24, and 2.18, the voltage input-referred noise of the RTS process can be written as:

$$S_{V_G} = \frac{4g(1-g)^2 \tau_e (q^*/C_{ox}A)^2}{1 + (2\pi(1-g)\tau_e f)^2} \tag{2.28}$$

Interestingly, at the corner frequency of the Lorentzian distribution ($f = f_0$), the expression $2\pi \times (1-g) \times \tau_e \times f_0 = 1$, and considering the probability of the trap to be occupied equal to 50% ($g = 0.5$), Equation 2.28 can be simplified to [12]:

$$S_{V_G} \approx 0.08 \times \frac{(q^*/C_{ox}A)^2}{f_0} \tag{2.29}$$

It should be noted that Equation 2.29 can be used to estimate the upper limit of RTS noise as a result of STP in a nanotransistor device.

The RTS noise in small-area (usually below 1 μm^2) devices often dominates over all the other noise sources in the low-frequencies range of the PSD spectrum. Therefore, RTS noise has been usually recognized as one of the most important problems for engineering of electronic devices especially considering the aggressive downscaling of transistors as main electrical components. However, RTS is a very interesting and important phenomenon that can be used as a powerful local microscopic tool for the study interface properties and single-trap kinetics allowing to derive different parameters such as the activation energy of the trap level, capture cross-section and special information on the trap position in the gate oxide [56]. Furthermore, the RTS effect may also reveal fundamental properties like Coulomb blockade effects that affect trap charging [52, 55] and electron heating effects [57] in the system. Moreover, due to its discrete nature and specific properties, the RTS effect is very promising for various practical applications in the semiconductor industry [58].

Below in this thesis, we will demonstrate that STP in liquid-gated nanobiosensors provide unique opportunities for the advanced biosensing applications since the effect is very sensitive to local changes in surface potential. In particular, we will show that characteristics of a single trap in a nanotransistor-based biosensor can be used as a sensory signal to enhance the sensitivity of the device. Moreover, we will demonstrate also that the low-frequency noise can be considerably suppressed even beyond the thermal limit level by monitoring the trap occupancy probability when a single trap is in the the regime of stochastic resonance.

2.5.1 Shockley-Read-Hall theory: trapping/detrapping processes in bulk semiconductors

Typically, the behavior of capture and emission times are described in the frame of the standard Shockley-Read-Hall (SRH) theory based on the local detailed balance mechanisms of trapping/detrapping processes under equilibrium conditions. Both processes are thermally activated and phonon-assisted [52, 55]. According to the theory, the time constants of the capture and emission processes to and from a neutral center can be expressed as follows:

$$\tau_e = \frac{1}{\sigma_n \upsilon_{th} n_1} = \frac{1}{\sigma_n \upsilon_{th} N_C} \cdot exp\left(\frac{E_T}{kT}\right) \tag{2.30}$$

and

$$\tau_c = \frac{1}{\sigma_n \upsilon_{th} n} \sim \frac{1}{I_D} \tag{2.31}$$

where σ_n is the capture cross-section, υ_{th} is the average thermal velocity of the charge carriers, n is the concentration of free electrons (in the case of electron capture) at the Si/SiO_2 interface, E_T is the energy level of the center relative to the bottom of the conduction band, N_C is the density of electron states at the bottom of the conduction band.

According to Equation 2.31, the capture time constant, τ_c is inversely proportional to the concentration of free electrons (n) at given bias conditions and temperature (T). At small constant drain-source voltage V_{DS}, drain current I_D is proportional to the concentration of free electrons n in the channel located near the Si/SiO_2 interface. Therefore, the capture time is inversely proportional to the drain current driven by the gate voltage applied. However, there are a large number of reports in the literature showing for different devices that capture time behaves like the power function of drain current:

$$\tau_c \sim \frac{1}{I_D^{\gamma}} \tag{2.32}$$

with $\gamma > 1$. Such a dependence of capture time on drain current is much stronger than that predicted by the SRH theory according to Equation 2.31. To explain such a deviation in capture time behavior, several more advanced models have been proposed. Below, we will briefly review a few of the most appropriate and widely used models.

2.5.2 Concept of Coulomb blockade energy for interface traps

A stronger than linear dependence of capture time on the reciprocal drain current (see Equation 2.32) can be understood within the framework of the Coulomb blockade theory proposed by Schulz and co-authors [52, 55]. The theory is based on the idea that additional Coulomb energy is involved in the transfer and localization of a single charge carrier into the interface trap. The capture of a charge carrier by the trap induces the image charge Q_G on the gate electrode which charges a gate capacitor electrode system by a displacement current I_{disp} (see Figure 2.9). This results in free energy change (Coulomb energy ΔE), which strongly affects the entire capture dynamic process.

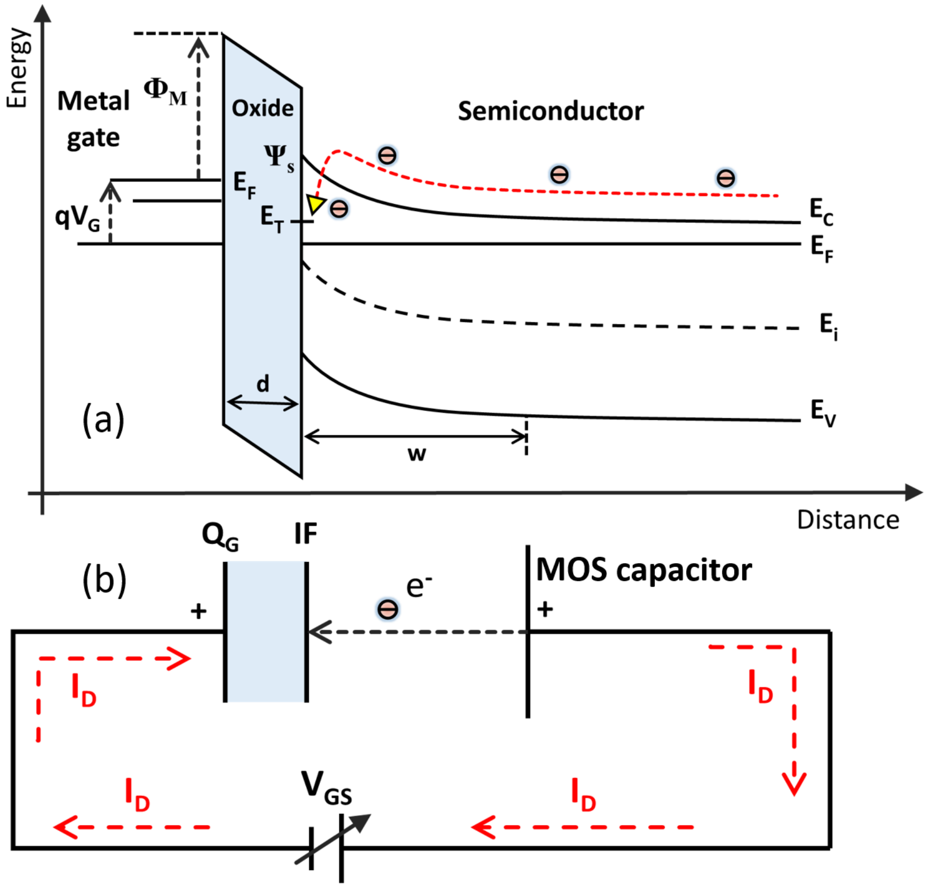


Figure 2.9: (a) Energy band diagram and (b) capacitance of a biased MOS structure. An image charge Q_G is induced on the metal gate during the transfer of an electron from the channel to the trap resulting in a displacement current I_D. The position IF shows the location of Si/SiO_2 interface. Figure is developed from Ref. [56].

The concept of Coulomb blockade energy is implemented by introducing into the SRH model Coulomb blockade energy (ΔE) which denotes additional energy that a charge carrier has to overcome while moving from the channel to the trap. Thus, in the case of a repulsive-type trap 2.10(a), capture and emission rates can be calculated as follows:

$$\frac{1}{\tau_c} = \sigma_n v_{th} N_C \cdot exp\left(-\frac{E_C - E_T}{kT} - \frac{\Delta E}{kT}\right) \tag{2.33}$$

$$\frac{1}{\tau_e} = \sigma_n v_{th} N_C \cdot exp\left(-\frac{E_b}{kT}\right) \tag{2.34}$$

$$\frac{\tau_e}{\tau_c} = exp\left(-\frac{E_{T_0} + \Delta E - E_F}{kT}\right) \tag{2.35}$$

where σ_n is the capture cross-section, υ_{th} is the average thermal velocity of the charge carriers, n is the concentration of free electrons at the Si/SiO_2 interface, N_C is the density of electron states at the bottom of the conduction band (E_C), E_T is the trap energy level, E_F is the Fermi level, E_b is the binding energy of the trap, E_{T_0} is the energy position of the neutral (not occupied) trap, and ΔE is the Coulomb blockade energy. In this case, only capture time is affected by ΔE. Thus, the mark space ratio τ_e/τ_c depends on the Coulomb energy. The parameter ΔE in Equation 2.33 is nothing but a fitting parameter allowing to explain the superlinear dependence of τ_c on I_D.

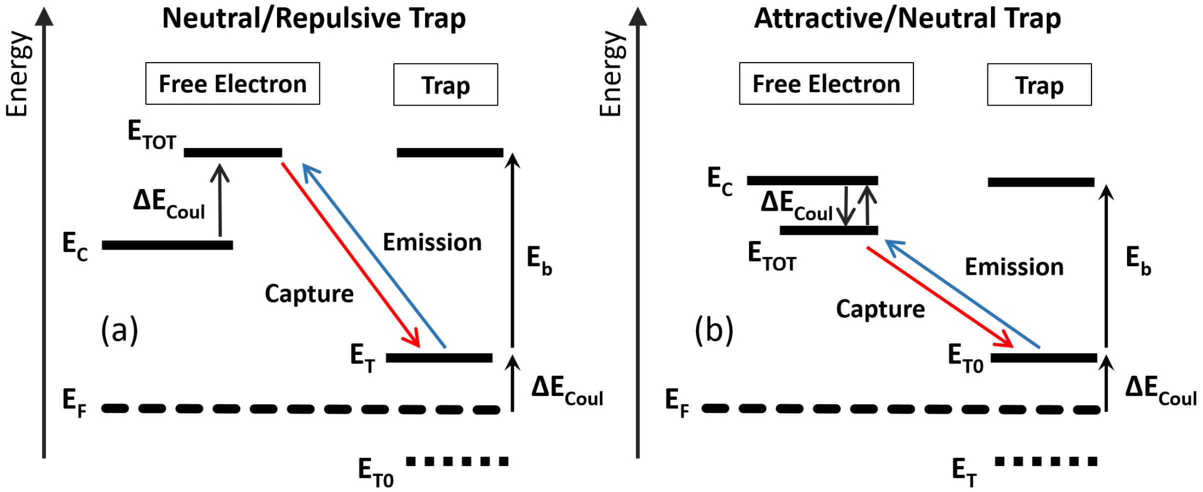


Figure 2.10: Energy-level diagram for the capture and emission of a single electron in a space-charge region by (a) acceptor trap and (b) donor trap. Trapping of a single electron into an acceptor trap with a binding energy (E_b) changes the trap state from the neutral (E_T) to the repulsive state (E_{T0}) which requires additional Coulomb energy (ΔE) to be gained by the electron to reach the total energy (E_{TOT}) and therefore to be captured by the trap. In the case of a donor trap, both capture and emission rates are affected by the Coulomb energy. The single electron gains the Coulomb energy at the position near the trap and changes the trap state from the attractive (E_T) to the neutral (E_{T0}) state. As a result, the unoccupied trap state (E_T) is lowered by the Coulomb energy (ΔE) and a reference level ($E_{T0} + E_b$) lines up with the bottom of conduction-band edge (E_C) in this case. The figure is adapted from Ref. [52].

Considering a donor-type trap that is repulsive for charge carriers when occupied, and following the energy-level scheme shown in Figure 2.10(b), the time constants can be defined as:

$$\frac{1}{\tau_c} = \sigma_n \upsilon_{th} N_C \cdot exp\left(-\frac{E_C - E_T}{kT} + \frac{\Delta E}{kT}\right) \tag{2.36}$$

$$\frac{1}{\tau_e} = \sigma_n \upsilon_{th} N_C \cdot exp\left(-\frac{E_b - \Delta E}{kT}\right) \tag{2.37}$$

$$\frac{\tau_e}{\tau_c} = exp\left(-\frac{E_{T_0} - E_F}{kT}\right) \tag{2.38}$$

Interestingly, as follows from Equation 2.38, the ratio τ_e/τ_c doesn't depend on ΔE for the donor-type trap. This is related to the fact that the donor-type trap becomes a neutral when occupied by a charge carrier, which doesn't induce an image charge on the gate and therefore doesn't change the free-energy of the system. The gate-bias dependence of trapping/detrapping processes accounting Coulomb blockade effect due to trap screening is described in detail in Refs. [52, 55].

2.5.3 Energy quantization model for single traps in nanoscale FETs

The effects of charge quantization on emission and capture times were originally introduced in Ref. [59]. The model is based on the assumption that charge carriers in an inversion layer at a Si/SiO_2 interface are confined in a potential well which results in the quantization of charge carriers motion in the direction normal to the interface. Therefore, two important facts were considered within the model: (1) in an inversion layer, electrons can be treated as two-dimensional electron gas contained in energy subbands; (2) to be captured in the split conduction band, electron emitted from the interface trap must have an additional energy $\Delta E_0 = E_0 - E_{CS}$, where E_0 is the first level of the conduction band and E_{CS} is the conduction band energy at the Si/SiO_2 interface.

Thus, considering the quantization effects of inversion layer, the emission time can be expressed as:

$$\tau_e = \frac{exp\left(E_{CS} - E_t + \Delta E_0/kT\right)}{\sigma_n(2D)\upsilon_{th}(2kTm_t b/5\hbar^2\pi)} \tag{2.39}$$

where $\sigma_n(2D)$ is an average capture cross-section, υ_{th} is an average thermal velocity of the carriers, ΔE_0 is additional energy for electrons to be captured in the conduction band defined as $\Delta E_0 = E_0 - E_{CS}$, where E_0 is the first level of the conduction band, m_t is the transverse effective mass of electrons, E_{CS} is the conduction band energy at the Si/SiO_2 interface, k the Boltzman constant, T is the absolute temperature, $\hbar$ is the reduced Planck's constant.

Considering the conduction band splitting effect and assuming that most of the carriers are located in the lowest (ground) sub-band E_0, capture time is given by:

$$\tau_c = \frac{1}{\sigma_n(2D)\upsilon_{th}n_{2D}\int_0^{\bar{z}}\frac{p(z)}{\bar{z}}dz} \tag{2.40}$$

where $\bar{z}$ is the charge centroid location of the inversion layer and $p(z)$ is the probability function of finding electrons, which defines the localization of the inversion charge (i.e., conductive channel).

Later, a detailed quantum calculation of the transition probabilities between a trap state in the gate oxide and a conductive channel state using the multiphonon transition approach was reported in Ref. [60] for MOSFETs in the inversion regime. Moreover, the contribution of the Coulomb energy [52, 55] was also considered to explain capture and emission time behavior observed for experimentally measured RTS processes in various devices.

2.6 Novel STP-based approach for biosensing with enhanced sensitivity

The extremely sensitive and high-speed detection of target biomolecules is one of the top priorities for the advanced biosensing. In this respect, a new generation of biosensors based on liquid-gated nanoscale FETs, which are electronically sensitive to the biochemical processes that occur on their surface has been recently established. Although the use of these devices as transducers offers considerable advantages such as cost-effective mass-production, there are still many debates around both the best transducer configuration and approach for the detection of the different target analytes. To address these problems and achieve higher sensitivity which may allow even a single-molecule detection, one has to consider the noise level of the transducer element, which usually affects the sensitivity of a sensor and determines its detection limit.

Typically, a single trap statistically capturing and emitting a charge carrier results in RTS noise which determines a noise level of a nanoscale device. Such an RTS process has been traditionally considered as a highly undesirable and parasitic effect in small electronic devices. However, due to its discrete nature and certain features, the RTS phenomenon provides excellent opportunities for its various practical applications including biosensing. For instance, if RTS parameters (e.g., trap occupancy probability, time constants) are monitored, **RTS as a result of STP becomes a signal** rather than just a noise component enabling sensitivity enhancement in comparison to the standard sensing approaches used in the conventional FET-based sensors.

Therefore, instead of the traditional view on this type of noise in liquid-gated FETs, here we propose and define a new separate class of NW FET biosensors exploiting RTS as a signal. For the demonstration purpose, the underlying working and biosensing principle of nanobiosensor exploiting STP is illustrated in Figure 2.11(a) and (b). Below, we introduce and determine all the benefits offered by STP in LG NW FETs for biosensing.

The sensitivity of a conventional LG FET-based sensor monitoring a change of drain current (ΔI_D) as a signal caused by the change of the surface potential ($\Delta\psi_s$) is usually defined as:

$$S_{(I_D)} = \frac{\Delta I_D}{\Delta \psi_s} \tag{2.41}$$

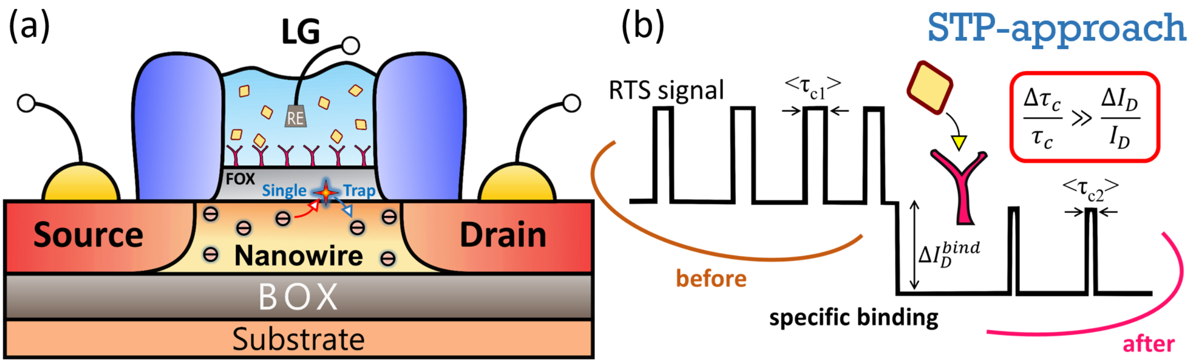


Figure 2.11: (a) Nanotransistor biosensor exploiting STP. The surface of the sensor is functionalized with antibodies providing a selectivity to the analyte; (b) The STP-based approach for biosensing: RTS is used as a signal and characteristic capture time is monitored as a sensing parameter. The sensitivity of the novel STP-approach is improved compared to the standard I_D - approach due to the enhanced RTS dynamic in LG nanosensors.

In the case of STP-approach, the capture time (τ_c) or capture rate ($R_c = \tau_c^{-1}$) can be used as the sensing parameter. Therefore, the sensitivity can be defined as:

$$S_{(R_c)} = \frac{\Delta R_c}{\Delta \psi_s} \tag{2.42}$$

In the bulk semiconductor material under equilibrium conditions, the RTS capture rate typically demonstrates a linear dependence on the concentration of the major charge carriers and can be described using the standard SRH model [61, 62]:

$$R_c^{(SRH)} = \sigma_p \upsilon_{th} p \tag{2.43}$$

where σ_p is the capture cross-section, υ_{th} is the average thermal velocity, and p is the concentration of free holes (in the case of hole capture) at the Si/SiO_2 interface. According to Equation 2.43 and assuming that the drain current is proportional to the concentration of free holes ($I_D \propto p$) in the conductive channel located near the Si/SiO_2 interface, a linear dependence of capture rate on I_D is expected. However, according to the experimental results [53, 56, 63], RTS fluctuations in various devices including LG NW structures demonstrate enhanced capture dynamic behavior indicating a strong dependence of the RTS capture rate on the carrier concentration:

$$R_c \propto p^{\gamma} \tag{2.44}$$

where γ is an exponent of the power function ($\gamma \geq 1$). In the case of SRH model, $\gamma = 1$ which reflects the linear dependence of R_c on concentration p (see Equation 2.43). It should be emphasized that the larger exponent γ in Equation 2.44 corresponds to a stronger dependence of R_c on the concentration of the major charge carriers which is determined by a surface potential as schematically demonstrated in Figure 2.12.

In the case of MOSFETs, the surface potential is controlled by the metal gate and the enhanced dependence of capture dynamic on the carrier concentration is explained within the Coulomb blockade model considering the additional Coulomb interaction of the major carriers with image charges induced on the metal gate electrode [52, 55]. At the same time, energy quantization effects [64–66] should be also considered in cases of the confinement of charge carriers in the conductive channel to explain the superlinear RTS capture rate behavior.

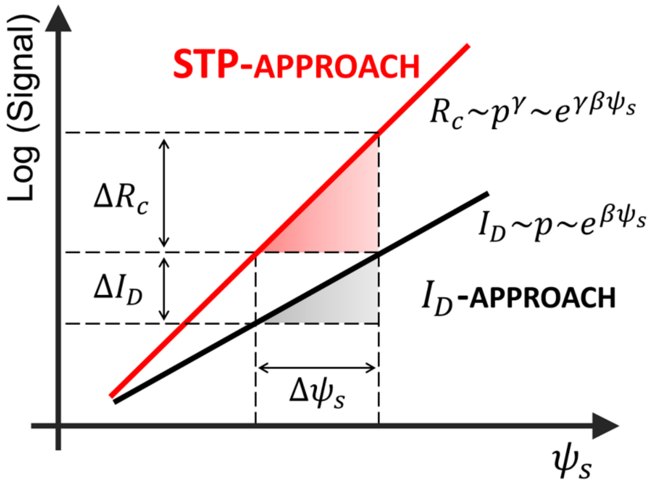


Figure 2.12: Schematic demonstration of a response of the NW sensor to the change in surface potential for different sensing approaches. The slope of the response curve defines the sensitivity of the detection approach. In the case of I_D*-approach*, the sensor demonstrates a linear response to the changes in surface potential (i.e., $\gamma = 1$), while the device exploiting *STP-approach* shows enhanced response with a slope $\gamma \geq 1$ reflecting the sensitivity improvement due to the enhanced RTS capture rate behaviour.

For the LG FET-based sensors, the surface potential is a function of physical and chemical changes caused by specific reactions of the target biomolecules with a sensor's surface. Thus, being a strong function of the surface potential ($\gamma \geq 1$), the enhanced RTS capture rate can be used as a novel sensing parameter to improve the sensitivity of LG FET-based biosensors as schematically shown in Figure 2.12. Below, in this thesis, which combines experiments and theoretical analysis at both numerical and analytical levels, we investigate and demonstrate the unique opportunities offered by STP in LG NW FETs to improve the sensitivity and performance of the nanoscale biosensors.

2.7 Summary

Real-time detection and monitoring of relevant biomarkers with high selectivity and superior sensitivity define a winning strategy against the progressive disease. In this perspective, one-dimensional Si NWs configured as liquid-gated FETs attract much attention as perfect candidates for the development of portable and highly sensitive point-of-care biosensing platform aiming to detect even ultralow concentrations of target biomarkers. A high surface-to-volume ratio of Si NWs and their remarkable scaling properties make them highly sensitive to changes in surface potential caused by electrically charged biomolecules. Such features allow fabrication of biosensors based on Si NWs which are capable of high-sensitive, high-speed, and label-free detection of various bio- and chemical analytes in real-time. To this end, such devices can be fabricated using well-developed CMOS-compatible technology with good size/shape control of NWs resulting in low device-to-device variations. This creates the possibility for mass-production and thus provides an opportunity for mass-screening.

In recent years, the application of Si NW FETs evidenced remarkable progress in biosensing. However, several challenges still have to be met especially from a technological perspective to develop an all-electrical, high-sensitive, high-speed, and portable bio-detection platform based on Si NW FETs capable of rapid and reliable testing of target biomarkers in real-time. For instance, the sensitivity and performance of such devices are still limited by the electrical noise in NW FETs which mainly originate from the interactions of charge carriers with traps in the gate oxide layer. However, as transistor dimensions are reduced, the number of electrically active traps also decreases. In this perspective, when a single trap remains active near the conductive channel in NW FET, a strong modulation of the conductance appears as single-trap phenomena, resulting in two-level characteristic switching known as random telegraph signal noise. Usually, the RTS effect in nanoscale devices is highly undesirable affecting their performance and reliability. However, due to discrete nature and outstanding properties such as ultra-high sensitivity to the changes of surface potential, STP in LG NW FETs provide excellent opportunities for various practical applications including biosensing with enhanced sensitivity and improved signal-to-noise ratio. The main idea is to use the change of STP parameters such as RTS time constants caused by the target analyte as a useful signal. Such a novel STP-based biosensing approach is revealed and discussed in the present work which combines experiments and theoretical analysis at both numerical and analytical levels.

EXPERIMENTAL SETUPS AND ANALYSIS METHODS

3.1 Advanced I-V measurement setup for characterization of nanobiosensors

Measurement of current-voltage (I-V) characteristics is the most common and fast method for obtaining reliable data on the conductivity behavior and transport properties of FET-based devices. To perform I-V characterization of fabricated NW devices, we employed the advanced I-V measurement setup developed in-house (see Figure 3.1).

In general, our fabricated structures can be operated by applying voltage either to the standard $Ag/AgCl$ reference electrode immersed in the electrolyte solution which acts as the liquid gate, or to the substrate which acts as the back gate, or by applying voltages to both gates simultaneously (*double-gate configuration*). For the single-gate measurement configuration, the I-V characterization of the fabricated transistor structures is performed using *Keithley 2400* and *2430* (*Keithley Instruments Inc.*) source-meter units (SMUs) with high bandwidth performance for maximum throughput. Both SMUs allow fully automated and highly accurate electrical characterization of a device under test (DUT) with a resolution of $10\ pA$. Two types of I-V curves known as transfer and output characteristics can be measured using the *I-V setup*. For the transfer characteristics, drain current is measured as a function of gate voltage (i.e. liquid-gate, back-gate) at a constant drain voltage, while for the output curves recording, drain current is measured as a function of drain-source voltage at a constant gate potential. All voltages are applied against the grounded source electrode. The DUT is usually placed in a dark Faraday cage to avoid impacts from any external electromagnetic fields. To control the device quality, the setup also allows simultaneous measurements of gate-induced leakage currents that usually associated with the degradation of the gate dielectric layer or poor quality of the passivation material. It should be noted that devices demonstrating leakage currents were eliminated from further use. To perform I-V measurements of fabricated structures in double-gate configuration, an additional single-channel *Keithley 2635B* SMU with voltage sourcing/measurement accuracy down to $1\ \mu V$ is employed. In this case, the current-voltage characterization is performed using three SMUs as it is schematically shown in Figure 3.1. All the SMUs are connected to a computer through a GPIB-USB adapter.

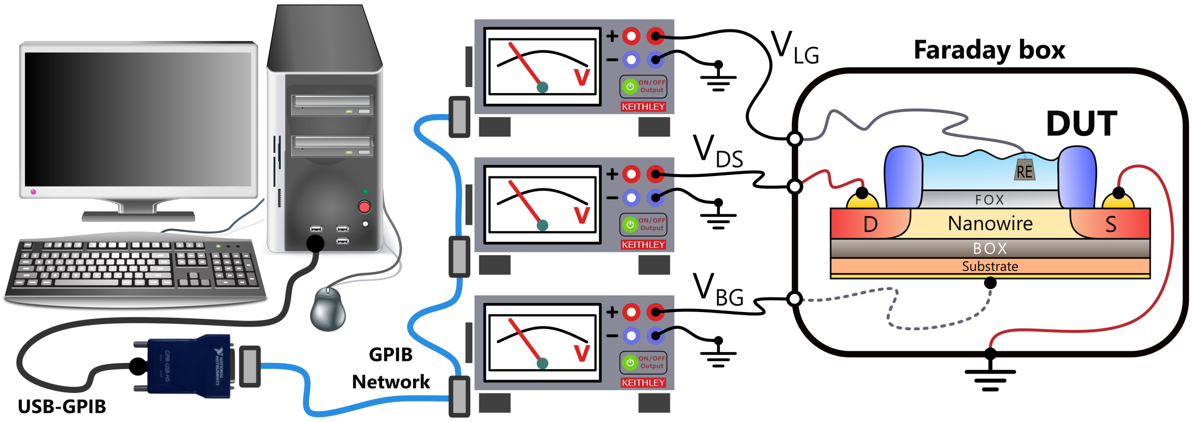


Figure 3.1: Advanced current-voltage characterization setup for the I-V characterization of LG NW FET biosensors.

To interact with the SMUs as well as to read out and collect the measured data, a home-made software package known as *PyIV* is used. The software was developed in our group by Dr. Ihor Zadorozhnyi using *Python* programming language (version 3.4.3) and allows a user to set a wide range of settings such as drain-source and gate-source voltage sweep values, integration time, current compliance, set-measure delay, averaging, etc. In addition, the program provides a possibility to measure both the output and transfer curves in the forward and reverse cycling mode to evidence the occurrence of hysteresis in DUT.

3.2 Noise spectroscopy setup developed in-house

Noise spectroscopy is a non-destructive tool that is indispensable for characterizing of transport as well as the quality and reliability properties of electronic low-dimensional systems such as silicon nanowire FETs. The electrical noise in such devices occurs due to the spontaneous fluctuations in current and voltage inside the device (e.g., due to the presence of traps, lattice damages or other defects) as a consequence of the discrete nature of the electrical charges. The measurement of noise is a very challenging task as the noise to be measured is usually weak signal and might be affected by external disturbances (e.g., electrostatic and electromagnetic irradiation, AC power lines) as well as by noise fluctuations generated from other components in the setup (bias circuit, amplifiers, etc.). Therefore, the noise measurement setup has to be designed carefully with high precision considering proper shielding and accurate measurement process control to avoid undesired disturbances and minimize measurement errors.

A schematic illustration of the low-noise measurement setup used for experimental investigation of low-frequency noise fluctuations in fabricated nanostructures is presented in Figure 3.2. The setup was initially developed in our group by Dr. Viktor Sydoruk, Dr. Mykhailo Petrychuk, and Prof. Dr. Svetlana Vitusevich. Later, the setup has been optimized and fully automatized by Dr. Ihor Zadorozhnyi. The detailed description of the fully automated ultralow-noise measurement setup (*FANS*) is presented in Ref. [67]. The setup allows acquiring the noise spectra in the frequency range from $1\ Hz$ to $250\ kHz$ and time-traces of the voltage fluctuations with the sampling rate up to $500\ kHz$. Such a fast high sampling rate (a high resolution) is required for accurate analysis of the RTS effect in the time domain ensuring that no transition events (capture or emission of a single carrier) are missed. The main parts of the noise measurement setup are briefly described below.

Voltage supply system. The voltage supply system is battery-operated to avoid parasitic fluctuations from circuitry (AC line pick-ups at $50\ Hz$ and its harmonics). Two $6.7\ V$ lead-acid batteries are used as power sources to bias DUT and set the working point. All voltages are applied against the grounded source contact of DUT using BNC cables. The values of the drain-source and gate-source voltage biases are tuned using motorized potentiometers of $2\ k\Omega$ each by applying an external voltage to the control terminals. Such external control of voltage sweep allows flexible operation of the setup leading to an accurate measurement process. The large shunting capacitance of $10\ mF$ connected in parallel to the variable resistor at the input is used to stabilize voltages as well as for AC grounding. The automated voltage supply system allows precise electrical biasing of DUT with the accuracy approaching $1\ mV$.

DC characterization and noise measurement system. The drain-source voltage bias is applied to the serial connection of DUT and a load resistance, R_L which should be selected in such a way that noise from DUT is maximized at the output. Thus, R_L should be larger than the channel resistance of DUT. At the same time, the additive thermal noise from the load resistance should be minimized. Therefore, metal film resistors with negligible low-frequency noise are usually preferable to use in the biasing circuit of the noise measurement setups. In our case, a high-precision, low-inductance resistance box was used as R_L ensuring the possibility to vary resistance value in the range from $1\ \Omega$ to $1\ M\Omega$. Such a connection of a DUT and R_L in series allows measuring drain current flowing through the device using a difference between readings of voltmeters V_m and V_s as follows:

$$I_D = \frac{V_m - V_s}{R_L} \tag{3.1}$$

At the same time, the gate bias is applied directly to the gate of DUT without the use of the load resistance. The value of the gate bias is controlled by voltmeter V_G. All the voltmeters showed in the noise measurements scheme (see Figure 3.2) are represented by the *Agilent U2542A* simultaneous data acquisition (*SDA*) analog input channels (in polling mode configuration). The voltmeters are disconnected from the noise measurement circuit (keys S_1, S_2, and S_3) during the noise data acquisition to avoid any impact on noise measurement results. Noise measurements are performed using an analog input channel in the AC configuration.

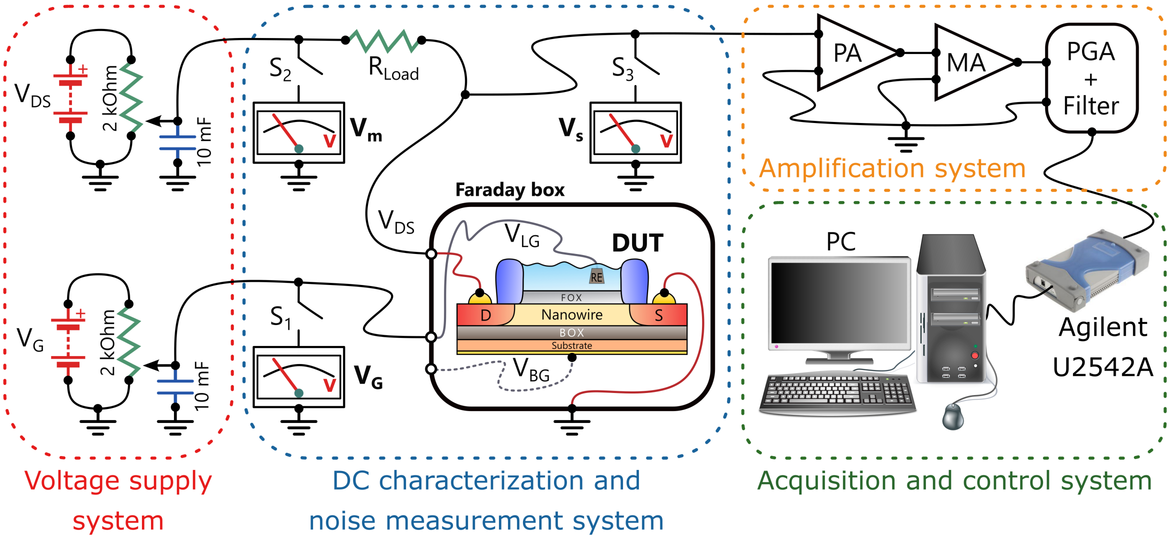


Figure 3.2: Fully automatized advanced noise measurement setup for the characterization of noise properties of LG NW FET biosensors. The setup allows recording of the noise timetrace with the sampling rate up to $500\ kHz$ and acquiring of noise spectra in the frequency range from $1\ Hz$ to $250\ kHz$.

Noise amplification system. Since a noise signal coming from DUT is usually weak to be measured, a low-noise amplification system is used for its amplification. However, the amplification system must be properly designed, since the noise of interest (noise signal from DUT) is inevitably mixed with the internal noise of the amplification system. Therefore, the internal noise of amplifiers used must be as low as possible to suppress the measurement noise limit of the setup. For this purpose, voltage fluctuations from DUT in our setup are firstly pre-amplified by a homemade ultra-low internal noise preamplifier ($k = 172$) developed by Dr. Viktor Sydoruk, Dr. Mykhailo Petrychuk, and Prof. Dr. Svetlana Vitusevich. The preamplifier has the intrinsic noise value $S_V = 10^{-17}\ V^2/Hz$ at $100\ Hz$ which is one order of magnitude lower than, for example, the noise level of the Stanford SR560 amplifier. Such an ultra-low internal noise level of the homemade preamplifier is extremely important for further amplification. The commercial amplifier ITHACO 1201 in AC mode (denoted by MA in Figure 3.2) with a variable gain from 1 to $10k$ in the sufficient frequency range (up to $300\ kHz$) is then used to further amplify the noise signal. Finally, the signal is fed to a low-noise general-purpose programmable-gain amplifier PGA-103 ($k = 1,\ 10$ or 100) and filtered using digitally controlled antialiasing continuous-time filter LTC 1564 with a selected cut-off frequency of $100\ kHz$. To prevent the signal of interest (i.e., noise from DUT) against unavoidable disturbances from the outer environment (e.g., electromagnetic signals, high-frequency pulses from radio transmitters and other active elements), the bias circuit, DUT, and the amplification system are shielded using Faraday cages made of iron. The background noise of the system can be measured separately and later substructed from the total noise measured with the device connected.

Acquisition and control system. The output from the noise amplification system is then recorded using the Agilent U2542A SDA device. The sampling rate is set to a maximum value of $500\ kHz$ allowing the best possible time resolution for the hardware used. To calculate the voltage noise power density spectrum from the measured time trace, the Fast Fourier Transform (FFT) of the data is performed as follows:

$$S_V(f) = \frac{FFT^*(signal) \times FFT(signal)}{N^2} \tag{3.2}$$

where N stands for the number of points in the measured signal array and $(*)$ represents a complex conjugate. To recalculate the current noise PSD from the measured voltage noise PSD spectrum, the following expression can be used:

$$S_I = \frac{S_V}{R_{eqv}^2} \tag{3.3}$$

where R_{eqv} is the equivalent resistance. At low frequencies, when the parasitic capacitance of the circuit and the capacitance of DUT are negligibly small, the equivalent resistance can be determined as follows:

$$R_{ekv} = \frac{R_S R_L}{R_S + R_L} \tag{3.4}$$

where R_L is the load resistance and R_S is the resistance of the sample. Two boundary regimes of noise measurements are possible: constant current mode (*idle mode*) when $R_L >> R_S$, and constant voltage mode (*short circuit mode*) when $R_L << R_S$. In practice, intermediate modes are usually implemented, with the equivalent resistance determined by the expression 3.4.

FANS is controlled using software called *PyFANS* that was developed in our group by Dr. Ihor Zadorozhnyi. The software is implemented using Python programming language (Python version 3.4.3) and allows us to control all main components of the measurement setup responsible for the voltage supply, data acquisition, and storage. It should be noted that FANS can also be used for the advanced measurement of low-frequency noise of not only Si NW FETs, but also of other similar nanodevices (e.g., BJTs, graphene FETs, carbon nanotube FETs).

3.3 Low-temperature cooling system for the identification of single traps

To investigate outstanding features of single-trap phenomena in detail and extract important characteristics of single traps (e.g., energy level, capture cross-section), electrical and transport properties of Si NW FETs have to be studied in a wide temperature range. For this purpose, we developed and assembled an advanced low-temperature setup allowing us to cool the device from the room temperature down to $70\ K$. This temperature range is sufficient for detailed investigation of transport properties to extract the aforementioned parameters of single traps. The composition of the setup is schematically presented in Figure 3.3. The setup consists of two main parts which are briefly described below: the *cryogenics* and the *electronics*.

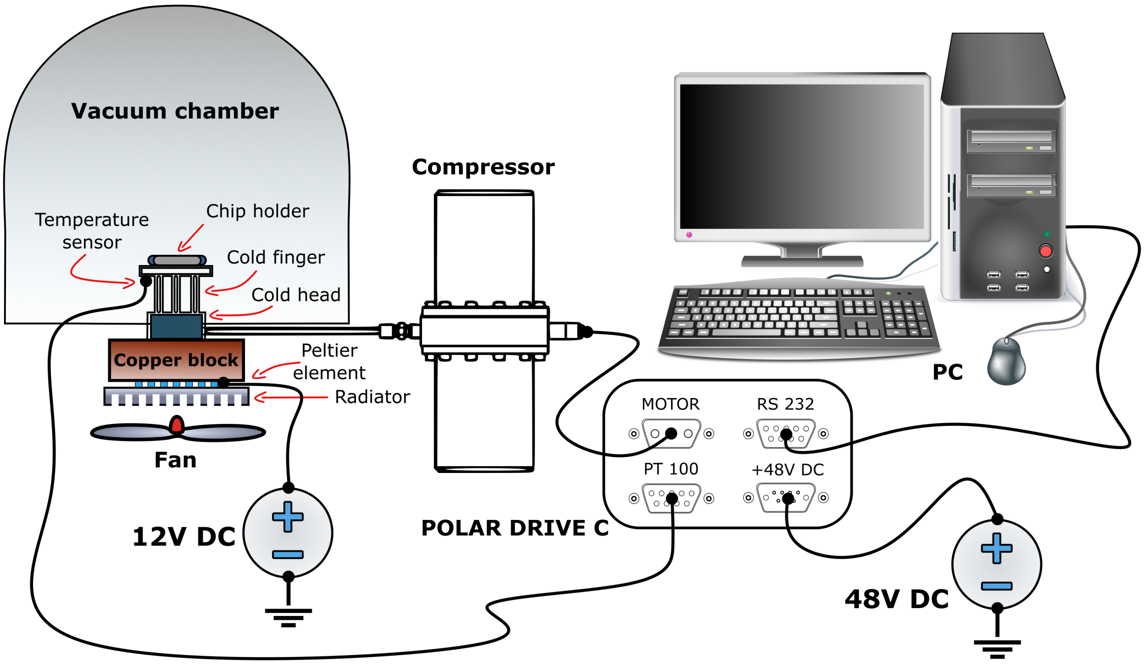


Figure 3.3: Low-temperature cooling system for the investigation of transistor devices at low temperatures down to $70\ K$.

The low-power Stirling cryocooler *POLAR SC-7 COM* purchased from *Leybold* was used as a main cooling unit. The operation of this cryocooler is based on the thermodynamic Stirling cycle in which helium is used as the working gas. The cold head with the cold finger on the upper part is linked through the helium line to the compressor equipped with the linear drive motor and dual-opposed pistons for vibration reduction. Such a configuration with temperature control allows the cold finger to be cooled down to cryogenic temperatures ($70\ K$). To avoid overheating of the compressor and the cold head, vibration-free thermoelectric coolers based on the Peltier phenomenon were used. The Peltier module consists of two bismuth-telluride Peltier elements which are directly connected to the $12\ V$ electrical power supply. The Peltier module pumps heat out from the large-sized copper block, which serves as a heat sink for the cold head of the Stirling system. To dissipate both the heat pumped by the Peltier module and its joule heat, the radiator and powerful fans were additionally mounted. Electronic control of the linear Stirling cooler is provided by the POLAR DRIVE D unit which ensures the necessary $48\ V$ AC voltage supply and controls the temperature at the cold finger within the range from $70\ K$ to $300\ K$. The POLAR DRIVE D unit is controlled via the RS 232 interface. To monitor the established temperature of the DUT, the PT 100 temperature sensor was mounted directly on the chip-holder, which is connected to the cold finger through a copper braid to decrease the vibration. The chip-holder can hold one encapsulated chip and provides electrical connections between contact pads of the chip and the electronics outside the vacuum chamber (i.e., I–V, C-V or noise measurement setup). The developed temperature setup allows the electrical characterization of DUT at different temperatures down to $70\ K$ with an achieved maximum deviation of $0.1\ K$ between established and desired temperatures. The time needed to stabilize the temperature depends on how low the desired temperature lies below the room temperature. For example, it takes only several minutes to cool a sample down to $200\ K$.

3.4 Analysis of Random Telegraph Signal (RTS) noise and extraction of the STP characteristic parameters

There are several techniques for extracting characteristic time constants and amplitudes of RTS [15, 68–70]. When the ratio of the RTS amplitude to background noise is relatively high and the low-frequency drift of the measured signal is low, the RTS parameters can be extracted directly from the time-trace. For instance, in this case, a relatively simple threshold level-crossing or time-derivative algorithms [71] can be applied to successfully determine all the transition events and thus to calculate the average characteristic times which system spends in each capture or emission state. A two-level clean RTS extracted from the noisy RTS data using the aforementioned methods is shown in Figure 3.4(a). More advanced methods for analyzing RTS in the time domain allowing to obtain more precise and detailed information about the RTS phenomenon are the weighted-time-lag technique [72, 73] and the segmental k-means method based on hidden Markov modeling [69, 74].

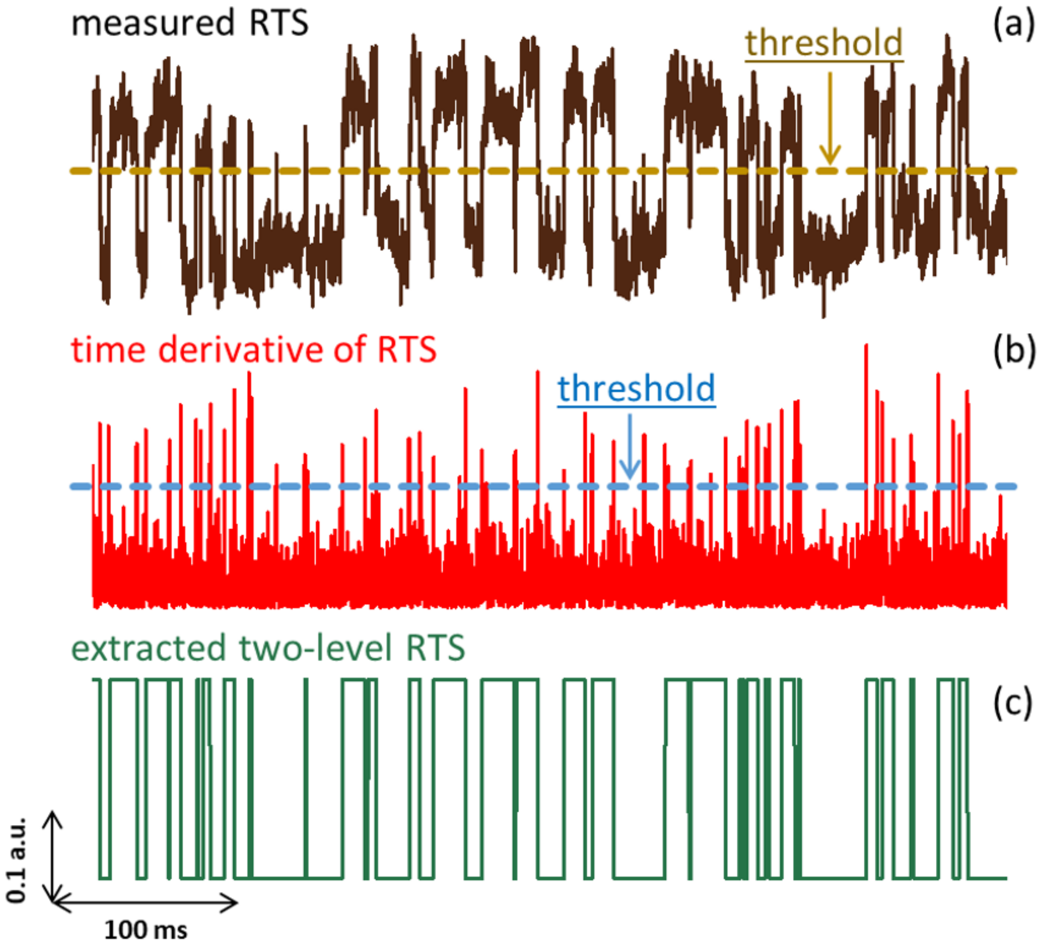


Figure 3.4: RTS analysis: (a) threshold level-crossing method and (b) time-derivative algorithm; (c) Reconstructed clear RTS time trace.

However, when the ratio of the RTS amplitude to background noise is low (see Figure 3.5(a)), another approach that involves the analysis of both time and frequency domain data can be applied. In this case, the analysis of time-domain data is performed using the signal level histogram method [53, 68]. The distribution of the RTS amplitude for each RTS state typically shows a good separation between the RTS signal levels, which are centered at the mean values and can be fitted with a Gaussian distribution function, $f_g(x)$ (see Figure 3.5(b)):

$$f_g(x) = \frac{1}{\sqrt{2\pi\sigma^2}} e^{-\frac{(x-\mu)^2}{2\sigma^2}} \tag{3.5}$$

where μ is the mean value of the distribution, and σ is its standard deviation.

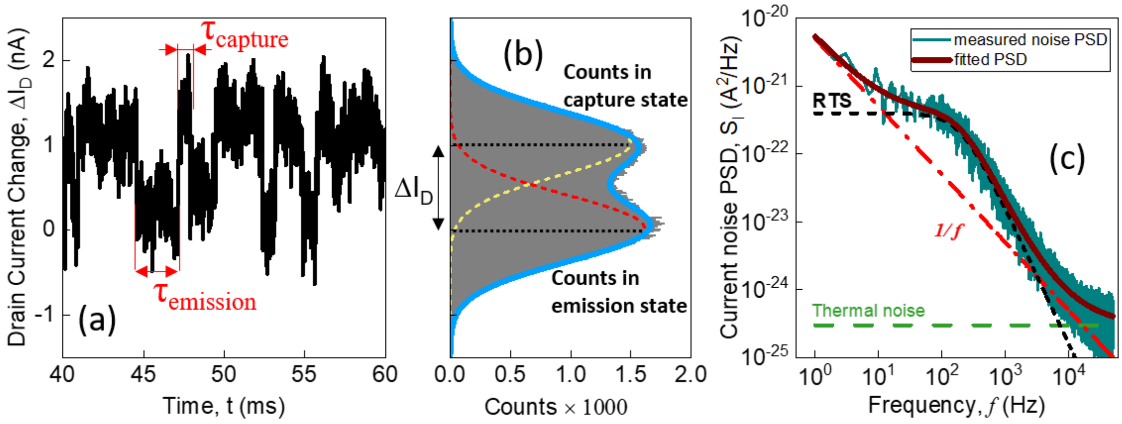


Figure 3.5: (a) Typical "noisy" RTS time trace which requires a statistical method to be applied for the analysis; (b) Amplitude histogram obtained from (a); (c) Current noise PSD of measured time trace as a function of frequency. The PSD spectrum is fitted using Equation 3.7.

In the case of two-level RTS noise, two Gaussian peaks are well-resolved demonstrating the two-level switching kinetic of the RTS signal due to STP. The distance between two Gaussian peaks corresponds to the RTS amplitude. At the same time, the height of each peak reflects the probability of finding the system in a certain RTS state. Therefore, the ratio between heights of two Gaussian peaks corresponds to the relation between capture and emission characteristic times. To extract the average capture and emission times, the following system of equations can be used:

$$\begin{cases} \tau = 1/(2\pi f_0) \\ \dfrac{\tau_c}{\tau_e} = \dfrac{Counts(capture)}{Counts(emission)} \\ \tau = \dfrac{\tau_c \tau_e}{\tau_c + \tau_e} \end{cases} \tag{3.6}$$

where f_0 denotes the corner frequency of the RTS noise, which can be obtaining from the fitting of the frequency domain data. Normally, the measured PSD contain several overlapping noise components at low frequencies. If the noise sources are not correlated with each other, then the

PSD spectrum can be decomposed. In the case of a FET device with a single trap, the current noise PSD spectrum can generally be mathematically expressed as:

$$S_I(f) = A + \frac{B}{f} + \frac{C}{1 + (f/f_0)^2} \tag{3.7}$$

where A, B and C are the white noise, the flicker noise, and the Lorentzian noise amplitudes, respectively, and f_0 is the RTS corner frequency. An example of the fitting of a PSD spectrum treated as a superposition of different noise components is presented in Figure 3.5(c).

3.5 Summary

In this chapter, we presented a brief overview of experimental setups employed for electrical and noise spectra characterization of the developed NW biosensors. The exploitation of advanced characterization methods such as I-V measurements and noise spectroscopy technique allows a comprehensive study of the electrical and noise performance as well as accurate investigation of transport features of fabricated transistor-based biosensors in a non-destructive manner. Moreover, detailed noise measurements using the fully automated noise measurement setup can be performed to characterize and localize individual traps responsible for the RTS noise in nanoscale devices. In this perspective, studies of the electrical transport and noise properties of fabricated NW structures can be also carried out at low temperatures using the advanced low-temperature measurement setup. In particular, the characterization at low temperatures is required to extract important information about the origin of single traps causing RTS noise in fabricated TL NW FETs. The main techniques of determining the average RTS characteristic times and amplitude of the RTS noise are also considered in this chapter. The described characterization tools and data analysis methods were used to obtain and analyze the results presented and discussed in this work.

NOVEL SILICON TWO-LAYER NANOWIRE BIOSENSORS

4.1 Design and fabrication of Two-Layer (TL) Nanowire (NW) FET devices

Nanowires are unique nanomaterial promising for many fundamental studies as well as for nano - and bioelectronics applications. In this work, we designed and fabricated nanowire structures configured as liquid-gated (LG) field-effect transistors (FETs) to study single-trap phenomena for the ultimate biosensors' scaling and sensitivity enhancement. To investigate the impact of channel doping concentration on the dynamics of charge exchange processes between a single trap and a nanowire channel, we developed unique **Two-Layer (TL) NW structures** that consist of two silicon layers with different doping concentrations. In this chapter, a fabrication process of silicon TL NWs on low-doped silicon-on-insulator (SOI) substrates is described and electrical as well as noise characteristics of fabricated devices are studied and discussed. The fabrication process flow is based on a top-down approach and involves electron-beam lithography and anisotropic wet chemical etching to define the NW structures. To specify the concept and determine optimal conditions for the application of STP for biosensing, the nanowire devices with different layouts and geometries were designed and fabricated. The main fabrication steps, as well as designs of the fabricated devices, are described below. All the steps were performed at the Helmholtz Nano Facility (HNF) of Forschungszentrum Jülich (FZJ) GmbH.

4.1.1 Chip layout designs and configurations

For the silicon nanowire chips, two different design layouts were developed and used. In the linear design layout, FET structures are spatially distributed along a straight line in the middle of a chip. In the case of the grid layout, the structures are arranged in a grid. Chips in linear and grid layouts are schematically shown in Figure 4.1(a) and Figure 4.1(b), respectively.

The linear configuration offers great potential for using a common microfluidic channel on top of the chip, which provides improved control over the gating solutions. At the same time, the grid layout gives a benefit to the device integration density allowing more dense packaging. The outer chip dimensions are $11 \times 11\ mm^2$. Regardless the layout, each chip contains 32 independent single-nanowire-based transistors. All the designs for the nanowire structures were developed using the *CleWin 4 Layout Editor* program (*Phoenix Software*).

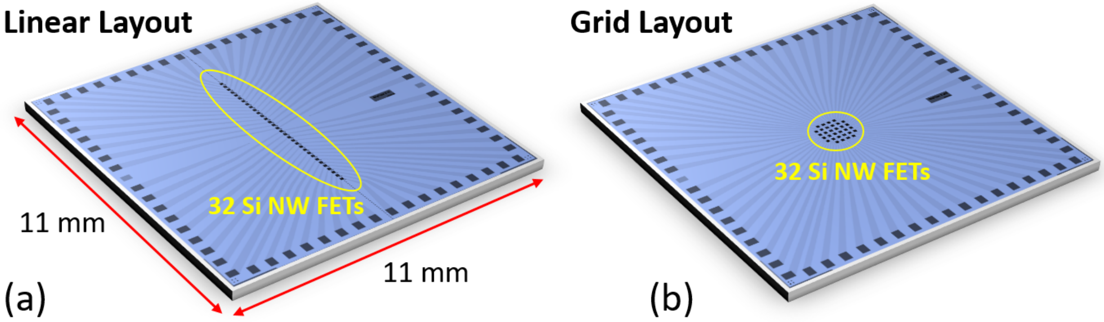


Figure 4.1: Chip Layouts: (a) linear, and (b) grid layouts. Each layout contains 32 independent FETs. The linear layout is more suitable for a microfluidic utilization, while the grid layout is important for the cell measurements allowing the mapping of electrical signal propagation [75].

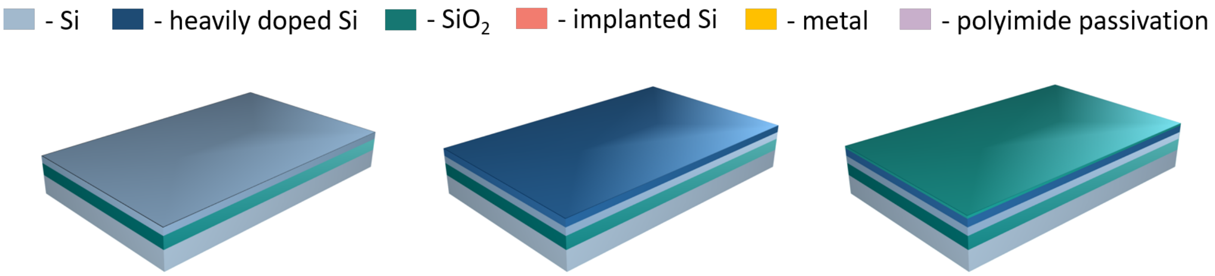
4.1.2 Development of the fabrication technology for TL NW FETs

The novel silicon two-layer nanowire structures were fabricated on the basis of uniform SOI wafers with the low-resistivity ($14 \div 18\ \Omega \cdot cm$) and the low-doped (boron-doped, $N_A = 10^{15}\ cm^{-3}$) p-type layer of silicon with (100) crystallographic orientation. The initial thickness of the top active Si layer of SOI wafers was 50 nm separated from the highly doped silicon substrate (boron-doped, $N_A = 10^{17}\ cm^{-3}$) by a $145\ nm$ thick buried oxide (BOX) layer. The SOI wafers were commercially purchased from SOITEC, France. The major steps of the developed fabrication technology are described below and schematically shown in Figure 4.2.

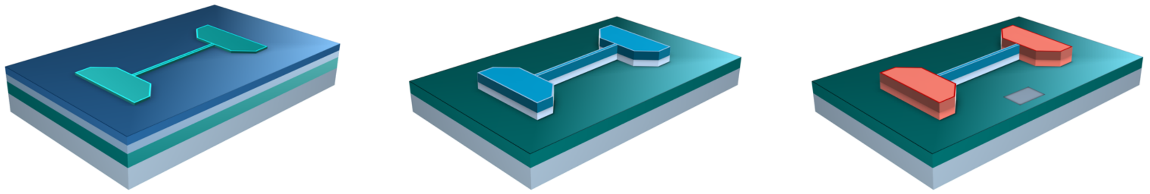
Epitaxial growth of doped silicon layers

To fabricate TL NW structures with different doping concentrations, the reduced-pressure chemical vapor deposition (RP-CVD) epitaxy was employed. The method relies on the decomposition of gaseous chemicals (precursor gases) and the absorption of their atoms onto the surface of the substrate resulting in the formation of the epitaxial film.

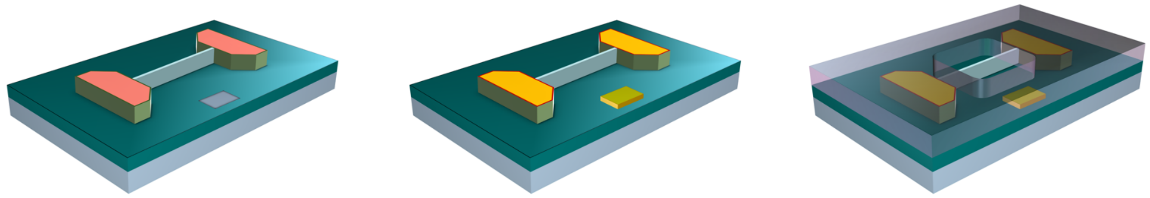
Before growth of doped Si layers, the SOI wafers were baked at a high temperature ($1000\ °C$) for $1\ min$ in H_2 atmosphere and treated with HF vapors to eliminate any surface contaminations and remove native oxide. Then, the silicon epitaxy process was performed at $800\ °C$ employing an industry-compatible metal cold-wall *AIXTRON Tricent RP-CVD* reactor. The disilane (Si_2H_6) and diborane (B_2H_6) have been used as silicon and dopant precursors, respectively. The average growth rate was around $10\ nm/min$. The doping level of newly grown films was controlled by changing the diborane flow rate according to the prior-performed calibration. All epi-layers with thickness $30\ nm$ were grown on the $200\ mm$ SOI wafers with the initial $50\ nm$ thin low-doped top Si layer ($N_A = 10^{15}\ cm^{-3}$) resulting in the two-layer p-type silicon material with different concentrations of Boron dopants.



(a) SOI wafer (b) Epitaxy (c) Oxidation



(d) NW patterning (e) NW etching (f) Implantation



(d) Gate oxidation (e) Metallization (f) Passivation

Figure 4.2: Process workflow for the fabrication of Si TL NW structures using the top-down approach. Note that the step (e) allows to obtain high-quality Si NW structures with almost atomically flat sidewalls and reduced defect density.

Doping profiles and concentrations of Boron dopants in the grown epi-layers were evaluated and analyzed by secondary ion mass spectrometry (SIMS) analysis method. The SIMS profiles of two SOI wafers (namely $SOI\#3R$ and $SOI\#7R$) after epitaxy are shown in Figure 4.3. Herein, two distinct regions (layers) of silicon with different contents of Boron dopants can be clearly distinguished. The lower region features a constant B-doping plateau which corresponds to the intrinsic $50\ nm$ thin low-doped Si layer of the initial SOI wafers. The top part of the depth profiles ($\sim\ 30\ nm$) shows a gradual depth distribution of Boron dopants obtained for both wafers. In the near-surface region ($1-3\ nm$ from the interface), a sharp increase in the concentration of boron dopants is also observed. This may be related to the excess of diborane molecules in the reactor chamber which leads to unintentional doping of the near-surface region. However, this region is sacrificed during further fabrication steps. Therefore, the highest impurity concentrations as determined from SIMS analyses can be considered as 10^{16} and $10^{17}\ cm^{-3}$ for $SOI\#3R$ and $SOI\#7R$, respectively. After the epitaxy, the SOI wafers

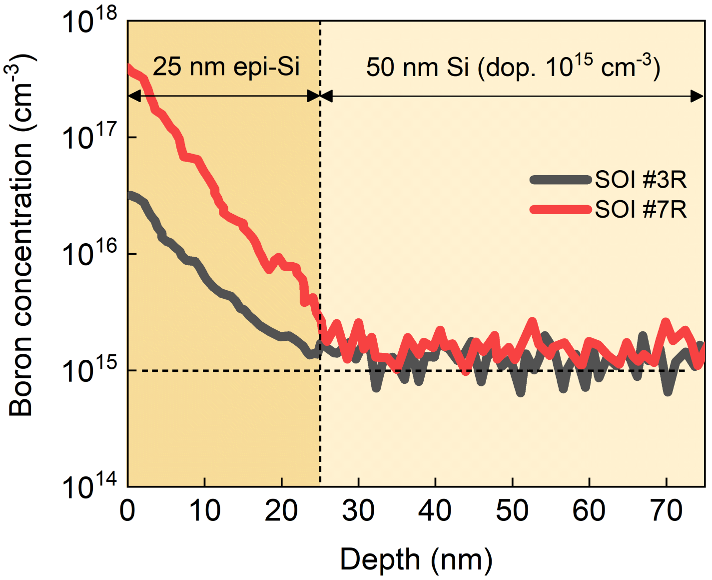


Figure 4.3: SIMS depth profiles for the p-type Si layers with different doping concentrations. The layers were epitaxially grown on top of the low-doped SOI wafers.

were further used to fabricate silicon nanowire structures. Devices fabricated on the basis of such epitaxially overgrown SOI wafers we will further refer to as silicon *"two-layer"* nanowire structures. At the same time, single-layer nanowire FETs with doping of $10^{15}\ cm^{-3}$, which are also studied in this PhD thesis from the STP performance point of view, were fabricated in our group by Dr. Ihor Zadorozhnyi.

SiO_2 hard mask formation

Etching of uniform and precisely defined silicon nanowire structures requires the utilization of a hard mask. For this purpose, an $18-20\ nm$ thin SiO_2 layer was thermally grown on top of the SOI wafers and used as a hard mask material for subsequent wet chemical etching of the nanowires. As an alternative, the oxide layer can be also deposited using a plasma-enhanced chemical vapor deposition (PECVD) method. However, thermally grown SiO_2 is usually denser than the PECVD SiO_2 layer and hence results in smaller edge roughness of Si NWs after patterning. Before the oxidation, a standard RCA cleaning procedure was performed to remove all the organic and non-organic residuals from the wafer surface. Afterward, the clean SOI wafers were directly oxidized in a rapid thermal oxidation furnace in a dry oxygen atmosphere at $1000\ ^{\circ}\mathrm{C}$ for $40\ min$ resulting in a high-quality and uniform silicon oxide surface. The thickness of the thermally grown SiO_2 layer across the wafers was systematically evaluated using an ellipsometer in a mapping mode. A typical mapping of the thickness of the SiO_2 hard mask layer is shown in Figure 4.4(a). The results demonstrate that the SiO_2 layer is uniform over the SOI wafer.

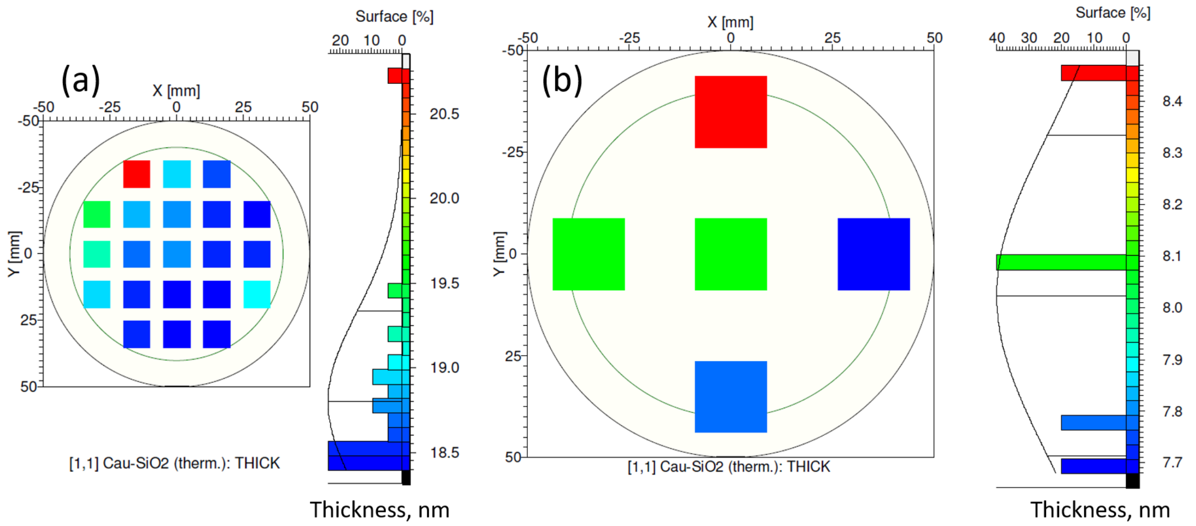


Figure 4.4: 2D mappings of the thickness profile of (a) SiO_2 hard mask layer and (b) gate oxide layer that were thermally grown on top of the SOI wafer during the fabrication process of NW structures.

Definition of alignment markers

Proper alignment of patterns is essential for the fabrication of high-quality and well-defined nanostructures. For this purpose, the alignment markers need to be implemented and used. The fabrication of designed nanostructures involves the utilization of both e-beam lithography and photolithography steps. As e-beam alignment markers, we used a pattern consisting of 4 squares with the side of 20 μm and a spacing of 100 μm located in the corners of every chip on the wafer. At the same time, the alignment markers for the optical lithography were defined on the periphery of the SOI wafers and contain patterns for a high precision alignment with an accuracy of 100 nm. Figures 4.5(a) and 4.5(b) depict the corresponding alignment markers. All markers are defined by the conventional photolithography followed by reactive ion etching (RIE).

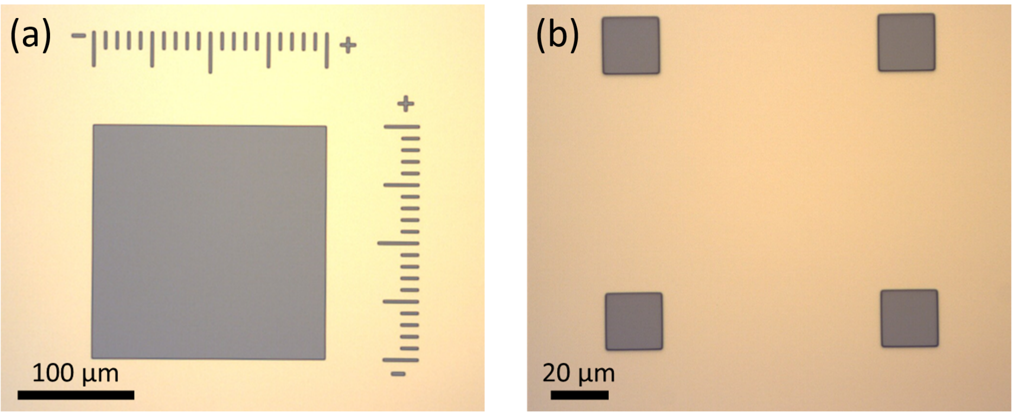


Figure 4.5: Alignment markers for (a) optical and (b) e-beam lithographies.

The general sequence for markers definition process is as follows:

- To obtain a resist film without any stains and spots due to residuals and also to prevent complete or partial delamination of the photoresist film during further processing, oxidized SOI wafers are properly cleaned using acetone and isopropanol (IPA) solutions, and dried with N_2 gas flow.
- To ensure proper wetting and good adhesion of the resist to the substrate surface, the substrate is dehydrated before coating during $5\ min$ at 180 °C hotplate followed by vapor priming with hexamethyldisilazane (HMDS) adhesion promoter at 130 °C.
- The deposition of negative photoresist $AZ^{®}nLOF$ 2020 is then performed by spin-coating at $4000\ rpm$ (for details see *Appendix A*).
- After applying the photoresist, the soft bake at 110 °C for $1\ min$ is performed to stabilize the photoresist layer by removing water and excess solvent. This reduces the thickness of the layer making it less sticky to a photomask used in the following exposure step.
- The alignment and exposure step are then performed using $Mask\ Aligner\ MA4$ from $Suss\ MicroTec$ (Germany) deploying a $365\ nm$ UV light source. For the UV exposure of the $AZ^{®}nLOF$ 2020 photoresist, the constant exposure dose of $40\ mJ \cdot cm^{-2}$ is used. To improve the results of the photolithography process and achieve the high-quality and high-resolution transfer of the pattern from the photomask to photoresist, the exposure is performed in the contact mode. The photomask is cleaned with acetone and IPA solutions and thoroughly blown dry with N_2 gas flow before the use.
- The next step is the post-exposure bake (PEB) for $1\ min$ at direct contact on a hotplate at 110 °C. The step is required for proper imaging of $AZ^{®}nLOF$ 2020.
- After the exposure and PEB, the wafers are developed with $AZ^{®}326\ MIF$ developer for $45\ s$, rinsed with DI water and blown dry with an N_2 gas flow.
- After the development, the wafers are hard-baked on a hotplate at 120 °C for $2\ min$ to harden the final pattern of the markers developed in the photoresist layer. This step determines the final shape of the photoresist profile and helps the developed structures to withstand the subsequent transfer into the SOI employing reactive ion etching (RIE).
- The final RIE process of markers etching consists of several steps. Firstly, the $20\ nm$ thin SiO_2 hard mask is etched for $40\ s$ in CHF_3/Ar plasma. Then, the active Si layer of SOI wafers is etched in SF_6/O_2 plasma for $17\ s$. As the next step, the BOX layer is completely etched through with CHF_3/Ar plasma within $7\ min$. Then, the silicon substrate of SOI wafers is etched withSF_6/O_2 plasma for $21\ s$. Finally, O_2 plasma is used for $2\ min$ to remove $AZ^{®}nLOF$ 2020 photoresist.

As a result, the $600\ nm$ deep holes in SOI wafers were patterned and further used as high-contrast markers in the following e-beam lithography as well as photolithography steps (see Figures 4.5(a) and 4.5(b)). After the alignment markers have been etched, the hard mask for patterning of silicon nanowire structures was then defined by a two-step approach. In the first step, a hard mask for later etching of silicon nanowires was defined by employing e-beam lithography and subsequent RIE etching. In the second step, the optical lithography followed by the RIE process was performed to define mask patterns for etching of mesa structures.

E-beam lithography

E-beam lithography was used to define the initial NW structures in the poly(methyl methacrylate) (PMMA) resist ($AR - P\ 649.04K$). PMMA is a positive-tone nonchemically amplified resist which demonstrates high-sensitivity to e-beam exposure enabling high-resolution and high-contrast lithographic performance. Being also easy to use and demonstrating very good adhesion to different materials including Si/SiO_2, the PMMA resist is commonly used for nanofabrication. The spin-coating of PMMA resist on the oxidized SOI wafers was performed at $4000\ rpm$ resulting in approximately $150\ nm$ thick resist layer (for details of PMMA coating procedure see *Appendix A*). The nanowire structures were then written by e-beam lithography into the PMMA layer. In our case, for the e-beam writing of nanowire structures in the PMMA resist, we used the dose of $270\ \mu C \cdot cm^{-2}$ with the beam step size of $5\ nm$. The dose was estimated as optimal after a batch of performed dose tests. After the e-beam exposure, the structures were developed in $AR - P\ 600 - 55$ solution for $1\ min$. The IPA solution was used to stop the development process. Then, the RIE process with CHF_3/Ar plasma was performed for $40\ s$ to transfer the developed nanowire structures into the SiO_2 layer, which served as the hard mask for the further transfer of the pattern into the silicon layers of SOI wafers using wet chemical etching. The remaining PMMA resist mask was then stripped-off using high-power inductively coupled O_2 plasma for $2\ min$.

Mesa structure definition

After the definition of the hard mask for nanowires etching, we then defined a pattern for mesa structures in the SiO_2 layer using photolithography followed by RIE etching. For this purpose, the wafers were coated with the optical photoresist $AZ^{®}\ 5214E$. Before the coating, the samples were first cleaned with acetone and IPA, and dehydrated at 180 °C for $5\ min$. To further prepare the surface of the wafers for good adhesion of the photoresist, a priming process at $130\ °C$ using HMDS was performed. Finally, the samples were spin-coated with the $AZ^{®}\ 5214E$ positive photoresist at the spin speed of $4000\ rpm$ and then soft-baked at 110 °C for $1\ min$. Afterwards, the wafers were aligned according to the previously defined high-precision markers and exposed to UV light with a constant dose of $75\ mJ \cdot cm^{-2}$. The development of the photoresist was then performed in $AZ^{®}$ 326 MIF basic developer for 1 min. Afterwards, the transfer of the developed mesa structures into the SiO_2 layer was carried out by means of RIE etching using the same recipe as for the definition of hard mask for nanowires (described above). Figure 4.6 shows the final SiO_2 hard mask defined for the following wet etching of the silicon nanowire structures.

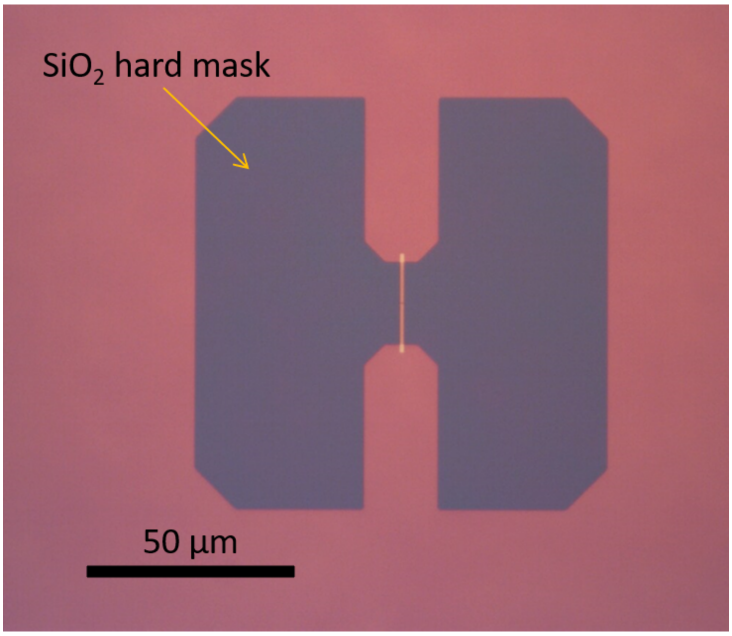


Figure 4.6: Optical image of the SiO_2 hard mask for the TMAH wet-etching step. The mask is defined using the developed two-step approach.

Etching of TL NW transistor structures

To achieve silicon TL NW devices with a smooth surface and reduced defect density, we transferred the previously defined hard mask pattern to the active silicon layers of SOI substrates using highly anisotropic wet chemical etching in tetramethylammonium hydroxide (TMAH) solution. To perform a uniform etching of silicon TL NW structures, the samples were first cleaned in the Piranha solution (1 : 3 v/v $H_2O_2(30\%)$: $H_2SO_4(96\%)$) for 10 min and extensively washed in pure DI water. After the cleaning step, the wafers were exposed in 1% HF solution for 30 s to remove a native SiO_2 and rinsed in DI water for 1 min. Finally, the wet chemical etching was then directly performed in the 5%-TMAH solution at 80 °C for 20 s and stopped by immersing the wafers in DI water. An optical image of a silicon chip and an individual TL NW transistor structure after wet-etching in TMAH solution are shown in Figure 4.7(a) and 4.7(b), respectively. Typical high-resolution scanning electron microscope (SEM) images of well-defined TL NW FET structures with different lengths are presented in Figure 4.8(a) and Figure 4.8(b).

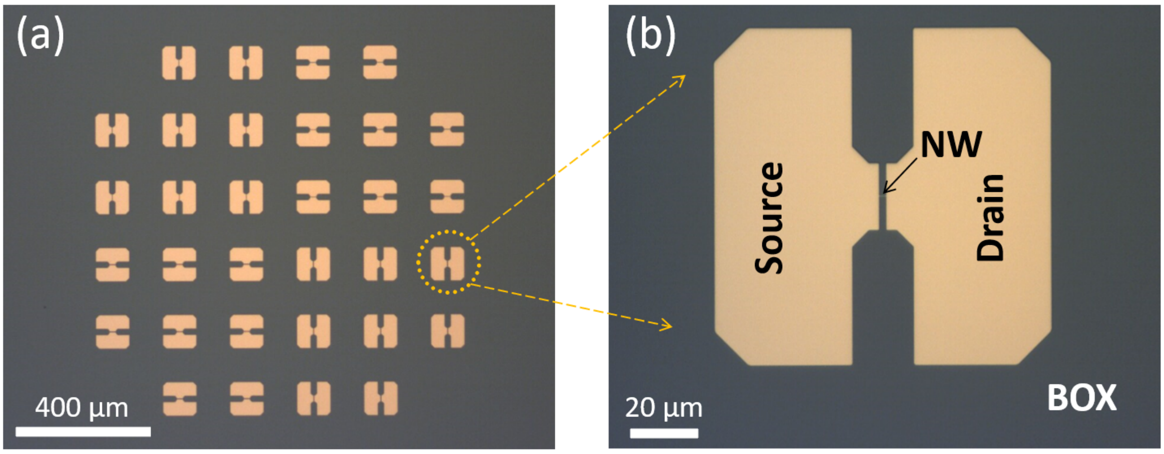


Figure 4.7: (a) Optical image of a silicon chip in grid layout after the TMAH wet-etching process. (b) An individual Si TL NW FET-based structure defined in Si layers of SOI wafer.

TMAH etching of silicon is a highly anisotropic process that depends on the crystal orientation of a Si substrate. The etch rate of Si in the vertical direction (Si (100) crystallographic plane) is usually much faster compared to the slow etching in the lateral direction (Si- (111) crystallographic plane). Therefore, locally defined Si NWs have a trapezoidal cross-section. Typical cross-sections of fabricated nanowires are shown in Figure 4.9(a). As can be seen, being the relatively slow etching plane in the TMAH solution, the (111)-plane sidewall facets can be clearly resolved. Moreover, by adjusting the etching time and initial width of SiO_2 hard mask, we were able to fabricate nanowires with different cross-sections – from trapezoidal to triangular - in order to find the optimal geometry of the TL NW devices from the perspective of STP. A triangular cross-section of the fabricated NW is shown in Figure 4.9(b). Therefore, TL NW structures with different geometrical parameters were designed and fabricated. The lengths of the fabricated devices vary from $100\ nm$ to $4\ \mu m$ and the widths vary from $70\ nm$ to $500\ nm$.

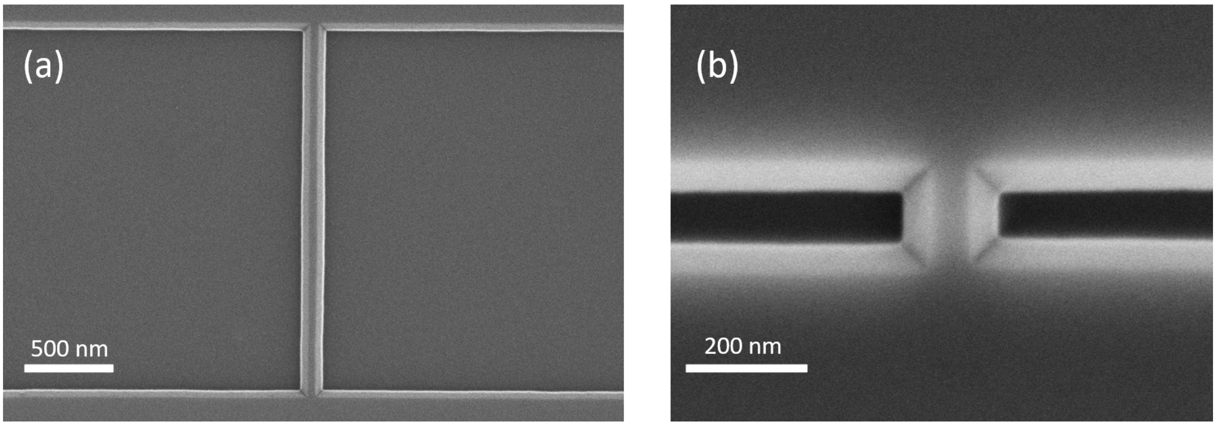


Figure 4.8: High-resolution SEM images of (a) $2\ \mu m$ and $200\ nm$ long fabricated Si TL NWs. The width of bottom part of depicted nanowires is $100\ nm$.

After the etching, the remaining SiO_2 hard mask was removed in a 1% HF solution for 3 min and a standard RCA cleaning step was carried out to clean the substrates. Afterward, a 5 nm thin SiO_2 layer was thermally grown on the top of the patterned structures to protect the surface of nanowires in the following ion implantation step.

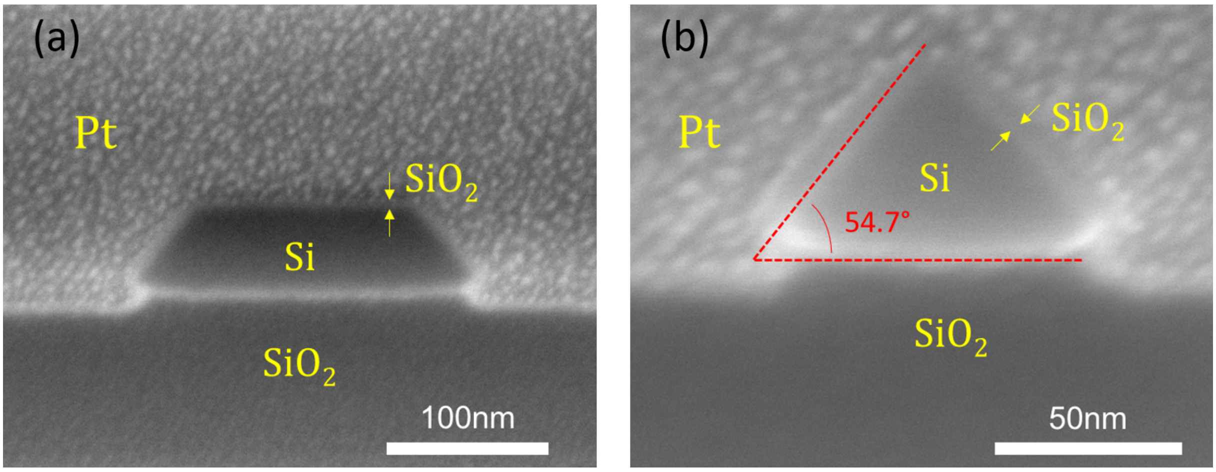


Figure 4.9: (a) Trapezoidal and (b) triangular cross-sections of Si TL NWs covered with 8 nm thick thermally grown SiO_2 layer. Cross-sectional cuts through the nanowires were performed using the focused ion beam technique with deposition of a protective Pt layer on top of the silicon nanostructures.

Source/drain contact implantation

The formation of source/drain contacts of the transistor structures was then performed using the ion implantation process followed by the rapid thermal annealing. The implantation area was defined by photolithography using $AZ^{®}$ $5214E$ photoresist. The process of photolithography was performed following the same workflow as described in the mesa definition step. The resist pattern defined for ion implantation is shown in Figure 4.10(a). Source/drain contact areas are well-defined in the resist layer on mesa structures, while NWs and rest of the wafer are covered with $AZ^{®}$ $5214E$ film. Once the implantation areas are defined, the wafers are implanted with $Boron$ (B) dopants at an energy of 4 keV to a dose of 1×10^{15} cm^{-2} to create accumulation mode p-type FET ($p^{+}-p-p^{+}$) structures. To create inversion mode n-type transistor structures ($n^{+}-p-n^{+}$), the samples are implanted with $Arsenic$ (As) dopants at an energy of 8 keV to a dose of 5×10^{14} cm^{-2}.

After the implantation, the residual resist mask is removed using acetone and IPA solutions for 24 $hours$. Due to the intense high-energy ion bombardment as well as the heating of the substrate during the implantation process, which leads to a strong molecular cross-linking of resist polymers, the relatively long cleaning time is required to completely remove the resist mask. The resist remaining on NW structures even after cleaning with acetone is removed

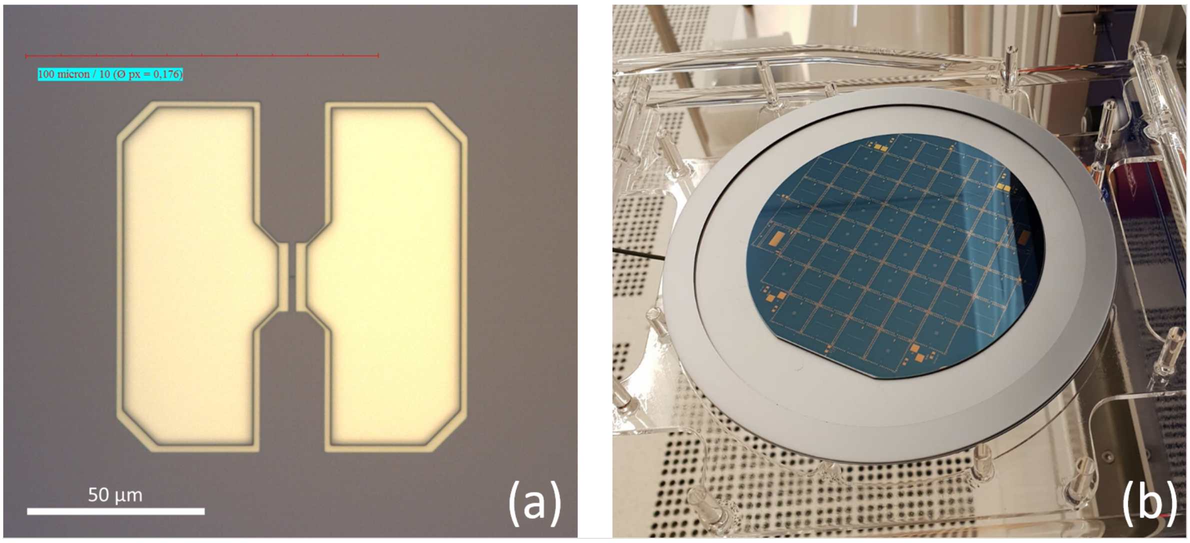


Figure 4.10: (a) Resist mask for the ion implatation of source/drain contacts of NW FET structure; (b) Optical image of SOI wafer with structures after ion implantation to be annealed in RTP system.

afterward by PIRANHA ($H_2SO_4 : H_2O_2 = 3 : 1$ v/v). The protective oxide covering NW structures is removed by etching in HF (1 %) for 1 min directly after the cleaning with the Piranha solution. Finally, the annealing process is subsequently performed to repair the crystal damage and activate the dopants. The wafers doped with Boron dopants were then annealed in a rapid thermal processing (RTP) system at 1000 °C for 5 s in N_2 atmosphere (see Figure 4.10(b)). The implanted As dopants have been activated by RTP annealing at 950 °C for 30 s. The $SOI\#3R$ and $SOI\#7R$ wafers were implanted with Boron dopants to define accumulation mode two-layer NW FET ($p^+ - p - p^+$) structures with p-type conductivity.

Gate oxidation

After the ion implantation step, an 8 nm thin uniform gate oxide layer is grown on the nanowire structures employing dry thermal oxidation (see Figure 4.4(b)). Before the oxidation, the native oxide on top of the silicon is removed by wet etching with 1% HF for 1 min. Directly after HF-etching, the oxidation process is performed at 850 °C for 45 min in an oxygen atmosphere using the $Tempress\ Omega\ Junior$ oxidation furnace. The SiO_2 layer thickness of 8 nm was selected as optimal to serve as a chemically-stable gate dielectric layer for liquid-gated NW FET-based biosensors and to protect the NW channel when operating in a liquid ionic environment. Moreover, the performed rapid thermal oxidation allows obtaining superior-quality gate oxide layers with low defect density and a smooth Si/SiO_2 interface. These features are essential to achieve high-quality biosensor devices and increase the chance to fabricate a transistor containing a single trap in the gate area resulting in RTS noise. The gate oxide grown on highly doped source/drain silicon contacts is removed in the following back-gate opening step.

Back-gate opening

Typically, Si NW FET consists of source/drain electrodes connected through the NW body that is covered by an individually-addressable top-gate. However, the utilization of SOI wafers in fabrication technology allows the use of a highly-doped substrate of the wafers as a back gate electrode located underneath the channel region. In such a back-gate configuration, the BOX layer serves as the gate oxide and transistor drain current is effectively controlled by the voltage applied to the substrate. A combination of both top and back electrodes can be used to control the transport over the channel even more precisely. Moreover, such a double gate device configuration and operation can be used to control also the parameters of a single trap as it will be shown below in this thesis.

To make electrical contact with the base substrate of SOI wafers, we first chemically etched the contact pad pattern through the BOX layer. For this purpose, the resist pattern was preliminarily defined by photolithography using $AZ^{®}\ 5214E$ photoresist as was described above. Before the etching, the wafers with the developed resist pattern were hard-baked on a hotplate at 120 °C for $2\ min$ to harden the resist mask for wet etching of the BOX layer. As an etchant, we used a buffered oxide etch (BOE, $7:1$) solution yielding the highly selective SiO_2 removal with a rate of around $100\ nm/min$ at room temperature. Such a fast etching rate and high-selectivity of BOE allow excellent control of the etching process of silicon oxide without undercutting. Therefore, the etching process lasting $2\ min$ and followed by rinsing in DI water was sufficient to etch through $145\ nm$ thick BOX layer. The resist mask was then removed using acetone and IPA solutions.

Metallization of the contacts

The next fabrication step is the metallization of the transistor contacts. The metal feedlines and contacts to the NW structures were formed using photolithography and metal deposition followed by the lift-off patterning and annealing process.

First, the mask for the metallization was defined in $AZ^{®}\ nLOF$ 2020 photoresist layer employing negative photolithography. The details of the photolithography process involving $AZ^{®}\ nLOF$ 2020 are described above (see markers definition step). $AZ^{®}\ nLOF$ 2020 photoresist is one of the most widely used negative resists which were specially designed for the lift-off process. The use of this photoresist allowed to achieve an undercut profile of the developed pattern which prevents the resist sidewalls from being metallized and therefore makes the subsequent lift-off process faster and easier. The patterned resist mask for the following metallization of defined structures is shown in Figure 4.11(a).

Before the metal deposition, the samples were immersed into $1\%\ HF$ for $30\ s$ to strip the native oxide. Afterward, the contact surfaces were cleaned with a short Ar-plasma step,

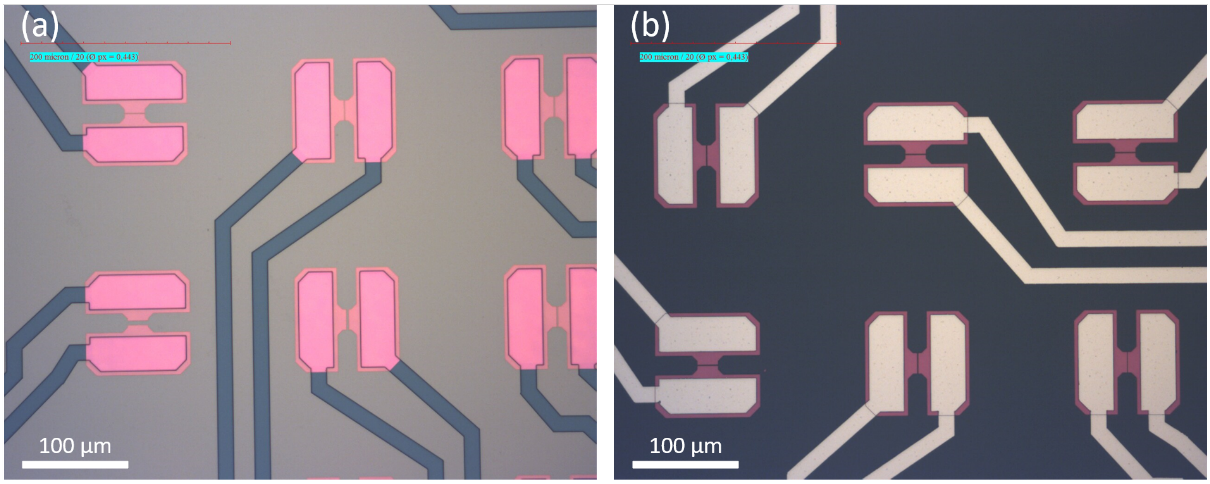


Figure 4.11: (a) Resist mask for defining metal contacts to TL NW structures. A negative tone lift-off photoresist $AZ^{\circledR}$ $nLOF$ 2020 is used; (b) Optical microscope image of the Al-metallized TL NW transistors.

and a metal stack consisting of 5 nm of TiN and 200 nm of Al was subsequently sputtered on the samples using the *LLS EVO II Oerlikon* sputter deposition system. A standard lift-off procedure using acetone was then performed to pattern metal contacts. Next, the surface of the wafers was additionally cleaned with O_2 plasma for 3 min to completely remove resist residuals. Subsequently, the samples were annealed in an RTP system at 450 °C for 10 min in forming gas atmosphere ($N_2 : H_2 = 5 : 5$) to achieve ohmic behavior of the contacts. An optical microscope image of the chip after the metallization step is shown in Figure 4.11(b).

An alternative option to achieve a good ohmic behavior of the contact leads is to use a low-resistive chromium/gold (Cr/Au) stack for metallization. The Cr/Au layer stack can be then patterned using lift-off technology as described above. Experience has shown that 10 $nm/200$ nm thick Cr/Au contacts formed by thermal evaporation and annealed at 350 $°C$ for 20 min show excellent ohmic behavior with a low contact resistance. Moreover, employing a Cr/Au metallization allows using a flip-chip bonding technique for further chip bonding step.

Passivation process

After the metallization, fabricated structures were passivated to protect metal leads against the liquid environment during measurements. Openings to metal pads for bonding and the access of a liquid to the NW regions were provided by patterning the passivation layer using photolithography.

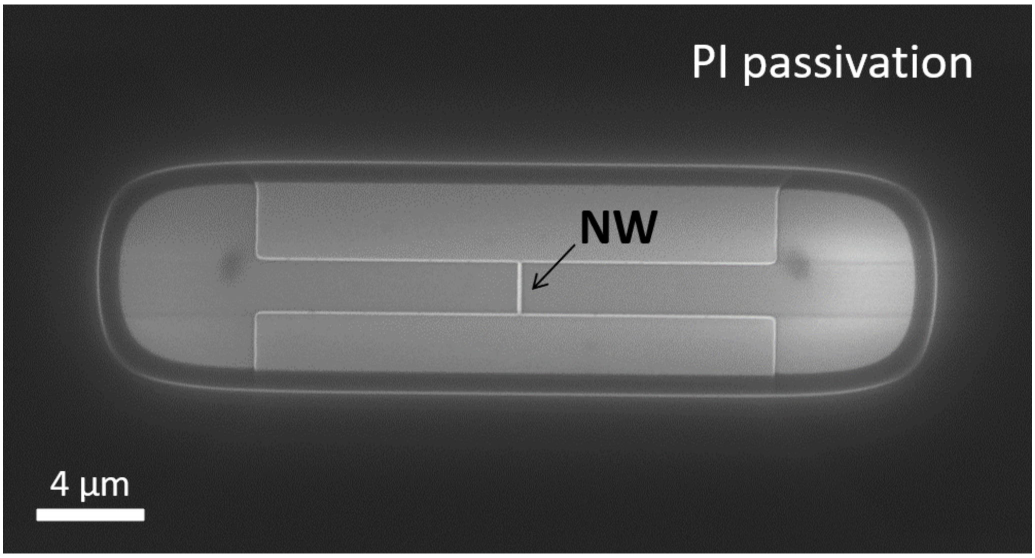


Figure 4.12: SEM image of the polyimide-passivated Si TL NW FET-based biosensor. The opening in the polyimide film is well-defined providing the access of the gating solution to the NW region.

Being a highly biocompatible material and demonstrating exceptional stability in liquid as well as excellent resistance to wet and dry-etch processing chemicals after high-temperature curing, the polyimide (PI 2545) resist was used as the passivation material. The passivation process consisted of several steps. First, the wafers were dehydrated at 180 °C for 30 min on the hotplate. The adhesion promoter VM 652 was then spin-coated on the samples at the spin speed of 3000 rpm and soft-baked at 110 °C for 1 min to improve the adhesive properties of the surface. Subsequently, polyimide was spin-coated on the wafers at 5000 rpm and soft-baked at 140 °C for 6 min. As a result, the uniform PI layer with a thickness of approximately 1.5 μm was formed on the wafers covering the fabricated structures. The used PI resist is non-photodefinable. Therefore, the utilization of additional photosensitive resist is required to selectively pattern the PI layer. For this purpose, a negative tone $AZ^{®}$ $nLOF$ 2020 photoresist was spin-coated at 4000 rpm on top of the PI layer and baked at 110 °C for 1 min. Afterward, the openings in the photoresist film were defined by photolithography using the same parameters as described above for $AZ^{®}$ $nLOF$ 2020 resist. Finally, the opening pattern was transferred into the PI passivation layer during the development process for 30 s in $AZ^{®}$ 326 MIF basic developer. The photoresist mask was then removed with acetone and IPA. In the end, the patterned PI passivation layer was hard-baked in a process furnace by ramping the temperature to 350 °C with the speed of 8 °C/min followed by a 30 min hold time under N_2 flow. The wafers were then cooled down to room temperature for 12 $hours$. The curing process converts the polyimide layer into an insoluble passivation film. A high-resolution SEM image of the PI-passivated nanowire structure is shown in Figure 4.12.

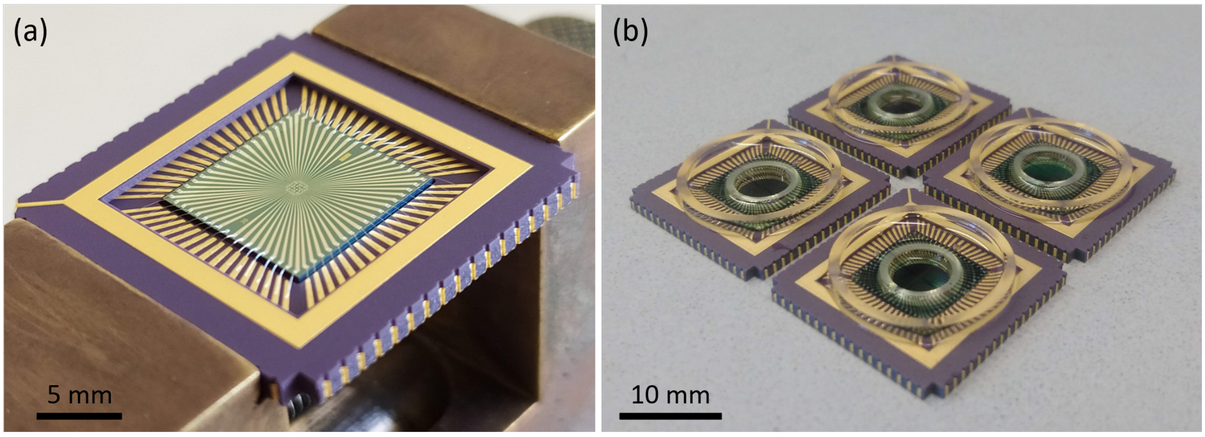


Figure 4.13: Optical images of (a) a wire-bonded chip and (b) finished TL NW FET-based sensors with reservoirs for liquid measurements.

Chip wire-bonding and encapsulation

After the fabrication in a cleanroom facility (HNF), the wafers were cut into individual $11 \times 11\ mm^2$ chips, which were further integrated into ceramic chip carriers, bonded, and encapsulated for the measurements in a liquid environment. The entire encapsulation process consists of the following steps:

- *Chip carrier packaging.* A bare individual chip is positioned in a special ceramic chip carrier and attached to the bottom of the carrier package using silver-based glue.

- *Bonding process.* There are different techniques used for chip bonding in the microelectronic industry. We used a conventional ultrasonic wire-bonding method that doesn't require any special surface treatment of the chip carrier and bond pads. Chips were appropriately wire-bonded to chip carriers using aluminum wires to match the measurement socket (see Figure 4.13(a)). For the samples metallized with gold, a low-cost flip-chip process can be used as an alternative bonding technique.

- *PDMS encapsulation.* To protect contact pads and metal wires from being exposed by liquid leading to a short-cut of electrical contacts, the chips are encapsulated using polydimethylsiloxane (PDMS) and glass rings. First, a small glass ring with an inner diameter of $8\ mm$ is glued on the top of the chip using PDMS to separate the NW structures in the middle of the chip from the electrical wiring. Subsequently, a bigger glass ring with an inner diameter of $20\ mm$ is glued on the top of the chip carrier defining an outer boundary of a vessel to be filled with PDMS. The PDMS is prepared by thoroughly mixing the silicone base elastomer (*Sylgard 184, Dow Corning*) with the curing agent in weight proportion $10 : 1$ at room temperature. The positioned and glued rings are pre-baked at $110\ °\mathrm{C}$ for $15\ min$. Space between the rings is then filled with freshly prepared PDMS solution. It should be noted that air bubbles should be carefully cleared from the poured

PDMS solution. Subsequently, the PDMS is hard-baken in an oven at 110 °C for 1 $hour$. Baked PDMS layer is a super-hydrophobic, highly adhesive and biocompatible material with good dielectric properties which make it well-suited for encapsulation purposes of FET biosensors. Finished devices with reservoirs prepared for measurements with a liquid gate are shown in Figure 4.13. After the encapsulation process, biological liquids can be delieverd to the NW surface for testing by drop-casting method. Alternatively, the NW FET sensors can be encapsulated with a PDMS-based microfluidic chamber fabricated using a specially designed and prepared silicon mold, patterned using photolithography and RIE.

4.2 Transport and noise properties of the fabricated TL nanostructures

Designing and prototyping of extraordinary sensitive biosensors require detailed characterization and investigation of transport and noise properties of transducer elements. Below, we present the measurement results of electrical and noise characteristics as well as study and discuss transport and noise peculiarities in fabricated LG TL NW structures. The electrical performance of fabricated sensors is characterized in terms of threshold voltage, subthreshold swing, field-effect mobility, and a maximum of transconductance. Noise spectroscopy characterization of TL nanostructures is performed to reveal the noise mechanisms as well as to study dynamic processes in fabricated devices. The input-referred noise as well as Hooge parameter as the measure of noise level are calculated for tested devices and compared with the results published for other state-of-the-art FET structures. A comprehensive analysis of the experimental data reveals a significant effect of the channel doping concentration on the dynamic processes in the unique TL NW structures.

4.2.1 Electrical characterization and transport peculiarities in TL NW FETs

Typical I-V transfer characteristics measured on fabricated Si TL NW FETs with channel doping concentrations of 10^{16} cm^{-3} and 10^{17} cm^{-3} are shown in Figures 4.14(a) and 4.14(b), respectively. The tested TL NW devices configured as accumulation-mode $p^+ - p - p^+$ structures with NW width of 90 nm and a length of 100 nm were liquid-gated at a constant drain-source bias of -100 mV to ensure a linear regime of operation for the transistor structures. A phosphate-buffered saline (PBS) with the physiological $pH = 7.4$ and ionic strength of 10 mM was used as a liquid-gate solution and an external standard $Ag/AgCl$ reference electrode was employed to apply the liquid-gate potential. The substrate of the chips, which may act as a back gate, was grounded while measuring the transfer curves in this case. The DC measurements of current-voltage characteristics were performed using the I-V measurement setup described in Section 3.1. As can be seen from Figures 4.14(a) and 4.14(b), fabricated devices showed transfer characteristics behavior typical for $p^+ - p - p^+$ FETs and demonstrated good working stability and reproducibility during the operation in a liquid environment. It should be noted that the leakage currents were negligibly small (below $100\ pA$) within the entire range of the applied liquid-gate voltages confirming the high quality and low level of defect density of $8\ nm$ thin thermally grown SiO_2 layer used as a front-gate dielectric. The threshold voltage (V_{th}), which is commonly defined as the value of the gate voltage at which the transition from the exponential to the linear gate dependence of drain current occurs, was calculated to be $-0.98\ V$ for the TL NW with $10^{16}\ cm^{-3}$ concentration of dopants and $-0.75\ V$ for the TL NW with $10^{17}\ cm^{-3}$ doping concentration, respectively. Here, the extraction of threshold voltages was performed from the transfer characteristics using the second derivative method [76]. It should be noted that the extracted threshold voltages with absolute values smaller than $1\ V$ reflect typical values of this parameter obtained for the LG devices studied in this thesis and further confirm a high level of the electrical performance of fabricated LG nanostructures.

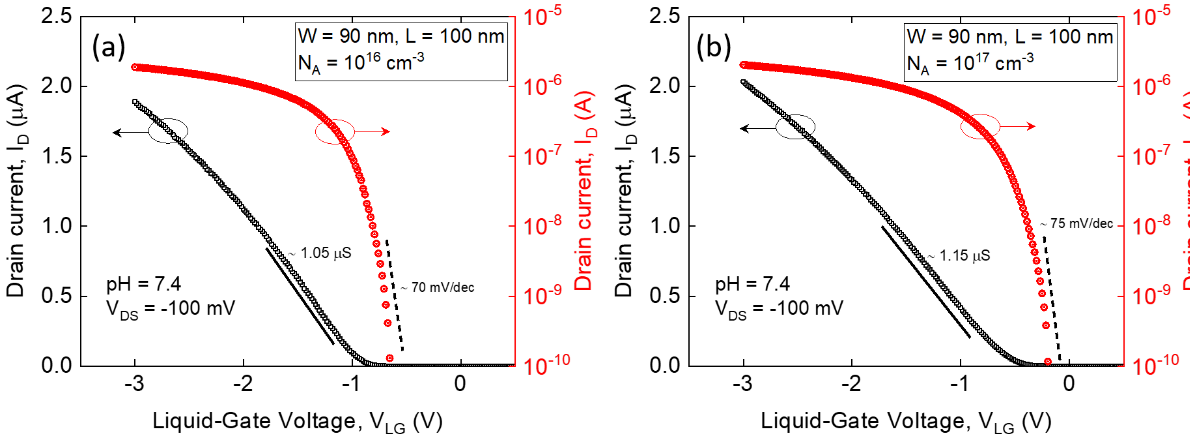


Figure 4.14: Transfer characteristics of $p^+ - p - p^+$ LG Si TL NW FETs with (a) $10^{16}\ cm^{-3}$ and (b) $10^{17}\ cm^{-3}$ concentrations of Boron dopants in the channel measured for a forward sweep of the liquid-gate voltage and shown in linear scale (black curves) and semilogarithmic scale (red curves). The TL NW structures with NW width of $90\ nm$ and a length of $100\ nm$ were biased at a drain-source voltage of $-100\ mV$, which corresponds to the linear working regime of the accumulation-mode $p^+ - p - p^+$ FETs.

As can be also evident from Figures 4.14(a) and 4.14(b), under the same operating conditions, higher values of drain currents are measured for the nanostructure with higher channel doping concentration. This is also valid for the maximum of transconductance, which was calculated to be $1.05\ \mu S$ and $1.15\ \mu S$ for devices with channel doping concentrations of $10^{16}\ cm^{-3}$ and $10^{17}\ cm^{-3}$, respectively. Such behavior is expected considering a configuration of the tested devices. Configured as accumulation-mode $p^+ - p - p^+$ FETs, devices with a higher concentration of dopants in the channel exhibit lower channel resistance due to the higher concentration of holes as majority carriers, which in turn results in higher drain currents. At the same time, the subthreshold swing extracted from the slope of the subthreshold current appears to be 70 mV/dec for the device with 10^{16} cm^{-3} concentration of dopants in the channel, and 75 mV/dec for the Si TL NW FET with 10^{17} cm^{-3} channel doping concentration. The extracted values of subthreshold swing are close to the ideal value of about 60 mV/dec for FET-based devices operating at room temperature [77, 78].

The dependence of the drain current on the drain-source voltage at a constant gate voltage is known as the output characteristic of the FET device. The measured output characteristics of the same investigated TL nanowires are shown in Figures 4.15(a) and 4.15(b). As can be seen, the output characteristics reflect a good control of the liquid gate over the current through the NW channel and demonstrate stable MOSFET-like behavior with a typical transition from ohmic (linear) to saturation regime.

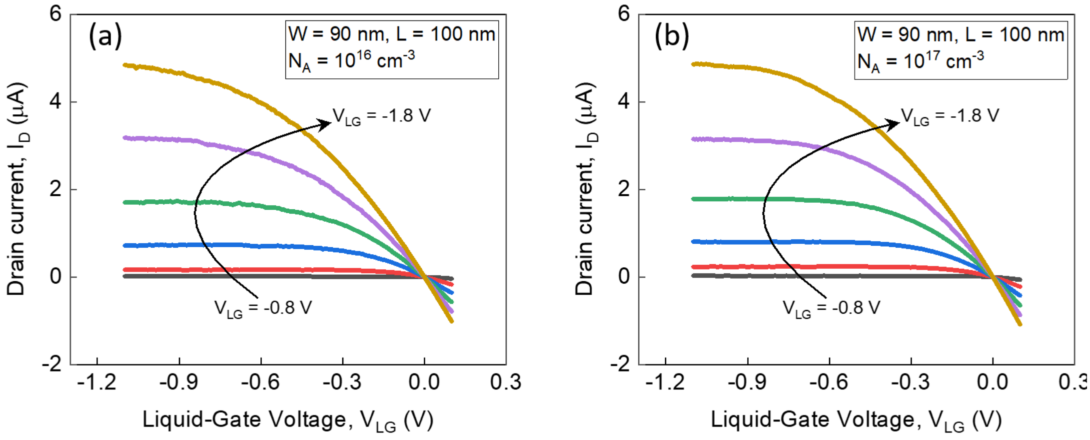


Figure 4.15: The set of output curves at different applied liquid-gate voltages measured for 90 nm wide and 100 nm long LG Si TL NW FETs with a doping concentration in the channel of (a) 10^{16} cm^{-3} and (b) 10^{17} cm^{-3}.

The experimental dependencies of the drain current on the liquid-gate voltage applied to the same nanowires with the width of 90 nm and the length of 100 nm biased at different drain-source voltages (V_{DS}) are shown in Figure 4.16(a) and 4.16(b) for TL NW FETs with channel doping concentrations of 10^{16} cm^{-3} and 10^{17} cm^{-3}, respectively. It should be noted that the measurement results are in good agreement with calculated hole density profiles shown in Figures 4.16(c) and 4.16(d) for the corresponding TL NWs. The distributions of holes as the majority carriers in p-type silicon nanostructures in the direction that is normal to the Si/SiO_2 interface were calculated at different gate voltages using the *NEXTNANO* simulation software for semiconductor nanodevices [79]. The modeled structures consisted of two silicon layers with different concentrations of dopants which correspond to that of designed and tested TL NWs: the first silicon layer with a thickness of 50 nm has 10^{15} cm^{-3} concentration of B-dopants, while the second layer with a thickness of 25 nm is highly-doped silicon with the concentration of acceptors to be 10^{16} cm^{-3}, or 10^{17} cm^{-3} to match the doping profiles of fabricated structures. As can be seen from simulation results shown in Figures 4.16(c) and 4.16(d), the greatest amount of positive charges (holes) are accumulated in the highly doped region of two-layer silicon nanostructures where they form the accumulation layer (conductive channel) with a thickness of several nanometers in the vicinity to the Si/SiO_2 interface. This fact indicates that the highly doped top silicon layer with advanced properties plays also a dominant role from the perspective of the single-trap phenomena that will be studied below.

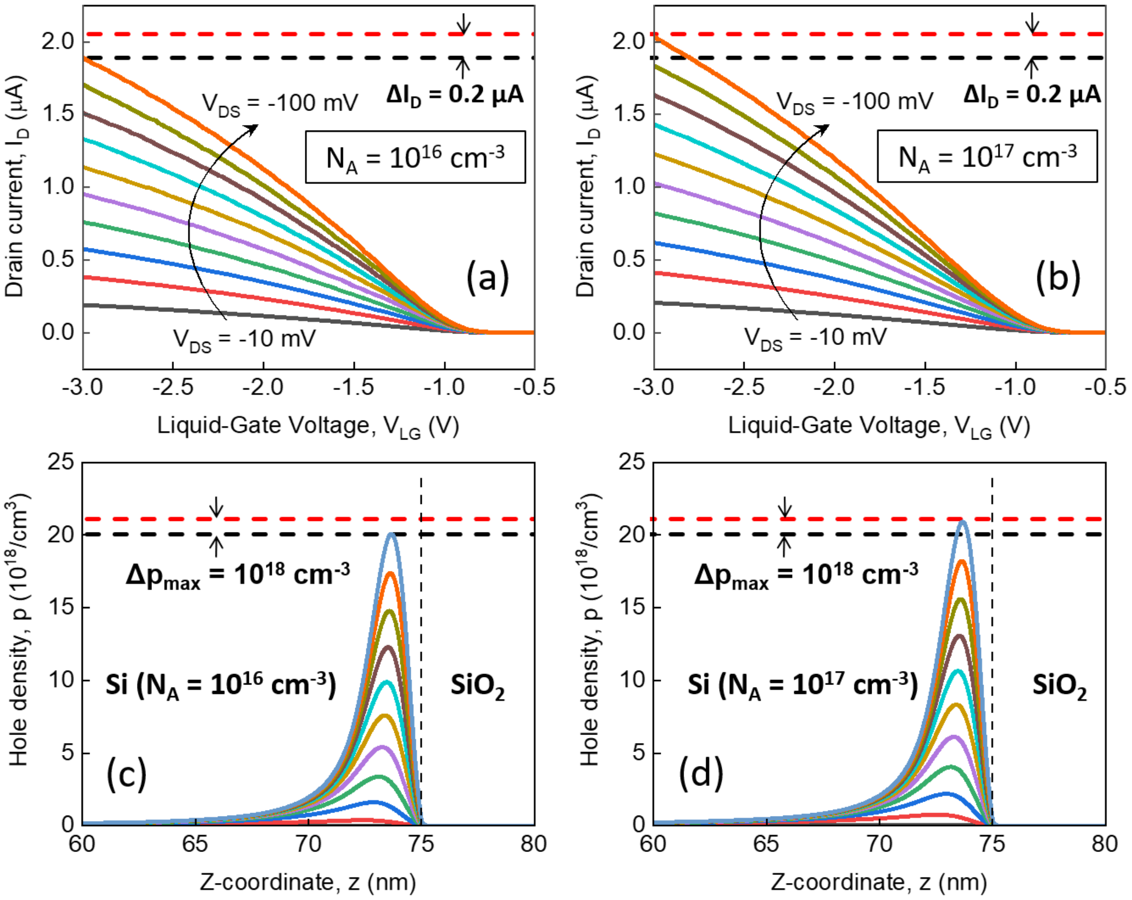


Figure 4.16: Set of transfer curves of Si TL NW FETs with doping concentration in the channel of (a) 10^{16} cm^{-3}, and (b) 10^{17} cm^{-3} measured at different drain-source voltages (V_{DS}). The same tested devices with a width of 90 nm and a length of 100 nm were liquid-gated using PBS solution with $pH = 7.4$ and ionic strength of 10 mM; (c,d) Simulated densities of holes as majority carriers in TL accumulated silicon NW with a doping level of 10^{16} cm^{-3}, and 10^{17} cm^{-3}, respectively. The distributions of holes were calculated using the *NEXTNANO++* software and plotted for the gate voltages varied in the range from (0 V) down to (-3 V) with a voltage step size of (-0.3 V). Z-coordinate corresponds to the direction that is normal to the Si/SiO_2 interface schematically shown as a vertical dashed line. The horizontal black and red dashed lines visualize the difference between drain currents (Figures 4.16(a) and 4.16(b)) and maximum densities of holes (Figures 4.16(c) and 4.16(d)) obtained for TL NW FETs with 10^{16} cm^{-3} and 10^{17} cm^{-3} channel dopants concentration gated at $V_{LG} = -3$ V.

Typical transfer curves measured on accumulation-mode p-type Si TL NW FETs with a width of 100 nm and different lengths are shown in Figure 4.17(a) for devices with a channel doping concentration of 10^{16} cm^{-3}. The corresponding set of curves measured for the Si TL NW FETs with the same channel dimensions but with a higher channel doping concentration (10^{17} cm^{-3}) are shown in Figure 4.17(b). Both types of devices were liquid gated and operated in the linear operation regime. As one can deduce from Figures 4.17(a) and 4.17(b), the drain current behavior in the investigated TL NW FETs with different doping concentrations scales well with the length of NWs.

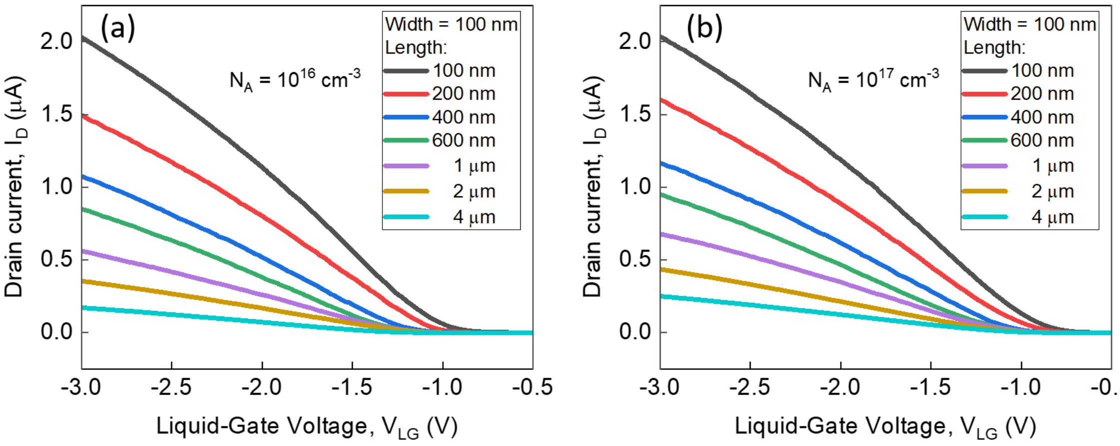


Figure 4.17: Transfer curves measured for $p^+ - p - p^+$ Si TL NW FET structures with the NW width of 100 nm and different lengths. The dependences shown in the figures (a) and (b) correspond to the devices with the concentration of B-dopants in the channel of 10^{16} cm^{-3} and 10^{17} cm^{-3}, respectively. During the measurements, V_{DS} was set to -100 mV to operate the devices in the linear operation regime.

One of the fundamental problems of FET structures is a contact resistance existing between metal feedlines and source/drain terminals. A significant value of contact resistance affects the transport properties of a transistor and alter its performance. Therefore, the contribution of the contact resistance has to be investigated and taken into account when developing high-sensitive FET-based biosensors. To exclude any contact effects, we performed an estimation of contact resistance for the fabricated TL NW sensors using the data shown in Figures 4.17(a) and 4.17(b). At small V_{DS} biases, the conductive channel of a nanotransistor can be considered as a resistor, whose value is proportional to the length of the channel determined by the length of NW. Therefore, NW resistance measured at the given value of the overdrive gate voltage ($V_{LG} - V_{th}$) should linearly scale with the length. Thus, by performing a linear fitting of the dependence of channel resistance on NW length, one can extract the contact resistance as the intercept of the fitted curve with the ordinate axis. The channel resistance as a function of NW length at $V_{DS} = -100$ mV and different values of the overdrive liquid-gate voltage are shown in Figures 4.18(a) and 4.18(b) for TL NW FETs with channel doping concentrations of 10^{16} cm^{-3} and 10^{17} cm^{-3}, respectively.

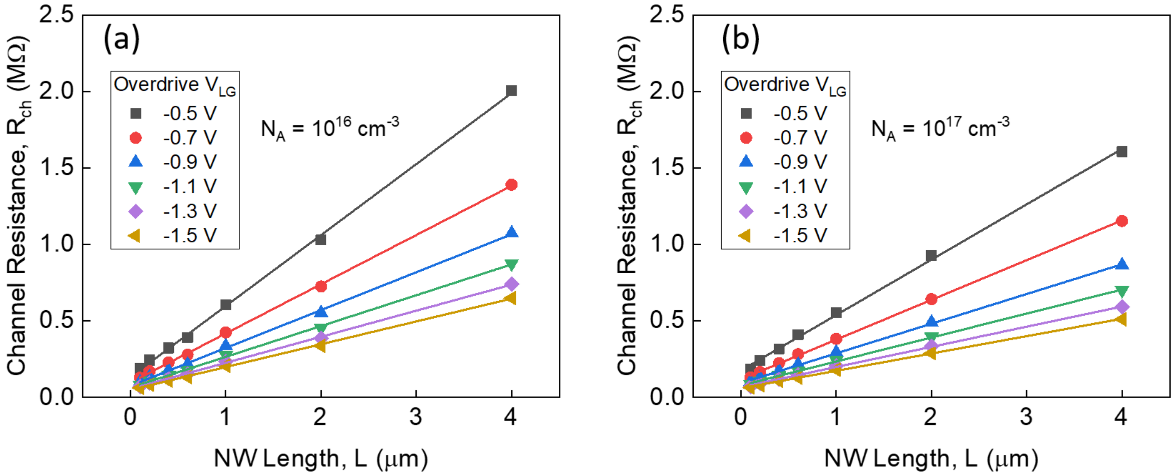


Figure 4.18: (a, b) The channel resistance of the $p^+ - p - p^+$ Si TL NW FETs extracted from Figures 4.17(a) and 4.17(b) for the nanostructures with a doping concentration in the channel of 10^{16} cm^{-3} and 10^{17} cm^{-3}, respectively. The resistance is plotted as a function of NW length. Solid lines represent linear fittings of the data and used to extract the value of contact resistance.

The extracted contact resistance as a function of the overdrive liquid-gate voltage is plotted in Figure 4.19. For comparative purposes, Figure 4.19 shows also the dependence of channel resistance on the overdrive liquid-gate voltage measured for 100 nm-wide and 2 μm-long Si TL NW FETs with different concentrations of dopants in the channel.

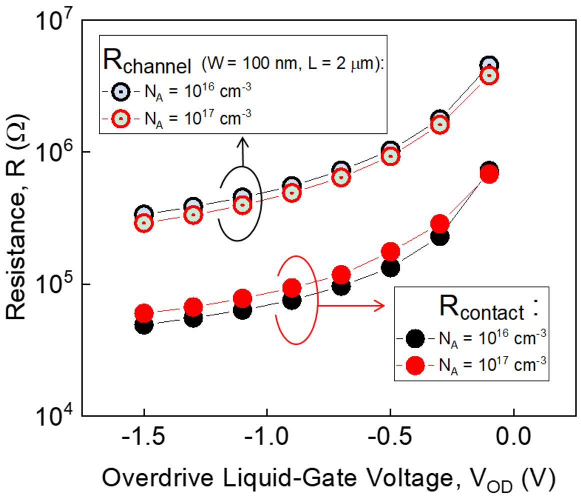


Figure 4.19: Contact resistance extracted for the $p^+ - p - p^+$ TL NW devices with different concentrations of dopants in the channel using the data shown in Figures 4.18(a) and 4.18(b) and plotted as a function of the overdrive liquid-gate voltage. The value of contact resistance is much lower than the nanowire channel resistance in the full operating range of the LG TL devices. Thus, the influence of the contact resistance on the electrical performance of the fabricated TL NW structures can be neglected.

It is evident from Figure 4.19 that contact resistance extracted for both types of investigated devices is almost one order of magnitude smaller than channel resistance of TL NWs for the whole range of overdrive liquid-gate voltages applied (the full operation range of the LG transistors). Thus, the impact of contact resistance on the electrical performance of fabricated nanostructures is negligible and can be neglected.

Set of the transfer curves measured on Si TL NW FETs with a channel doping concentration of $10^{17}\ cm^{-3}$ configured as inversion-mode $n^+ - p - n^+$ nanostructures with a width of $100\ nm$ and different lengths in the range from $100\ nm$ to $4\ \mu m$ are shown in Figure 4.20(a). The tested $n^+ - p - n^+$ devices also demonstrate good scalability with the length of the nanowire as can be seen in Figure 4.20(a). Similarly as for $p^+ - p - p^+$ structures, the contact resistance was also extracted for $n^+ - p - n^+$ devices and shown in Figure 4.20(b). The high doping of silicon mesa structures as well as appropriate annealing of metal contacts during the fabrication process ensured good ohmic contact to the silicon NW channel which resulted in low contact resistance for both $p^+ - p - p^+$ and $n^+ - p - n^+$ TL NW transistor structures.

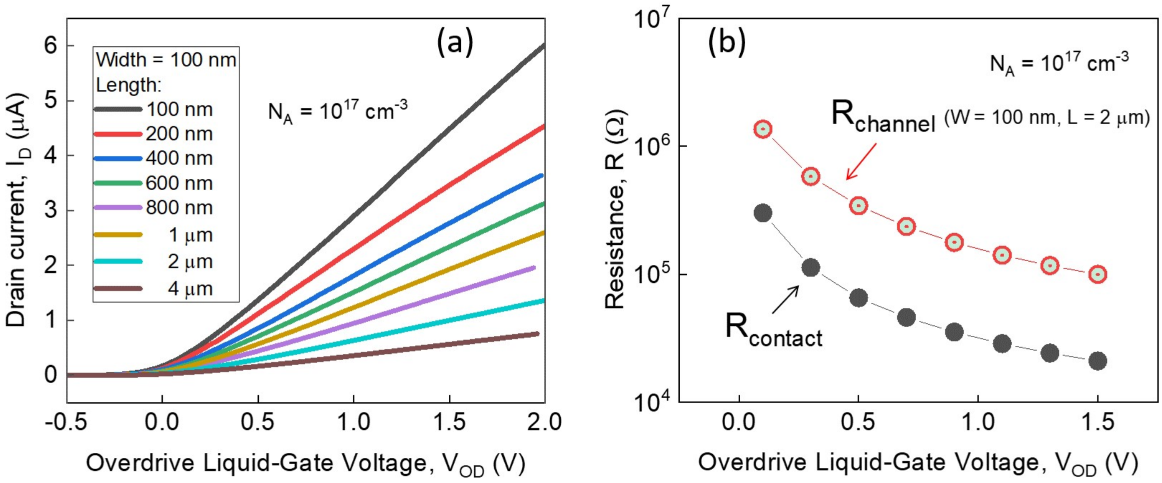


Figure 4.20: (a) Transfer characteristics measured at $V_{DS} = 100\ mV$ for $n^+ - p - n^+$ Si TL NW FETS with the NW width of $100\ nm$ and different lengths varying from $100\ nm$ to $4\ \mu m$; (b) Contact resistance extracted from the transfer curves shown in (a) for $n^+ - p - n^+$ structures.

Further analysis of the TL NW FET transfer characteristics allows the quantitative determination of such important transistor parameters as the maximum of transconductance and field-effect mobility of charge carriers. Figure 4.21(a) demonstrates a distribution of the maximum values of transconductance obtained for TL NW FETs with different doping concentrations and the same width of $100\ nm$ and the length of $1\ \mu m$. All tested devices were liquid-gated and operated in the linear regime of operation. The maximum of transconductance was determined as the slope of the linear part of the transfer characteristic measured on the TL NW FETs. As it follows from the data shown in Figure 4.21(a), the mean value of transconductance maximum was obtained to be $0.25\ \mu S$ and $0.40\ \mu S$ for $p^+ - p - p^+$ TL NW structures with the concentration of B-dopants in the channel of $10^{16}\ cm^{-3}$ and $10^{17}\ cm^{-3}$, respectively. At the same time, the value of $1.05\ \mu S$ was obtained for $n^+ - p - n^+$ TL NW structures with the concentration of B-dopants in the channel of $10^{17}\ cm^{-3}$. For the $p^+ - p - p^+$ devices, the increased value of transconductance in highly doped nanostructures can be explained by the increase of drain current due to the increase of concentration of free holes defined by the concentration of acceptors in the p-type semiconductor material. Simultaneously, the mean value of $1.05\ \mu S$ of the transconductance was obtained for similar devices with a width of $100\ nm$ and a length of $1\ \mu m$ but configured as inversion-mode $n^+ - p - n^+$ TL NWs where electrons are used as majority charge carriers. It should be noted that the mean value of transconductance obtained for n-type structures is about 2.5 times higher than for their p-type analogs fabricated in the same technological run. This can be attributed to the difference between electron and hole effective mass resulting in different drift velocities and tunnelling parameters.

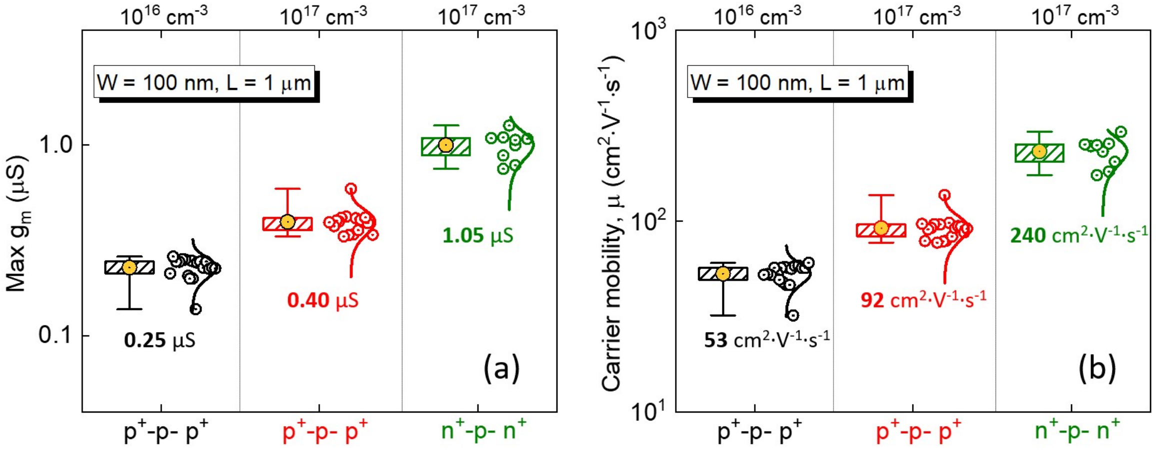


Figure 4.21: (a) The statistics of the maximum values of transconductance calculated for different types of LG TL NW FETs with a width of $100\ nm$ and a length of $1\ \mu m$. The whiskers denote minimum and maximum of calculated values, while the boxes are determined by the $25th$ and $75th$ percentiles. The solid dots shown inside the boxes denote mean values of transconductance measured in different devices; (b) The distribution of carrier field-effect mobility estimated for holes in the p-type accumulation-mode structures with different channel doping concentrations and electrons in the n-type inversion-mode devices.

The field-effect mobility of charge carriers in the NW channel can be estimated using the following expression:

$$\mu = \frac{g_m L}{W C_{ox} V_{DS}} \tag{4.1}$$

where g_m is the transconductance of NW FET with a width of W and length of L, V_{DS} is the drain-source bias, and C_{ox} is the gate oxide capacitance per unit area given by Equation 2.7. It should be noted the Equation 4.1 is valid for both inversion-mode and accumulation-mode NW transistors and allows the carrier mobility to be estimated for devices operating in the linear regime. From the results shown in Figure 4.21(b), we see that the mean value of field-effect mobility calculated for holes in $p^+ - p - p^+$ devices with $10^{16}\ cm^{-3}$ doping concentration is equal to $43\ cm^2\ V^{-1}\ s^{-1}$. For the highly doped NWs with the same channel dimensions, this parameter approaches the value of $92\ cm^2\ V^{-1}\ s^{-1}$. At the same time, the mean value of field-dependent electron mobility was obtained to be $240\ cm^2\ V^{-1}\ s^{-1}$ for the structures configured as $n^+ - p - n^+$ devices. It should be noted that the extracted values of carrier mobility are in good agreement with those reported in the literature for the state-of-the-art single-layer undoped NW devices [80]. Therefore, based on the experimental results presented and discussed in this section one can assert that the newly fabricated LG Si TL NW FETs with different concentrations of dopants in the channel demonstrate high-quality electrical characteristics and thus can be further employed for single-carrier studies and biosensing applications.

4.2.2 Biosensing performance of the liquid-gated TL NW FETs

Here, we employ fabricated Si TL NW FETs as highly sensitive biosensors to detect various target bio-species in liquid using a standard sensing approach based on monitoring of drain current as a signal. A specially designed polydimethylsiloxane (PDMS) microfluidic chamber was fabricated and integrated to deliver and exchange biological liquids. As the analyte, we chose cardiac troponin I (cTnI) and C-reactive protein (CRP) biomolecules, which are gold-standard biomarkers for the early diagnosis of cardiomyopathy and myocardial necrosis due to high cardio-specificity, high elevation level and fast release time [3, 26]. To implement an exclusive specificity and selectivity of TL NW biosensors to the target analyte, the surface of TL NWs has been modified with the special linker molecules and analyte-specific receptors. In particular, TL NW devices aiming to detect low concentrations of CRP molecules were functionalized with monoclonal anti-CRP antibodies, while biosensors aiming to detect cTnI proteins were modified with newly designed dibenzocyclooctyne (DBCO)-linked cTnI-specific aptamers. The developed immobilization protocols are described in detail in $Appendix\ C$. Before the cTnI and CRP biomarkers detection experiments, the response of LG Si TL NW FETs to the different pH of PBS buffer solitons and different concentrations of ions was investigated. All sensing experiments were performed at room temperature inside a metal Faraday cage to avoid any parasitic external disturbances. An external standard $Ag/AgCl$ reference electrode was employed to apply the liquid-gate potential.

pH sensing

The hydrogen-ion concentration (pH) defines the acidity of a solution and is widely used as the indispensable parameter for monitoring the quality and chemical conditions of various substances. Controlling the pH value of water, food, and beverage products is extremely essential for humans. For instance, a change in pH value as small as $0.03\,pH$ units in the human blood can significantly affect body functions. Therefore, the monitoring of pH values of liquids requires the application of highly sensitive and accurate pH-sensors. In this perspective, ion-sensitive LG NW-based FETs are promising candidates to meet the requirements. Here, we report the pH responses of the fabricated TL nanostructures with different concentrations of dopants in the channel covered with an $8\ nm$ thin SiO_2 gate dielectric layer.

Figure 4.22(a) shows a set of transfer I-V characteristics measured on a typical $100\ nm$ wide and $1\ \mu m$ long Si NW FET with a channel doping concentration of $10^{15}\ cm^{-3}$ under different pH conditions. The fabricated PDMS microfluidic channel was used to successively change the gating solutions with pH values ranging from 6.64 to 8.44 with a step of about $0.2\ pH$.

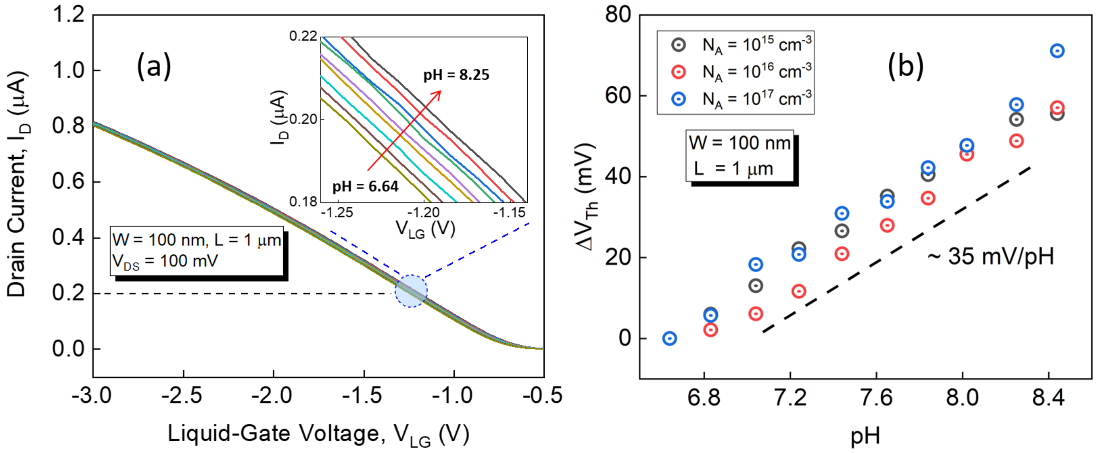


Figure 4.22: (a) Typical transfer curves measured on $100\ nm$ wide and $1\ \mu m$ long Si NW FET with $10^{15}\ cm^{-3}$ concentration of dopants in the channel that was liquid-gated in solutions with different pH values. The liquids were delivered to the NW sensing area using the home-made PDMS microchannel. The standard $Ag/AgCl$ reference electrode was integrated into the outlet Teflon tube close to the microchannel and used to apply liquid-gate potential. The measured characteristics shift to more positive voltages with increasing pH showing a typical behavior registered for all tested p-type devices with different concentrations of dopants in the channel; (b) threshold voltage shift (ΔV_{th}) plotted as a function of pH for the devices with NW width of $100\ nm$ and length of $1\ \mu m$, but different channel doping concentrations. The dashed line with a slope $35\ mV/pH$ reflects a pH response of the tested devices.

With the increase of pH value, the transfer curves shift laterally in the positive voltage direction which reflects a decrease of the threshold voltage for the accumulation-mode p-type FET. Such behavior is due to the deprotonation of the SiO_2 surface which increases the density of holes inside the p-channel structure. It should be noted that the transfer characteristics demonstrate no degradation of the subthreshold slope, while the threshold voltage of the FET device increases linearly as the pH value increases within the measured pH range. The results are shown in Figure 4.22(b). Interestingly, all tested devices with the same dimensions but different channel doping concentrations demonstrated about the same pH response of $35\ mV/pH$. The results are in good agreement with the data reported for ISFETs covered with SiO_2 [81] and confirm the high-quality performance of the fabricated sensors.

Ion sensing

Fabricated Si NW biosensors were further used to detect variations in KCl and $MgCl_2$ concentrations at constant pH value. Figure 4.23(a) shows the drain current vs. liquid-gate voltage characteristics of the $100\ nm$ wide and $4\ \mu m$ long Si NW FET measured at different concentrations of $MgCl_2$ divalent salt diluted in pure DI water. The pH of the DI water used to prepare the solutions with different concentrations of salts was about 6.4 and it remained about constant with adding of salts. As can be seen from Figure 4.23(a), the measured curves shift toward more negative values of liquid-gate voltage which reflects an increase of the threshold voltage for the accumulation-mode p-type sensors used in the experiment. Such behavior suggests that the observed effect is due to the adsorption of positive ions, which are Mg^{2+} cations in our specific case. It should be noted that a similar tendency was observed for both $MgCl_2$ and KCl salts sensing using also other p-type devices with different concentrations of dopants in the channel. The obtained results are in good agreement with the data published for non-doped Si NW FETs that were also covered with SiO_2. Interestingly, as it was reported in Ref. [17], silicon nanowires coated with high-k dielectrics such as HfO_2 and Al_2O_3 demonstrate the responses to variations in the concentration of anions Cl^- rather than in the concentration of cations K^+. Thus, we can emphasize a unique feature here that devices covered with different dielectric materials respond differently to different ions due to the surface-dependent affinity of anions and cations. Such an effect offers a promising opportunity to develop the system capable to perform selective-layer-free ion-specific sensing.

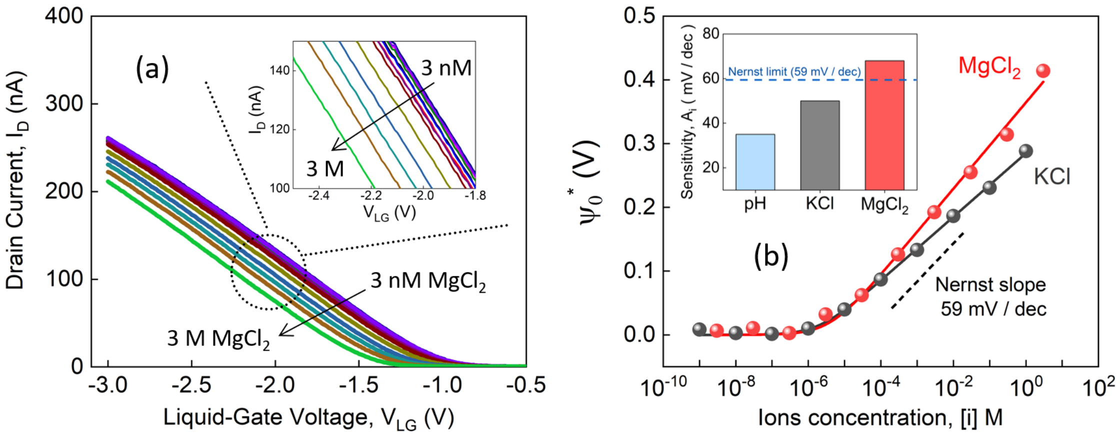


Figure 4.23: (a) Transfer characteristics of accumulation-mode p-type Si TL NW FET biosensor with $100\ nm$ wide and $4\ \mu m$ long NW channel with $N_A = 10^{16}\ cm^{-3}$ measured at different concentrations of $MgCl_2$ in DI water. The curves laterally shift to more negative voltages and reflect the typical behavior of the p-type sensors upon the adsorption of positively charged ions on the NW surface; (b) The variation of the surface potential of the sensor (ψ_0^*) with the concentration of monovalent KCl, and divalent $MgCl_2$ salts. The Nernst slope of $59\ mV/dec$ is shown as a reference. The inset shows the sensor's sensitivity to different ions obtained from fittings with Equation 4.2. Remarkably, the fabricated biosensor demonstrates the response to Mg^{2+} cations with sensitivity larger than the Nernst limit.

The response of the sensor to variations in KCl and $MgCl_2$ concentration in DI water is shown in Figure 4.23(b) in terms of the surface potential shift (ψ_0^*). As is evident in Figure 4.23(b), the device demonstrated no clear response until the concentration of KCl or $MgCl_2$ is reached the value of $1\ \mu M$. At higher concentrations, the sensor starts responding strongly to the changes in the concentration of salts. It should be noted that the detection limit of $1\ \mu M$ obtained for the fabricated devices is about two orders of magnitude smaller than values previously reported for the state-of-the-art NW FET-based sensors. This result confirms the high-level sensing performance of fabricated devices. Interestingly, some of the tested devices demonstrated a “J-shape” response to different concentrations of ions (data is not shown here). We attribute such a “J-shape” behavior to be caused by an overscreening effect related to the initial surface charge. The observed results are consistent with the effect of inversion of electrophoretic mobility in biomolecular or nanofluidic systems due to electrostatic correlations [22].

All the response curves showed in Figure 4.23(b) are fitted using the following equation [22]:

$$\psi_0^* = \psi_0 + const = (A_i/z_i)\, log\,([i] + [i_0]) - (A_i/z_i)\, log\,([i_0]) \tag{4.2}$$

where $[i_0]$ is an ion-specific constant that accounts for the plateau at low ion concentration $[i]$ (see Figure 4.23(b)), z_i is the ion valency, and A_i is the thermodynamic Nernst limit as a result of Boltzmann ion distribution in a liquid defined as $A_i = \delta\psi_0/\delta log[i]$. At room temperature ($T = 290\ K$), the Nernst-limited sensitivity $A_i = kTlog(10)/(qz_i) = 59\ mV$ per $log[i]$, where k is the Boltzmann constant and q is the elementary charge.

Fittings using Equation 4.2 demonstrated that $A_i = 48\ mV$ for KCl and $A_i = 64\ mV$ for $MgCl_2$. It should be noted that the experimentally determined sensitivity of $A_i = 64\ mV$ to divalent Mg^{2+} ions is larger than Nernst sensitivity. The obtained results are consistent with molecular dynamics simulations and can be explained by considering ion-specific surface interactions, yielding a surface that is high-sensitive especially to multivalent cations [22]. The ion-specific sensitivities of the tested biosensor including the pH response of the device are summarized in the inset of Figure 4.23(b). Interestingly, obtained experimental data also suggest that the sensitivity of fabricated biosensors to different ions in liquid solution scales corresponding to a reversed Hofmeister series for cations according to their ability to salt out/in proteins [22].

Detection of CRP and cTnI proteins using I-V approach

The detection of CRP and cTnI proteins was performed using several individual TL NW biosensors specifically functionalized with receptor molecules according to the functionalization protocols described in *Appendix C*. Figure 4.24(a) shows a set of transfer characteristics measured on the $100\ nm$ wide and $200\ nm$ long TL NW FET functionalized with troponin-specific aptamers at different concentrations of cTnI molecules in the PBS gating solution.

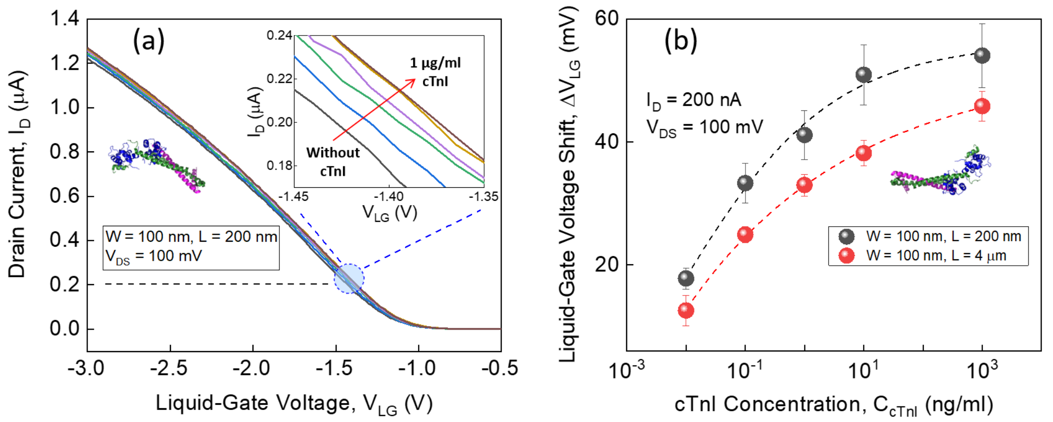


Figure 4.24: (a) Set of transfer curves measured on 100 nm wide and 200 nm long Si TL NW FET at different cTnI concentration levels in the gating solution; (b) Change of the measured signal as a function of the logarithm of cTnI concentration. The data is shown for two sets of TL NW sensors with the NW width of 100 nm and lengths of 200 nm and 4 μm. Vertical error bars represent statistical errors obtained for different sets of NW devices.

Each I-V curve was measured 5 minutes after introducing a certain concentration of target proteins. The incubation time is required to achieve an equilibrium state of the bio-system, and thus reliable experimental data. When the protein concentration increases, the transfer curves are shifted to the positive voltage direction which corresponds to the increase in the drain current at the same liquid-gate potential in the accumulation-mode p-type NW FET biosensor. Such behavior is due to the binding of the negatively charged cTnI proteins to the aptamer-functionalized surface of the nanowire, which induces the accumulation of holes in the p-type device. Therefore, with the increase of cTnI protein concentration, the drain current increases due to the gating field-effect caused by the negatively charged biomolecules on the TL NW surface. It should be noted that similar behavior in response to the change of cTnI concentration was registered for TL NW sensors with different sizes.

Figure 4.24(b) shows the shifted values of transfer curves in terms of the liquid-gate voltage shift extracted at the drain current level of 200 nA and constant V_{DS} value of $0.1\ V$. Vertical error bars represent statistical errors calculated using the least square root method when analyzing the experimental data measured on different TL NW biosensors. As can be seen in Figure 4.24(b), the measured response of the sensors with different NW lengths monotonically increases with increasing cTnI protein concentration and saturates at higher concentrations of troponin molecules. However, for small NWs with a width of 100 nm and a length of 200 nm, the signal starts to saturate at relatively lower concentrations around 1 ng/ml, while the sensors with the same width of 100 nm and length of 4 μm demonstrate saturation at concentrations as high as 1 $\mu g/ml$ due to the larger sensing area. This result suggests that NWs of different sizes functionalized with a novel dibenzocyclooctyne (DBCO) functionalization approach can be effectively used to reliably detect and monitor cTnI biomarkers in a wide dynamic range.

Figure 4.25(a) and 4.25(b) represent the experimental results on the detection of different CRP concentration levels in a buffer solution with $pH = 7.4$. In this case, two sets of TL NW sensors with the same width of $100\ nm$ and lengths of $200\ nm$ and $1\ \mu m$ modified with monoclonal anti-CRP antibodies were used. The pronounced shift of transfer I-V characteristics towards higher currents with increasing CRP concentration was registered for both sets of TL NW biosensors. Considering that the FET-based sensors used in the experiment demonstrate p-type conductivity, the increase in drain current is equivalent to applying a negative potential voltage to the liquid gate which results in the accumulation of holes due to the negative field effect. Therefore, the data shown in Figure 4.25(a) suggest that CRP biomarkers carry a net negative charge in the buffer solution with $pH = 7.4$. The measured responses of the TL NW FET devices to different CRP concentrations are shown in Figure 4.25(b).

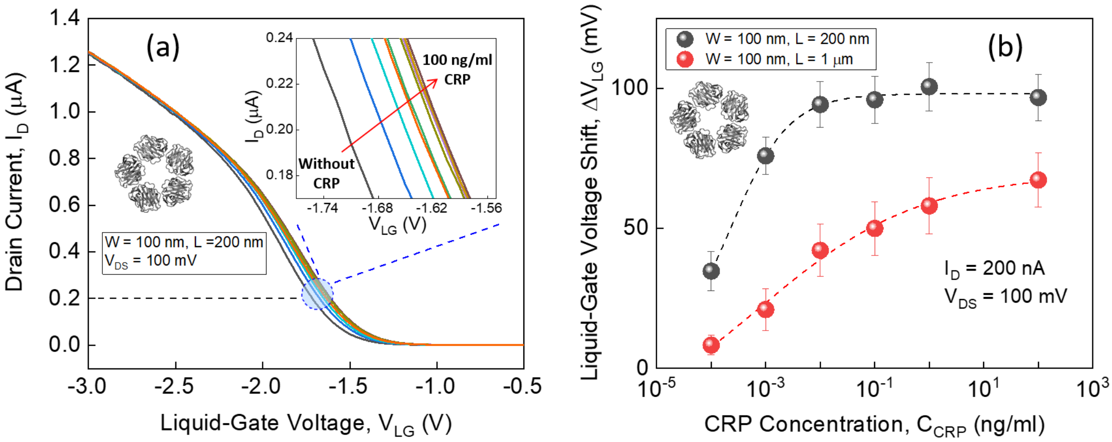


Figure 4.25: (a) Transfer characteristics of the LG TL NW sensor with the NW width of $100\ nm$ and length of $200\ nm$ functionalized with anti-CRP antibodies and measured for various CRP concentrations in PBS solution with $pH = 7.4$; (b) Responses of the developed TL NW sensors to different concentrations of CRP biomarkers. Vertical error bars account for statistical errors obtained for devices with different lengths.

Similarly to the detection of cTnI biomarkers, the $200\ nm$ long NW FETs saturate much faster with increasing CRP concentration than devices with a length of $1\ \mu m$. The reason is a larger sensing area of longer nanowires which allows immobilization of a larger number of antibodies responsible for selective binding of CRP antigens. To confirm the selectivity and absence of anti-interference during the sensing experiments, we performed the control measurements. The results are shown in Figure 4.26.

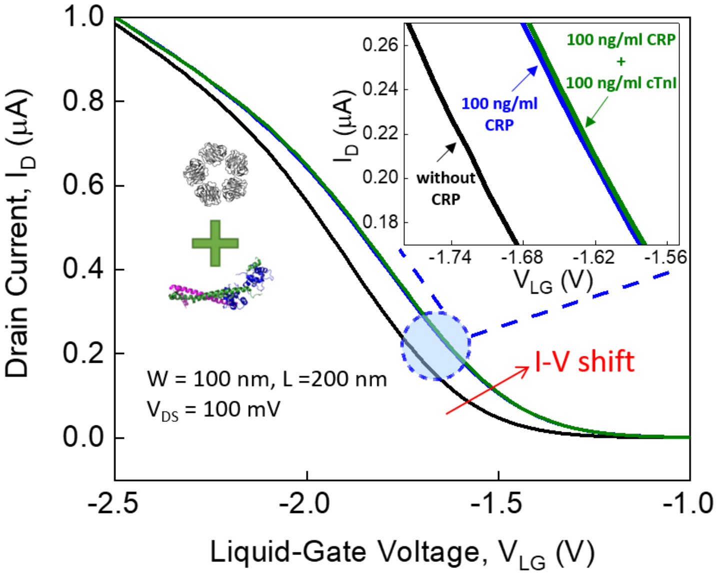


Figure 4.26: The control sensing experiment performed for the TL NW biosensor functionalized with anti-CRP antibodies. The cTnI antigens are used as the competitive analyte molecules. The black curve corresponds to the anti-CRP functionalized NW biosensor incubated in the pure PBS solution with no analytes. The same device is further exposed, in sequence, to the buffer solution containing $100\ ng/ml$ of CRP antigens (blue curve). The green curve shows the control I-V curve measured after adding $100\ ng/ml$ concentration of cTnI antigens. The results demonstrate the high selectivity of the developed biosensors.

First, the nanowire sensor functionalized with anti-CRP antibodies was exposed to the buffer solution containing $100\ ng/ml$ concentration of CRP. As expected, a pronounced shift of the I-V characteristics was registered upon the injection of CRP antigens. A high concentration ($100\ ng/ml$) of cTnI antigens was then added into the gating solution and the I-V measurements were repeated. As can be seen in Figure 4.26, the device demonstrated good stability of I–V characteristics reflecting that no noticeable changes were registered when cTnI molecules are introduced in the testing solution. This result confirms the high selectivity and specificity of the developed TL NW FET biosensors.

To evidence the efficient attachment of CRP biomarkers on the nanowire surface of the developed biosensors, we performed a profile imaging of NW structures using atomic force microscopy (AFM). Typical 2D AFM images of the SiO_2-covered TL NW structures before the functionalization step and after the detection of CRP molecules are shown in Figures 4.27(a) and 4.27(b), respectively. Corresponding 3D AFM micrographs are displayed in Figures 4.27(c) and 4.27(d).

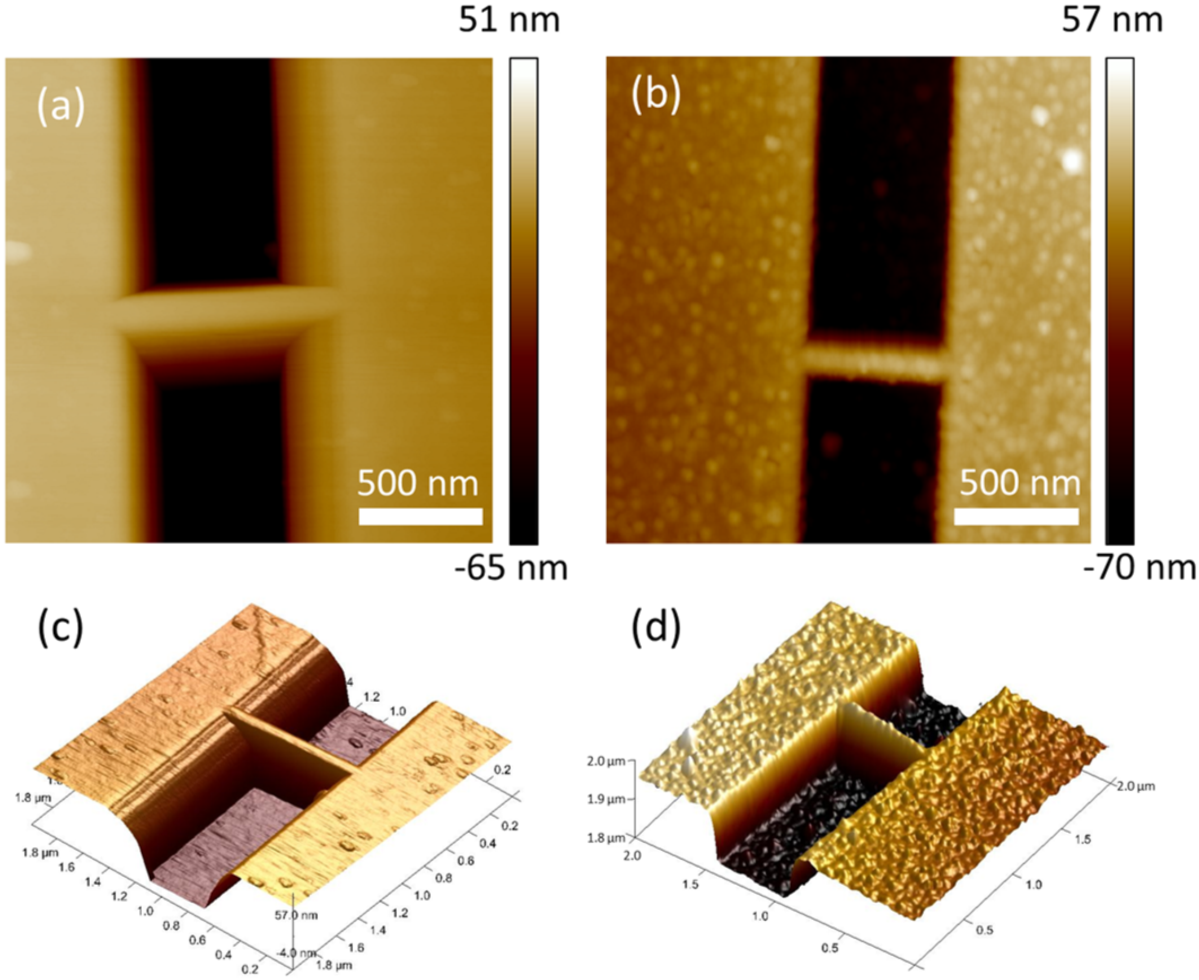


Figure 4.27: Typical AFM images of the fabricated TL NW FET biosensor before the functionalization step (a, c) and after detection of CRP antigens (b, d).

As can be seen, the roughness of the TL NW surface before the functionalization procedure was about $2\ nm$, which is a typical value for the bare SiO_2-covered structures. However, the roughness of the surface has been increased to $12\ nm$ after the performed sensing experiment. The value is consistent with a typical dimension of a single CRP antigen molecule [20, 82] and confirms the efficient attachment of CRP biomarkers to the sensing area of the fabricated devices.

4.2.3 Noise spectroscopy characterization of TL nanostructures

Nanotransistor-based biosensors that are very similar to the state-of-the-art semiconductor transistors demonstrate considerable advantages such as cost-effective mass production and biocompatibility as well as have a great potential to be reliable, simple, fast, highly sensitive, user-friendly and portable bioanalytical tools for biosensing and biomedical applications. For these challenges, careful consideration of noise is required. It has been traditionally considered that the electrical noise is the limiting factor that typically affects the sensitivity of the sensor and defines its detection limit. However, for the nanoscale devices, noise becomes single-carrier phenomena and provides excellent opportunities for its various practical applications including biosensing.

The primary objective of this thesis is to demonstrate that the intelligent use of noise peculiarities in nanoscale devices lead to a clearly enhanced performance with increased sensitivity and improved signal-to-noise ratio. Here, we perform and discuss the results on noise spectroscopy characterization of the unique LG TL nanostructures of different widths and lengths to study the fluctuation phenomena and dynamic processes in newly fabricated TL NW sensors. The detailed description of the experimental setup used for measurement of the low-frequency noise in Si TL NW FETs is presented in Section 3.2. Noise spectra in the frequency domain allow us to directly analyze contributions from different noise sources and reveal the origin of the noise in tested devices. The potential sources of noise in typical nanoscale FETs are discussed in detail in Section 2.4.2. All measurements of low-frequency noise were performed in a custom-built Faraday cage to block any external electromagnetic fields and thus to obtain reliable noise characteristics of the devices under study. The obtained experimental results demonstrate that the devices with gate area $A > 1\ \mu m^2$ exhibit $1/f$ flicker noise as the result of interactions of charge carriers with different traps randomly distributed in the gate oxide layer of the tested FETs. At the same time, RTS noise as a result of single-trap phenomena emerges as a dominant noise source in $sub-\mu m$ LG Si TL NW FETs. We focus our attention primarily on the RTS process in fabricated LG devices as it provides a unique possibility to sense target analytes interacting with the NW sensors. Such a possibility is demonstrated and discussed below in this thesis.

Study of $1/f$ ***noise in Si TL NW FETs***

Typical low-frequency (LF) noise spectra measured on the accumulation-mode $p^+ - p - p^+$ TL NW FET structures with doping concentrations of $10^{16}\ cm^{-3}$ and $10^{17}\ cm^{-3}$ are shown in Figures 4.28(a) and 4.28(b), respectively. The devices with the NW width of $100\ nm$ and a length of $4\ \mu m$ were liquid-gated and operated in a linear regime by applying a constant drain-source bias of $-100\ mV$. The back-gate contact was grounded. The noise measurements were performed under the same conditions for both FETs to compare the noise performance. The noise characteristics were acquired at different values of the liquid gate voltage applied in the range from $V_{LG} = -1\ V$ to$V_{LG} = -3\ V$. As can be seen from Figures 4.28(a) and 4.28(b), both devices demonstrate a clear $1/f$ flicker noise behavior within the entire range of the liquid-gate voltages applied. It should be noted that such registered noise behavior is typical for both $n^+ - p - n^+$ and $p^+ - p - p^+$ fabricated TL NW FETs with the gate area $A > 1\ \mu m^2$. For the LG transistors with the gate area in the range $A < 1\ \mu m^2$, the noise spectra typically contain one or a few Lorentzian-shaped components that correspond to generation-recombination processes related to individual traps.

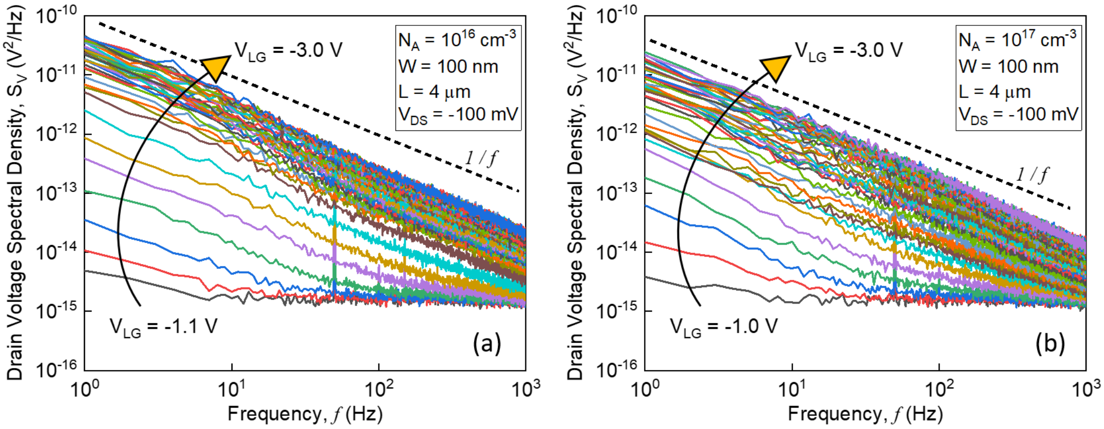


Figure 4.28: Typical voltage noise PSD spectra of $p^+ - p - p^+$ Si TL NW FETs with doping concentration in the channel of (a) $10^{16}\ cm^{-3}$, and (b) $10^{17}\ cm^{-3}$ measured at different liquid-gate voltages varying from $-1\ V$ to $-3\ V$ with the step of $-0.1\ V$. The TL FET structures with the NW width of $100\ nm$ and a length of $4\ \mu m$ were biased at a constant drain-source voltage of $(-100\ mV)$.

The dependences of the current noise power spectral density (PSD) taken at 10 Hz are plotted in Figure 4.29(a) as a function of the overdrive liquid-gate voltage (V_{OD}) from subthreshold to saturation for TL NW devices with different concentrations of dopants in the channel. As can be seen from Figure 4.29(a), a very good correlation between current noise PSD and applied liquid-gate voltages observed for both types of devices demonstrating a near-linear dependence of S_I on V_{OD}. This result indicates that mobility fluctuations [13] are the dominant noise-causing mechanism in the tested structures. To further investigate this assumption and make a valid comparison of noise characteristics among TL NW FET structures with different concentrations of dopants in the channel, we plotted in Figure 4.29(b) the dependencies of normalized drain current PSD at $10\ Hz$ as a function of measured drain current.

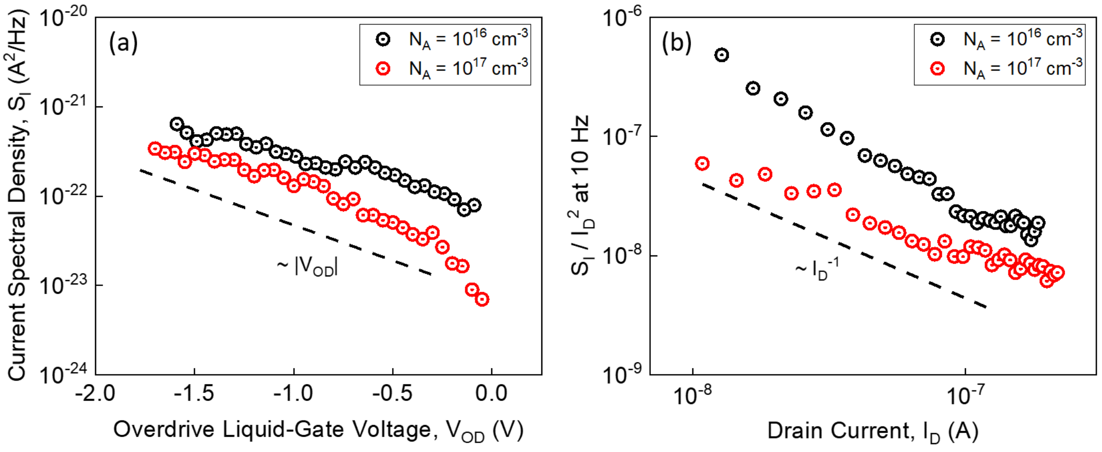


Figure 4.29: Measured drain current noise PSD, S_I taken at 10 Hz and plotted as a function of the overdrive gate voltage (V_{OD}) for different devices. S_I behaves as a monotonous function of gate voltage with a slope close to 1 in semi-logarithmic scale for both types of structures under study. Such noise behavior implies that the mobility fluctuation model can be applicable to interpret the origin of $1/f$ flicker noise registered in tested devices. (b) Normalized drain current PSD at 10 Hz measured for the same TL NW devices and plotted as a function of drain current. The solid straight lines in figures (a) and (b) are drawn as a guide to the eye to depict $\sim |V_{OD}|$ and $\sim |I_D^{-1}|$ trends, respectively.

As can be seen from Figure 4.29(b), a higher noise level is registered for TL NW FET with 10^{16} cm^{-3} concentration of dopants in the channel compared to its highly doped analog with $N_A = 10^{17}$ cm^{-3}, albeit both devices were measured at the same conditions. It is also evident from Figure 4.29(b) that the normalized current noise varies as the reciprocal of the drain current from weak to strong accumulation for the device with the channel doping concentration of 10^{17} cm^{-3}, while for the TL NW device with $N_A = 10^{16}$ cm^{-3} in the channel, S_I/I^2 versus I_D exhibit a dependence with a slope close to (-1) at the strong accumulation of holes and with a slope close to (-2) in the subthreshold region. From Equation 2.21, it follows that S_I/I^2 is reciprocally proportional to the number of carriers in the channel and thus to the drain current in devices operating in the linear (ohmic) working regime. If such dependence of S_I/I^2 versus I_D is observed, it can be concluded that $1/f$ noise is due to the mobility fluctuations. Therefore, the results showed in Figure 4.29(b) further confirm that the mobility-fluctuation noise generation mechanism is dominant for both types of devices. A stronger than linear dependence of normalized drain current PSD on I_D for the device with the channel doping concentration of 10^{16} cm^{-3} operating in the subthreshold region indicates the contribution of other noise generation mechanisms such as diffusion-assisted or trap-assisted generation-recombination processes in accumulation-mode Si TL NW FETs [83].

To fully characterize the liquid-gate-dependent noise in tested devices, we also plotted in Figure 4.30(a) the dependence of the input-referred voltage noise (S_{V_G}) on the overdrive liquid-gate voltage. If the input-referred gate voltage noise show no dependence on overdrive gate voltage, one can conclude that the carrier-number fluctuations model is involved. However, the data showed in Figure 4.30(a) clearly demonstrate that S_{V_G} is a function of the the overdrive liquid-gate voltage for both devices. Therefore, in this case, it can be inferred that mobility fluctuations are indeed the main LF noise source in the large-area accumulation-mode LG Si TL NW FETs as expected for p-type FET devices. It should be also noted that fabricated high-doped TL nanostructures demonstrate a lower level of the input-referred voltage noise compared, for example, to the undoped single-layer nanowires with the same gate area (see Figure 4.30(a)). This confirms the high-quality of the fabricated TL NW devices.

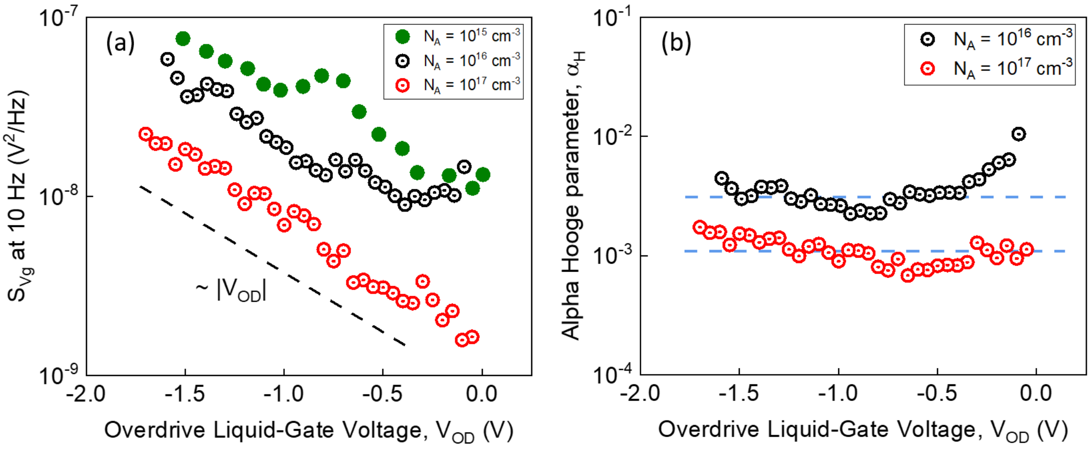


Figure 4.30: (a) Input-referred noise, S_{V_G} as a function of the overdrive gate voltage calculated using measured noise spectra shown in Figures 4.28(a) and 4.28(b) for devices with a doping concentration in the channel of (a) $10^{16}\ cm^{-3}$ and (b) $10^{17}\ cm^{-3}$, respectively. The tested FETs demonstrate a gate-dependent S_{V_G} noise behavior which is typical for p-type devices. (b) Dimensionless Hooge parameter, α_H obtained from the measured $1/f$ noise spectra and plotted as a function of the overdrive liquid-gate voltage (V_{OD}).

Figure 4.30(b) shows the dependence of the dimensionless Hooge parameter (α_H) on the overdrive liquid-gate voltage for the tested devices with different concentrations of dopants in the channel. To evaluate the Hooge parameter as a measure of the "noisiness" of the transistor structure, the following expression was used:

$$\alpha_H = \frac{fS_I}{I_D^2}\frac{I_D L^2}{q\mu_{FE}V_{DS}} \tag{4.3}$$

where $\dfrac{fS_I}{I_D^2}$ is normalized flicker noise amplitude obtained from the measured $1/f$ noise spectra, I_D is drain current in a transistor with the NW length of L biased at the drain-source bias of V_{DS}; q is the elementary charge, and μ_{FE} is field-effect mobility estimated using Equation 4.1. For the $p^+ - p - p^+$ TL NW FET with $N_A = 10^{17}\ cm^{-3}$ in the channel, the calculated α_H demonstrates a nearly constant behavior with small variations around the average value of 1.1×10^{-3} within the entire range of the liquid-gate voltages applied. It should be noted that such behavior of α_H is typical for the Hooge mobility fluctuations model. For the device with $N_A = 10^{16}\ cm^{-3}$ in the channel, α_H exhibits behavior which is different in weak and strong accumulation regimes of operation. In the voltage range $V_{OD} < -0.5\ V$, α_H is the function of V_{OD} confirming the contribution of other noise mechanisms different from mobility fluctuations (e.g., trapping/detrapping noise, dielectric polarization noise). At higher V_{OD}, α_H is nearly constant and approaches the value of 3.1×10^{-3}. It should be noted that the obtained dimensionless α_H values are comparable with those obtained for the conventional LG NW structures covered with SiO_2 [36]. These results certainly confirm the high quality and low-noise performance of the unique LG TL NW FETs.

Figure 4.31(a) shows some of the state-of-the-art experimental results of input-referred voltage noise (S_{V_G}) as a function of transistor gate area A, with A down to a few tens of nm^2. The results also include the data that was experimentally obtained for the fabricated TL NW devices with different channel doping concentrations. As predicted by Equation 2.20, S_{V_G} noise is inversely proportional to the transistor gate area A. This latter statement seems to be valid in the majority of experimental cases as can be seen in Figure 4.31(a). We also see that our LG devices with different channel doping concentrations perfectly follow the scaling noise trend that can be guided by Equation 2.20 with $N_{ot} = 10^{10}\ cm^{-2}$ and $N_{ot} = 10^{8}\ cm^{-2}$ as upper and lower approximations, respectively. Interestingly, as one can deduce from Figure 4.31(a), the guidelines based on Equation 2.20 are valid over the full range of A, even in the area where there is statistically no traps in a gate dielectric of a nanotransistor. This fact can be understood if one considers the dielectric-polarization noise as the fundamental limit for nanoscale devices due to the thermal fluctuation of dipoles in the gate oxide. In particular, we see that the consideration of Equation 2.15 with a typical dielectric loss tangent of $tg\ \delta = 3.8 \times 10^{-3}$ for the SiO_2 provides a reasonable approximation of S_{V_G} noise in the range of A which corresponds to the absence of traps.

At the same time, considering the lower trap density of $N_{ot} = 10^{8}\ cm^{-2}$, one can see that $N_{ot} \times A = 1$ corresponds to a single trap in a nanotransistor if its gate area is $A = 1\ \mu m^2$. Indeed, our experiments performed for the $sub-\mu m$ NW devices demonstrate that S_{V_G} noise might be increased by up to two orders of magnitude when compared to devices with no active traps due to the RTS noise. However, as we will show below in this thesis, the nanoscale devices exploiting RTS noise as the result of single-trap phenomena offer unique opportunities for noise suppression.

Figure 4.31(b) shows the role of the transistor gate area A for the charge noise S_q defined as:

$$S_q = \frac{C_{ox}^2 S_{V_G}}{q^2} \tag{4.4}$$

where q is the elementary charge, C_{ox} is the gate oxide capacitance per surface unit, and S_{V_G} is the input-referred voltage noise of a nanotransistor. In principle, S_q reflects the smallest charge

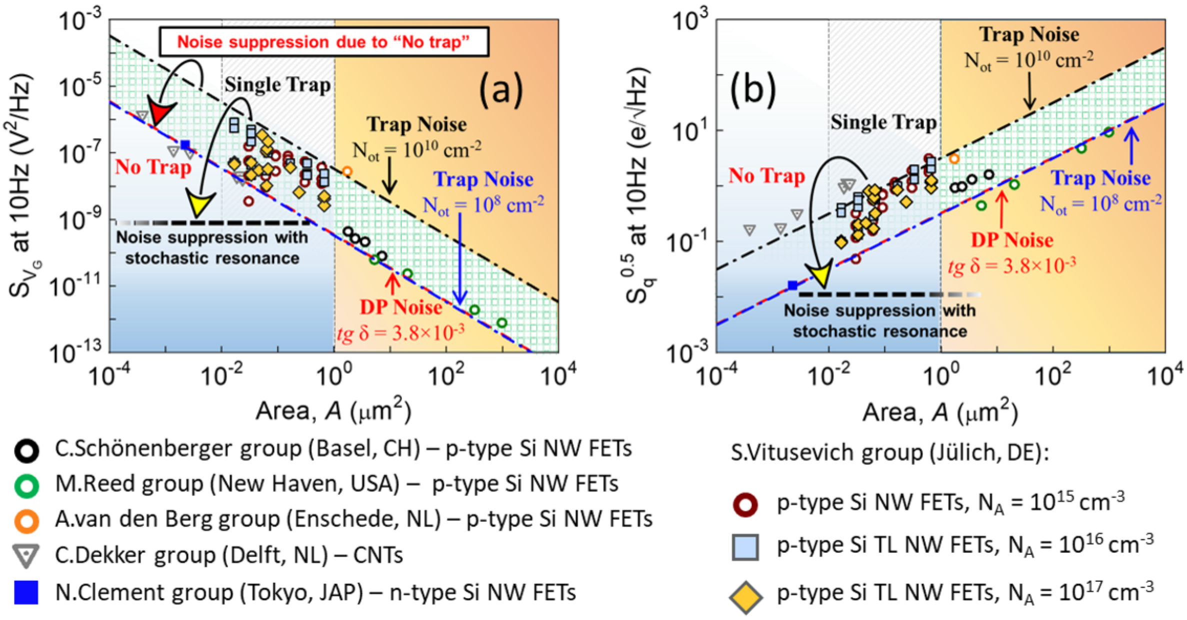


Figure 4.31: Low-frequency noise in nanoscale biosensors. Experimental results of (a) S_{V_G} and (b) $S_q^{0.5}$ noise at $10\ Hz$ plotted as a function of gate area A for Si NW FETs with different channel doping concentrations. The tested devices demonstrate the common scaling trends which are predicted by theory and based on the experimental results obtained by different worldwide known research groups: C. Schönenberger [13], M. Reed [84], A. van den Berg [85], C. Dekker [32], N. Clement [18]. The red arrow indicates noise suppression due to no traps, while the yellow arrow shows the noise suppression below the thermal limit when considering RTS noise as a signal.

quantity that can be detected with such transistor-based biosensors. As it appears from Equation 4.4 and is evident from Figure 4.31(b), S_q scales as A demonstrating that smaller devices tend to have lower charge noise which is promising for the development of ultrahigh-sensitive biosensors. It should be emphasized that our fabricated devices also demonstrate the same tendency and possess the ability for the sub-elementary charge or even single-charge sensitivity in liquid. However, as it is evident in Figures 4.31(a) and 4.31(b), the sensing capability of even the smallest biosensors still limited by the presence of dielectric-polarization noise. Later in this thesis, we discuss this issue and show in particular that, by analogy with the stochastic resonance noise suppression approach found in biological systems, STP in the nanoscale devices can be used for noise suppression even beyond the thermal noise limit level.

Study of RTS noise in Si TL NW FETs

As mentioned above, a main physical source of low-frequency noise in transistor-based structures is attributed to the interactions of charge carriers with traps that are randomly distributed at the Si/SiO_2 interface or in a gate oxide layer of a nanotransistor. If the number of active traps is reduced to a single trap, a strong modulation of nanotransistor conductance appears as single-trap phenomena (STP), resulting in two-level characteristic switching events known as random telegraph signal (RTS) noise.

In this section, we investigate and discuss the fabricated TL NW structures configured as liquid-gated FETs from the viewpoint of STP performance. The detailed fabrication process of the unique Si TL NW FETs is described in Section 4.1. Figure 4.32 schematically illustrates a liquid-gated TL NW structure with a single trap in the gate oxide that randomly exchanges mobile charge carriers with a conductive channel of the nanotransistor. Such random trapping and detrapping of charge carriers result in the RTS signal which dominates the LF noise in the nanoscale device.

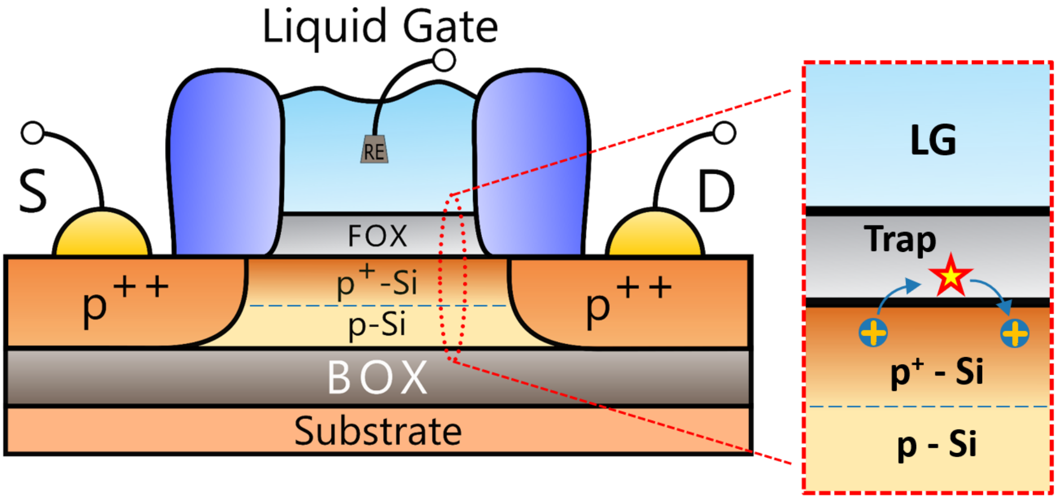


Figure 4.32: Schematic illustration of LG Si TL NW FET configured as a liquid-gated accumulation-mode p-type FET-based biosensor. The nanostructure contains a single trap in the front-gate oxide layer that randomly exchanges charge carriers (holes) with a conductive channel.

Figure 4.33(a) shows a typical RTS time trace as time-dependent fluctuations in the drain current measured in a 100 nm wide and 200 nm long Si TL NW structure with 10^{17} cm^{-3} concentration of Boron dopants in the channel. The tested device was liquid-gated at a constant drain-source bias of -20 mV and measured at room temperature. As can be seen from Figure 4.33(a), the drain current of the TL nanostructure fluctuates between two distinct levels that correspond to the “capture” and “emission” states. The mean duration of stay of a charge carrier in the capture and the following emission states are characterized by the average emission (τ_e) and capture (τ_c) time constants, respectively. A probability for a single trap to be empty or occupied by a charge carrier is governed by the capture rate $R_c = 1/\tau_c$, and the emission rate $R_e = 1/\tau_e$, respectively. At the same time, a change of the signal when a transition event between the sates occurs is characterized by the RTS amplitude (ΔI).

In principle, if the RTS amplitude to background noise is high as in the case shown in Figure 4.33(a), the analysis of the RTS phenomenon and extraction of all the RTS parameters can be performed using only the time domain data. For instance, in such a case a relatively simple threshold level-crossing or time-derivative algorithms [86] can be applied to extract characteristic time constants directly from the measured time trace. Otherwise, the measurements in the frequency domain are required to fully characterize "noisy" RTS. The detailed procedure for the analysis of RTS data is described in Section 3.4. Figure 4.33(b) shows the amplitude histogram of the recorded two-level drain current RTS fluctuations. As can be seen, the amplitude distribution curve is characterized by two Gaussian peaks. Each peak denotes the corresponding RTS states and can be fitted to a Gaussian distribution (see Equation 3.5) due to the presence of background noise (e.g. DP noise, thermal noise). The distance between peaks corresponds to the RTS amplitude. The PSD of the measured RTS noise is shown in Figure 4.33(c). The PSD is calculated by performing the Fast Fourier transform. As expected for the RTS process, the PSD of the measured current fluctuations has a Lorentzian shape that can be fitted with Equation 3.7. A red dashed line represents a pure Lorentzian spectrum of two-level RTS described by Equation 2.25. A black dash-dotted line with a slope of $1/f$ in Figure 4.33(c) reflects the PSD of the device background noise. The fitting of the PSD spectrum provides a value of the RTS corner frequency which is the function of both capture and emission time constants (see Equation 2.26).

Figure 4.33(d) shows the distribution of dwell times in capture and emission states. As can be seen from Figure 4.33(d), the durations of both RTS capture and emission characteristic times obey a Poisson distribution $P(t) \sim exp(-t/<t>)$, where $<t>$ denotes a capture or emission time constant averaged over all states of an ensemble at a given time t. This confirms that the measured RTS noise is a fully stochastic Poisson process as expected. If the registered RTS time trace contains a relatively large number of transition events between capture and emission states (at least 200), a fit of dwell times histogram to the Poisson distribution can be used as an alternative method to extract RTS characteristic time constants. Otherwise, the accurate analysis of RTS data should be performed using a statistical method that requires both frequency and time domain measurements.

Average capture and emission time constants characterizing the registered RTS process are shown in Figure 4.34(a) as a function of drain current. As can be seen from Figure 4.34(a), the average emission characteristic time remains about constants in the entire measured current range, while the average capture time demonstrates a sharp decrease with increasing transistor drain current. It should be noted that such enhanced behavior of characteristic capture time constant is typical for the RTS processes measured in LG TL NW FETs. In particular, the data showed in Figure 4.34(a) clearly demonstrate that the capture time constant depends on the drain current with a slope of (-3) on the logarithmic scale. It should be emphasized that the registered dependence of capture time on drain current that is controlled by the surface potential is much stronger than that with a slope of (-1) predicted by a standard SRH model (see Equation 2.31). This result highlights the fact that the RTS process is extremely sensitive to the changes in

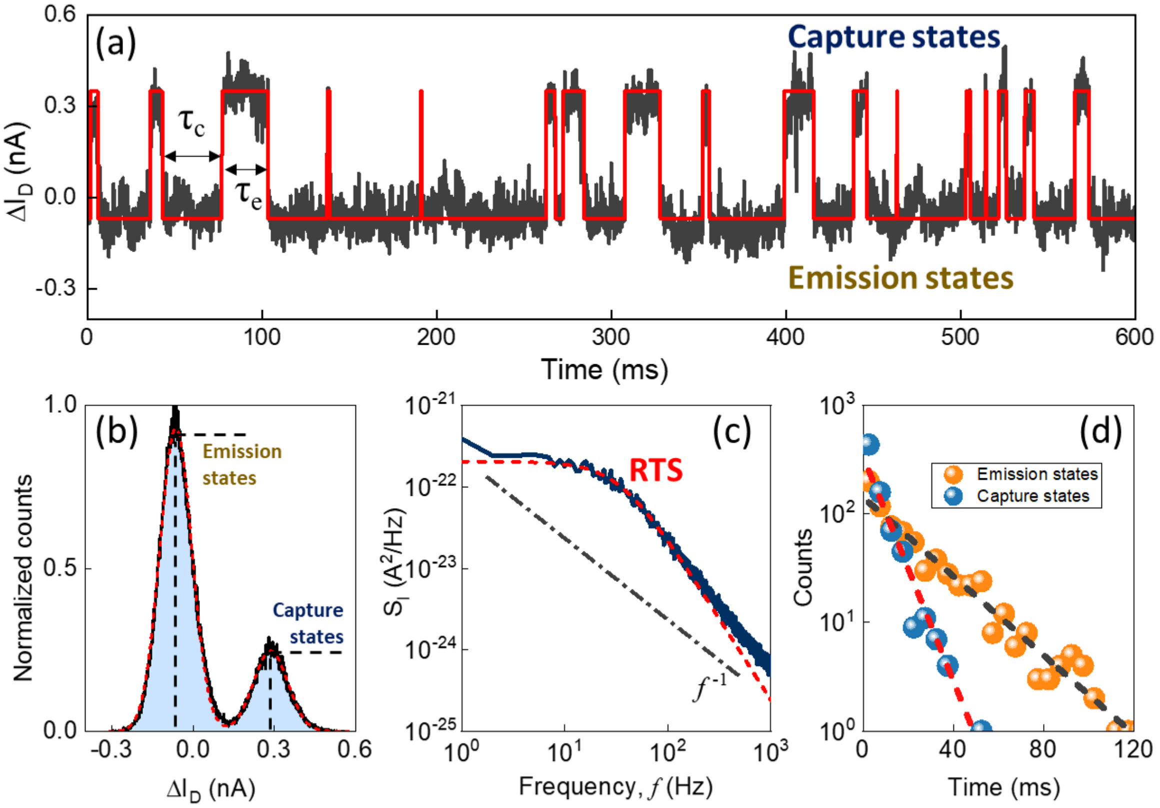


Figure 4.33: (a) Drain current time trace measured in a $100\ nm$ wide and $200\ nm$ long LG Si TL NW FET with $10^{17}\ cm^{-3}$ concentration of dopants in the channel. The drain current randomly switches between capture and emission states reflecting a typical two-level RTS behavior in the fabricated LG TL nanostructures; (b) Normalized distribution of drain current values obtained from the time trace shown in (a). The amplitude histogram contains two maxima fitted with Gaussian peak functions; (c) Drain current PSD as a function of frequency. A dashed red curve shows the Lorentzian-shaped component that corresponds to the RTS. A dashed blue line with $1/f$ slope corresponds to the device background noise; (d) Distributions of time durations in capture and emission states fitted with Poisson distributions.

surface potential. In the case of LG NW biosensors, the latter depends on V_{LG} and is a function of the analyte concentration interacting with the surface of the sensors. Therefore, the changes in surface potential due to the interaction of nanosensors with the target analytes modulate the population of channel charge carriers (drain current) and thus simultaneously induce a change in RTS capture time. This fact suggests that the monitoring of RTS characteristic capture time constant as a signal of interest is an efficient and absolutely new strategy for highly sensitive biosensing with enhanced sensitivity. The validity of the approach is demonstrated further in this thesis.

Figure 4.34(b) displays the trap occupancy probability (g-factor, g) calculated using Equation 2.24, and plotted as a function of V_{LG} applied. As expected for STP, g-factor follows a widened Fermi-type distribution due to the partial potential drop at the trap energy level. It is evident from the gate-bias dependence of g that at low liquid-gate voltages, the probability of a

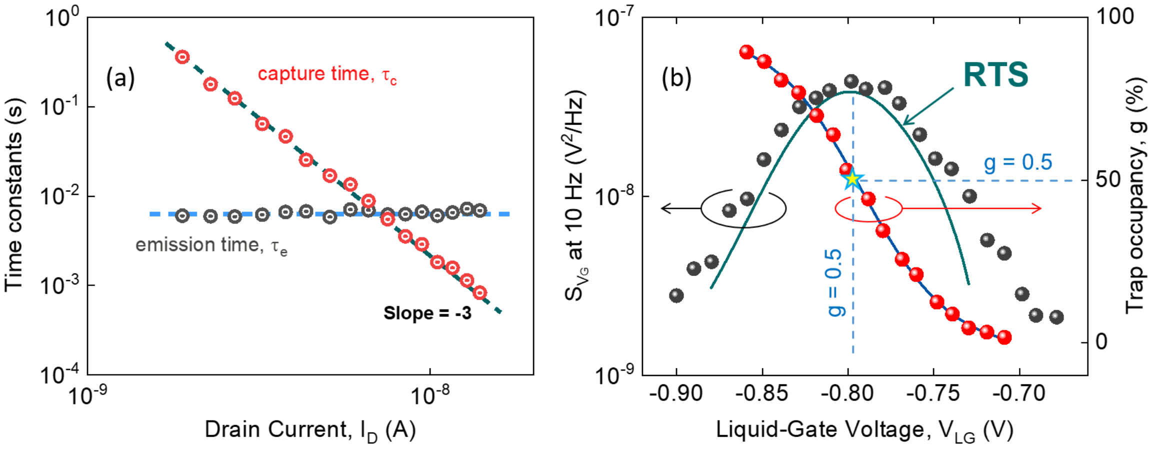


Figure 4.34: (a) RTS characteristic capture and emission time constants plotted as a function of drain current. The behavior of RTS time constants is typical for LG TL NW FETs. The dashed colored lines represent a visual guide; (b) Input-referred voltage noise taken at 10 Hz (left axis) and trap occupancy probability (right axis) plotted as a function of liquid-gate voltage for the measured RTS noise. The noise is maximized when $g = 0.5$ (shown as asterisk). The solid blue line shows the fitting of the measured g-factor values with the sigmoid function. The solid dark green line represents S_{V_G} calculated using Equation 2.28 considering fitted g-factor values.

charge carrier to be captured by the trap is small, while the latter is fully occupied at high V_{LG}. It should be noted that the increase of g-factor with increasing carrier concentration controlled by the gate voltage reflects a behavior typical for acceptor-type traps [52, 55].

As it follows from Equation 2.28 and can be seen also in Figure 4.34(b), the RTS noise is maximized relative to the background noise if the probability of the trap to be occupied equal to 50% (i.e., $g = 0.5$), which corresponds to the case when the trap energy level coincides with the Fermi level of the system. The result is to be expected since at this condition the number of switching events between capture and emission states is maximized. Interestingly, the RTS effect as a result of STP has been usually avoided in small electronic devices as it gives rise to the noise level (see Figure 4.34(b)). However, if RTS parameters (e.g., trap occupancy probability, time constants) are monitored as a signal, then RTS noise becomes an object of increasing interest providing excellent opportunities for ultimate scaling, sensitivity enhancement, and even for noise suppression as it will be shown below in this thesis (see Chapter 5). Intuitively, one could expect that the utilization of RTS as a signal would provide a noise reduction corresponding to the difference between a single-trap and a trap-free structure, which is between one or two orders of magnitude as can be seen in Figure 4.31(a). However, we demonstrate below that the potential of single-trap phenomena for the noise suppression is even larger revealing that the low-frequency noise in nanoscale devices can be indeed suppressed even beyond the thermal limit by monitoring RTS parameters in an approach similar to the stochastic resonance effect.

4.2.4 Identification of single traps in fabricated TL NW devices

The RTS phenomenon in small electronic devices provides a unique opportunity to study single-electron and single-atom features at the nanoscale. In particular, bias and temperature dependences of RTS noise can be used to extract important information such as single trap energy level, capture and emission kinetics, capture cross-section, and spatial location of the trap. In this section, we investigate transport and noise properties of back-gated Si TL NW FETs in a wide temperature range ($100 - 300\ K$) to obtain the physical characteristics of the single traps responsible for the RTS noise in the unique TL NW structures. All electrical and low-frequency noise characterization of the tested devices were performed using ultra-low noise home-made measurement setup, which allows setting the definite temperature of a sample introduced into a custom-built vacuum chamber. The detailed description of the temperature setup is presented in Section 3.3 of this thesis, while the noise measurement setup is described in detail in Section 3.2. The structures under study here are p-channel accumulation-mode TL NW FETs with the channel doping concentration of $10^{16}\ cm^{-3}$. The devices were biased at low drain-source voltage, $V_{DS} = -100\ mV$ that corresponds to the linear working regime of the transistors.

Figure 4.35(a) shows typical dependencies of the drain current on the applied back-gate voltage measured on Si TL NW FET with a width of $100\ nm$ and a length of $200\ nm$ at different temperatures. As can be seen in Figure 4.35(a), the slope of transfer I–V characteristics increases with a temperature decrease. It should be noted that such behavior is typical for silicon-based devices and can be explained by considering the temperature dependence of carriers' mobility. In the measured temperature range, the effective mobility of holes as majority carriers in accumulation mode p-type FETs is mostly affected by the phonon scattering. The latter occurs due to the lattice vibrations which decrease with the temperature. Therefore, the slope of I–V curves increases in the measured temperature range as temperature decreases.

Figure 4.35(b) displays the drain-source voltage noise PSD as a function of frequency at the overdrive back-gate voltage ($V_{BG} - V_{th} = -1\ V$) and at different temperatures measured on the same $100\ nm$ wide and $200\ nm$ long Si TL NW FET. The measured noise spectra of the TL nanostructure demonstrate a Lorentzian-shaped noise PSD behavior indicating the RTS noise as a result of STP in the TL NW device under study. As can be seen in Figure 4.35(b), a shift of the characteristic corner frequency (f_0) of the Lorentzian-type PSD to the lower frequency range at fixed back-gate voltage is registered with a temperature decrease. This fact confirms that the Lorentzian-type PSD is the result of the thermally activated dynamic processes related to a single trap.

Typical time-dependent fluctuations of the drain current measured at room temperature on the same Si TL NW FET is shown in Figure 4.35(c). As can be seen, the recorded time trace displays discrete switching of the transistor drain current between two distinct levels due to the random trapping and detrapping of charge carriers. Such current behavior is typical for Si

TL NW FETs demonstrating RTS noise. The amplitude histogram of the recorded two-level fluctuations of the drain current is shown in Figure 4.35(d). The histogram can be perfectly fit with two Gaussian peaks which confirm two-state RTS switching kinetics. The height of each peak reflects the probability for a hole to be either in the free state or captured by the trap. The distance between the two peaks denotes the RTS amplitude, which is calculated to be around $\Delta I = 1.2\ nA$ for the measured RTS.

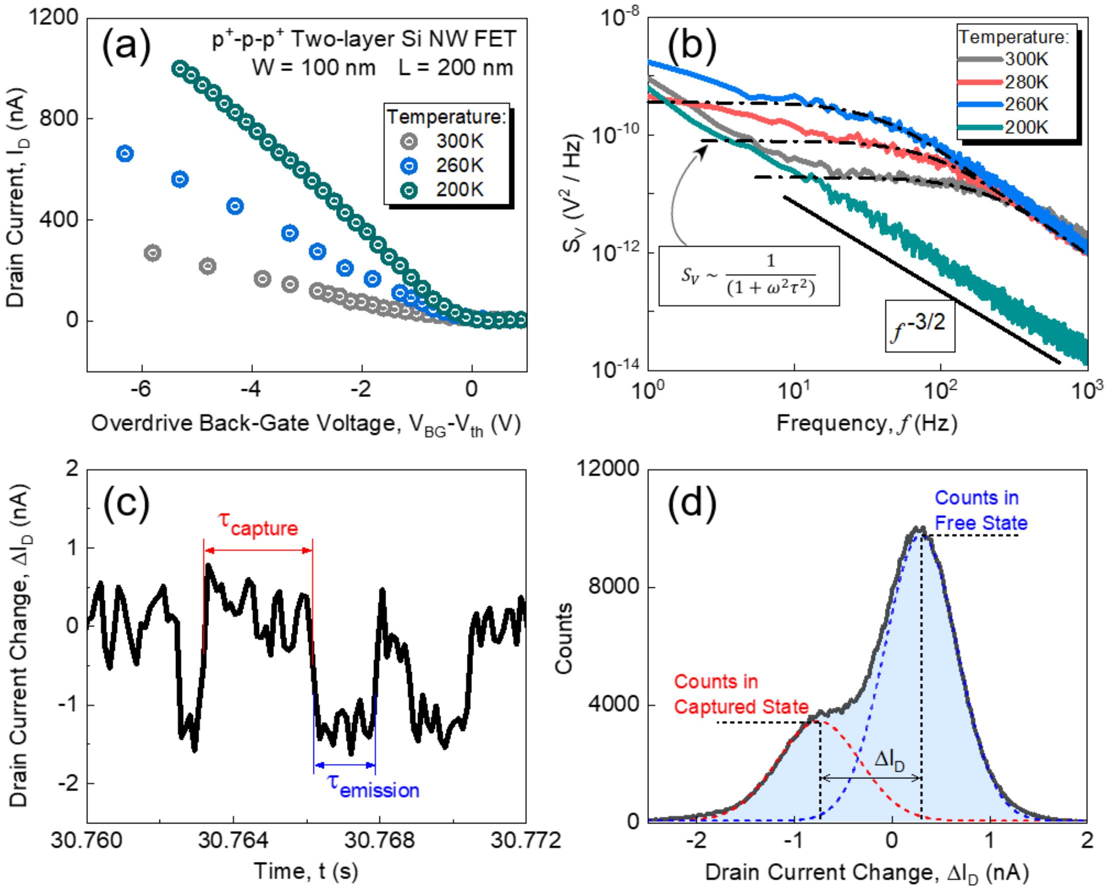


Figure 4.35: (a) Drain current versus overdrive back-gate voltage measured in $100\ nm$ wide and $200\ nm$ long Si TL NW FET at different temperatures and constant $V_{DS} = -100\ mV$; (b) Drain-source voltage noise PSD (S_V) for the same TL NW structure measured at overdrive back-gate voltage of $-1\ V$ and different temperatures; (c) Typical RTS time trace registered in the back-gated TL NW FET; (d) Amplitude histogram of the measured time-dependent drain current fluctuations shown in (c). The distribution of drain current values shows two well-resolved Gaussian peaks which confirm two-state RTS switching kinetics.

The effective time constant as well as average capture and emission characteristic time constants of the single trap are shown in Figure 4.36(a) versus drain current controlled by the back-gate voltage. As can be seen in Figure 4.36(a), the emission time constant slightly increases, while the capture time constant is linearly reduced in the log-log scale with increasing drain current. It should be noted that such behavior of time constants is predicted by the SRH model. As it can be also evident in Figure 4.36(a), the registered RTS is a relatively slow trapping/detrapping process with the characteristic time constants in the range of milliseconds. Such relatively large characteristic times suggest that the trap is located in the top oxide layer near to its interface with the silicon NW channel. The calculated ratio of capture time to emission time is plotted in Figure 4.36(b) as a function of overdrive back-gate voltage. As can be seen, the ratio demonstrates a linear dependence on a semi-logarithmic scale versus the back-gate voltage. Therefore, the trap depth in the gate oxide (x_t) can be estimated using the following expression [87]:

$$x_t = -d_{ox}\frac{kT}{q}\frac{d(ln(\frac{\tau_c}{\tau_e}))}{dV_{BG}} \tag{4.5}$$

where q is the elementary charge, k is the Boltzmann constant, d_{ox} stands for the oxide thickness and T is the temperature. Using the minimum least-square fit of the data shown in Figure 4.36(b) and the $d_{ox} = 8\ nm$ as the thickness of the front-gate SiO_2 layer in the fabricated structures, the depth of the active trap was estimated using Equation 4.5 to be $0.14\ nm$.

To further reveal the information concerning the trapping/detrapping mechanism and establish the origin of the trap in the tested Si TL NW FET, we performed a detailed analysis of measured temperature-dependent low-frequency (LF) noise. Figure 4.36(c) shows the Arrhenius plot of the experimental data. It is established that the effective time constant of the RTS process is related to the trap energy-level and capture cross-section as follows [83]:

$$ln\left(T^2\tau\right) \approx \left(\frac{\Delta E}{kT}\right) - ln\left[\left(\frac{4k^2\sigma_p}{gh^3}\right)(6\pi^3 m_e^{3/2} m_h^{1/2})^{1/2}\right] \tag{4.6}$$

where ΔE is the trap activation energy, σ_p is the hole cross-section in case of hole capture, m_e and m_h are the electron and hole masses, respectively, and g denotes here a degeneracy factor. It should be noted that Equation 4.6 is valid for our case since the measured characteristic time constant τ and the emission time constant τ_e demonstrate a nearly constant behavior at small concentrations of holes (small drain currents). Therefore, by fitting the data in Figure 4.36(c) to Equation 4.6, we calculated the activation energy of the single trap responsible for the RTS noise to be $0.29 \pm 0.02\ eV$. At the same time, from the intercept of the fitted curve and considering $g = 1$, the hole capture cross-section was estimated to be $(2.22 \pm 0.15)^{-18}\ cm^2$. The obtained trap parameters indicate that the single trap responsible for the RTS process in Si TL NW FET can be identified as a vacancy-boron complex [83]. The result highlights the contribution of boron dopants to the transport features of the fabricated two-layer nanowire structures.

The input-referred voltage noise at $10\ Hz$ measured for the same Si TL NW FET at room temperature is shown in Figure 4.36(d) as a function of a back-gate voltage. The registered bell-shaped noise behavior confirms that the trapping/detrapping processes due to the single trap are a dominant noise source in the nanoscale device when the trap is activated (at temperatures higher than $200\ K$). Interestingly, the investigated RTS noise in the tested device was

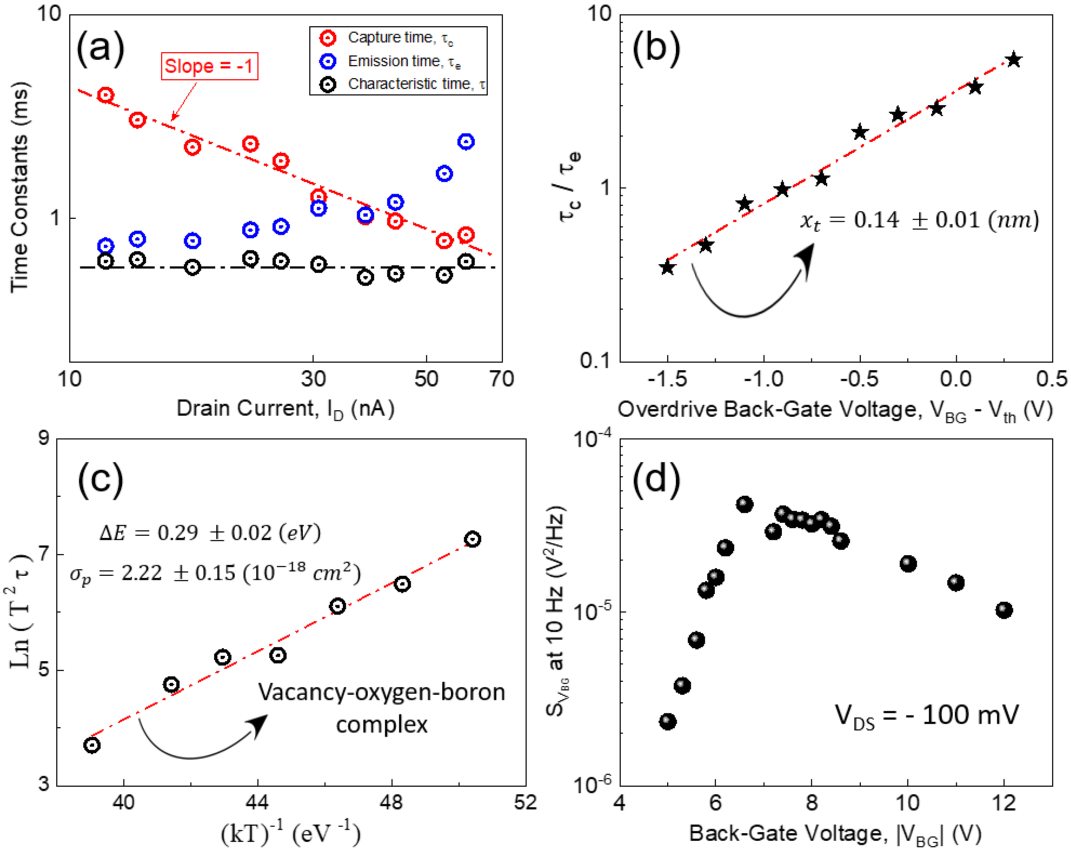


Figure 4.36: (a) Average time characteristics of the measured RTS noise plotted as a function of drain current at room temperature. The dash-dotted red line with the slope (-1) corresponds to the conventional SRH model. The dash-dotted black line demonstrates that the effective characteristic time, τ does not depend on drain current; (b) Calculated τ_c/τ_e ratio plotted versus overdrive back-gate voltage $(V_{BG} - V_{th})$; (c) The Arrhenius plot of the $ln(T^2\tau)$ versus $(kT)^{-1}$. The dash-dotted red line shows the fitting of the experimental data used to estimate the activation energy and capture cross-section of the trap responsible for the RTS noise in the tested Si TL NW FET. (d) The input-referred voltage noise as a function of a back-gate voltage (V_{BG}) measured for the same TL NW device at room temperature.

not further registered in the measured frequency range $(1\ Hz - 100\ kHz)$ at temperatures below $200\ K$ (see Figure 4.35(b)). Instead, the LF noise with PSD proportional to $1/f^{3/2}$ was observed and measured. It should be noted that the high-frequency parts of the noise spectra acquired at temperatures higher than $200\ K$ also demonstrate a characteristic slope of $(-3/2)$ (see Figure 4.35(b)). Such noise behavior suggests that the diffusion-assisted transport processes contribute to the generation-recombination processes in accumulation-mode p-channel Si TL NW FETs. This can be explained taking into account the interaction of holes with boron dopants in TL NW structures that consist of two Si layers with different doping concentrations. Considering that the low-doped silicon layer is approximately two times thicker than the high-doped top silicon layer, we assume that the conductive channel is mostly localized in the low-doped part of the silicon TL structure when applying back-gate voltage. Therefore, holes from the conductive channel randomly diffuse to the highly doped part of TL NW where they interact with active boron dopants. Such interactions induce a specific LF noise demonstrating $1/f^{3/2}$ characteristic behavior. It should be noted that this result confirms the specific two-layer design of the fabricated structures.

4.3 Single-carrier dynamics in liquid-gated TL NW FETs with different channel doping concentrations

When a single trap is active near the conductive channel of a nanosensor, it offers a unique opportunity to be used for transducing biological signals with enhanced sensitivity. The efficiency of such a biosensing approach based on single-trap phenomena is determined by the dynamics of trapping/detrapping processes related to a single trap (see Equation 2.42). Therefore, relevant parameters required to optimize the performance of nanobiosensors exploiting STP have to be determined and carefully investigated. In this chapter, we study the effect of channel doping concentration on the single-trap dynamics in liquid-gated NW FETs. For this purpose, we have specially designed and fabricated the unique Si TL NW FET structures with different concentrations of dopants in the channel. The optimized steps involved in the fabrication process are described in detail in Section 4.1. The only devices demonstrating RTS noise as the result of STP were of interest in this case.

Experimental dependencies of RTS characteristic capture times on drain current measured on the fabricated NW FETs with cannel doping concentrations of $10^{15}\ cm^{-3}$, $10^{16}\ cm^{-3}$, and $10^{17}\ cm^{-3}$ are presented in Figures 4.37(a), 4.37(b), and 4.37(c), respectively. All the devices under study were accumulation-mode $p^+ - p - p^+$ NW FETs biased at small constant $V_{DS} \leq 100\ mV$ and liquid-gated using a standard $Ag/AgCl$ reference electrode immersed in 10 mM physiological PBS buffer with $pH = 7.4$. Note, extracted RTS characteristic capture times rapidly decrease with increasing drain current of LG NW transistors. Such behavior is typical for acceptor-type traps responsible for the RTS noise in nanoscale devices. As can be evident in Figures 4.37(a), 4.37(b), and 4.37(c), the majority of measured RTSs demonstrate non-SRH behavior with a considerably stronger (superlinear) dependence of capture time on drain current compared to the classical SRH model (i.e., exponent $\gamma > 1$, see Equation 2.32). Figure 4.37(d) shows the distribution of RTS capture rate slopes, γ $(R_c = 1/\tau_c \sim I_D^{\gamma})$ extracted for the 100 nm wide and 200 nm long LG NW transistors with different doping concentrations in the channel demonstrating STP. As can be seen in Figure 4.37(d), the exponent γ increases with an increasing concentration of acceptor dopants in the accumulation-mode p-type NW FETs. It should be noted that the superlinear RTS capture time behavior with γ approaching even the value of 10 was registered for some traps in our highly doped TL nanostructures. These results reveal a significant effect of channel doping on STP dynamics in LG NW FETs.

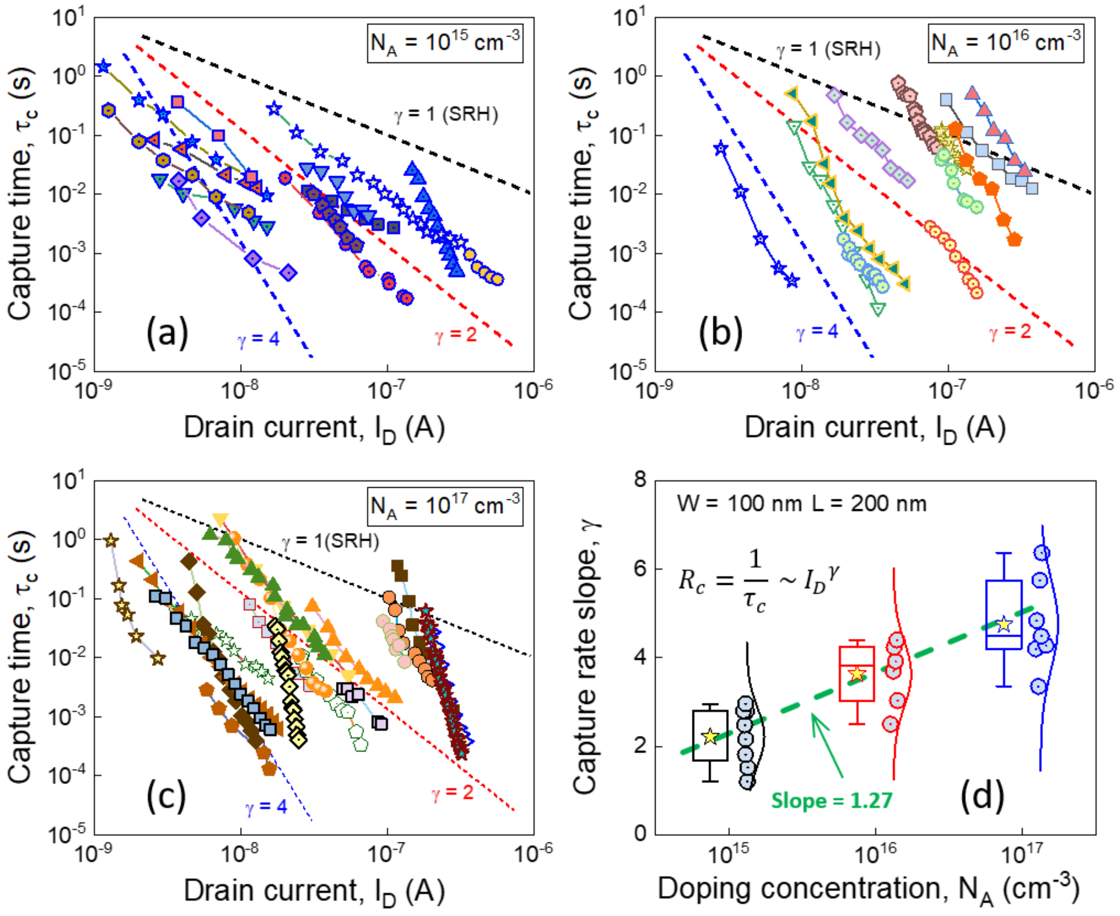


Figure 4.37: Comparison of RTS capture dynamics in LG Si NW FETs with different concentrations of dopants in the channel. (a-c) RTS characteristic capture time is plotted as a function of drain current measured for different liquid-gated FET nanostructures with the channel doping concentration of $10^{15}\ cm^{-3}$, $10^{16}\ cm^{-3}$, and $10^{17}\ cm^{-3}$, respectively. The dashed colored lines with indicated slopes are visual guidelines. The dashed black line with a slope $\gamma = 1$ reflects the behavior predicted by the SRH model; (d) The statistics of the RTS capture rate slopes measured for LG NW FETs with a width of $100\ nm$ and length of $200\ nm$. The whiskers are determined by the 5^{th} and 95^{th} percentiles. The solid yellow stars inside the boxes denote the calculated mean values of the γ slopes obtained for different concentrations of dopants in the NW FET channel. The dashed green line with a slope of 1.27 in the semilogarithmic scale represents the increase of the mean value of registered R_c slopes (γ) with increasing channel doping concentration.

As can be evident in Figure 4.37(d), γ demonstrates an approximately linear dependence with a slope of (1.27) in the semilogarithmic scale on the channel doping concentration in fabricated devices. Note, such behavior of measured RTS capture time constants is in a good agreement with the results previously reported for inversion-mode MOSFET devices [88], whereby the effect was attributed to the increase of the vertical electric field at the Si/SiO_2 interface with increasing channel doping concentration resulting in the stronger interaction of traps with charge carriers in the channel.

To understand and explain the mechanism behind the enhanced RTS capture dynamic in liquid-gated highly doped structures, we developed an analytical model based on the detailed description of the additional energy barrier (AEB) that mobile charge carriers have to overcome to be captured by the single trap at different values of surface potential controlled by a liquid-gate voltage. The model is derived for the acceptor-type traps [52, 89] according to the obtained experimental results shown in Figures 4.37(a), 4.37(b), and 4.37(c).

Proposed analytical model for enhanced RTS dynamic in LG NW FETs

In the case of the acceptor-type trap, which is neutral when empty and charged after trapping a charge carrier, the RTS capture rate is expressed as [52]:

$$R_c = 1/\tau_c = C_p N_V \cdot e^{-(E_F - E_V - q\psi_s)/kT} \cdot e^{-\Delta E/kT} = R_{SRH} \cdot e^{-\Delta E/kT} \tag{4.7}$$

where $R_{SRH} = C_p N_V \cdot e^{-(E_F - E_V - q\psi_s)/kT}$ is the conventional SRH capture rate of holes as majority carriers, C_p is the capture constant, $N_V = 2\left(\dfrac{2\pi m_p^* kT}{h}\right)^{3/2}$ is the effective density of states, E_V is the top of the valence band, E_F is the Fermi energy, ψ_s is the surface potential defined by the applied gate voltage, and ΔE is AEB due to the interaction of a hole with its image charge in the accumulation-mode p-type LG NW FET structures. The image charge appears on a liquid gate as the free charge carrier approaches the interface between media with different permittivities (e.g., Si/SiO_2 interface) [90]. As a consequence, the image force potential emerges, yielding the energy barrier for other charge carriers flowing near the Si/SiO_2 interface. Therefore, the total potential $\Psi(x)$ for the holes near the point of capture is a superposition of two components: the band bending potential, $\psi(x)$ caused by the difference in the work functions of the gate and dielectric materials and AEB induced by the mirror image charges ($\phi(x)$):

$$\Psi(x) = \psi(x) + \phi(x) \tag{4.8}$$

Being independent of the charge capture mechanism, the electrostatic potential (i.e., band bending), $\psi(x)$ can be obtained by solving the Poisson equation [77]:

$$\frac{\partial^2 \psi(x)}{\partial x^2} = -\frac{q}{\epsilon_0 \epsilon_s} \cdot \left(p_{p_0} \cdot e^{-\dfrac{q\psi}{kT}} - N_A - n_{p_0} \cdot e^{\dfrac{q\psi}{kT}} \right) \tag{4.9}$$

where q is the elementary charge, k is the Boltzmann constant, T is the absolute temperature, ϵ_0 is the dielectric constant, ϵ_s is the relative dielectric permittivity of the semiconductor, N_A is the concentration of the ionized acceptor dopants in the semiconductor, p_{p_0} is the equilibrium concentration of free holes, and n_{p_0} is the equilibrium concentration of free electrons. As can be seen in Equation 4.9, the concentration of dopants, N_A is an important parameter governing the potential distribution and thus transport phenomena in FET-based devices. Figure 4.38

shows the distribution of $\psi(x)$ in the p-doped Si structure covered with SiO_2. The negative bias voltage is applied to the gate of the structure, which corresponds to the p-type FET device in accumulation mode. To account for the interaction of a charge carrier with its image charge, we consider the additional potential due to the image force given by [77, 90]:

$$\phi(x) = \frac{1}{16\pi\epsilon_0\epsilon_{Si}} \cdot \left(\frac{\epsilon_{SiO_2} - \epsilon_{Si}}{\epsilon_{SiO_2} + \epsilon_{Si}}\right) \cdot \frac{1}{x} \tag{4.10}$$

where ϵ_{Si} and ϵ_{SiO_2} are the relative permittivities of Si and SiO_2 layers, respectively; q is the elementary charge, and x is the position of the mirror image charge related to the Si/SiO_2 interface. It should be noted that the dielectric permittivity of SiO_2, $\epsilon_{SiO_2} = 3.9$ is smaller than the dielectric permittivity of Si, $\epsilon_{Si} = 11.7$. Therefore, as it follows from Equation 4.10, $\phi(x)$ changes sign at the Si/SiO_2 interface and thus becomes “repelling” for the holes coming to the interface when a negative gate voltage is applied. This leads to AEB for charge carriers being captured by the single trap located at the Si/SiO_2 interface or in the gate oxide layer.

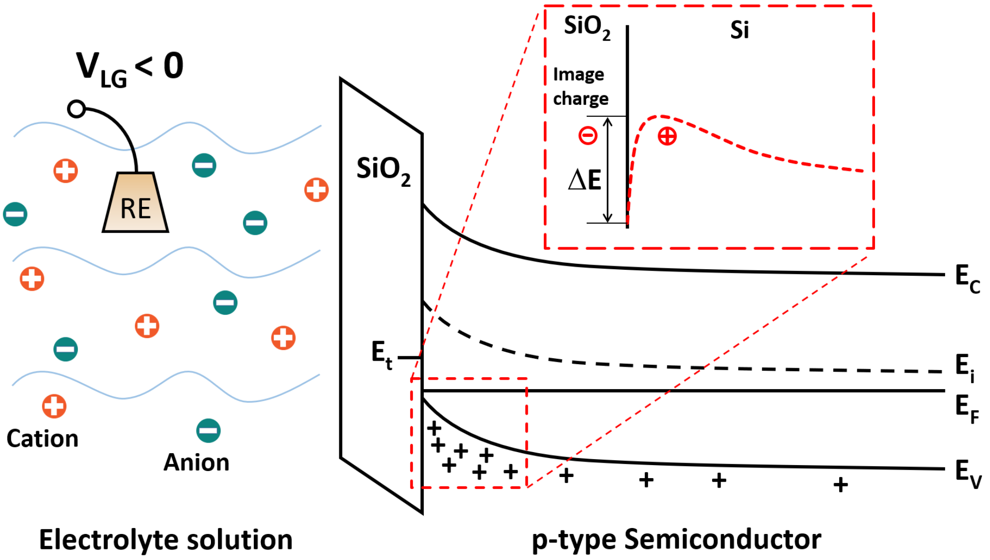


Figure 4.38: Schematic demonstration of the energy profiles in the accumulation-mode p-type Si NW FET with a trap at the Si/SiO_2 interface. The electrolyte solution is used as liquid gate. The biochemical processes occurring on the liquid-solid interface lead to changes in the surface potential influencing the charge exchange processes between the single trap and the conductive channel of the underlying FET. The inset shows an additional barrier for a hole in the p-doped Si before it is captured by the trap. In the figure, E_C is the conductance band, E_V is the valence band, E_t denotes the trap energy level, E_i is the intrinsic Fermi level, and E_F is the Fermi level position in the p-doped Si under a negative gate-voltage bias (i.e., a p-type NW FET in the accumulation mode).

The superposition of $\psi(x)$ and $\phi(x)$ is schematically shown in the inset of Figure 4.38. The image force potential lowers the valence energy band inducing the AEB for the holes. In such a specific case, the height of the barrier can be calculated as the difference between the maximum energy of the lowered valence band and the effective energy which hole attains when approaching a critical distance to the point of capture that is usually less than $1\ nm$ to the trap.

Figure 4.39 displays the dependence of AEB height on the surface potential for NW FET devices with different channel doping concentrations. As can be seen in Figure 4.39, the hight of the barrier decreases with increasing surface potential controlled by a liquid gate. Such behavior can be explained by the increase in the electrostatic screening of the image charge originating from the increased concentration of free holes accumulated at the Si/SiO_2 interface in p-type devices with increasing gate voltage [12]. It is important to note that the height of AEB diminishes faster for NW FETs with a high channel doping concentration as it is evident from Figure 4.39. This fact can be explained by the increase of vertical electric field at the Si/SiO_2 interface with increasing concentration of dopants in NW channel. Therefore, the results shown in Figure 4.39 reveal a significant impact of dopants on the interaction of charge carriers with image charges and thus on the single-trap dynamics in nanoscale devices.

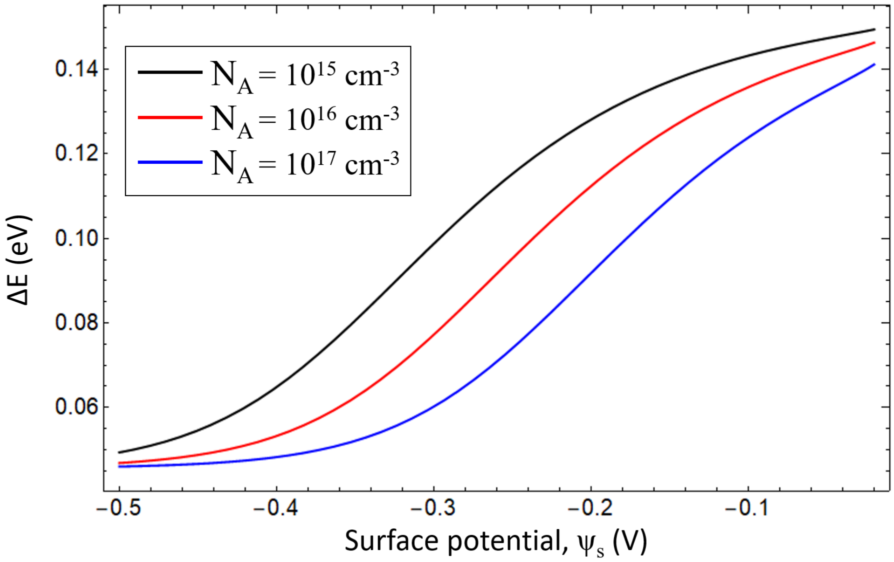


Figure 4.39: (a) AEB height as a function of surface potential. The dependences are calculated for three different channel doping concentrations of LG NW FETs: black curve - $N_A = 10^{15}\ cm^{-3}$, red curve - $N_A = 10^{16}\ cm^{-3}$, and blue curve - $N_A = 10^{17}\ cm^{-3}$.

The dependences of RTS capture rate ($R_c = 1/\tau_c$) on surface potential (ψ_s) calculated for NW FETs with different channel doping concentrations are shown in Figure 4.40(a). As can be seen, R_c demonstrates non-monotonic behavior versus ψ_s controlled by the gate voltage. At least two regimes can be distinguished. In particular, at small values of surface potential that correspond to the subthreshold operation mode of NW FET, R_c behaves as a complex function of ψ_s reflecting enhanced non-SRH single-trap-related dynamic with $\gamma > 1$. In the first approximation, the dependence is superlinear on a semilogarithmic scale and can be fitted with a polynomial-type function $R_c \sim \psi_s^{\gamma}$, where γ is used as a fitting parameter. Simultaneously, at higher values of ψ_s, AEB is reduced due to high electrostatic screening and therefore R_c

starts to behave as a linear function of surface potential as predicted by the conventional SRH model. It should be noted that AEB diminishes faster for devices with a high channel doping concentration. This leads to higher capture rate slopes meaning the increased sensitivity for devices exploiting STP. The normalized values of the slope γ are shown in Figure 4.40(b) as a function of the channel doping concentration. As can be observed, γ increases with the concentration of dopants in the channel, which is consistent with the experimental results presented in Figure 4.40(d). However, as is evident in Figure 4.40(b), the experimental data demonstrate a stronger dependence of γ on the channel doping concentration than the one predicted by the developed model. The difference between the experimental and modelling results can be explained considering that: 1) our calculations have been performed for only over-barrier transport of carriers being captured by a single trap at the Si/SiO_2 interface; 2) for the traps in the gate oxide, the trap depth (i.e., a distance from the trap site in the gate oxide to the Si/SiO_2 interface) impacts the probability of carriers to be captured/emitted to/from the single trap leading to a potential drop at the trap energy level that induces a variation in the height of AEB; and 3) quantum and strain effects [91] additionally influence the interactions of a single trap with charge carriers in the channel of the underlying NW FET and thus have to be taken into account.

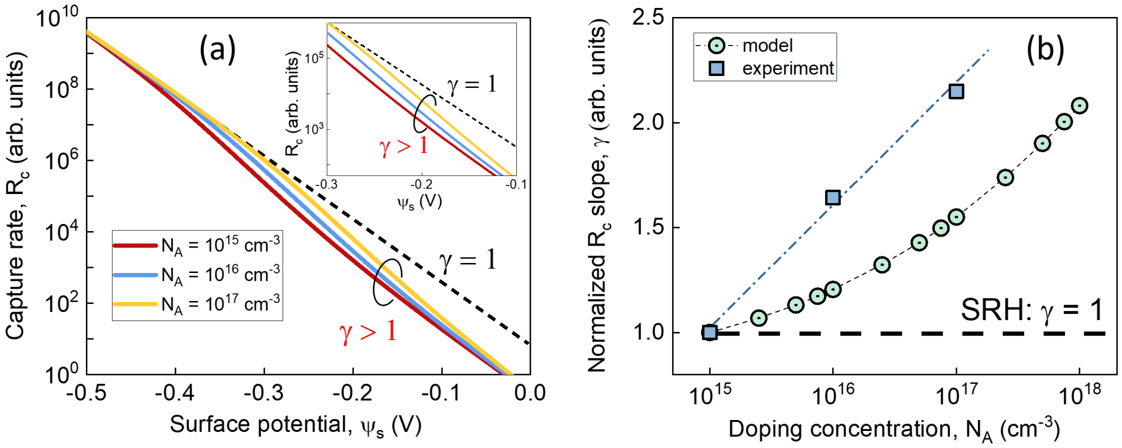


Figure 4.40: (a) Single-trap capture rate calculated for NW FET devices with different concentrations of dopants in the channel and plotted as a function of surface potential. At small values of ψ_s, a non-SRH-behaviour with a strong dependence of R_c on ψ_s (i.e., $\gamma > 1$) is registered as shown in the inset; (b) Normalized capture rate slope versus channel doping concentration to compare calculated and measured results. The black dashed horizontal line with $\gamma = 1$ reflects the behavior predicted by the conventional SRH theory. In contrast, R_c slopes with $\gamma > 1$ reflect the sensitivity enhancement (amplification) for the STP-based biosensing approach.

Steeper capture rate slopes for the traps in the gate oxide were thus revealed experimentally in this thesis for LG NW FET devices with different concentrations of dopants in the channel. Therefore, the effect of doping on single-trap dynamics in LG NW FETs that was demonstrated and discussed in this section has to be taken into account for the development of ultrasensitive FET-based biosensors exploiting STP.

4.4 Revealed Gate-Coupling Effect (GCE) for sensitivity fine-tuning and TCAD modelling of GCE in TL NWs

Si NW FET-based biosensors fabricated on the basis of SOI wafers possess a unique possibility to be operated by applying the electrostatic potential to the liquid surrounding NW (*liquid-gate configuration*), or to the high-doped silicon substrate of SOI wafer acting as a back gate (*back-gate configuration*), or by applying voltages to both gates simultaneously (*dual-gate configuration*) resulting in a **gate-coupling effect** (GCE) [14, 92, 93]. A schematic representation of the Si NW FET biosensor in the dual-gate measurement mode is depicted in Figure 4.41.

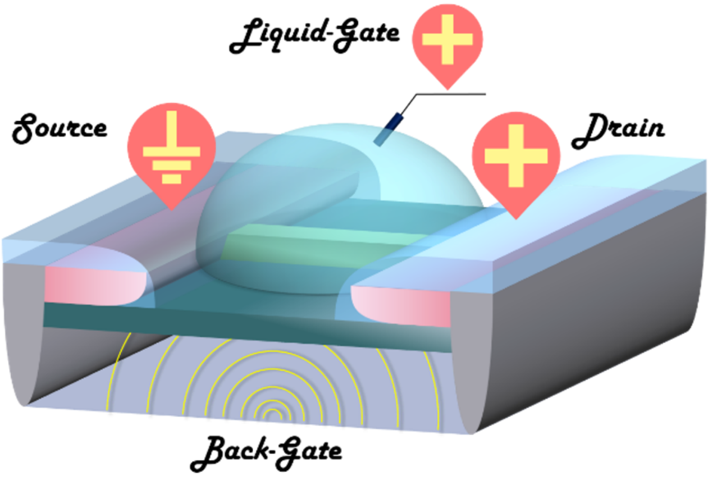


Figure 4.41: Schematic illustration of a liquid-gated Si NW FET biosensor fabricated on the SOI wafer. The liquid-gate voltage is applied using $Ag/AgCl$ reference electrode and a highly doped silicon substrate of the SOI wafer is used as a back-gate electrode.

It has been recently demonstrated that the use of dual-gate configuration allows precise control of a charge carrier density in NW channels and thus can be successfully exploited to establish the optimal regime of operation of underlying NW FETs. This provides the possibility to capacitively amplify the signal and therefore improve the sensing capability of such devices [94]. Moreover, as it was experimentally shown in Ref. [14], the simultaneous utilization of both liquid and back gates allows the switching of the dominant mechanisms responsible for the $1/f$ noise in NW sensors, which leads to the suppression of low-frequency noise and thus improvement of signal-to-noise ratio. In this section, we investigate the impact of GCE on charge exchange processes related to single traps in fabricated TL NW FETs. The obtained results demonstrate that a strong GCE between the liquid gate and back gate in TL NWs allows the parameters of single traps to be adjusted in a controlled way enabling the sensitivity to be fine-tuned for the sensors exploiting STP. To evaluate the full potential of GCE and better understand the mechanism behind the significant GCE revealed in the unique TL NWs, we also performed three-dimensional technology computer-aided design (TCAD) numerical simulations.

GCE features in fabricated Si TL NW FETs: modeling and experiment

Figure 4.42(a) shows typical transfer I-V characteristics of an n-type enhancement-mode Si TL NW FET with the channel doping concentration of 10^{17} cm^{-3}, the NW width of 100 nm, and the NW length of 200 nm measured in either liquid-gate or back-gate configuration at a constant drain-source bias of 100 mV. The measurements were performed at room temperature and the physiological PBS buffer with $pH = 7.4$ and ionic strength of 10 mM was used as a gating solution. Owing to the only 8 nm thin front-gate SiO_2 compared to the 145 nm thick BOX layer, the liquid gate possesses a stronger impact on the charge carrier flow in the TL NW device compared to the back gate as it is evident in Figure 4.42(a). This results in higher drain currents when the device is operated in the liquid-gate configuration. It should be noted that the leakage currents through both front-gate and back-gate oxide layers remained negligibly small (below 10 pA) during I-V characterizations in both measurement configurations, which confirms the high-level performance of fabricated devices.

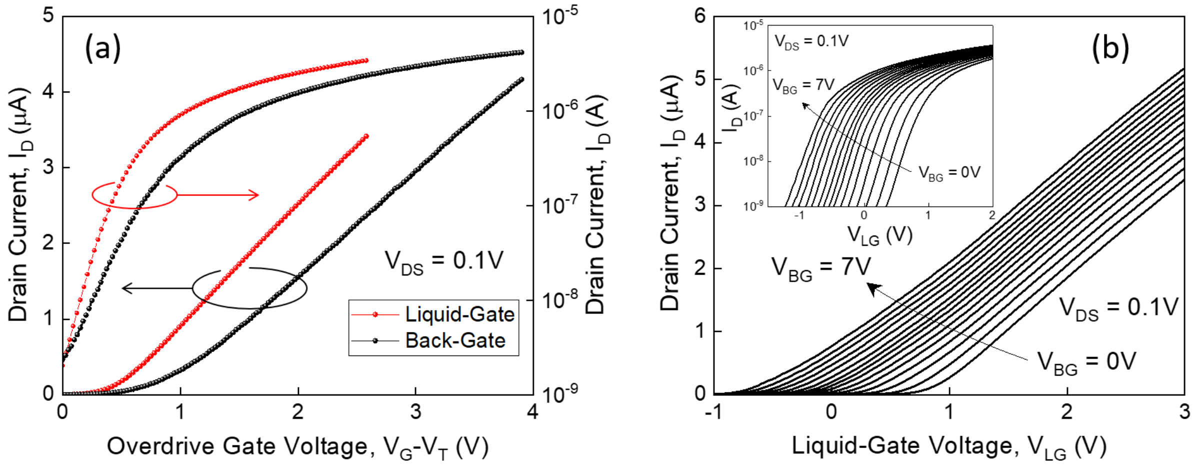


Figure 4.42: (a) Typical I-V transfer characteristics of the n-channel enhancement-mode Si TL NW FET with the channel doping concentration of 10^{17} cm^{-3} measured in liquid-gate (red curve) and back-gate (black curve) configurations at a constant $V_{DS} = 100$ mV (left axis - linear scale, right axis - semilogarithmic scale). The width of NW is 100 nm, while the length is 200 nm; (b) Transfer curves of the same LG TL NW device measured at different back-gate voltages that were varied in the range from 0 V to 7 V with a voltage step size of 0.5 V.

Figure 4.42(b) shows the set of transfer I-V characteristics measured on the same liquid-gated Si TL NW FET biased at $V_{DS} = 100$ mV and different values of back-gate voltages (V_{BG}) applied to the tested sample. The data showed in Figure 4.42(b) demonstrates clear lateral shifts of the I-V curves in the negative voltage direction with applying positive back-gate voltages. Such behavior corresponds to the decrease of threshold voltage and thus increase of conductance in the n-channel inversion-mode transistor due to the capacitive coupling between the liquid gate and the back gate [53]. The observed effect is demonstrated more clearly in the inset of Figure 4.42(b) which presents the dependence of measured drain current on liquid-gate voltage in a semilogarithmic scale for different back-gate bias conditions. The data shows that the experimentally revealed GCE in TL nanostructures can be effectively used to adjust the operating point of the fabricated devices.

To better understand GCE in TL NW FETs, we performed numerical TCAD simulations. The modeled TL NW structure is rectangular in cross-section and consists of two silicon layers with different concentrations of Boron dopants in the NW channel. The first NW layer with a thickness of $50\ nm$ is low-doped Si with $10^{15}\ cm^{-3}$ concentration of Boron dopants, while the second layer with a thickness of $25\ nm$ is highly doped Si with the doping concentration of $10^{17}\ cm^{-3}$ to match the doping profile of the device used in the experiment. Figure 4.43(a) displays the distributions of electron current density in the modeled TL NW structure with the NW width of $100\ nm$, and the NW length of $200\ nm$ that was gated at a constant $V_{FG} = 0.8\ V$ and different applied V_{BG}.

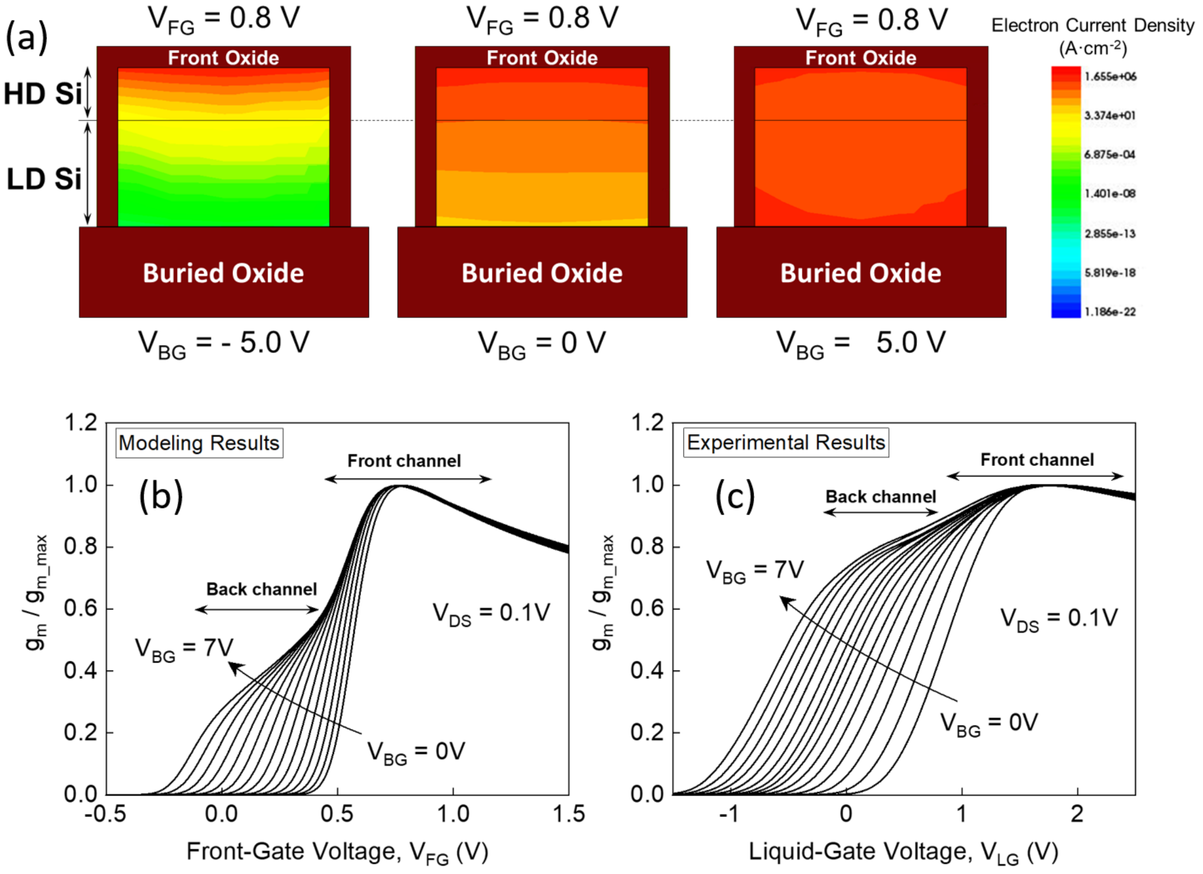


Figure 4.43: (a) Distributions of charge carriers in Si TL NW FET with a rectangular cross-section at a constant front-gate-voltage of $0.8\ V$ and various back-gate voltages applied. The black horizontal line denotes the conditional boundary between the highly doped and low-doped Si layers. The results are obtained using TCAD simulation software and confirm the efficient coupling between the front and back gates in TL nanostructures; (b) and (c): the normalized transconductance characteristics of the $100\ nm$ wide and $200\ nm$ long Si TL NW FET obtained from the simulated and measured I-V curves, respectively. Both experimental and simulated results reveal the appearance of the additional well-pronounced local maximum that corresponds to the back conductive channel as a result of back-gating in unique TL NW FETs.

As can be seen in Figure 4.43(a), the BG biasing has a strong influence on the inversion charge distribution in TL NW FETs. In particular, it is evident that a negative BG bias results in the increased electron charge density in the high-doped region of the p-type NW that corresponds to the front channel of the inversion-mode FET device. In contrast, when positive voltages are applied at both gates, the back inversion channel additionally appears near the BOX layer due to the increased number of accumulated free electrons. The effect results in an increase in the overall conductivity of the device. Moreover, the application of the positive back-gate voltage in fabricated n-channel TL NW FET devices shifts the position of the front channel away from the front interface towards the low-doped part of the nanowire. The effect observed in the novel TL nanostructures plays a dominant role concerning the single-trap phenomena as it will be analyzed below.

The formation of a back inversion channel is can be further confirmed in Figures 4.43(b) and 4.43(c), which present the transconductance of the modeled and measured transistors as a function of the front-gate voltage for different back-gate bias conditions, respectively. The transconductance curves were obtained from the corresponding simulated and measured transfer characteristics. For the comparison purpose, the transconductances in Figure 4.43(b) and 4.43(c) are normalized by their maximum values. It can be seen that at $V_{BG} = 0\ V$, the transconductance dependence displays a single peak that corresponds to the front channel of the nanotransistor. However, as the positive back-gate bias is applied ($V_{BG} > 0\ V$), the additional peak in the transconductance appears revealing the formation of the back conductive channel. It should be noted that similar transconductance behavior was observed for both simulated and tested devices. The obtained data, therefore, clearly demonstrate that the back-gate biasing in fabricated TL NW devices enables the inversion-charge carrier concentration distribution to be effectively changed and thus reveal that the double-gate measurement configuration can be effectively used for the precise tuning of the transport properties of fabricated Si TL NW FETs. Under these conditions, the single-electron fine-tuning effect was revealed as we demonstrate and discuss below.

Impact of GCE on the single-carrier dynamics in LG Si TL NW FETs

The ability to change the charge distribution in the LG TL NW devices in a well-controlled manner by applying the back-gate potential opens up a unique possibility to intentionally modify the dynamics of charge exchange processes related to single traps in fabricated TL NW FETs. To prove this feature, we investigated the impact of back-gate biasing on the capture process of charge carriers by a single trap in the fabricated LG TL NW FETs.

Figure 4.44(a) shows typical PSD curves measured for the n-channel enhancement-mode Si TL NW FET (NW width, $100\ nm$; NW length, $200\ nm$) with the channel doping concentration of $10^{17}\ cm^{-3}$ biased at a constant $V_{DS} = 100\ mV$ and liquid-gated at different V_{LG}. A physiological PBS buffer with $pH = 7.4$ and ionic strength of $10\ mM$ was used as a liquid-gate solution and the back gate was grounded during all noise measurements in this case. As can be seen, the measured noise spectra demonstrate a Lorentzian-type shape with a characteristic frequency that shifts to higher frequencies with increasing V_{LG}. The observed behavior reveals the RTS process as a result of STP in the tested device.

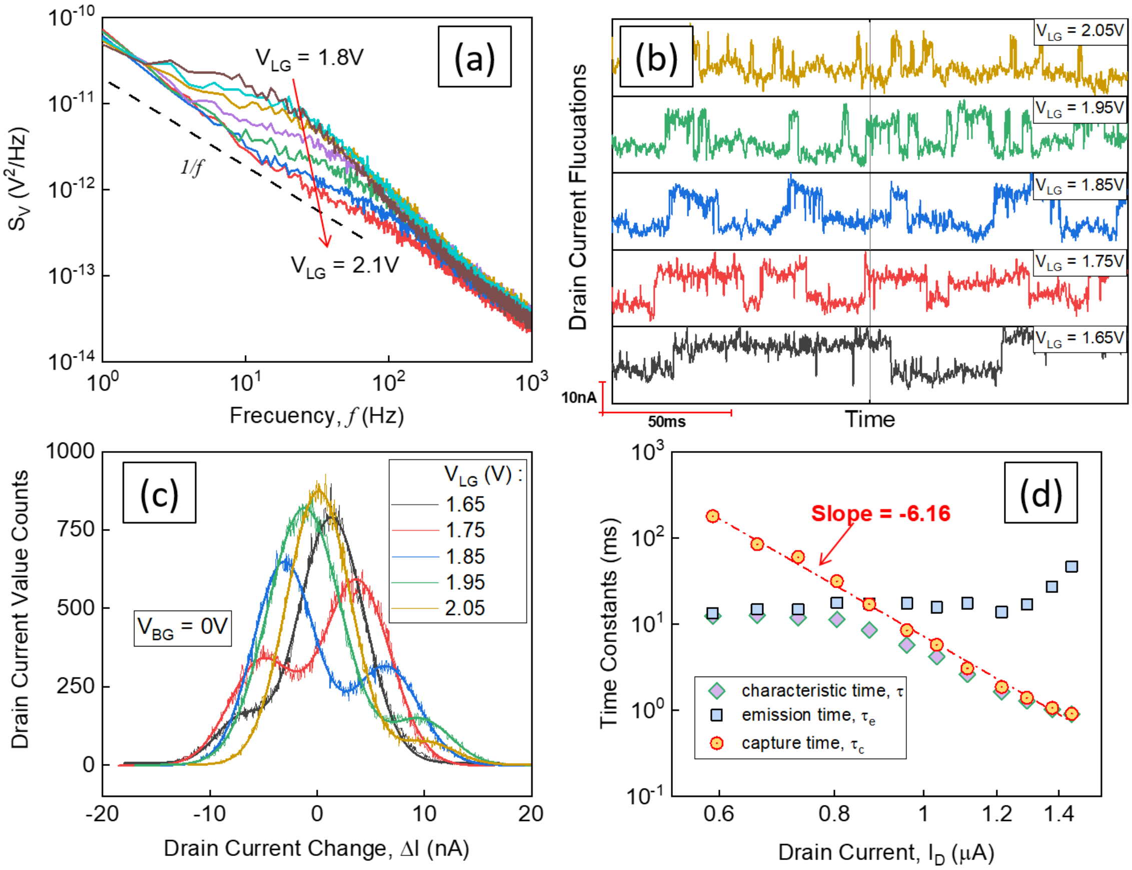


Figure 4.44: (a) Voltage noise PSD curves measured on the 100 nm wide and 200 nm long Si TL NW FET at $V_{DS} = 0.1\ V$ and different liquid-gate voltages, while the back-gate was grounded; (b) Typical RTS fluctuations in drain current registered in the same device; (c) Histograms of the two-level RTS noise calculated from the data in (b). The solid curves show the fitting of the data with two-Gaussian distributions; (d) Characteristic time constants of the registered STP plotted versus drain current. The dot-dashed red line with a slope of (-6.16) reflects the behavior of the capture characteristic time in the semilogarithmic scale which is a considerably stronger dependence in comparison to the one predicted by the SRH model with the slope $\gamma = -1$.

The recorded time traces of registered RTS noise are shown in Figure 4.44(b), while the corresponding amplitude histograms are presented in Figure 4.44(c). The data clearly demonstrate that STP is well-pronounced in the tested device and dominates over all the other noise sources in the measured V_{LG} range. After the detailed data analysis using the amplitude histogram method [53], the effective characteristic time (τ) as well as average capture (τ_c) and emission (τ_e) time constants are calculated and plotted as functions of drain current (I_D) in Figure 4.44(d). As can be seen in Figure 4.44(d), τ_e shows only a weak dependence on I_D, while τ_c strongly depends on the drain current controlled by the liquid gate. The dependence of characteristic capture time can be approximated as a power function with an exponent of (-6.16). It should be noted that this result suggests a very strong relationship between the STP-related capture process and the concentration of charge carriers tuned by the liquid-gate voltage in this case. However, as demonstrated above, the latter can also be successfully modulated by applying a voltage to the substrate, which acts as the back-gate electrode. Therefore, below we investigate and analyze the impact of back-gate biasing on the single-trap parameters controlled by the liquid gate potential.

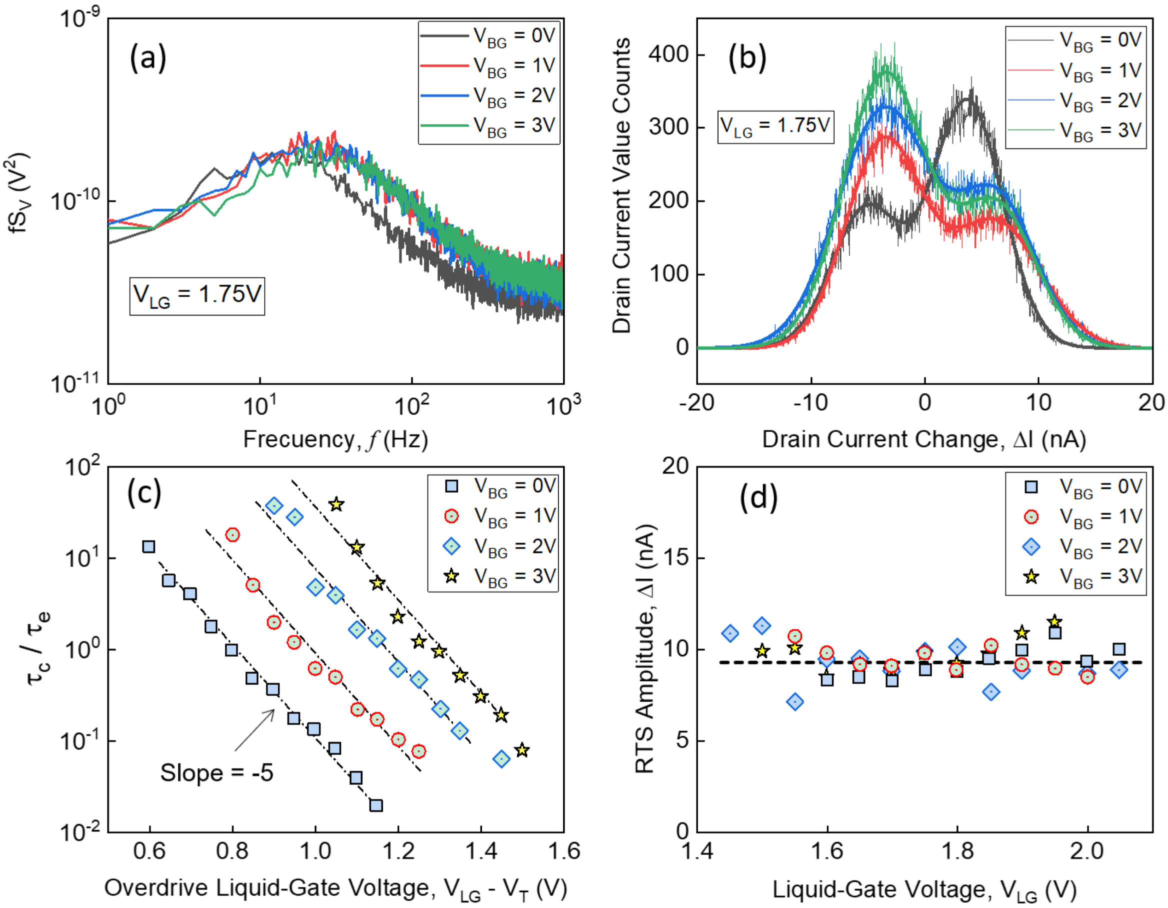


Figure 4.45: (a) Voltage noise PSD spectra measured on the $100\ nm$ wide and $200\ nm$ long Si TL NW FET at $V_{DS} = 0.1\ V$ and different back-gate voltages, while the liquid-gate potential was set to a constant value, $V_{LG} = 1.75\ V$; (b) Amplitude histograms of the corresponding RTS drain current fluctuations; (c) Experimental τ_c/τ_e ratio plotted as a function of overdrive liquid-gate voltage. The dashed lines with a slope of (-5) stand for visual aid; (d) The dependence of the RTS amplitude on the liquid-gate voltage at the different back-gating conditions. The amplitude remains about constant confirming that the RTS noise measured at the different back-gate voltages is caused by the same single trap located in the top $8\ nm$ thin SiO_2 layer.

Noise PSD spectra measured for the same Si TL NW FET at a constant V_{LG} of $1.75\ V$ and different V_{BG} are shown in Figure 4.45(a). To compensate for the background $1/f$ flicker noise and provide better resolution of the RTS noise component, the measured PSD spectra are multiplied by the frequency f. On such a coordinate scale, the RTS noise PSD is maximized at the corner frequency f_0. As can be seen, f_0 remains about constant for different back-gate voltages applied to the LG device. In contrast, significant changes in the τ_c/τ_e ratio that was calculated from the corresponding histograms shown in Figure 4.45(b) were registered with applying the back-gate potential. It should be noted that such behavior reflects a considering impact of back-gating on the RTS capture dynamics in the TL NW FETs compared to the conventional NW FETs exhibiting only negligible dependence of RTS parameters on the back gate voltage [87]. The calculated τ_c/τ_e ratio is shown in Figure 4.45(c) as a function of overdrive liquid-gate voltage at different back-gate voltages applied to the device. It is seen that the ratio of time constants decreases with increasing V_{LG}. The behavior is typical for the acceptor-type traps [52, 55] responsible for RTS in the inversion-mode FETs. As can be also evident from Figure 4.45(c), the characteristic slope of τ_c/τ_e ratio does not change with the applying back-gate potential suggesting that the RTS noise, measured at different back-gate voltages, is caused by the same single trap located in the front-gate SiO_2 layer. The statement is also confirmed in Figure 4.45(d) showing that the RTS amplitude remains almost unchanged when applying the back-gate potential.

Figure 4.46(a) shows the experimental dependences of the extracted RTS characteristic capture times on the drain current at different back-gate voltages applied to LG Si TL NW FET. It should be emphasized that the RTS capture time constant strongly depends on the carrier concentration in fabricated Si TL NW FETs controlled by the liquid-gate. At the same time, as can be seen from Figure 4.46(a), the characteristic capture time slope increases with increasing back-gate potential, which effectively modulates the distribution of charge carriers in the TL NW structures and therefore enhances the single-trap kinetic. This result indicates the significant effect of back-gate biasing on RTS trapping/detrapping processes in such LG TL NW devices. As demonstrated in the inset of Figure 4.46(a), an approximately linear dependence of the capture characteristic slope on the back-gate potential was registered for the range of the back-gate voltages applied. Below, we demonstrate that the revealed effect is highly important for the new type of sensors exploiting STP characteristic parameters such as RTS capture time as a signal. The key aspect is that we can tune the sensitivity of such sensors by changing the STP characteristics (e.g., slope of the capture rate) in a controlled way.

As proof of concept, we performed the experiment in which we measured and analyzed the response of the same TL NW sensor to the change of ionic strength in the sodium-based solutions. The tested liquids with different ionic strengths were prepared by diluting a stock sodium-based buffer solution containing $0.14\ M\ NaCl$, $0.0027\ M\ KCl$, and $0.01\ M\ PO_4^{3-}$ with deionized water to keep the pH value of the new solutions about constant. The ionic

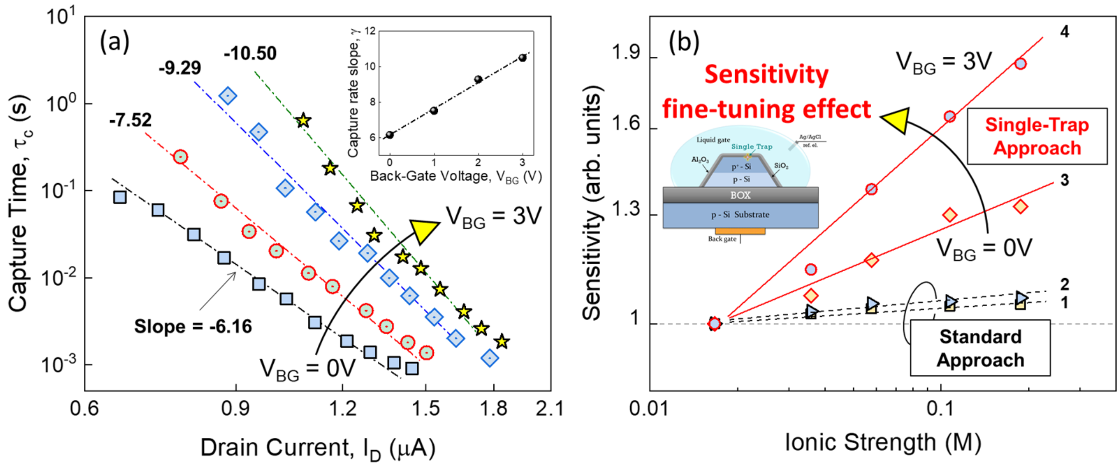


Figure 4.46: (a) RTS characteristic capture time plotted as a function of drain current measured at different back-gate voltages, V_{BG}: $0\ V$; $1\ V$; $2\ V$, $3\ V$. The colored dash-dotted lines with indicated slopes represent the characteristic behavior of the measured RTS capture time. The increase of characteristic capture time slope with increasing back-gate potential is observed as demonstrated in the inset; (b) The response of the TL NW sensor to the change of ionic strength of the gating solution in terms of sensitivity calculated for the standard approach: I_D/I_D^{min} (black dashed line 1 - $V_{BG} = 0V$; black dashed line 2 - $V_{BG} = 3\ V$) and for the STP-based approach: τ_c^{max}/τ_c (red solid line 3 - $V_{BG} = 0\ V$; red solid line 4 - $V_{BG} = 3\ V$). Only a slight increase of the sensitivity slope on the applied back-gate voltage was observed for the standard approach, while the STP-based approach demonstrated a pronounced sensitivity fine-tuning effect in developed TL NW FET sensors.

strength of the stock buffer with $pH = 7.4$ was $0.18\ M$. The sensing experiment was performed using both: the *standard approach* by monitoring changes in the drain current and the *STP-based approach* by monitoring changes in the RTS capture time as the characteristic parameter of the single trap. The results of the experiment are presented in Figure 4.46(b). The increase of the drain current at a constant $V_{LG} = 2\ V$ and $V_{BG} = 0\ V$ with increasing of ionic strength of the gating solution (see black dashed $line\ 1$ in Figure 4.46(b)) was measured. Such behavior is due to the change in the electrochemical potential caused by the adsorption of negative ions (Cl^- and phosphate PO_4^{3-}) on the Al_2O_3-covered NW surface [17]. By applying a positive back-gate voltage ($V_{BG} = 3\ V$) to the substrate of the device, a slight increase in sensor sensitivity was observed as denoted by a black dashed $line\ 2$ in Figure 4.46(b). Note, this also demonstrates the positive role of dual-gate configuration for FET-based sensing. At the same time, changes in the surface potential caused by variations of the solution ionic strength were registered with enhanced sensitivity by monitoring changes in the RTS capture time (see red solid $line\ 3$ in Figure 4.46(b)). It should be emphasized that the slope of $line\ 3$ that corresponds to the STP-based approach is considerably larger (approximately $5\ times$) than the slope of $line\ 1$ that corresponds to the standard I_D-approach. Moreover, what is more important, as the positive back-gate potential was applied ($V_{BG} = 3\ V$, the sensitivity of the sensor exploiting STP has been significantly increased (see red solid $line\ 4$ in Figure 4.46(b)) due to the enhancement of single-trap dynamic by the back biasing in TL NW FETs. This reveals a novel effect that allows for the fine-tuning of sensitivity in fabricated Si TL NW FET sensors whose sensing principle is based on the STP-approach.

4.5 Summary

Nanowire FET-based biosensors have recently emerged as a promising class of electronic sensors for chemical and biomolecular detection. In this chapter, we presented a detailed fabrication process flow that we developed and optimized to fabricate the **unique two-layer NW FET** structures which consist of two silicon layers with different doping concentrations. The devices were specially designed and fabricated **to investigate single-trap phenomena** for the ultimate biosensors' scaling and sensitivity enhancement. The detailed characterization of transport and noise properties of fabricated devices configured as liquid-gated FETs has been performed. The TL NW FETs with different concentrations of dopants in the channel demonstrated leakage-free and low-noise performance as well as good working stability while operating in a liquid. Mobility fluctuations were confirmed as the main low-frequency noise source in the accumulation-mode p-type TL nanostructures, while the number fluctuation model well explains the noise behavior in the n-type devices.

Furthermore, the electrical and noise characteristics of fabricated FETs were studied at low temperatures. The back-gated TL nanostructures demonstrated clear generation-recombination noise with PSD proportional to $1/f^{3/2}$ at temperatures below $200\ K$. The observed behavior reflects the diffusion-assisted transport processes in TL NW FETs confirming the contribution of the high-doped top silicon layer to the transport properties of TL NW devices. The detailed analysis of the RTS noise measured at different low temperatures allowed us to identify the **origin** of the single traps as **boron-vacancy-complex** responsible for the RTS processes in TL nanostructures.

The fabricated sensors were applied for the biosensing applications using the standard biosensing approach when a drain current or threshold voltage was used as a signal. The developed biosensors demonstrated good pH and ion sensitivity and showed excellent capability for high-speed, high-sensitive, and label-free biosensing of **various targets** such as cTnI and CRP biomarkers. Therefore, the obtained experimental results confirmed the high sensing capabilities of fabricated devices. However, as will be demonstrated in Chapter 6, the sensitivity and limit of detection can be even further enhanced using a novel STP-based biosensing approach.

The liquid-gated TL NW FETs demonstrate pronounced RTS noise as the result of STP with advanced characteristics. In this chapter, we evaluated and demonstrated how doping in NW FETs modifies the RTS dynamic. In particular, the considerably enhanced RTS capture dynamic with increasing channel doping concentration compared to the SRH theory has been revealed. **The analytical model** was derived to explain the doping effect on STP behavior in the nanoscale LG transistors. The calculations were performed while considering the additional energy barrier that a charge carrier has to overcome to be captured by a single trap. The accurate model gives a clear description of the mechanisms behind the enhanced RTS processes in fabricated TL NW FETs. Moreover, in this chapter, we investigated the impact of back-gate bias on the transport and noise properties of the Si TL NW FETs operated in the liquid-gate configuration. We demonstrated that the utilization of the **gate-coupling effect** in fabricated devices enables us to precisely modify the single-trap kinetic and therefore, to fine-tune the sensitivity of the sensors exploiting STP. The strong impact of the back-gate bias on the charge distribution in the Si TL NW FETs, which leads to the experimentally revealed single-carrier fine-tuning effect, has been also confirmed by the performed **TCAD simulations**. Thus, the results presented and discussed in this chapter provide clear directions and guidelines for the future STP-based biosensors promising to push further the limits of label-free biosensing towards high-performance and ultrahigh-sensitivity.

STP MODELING AND NOISE SUPPRESSION IN NW FET BIOSENSORS

The understanding of noise mechanisms in any electrical system is an important task. It becomes especially essential and useful at the nanoscale ($A < 1\ \mu m^2$), where the relative noise level increases with shrinking down the device area (see Equation 2.20) resulting in fewer charge carriers. Despite this fact, nanoscale devices offer unique opportunities for noise suppression and therefore for enhancement of the signal-to-noise ratio. In this chapter, we **introduce a novel principle for the low-frequency (LF) noise suppression technique** in nanobiosensors exploiting single-trap phenomena (STP). Similarly to the stochastic resonance (SR) noise suppression approach found in biological systems, we theoretically and numerically demonstrate as well as experimentally prove that the exploitation of the trapping/detrapping of a single charge carrier in a single defect allows suppression of the intrinsic transistor noise by orders of magnitude, even below the thermal limit of the state-of-the-art FET based biosensors.

5.1 Single-trap phenomena as a stochastic resonance effect

Signals coming from the target bio-objects are usually extremely small to be detected, therefore the physical mechanisms and effects leading to noise reduction as well as signal amplification have to be thoroughly investigated. The effect of stochastic resonance (SR) is one of the useful phenomena in this regard as it allows to amplify the weak input signals with the help of noise [95–98].

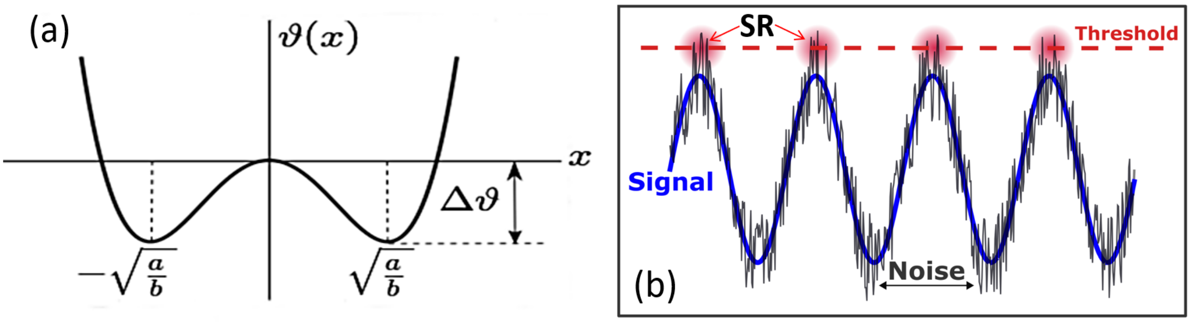


Figure 5.1: (a) Symmetric double-well potential function. The figure is adopted from Ref. [96]. A synchronized hopping between the two minima occurs due to SR effect when an optimal value of a Gaussian noise is added to the system; (b) Schematic interpretation of the threshold SR: an optimal amount of white noise is added to a system to detect weak periodical signals under the system threshold.

The SR phenomenon has been observed in a variety of systems and effectively used in many different applications including signal processing, control systems, and network design [96]. Usually, to explain the physical mechanism of the SR effect, one can simply consider the motion of a particle in a double-well potential in the presence of a weak periodic forcing signal and a Gaussian noise [96]. In the absence of the noise, the system is confined to its initial state and transition events between the states (wells) don't occur until the white noise is added to the system (see Figure 5.1(a)). In such a case, the presence of the noise causes an effective lowering of the barrier which provides a possibility to change the state. The most important thing is that the noise-induced transitions between the states does not depend on the periodic input and result in two-state random telegraph signal output with distributions of time intervals between these transitions that follow exponentially decreasing function [96]. It should be noted that such random physical processes are very similar to STP in nanoscale FET when a single trap is active near the conductive channel of a nanotransistor and therefore, randomly capture/emit the carrier from/to the channel resulting in RTS noise.

Another example of a system in the regime of SR is schematically shown in Figure 5.1(b). In this case, the SR phenomenon is considered as a threshold effect [97, 99] when the amplitude of the initial input signal is not sufficient to cross the threshold level meaning that the signal can not be detected at given conditions. However, when an optimal level of noise is added to the signal, the SR effect appears enabling the signal to pass the threshold and therefore enhances the detection performance. Importantly, by varying the noise amplitude, one can change the modulation intensity and therefore tune the response of the system. Thus, adding an optimal amount of noise to the input signal under appropriate conditions improves the information transmission process giving rise to the performance of the system.

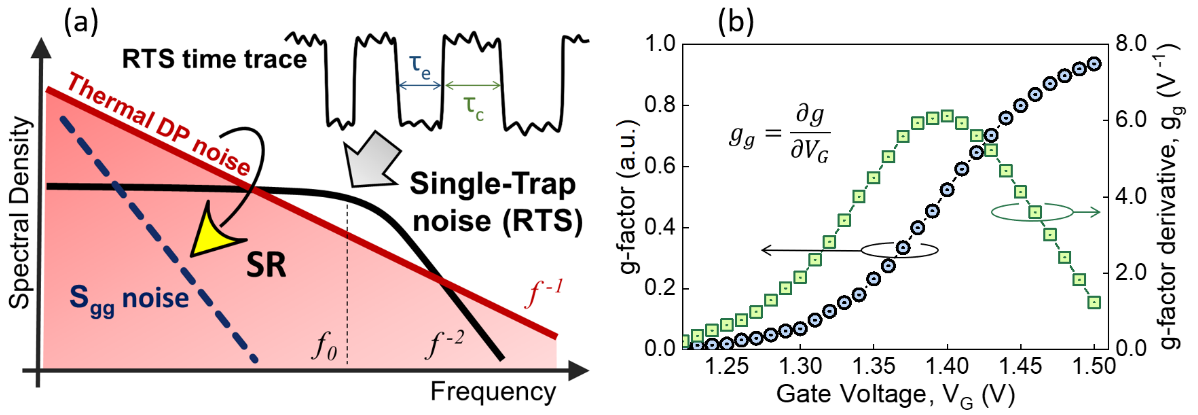


Figure 5.2: (a) DP noise suppression due to STP considering a single trap as a nonlinear bistable system that can amplify the signal in the regime of SR; (b) Typical dependencies of g-factor (left axis) and its derivative (right axis) on gate voltage.

In general, noise is an intrinsic property of any electronic system. In nanobiosensors exploiting STP, the RTS noise is used as a signal of interest carrying the information about the analyte. Below a cut-off frequency, the RTS process as a result of STP in the nanoscale transistor can be considered as a white noise. Therefore, the idea of using RTS as a signal implies the noise reduction principle similar to that of the SR effect (see Figure 5.2(a)). In other words, a single trap in a nanoscale device can be considered as a bistable stochastically driven nonlinear system which can transmit and amplify the weak signals coming from the target bio-objects. The noise reduction mechanism is schematically demonstrated in Figure 5.2(a). Below, we combine simulation and experiments to push the limits of noise suppression offered by STP in nanoscale devices. Moreover, we propose an analytical model to reveal the noise reduction mechanism in single-trap-based nanosensors making the analogy with the SR phenomenon.

5.2 Analysis of the novel type of noise: fluctuations of trap occupancy factor

Unlike usual transistor-based biosensors where the shift of threshold voltage or drain current is considered as the signal and voltage fluctuations are the noise, the signal in STP-based biosensors is an STP-characteristic parameter such as a trap occupancy probability (g-factor) that can be calculated using Equation 2.24. Therefore, the fluctuations of g-factor become the noise in devices exploiting STP. Typical gate-voltage dependencies of trap occupancy probability and its derivative are shown in Figure 5.2(b). To evaluate the g-factor noise considering a two-level RTS time trace, we convert RTS voltage fluctuations in time into fluctuations of the trap occupancy factor using a so-called sliding window algorithm schematically shown in Figure 5.3.

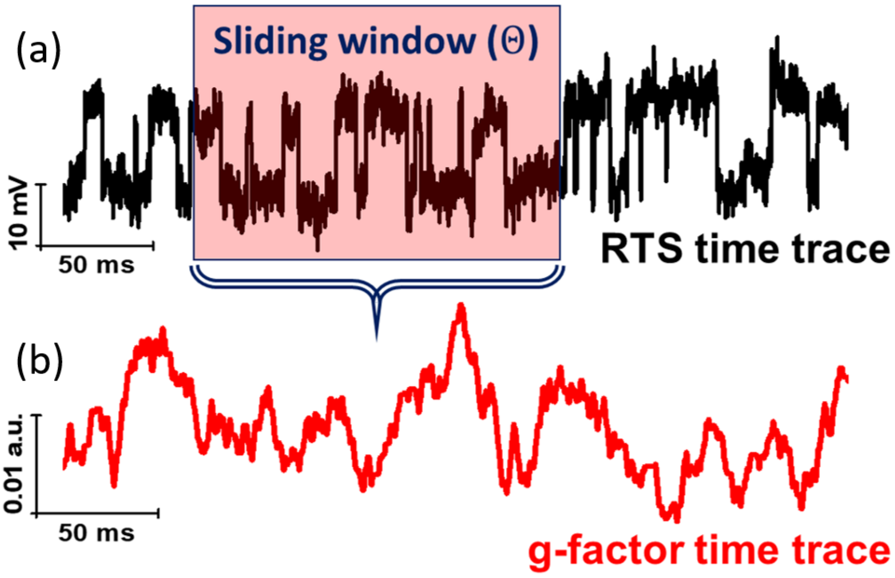


Figure 5.3: Schematic illustration of the conversion of (a) RTS voltage fluctuations into (b) the fluctuations of trap occupancy probability (g-factor noise).

More precisely, we extract g-factor, $g(t)$ over a given time window (Θ) directly from the time distribution of RTS voltage fluctuations. Then, by sliding the window along with the RTS time trace, a new time trace with the trap occupancy factor fluctuations in time is constructed. Finally, the time-domain data of g-factor noise can be then translated into a frequency spectrum resulting in the g-factor noise power spectral density (S_g).

g-factor noise: experiment and numerical simulations

Figure 5.4(a) displays typical two-level drain current RTS fluctuations measured at room temperature on a liquid-gated Si TL NW FET with NW width and length of $100\ nm$. The device was biased at a constant $V_{DS} = 20\ mV$ that corresponds to the linear FET-operation regime. An analysis method based on a hidden Markov model was applied to extract drain current states for measured RTS time trace. The calculated capture and emission time constants characterizing measured RTS as a result of STP are plotted in Figure 5.4(b) as a function of the liquid-gate voltage applied. As can be seen, both RTS characteristic time constants demonstrate a behavior typical for liquid-gated NW FETs when average emission time remains about constant, while capture characteristic time sharply decreases with increasing liquid-gate potential.

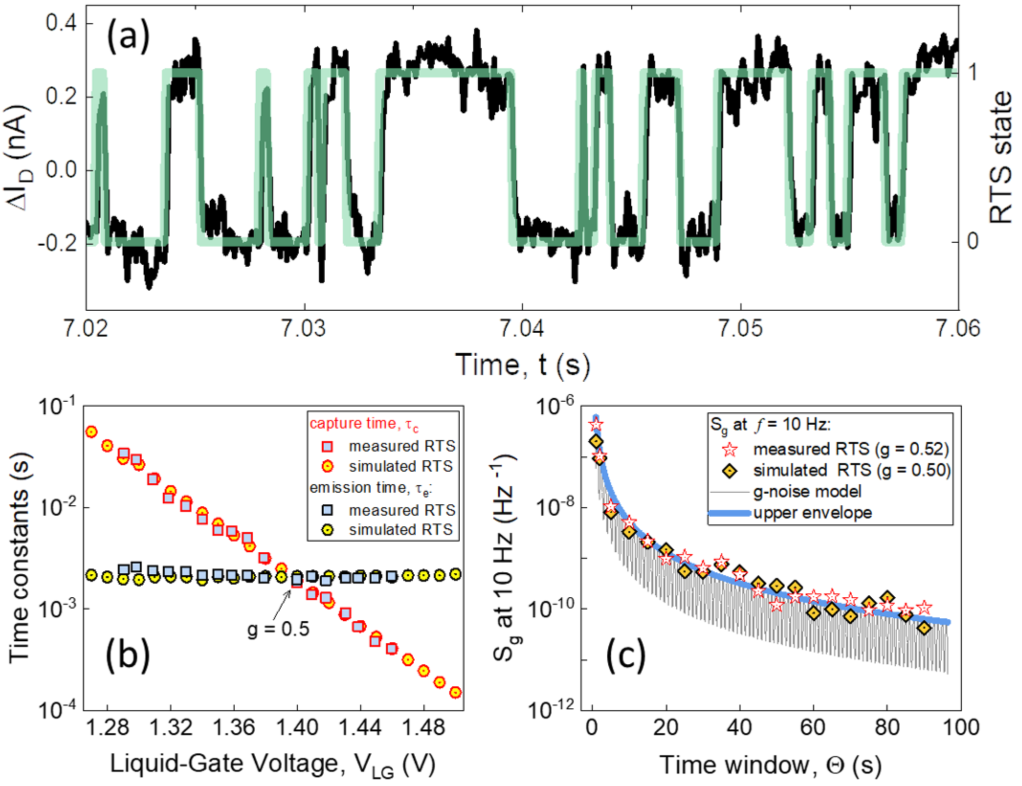


Figure 5.4: RTS noise characteristics. (a) Typical two-level drain current RTS fluctuations and the corresponding extracted RTS states measured in a liquid-gated Si NW FET with NW width of $100\ nm$ and length of $100\ nm$; (b) RTS characteristic capture and emission times plotted as a function of liquid-gate voltage for both simulated and measured RTS time traces; (c) The g-factor noise (S_g) at $10\ Hz$ as a function of time window Θ calculated for the measured and generated RTS. The upper envelop of the derived analytical Equation 5.5 perfectly represents S_g noise behaviour obtained for both experimental and simulation results at $g = 0.5$.

For obtaining long enough RTS time traces for the meaningful evaluation of g-factor noise, we also generated RTS noise numerically using master Equations [100] with the additional consideration of DP noise defining thermal limit in the nanoscale FET-based biosensors [18, 101, 102]. The RTS simulation procedure is described in *Appendix B*. Average capture and emission time constants characterizing simulated RTS noise are also shown in Figure 5.4(b). It should be noted that simulated RTS noise has time characteristics similar to that extracted for experimentally measured RTS process. Figure 5.4(c) presents the trap occupancy factor noise (S_g) taken at $10\ Hz$ for both measured and simulated RTS time traces. Note, the data in Figure 5.4(c) is calculated for the case when $g = 0.5$ obtained at $V_{LG} = 1.4\ V$. At this condition, the trap energy level coincides with the Fermi level of the system and therefore the number of trapping/detrapping events is maximized, so the g-factor noise is also maximized. As is evident in Figure 5.4(c), S_g decreases with increasing the time window Θ. Such behavior of S_g with increasing Θ can be explained considering that the larger time window yields more transitions between the trap states (see Figure 5.3). This allows the g-factor to be estimated with higher accuracy resulting in smaller S_g noise as demonstrated in Figure 5.4(c).

g-factor noise analytical model

To thoroughly investigate the newly introduced g-factor noise in nanotransistor sensors exploiting STP and thus estimate the full potential of STP for noise suppression, we developed an analytic model. For this purpose, we considered a two-level RTS signal (X_t) that jumps between states 0 and 1 as a continuous-time and discrete-state random process. In this case, the transition probabilities (P) for RTS process with states $(0, 1)$ and rates (λ, μ) to jump from the states 0 to 1, and 1 to 0, respectively, are given by Kolmogorov's forward equation:

$$P(t) = [\mathcal{P}(X_t = j|X_0 = i)]_{i,j} = \frac{1}{\lambda+\mu}\begin{pmatrix}\mu & \lambda\\ \mu & \lambda\end{pmatrix} - \frac{1}{\lambda+\mu}e^{-(\lambda+\mu)t}\begin{pmatrix}-\lambda & \lambda\\ \mu & -\mu\end{pmatrix} \tag{5.1}$$

Then, we consider our signal as a trap occupancy probability (g) that is averaged over a time window (Θ) and therefore defined as:

$$g^{\Theta}(t) := \frac{1}{\Theta}\int_t^{t+\Theta} 1_{\{X_s=1\}}ds \tag{5.2}$$

where $1_{\{X_S=1\}}$ is the indicator function that is equal to 1 if $X_S = 1$, and 0 for all other cases. To obtain the autocorrelation function $C(s)$ of g, we consider the expected value E and obtain:

$$C(s) = E[g(t)g(t+s)] = E\left[\left(\frac{1}{\Theta}\int_t^{t+\Theta} 1_{\{X_s=1\}}ds\right) \times \left(\frac{1}{\Theta}\int_{t+s}^{t+s+\Theta} 1_{\{X_s=1\}}ds\right)\right] \tag{5.3}$$

where s denotes the time lag.

Then, autocorrelation function $C(s)$ can be written as:

$$C(s) = \frac{1}{\Theta^2}\left[\int_0^{\Theta}\int_s^{s+\Theta} \mathcal{P}(X_{max(u,v)} = 1|X_{min(u,v)} = 1) \times \mathcal{P}(X_{min(u,v)} = 1)dudv\right] \tag{5.4}$$

As it follows from Equation 5.4, $C(s)$ evolves two regimes that are related to the averaging filter and the stochastic charge transfer. Finally, after some mathematical simplifications and following a statistical analysis formalism, an analytical model can be obtained for the PSD of the g-factor noise in the case when $g = 0.5$ (i.e., $\lambda = \mu = \gamma$) as:

$$S_g^{(\Theta)}(\omega) = \frac{2\gamma\big(1 - \cos(\Theta\omega)\big)}{\Theta^2\omega^2(4\gamma^2 + \omega^2)} \tag{5.5}$$

where $\omega = 2\pi f$ and Θ is a duration of a sliding time window (see Figure 5.3). As can be seen in Figure 5.4(c), Equation 5.5 perfectly describes the behavior of S_g noise calculated for both experimental and simulation results.

5.3 Estimation of signal-to-noise ratio for STP-based NW FET biosensors

The signal-to-noise (SNR) ratio is an important parameter for any type of sensors aiming to detect the target analyte with high sensitivity and accuracy. To estimate SNR for such STP-based nanosensors and thus to compare their performance and efficiency with classical FET-based devices, one should first introduce and calculate an equivalent input-referred noise caused by the variation of the g-factor used as a signal. This can be done similarly as for the input-referred voltage noise (see Equation 2.18) defining the input-referred trap occupancy factor noise as:

$$S_{gg} = \frac{S_g}{g_g^2} \tag{5.6}$$

where S_g is the g-factor PSD and g_g is the g-factor derivative calculated as $\dfrac{\partial g}{\partial V_G}$.

The input-referred voltage noise PSD curves measured for the same 100 nm wide and 100 nm long liquid-gated Si NW FET demonstrating pronounced two-level RTS noise are shown in Figure 5.5(a). Lorentzian fittings display the dominant contributions of the RTS noise to the overall spectra. A red dashed line represents the $1/f$ DP noise dependence as a thermal limit for the tested device calculated using Equation 2.15 with $tg\ \delta = 3.8 \times 10^{-3}$. A typical spectrum of the input-referred g-factor noise, S_{gg} calculated using Equation 5.6 with $g = 0.5$, $\gamma = 488\ s^{-1}$ (as for the experimental data), and $\Theta = 20\ s$ is plotted in Figure 5.5(a) as a grey solid line. A green line denotes the upper envelope of S_{gg} spectrum. As can be seen in Figure 5.5(a), the calculated S_{gg} noise is considerably lower than the measured voltage noise.

This result demonstrates that the LF noise in the nanosensors exploiting STP, in fact, can be suppressed under optimized conditions for calculation of g-factor as the signal. In this regard, mainly three parameters have to be carefully considered and investigated: time window Θ, RTS corner frequency f_0 (i.e., trap operation frequency), and a slope of the g-factor dependence on the gate voltage applied (g_g).

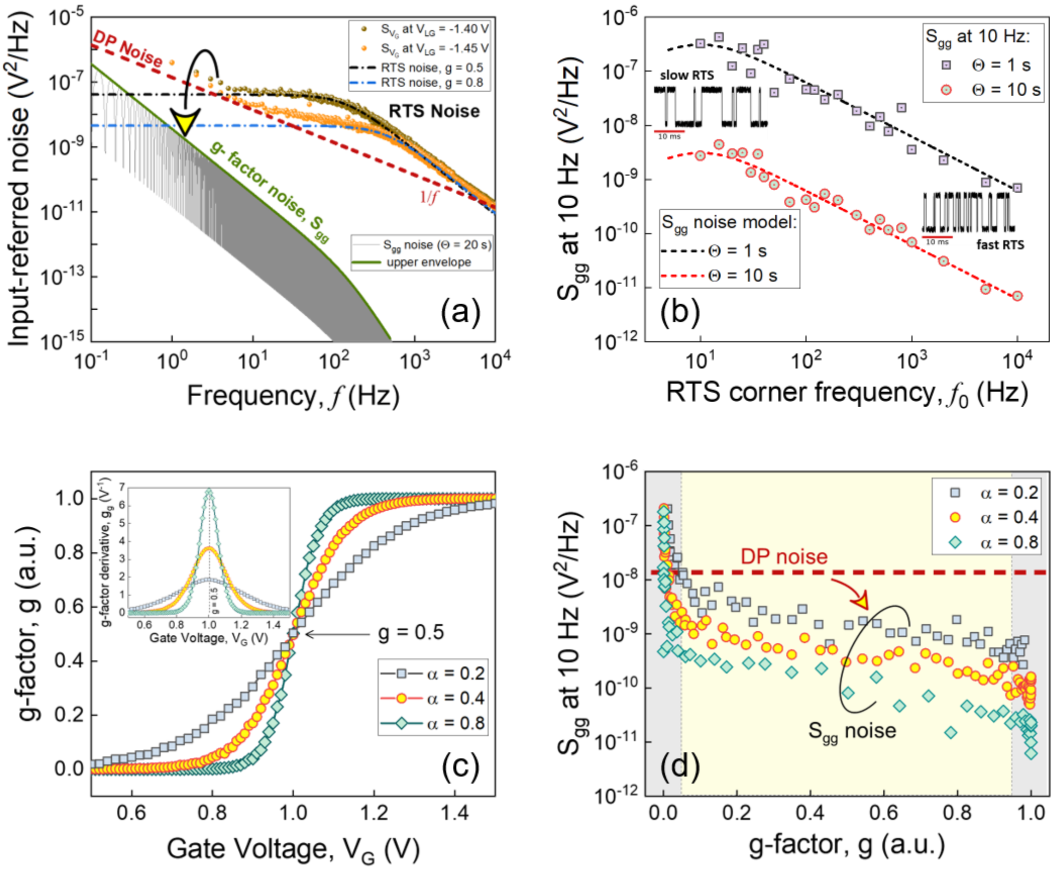


Figure 5.5: Noise suppression in STP-based biosensors. (a) Input-referred voltage noise of the $100\ nm$ wide and $100\ nm$ long Si NW FET measured at different V_{LG}. The dash-dotted color lines show the Lorentzian fittings of the RTS noise. The red dashed line represents DP noise calculated for the same device. The arrow indicates the LF noise suppression to the calculated S_{gg} noise; (b) Trap occupancy noise as a function of the RTS corner frequency for the time windows $\Theta = 1\ s$ and $\Theta = 10\ s$ when $g = 0.5$; (c) Trap occupancy factor (g) and its derivative (g_g) shown in the inset and calculated for the RTS noise simulated with different α (a ratio between gate capacitance (C_G) and tunneling capacitance (C_j) - see Equation 7.1 in *Appendix B*); (d) S_{gg} noise at $10\ Hz$ and $\Theta = 10\ s$ plotted as a function of g for different conditions. The horizontal dashed line shows the DP noise level at $10\ Hz$ calculated for the same Si NW FET. The arrow indicates noise suppression below the DP thermal limit when considering g as a signal.

The impact of Θ on S_g is demonstrated in Figure 5.4(c). As mentioned above, a large enough window that contains enough number of trapping/detrapping events (> 200) is required for the meaningful statistical evaluation of the g-factor. The RTS corner frequency which also has a strong impact on the number of transition events between the trap-states within a given period of time is another important parameter to be considered in this regard. It should be noted that the number of RTS characteristic switchings over time Θ is higher for the high-frequency RTS process compared to the low-frequency RTS in the case of the same trap occupancy probability. This leads to a more accurate evaluation of g-factor and thus lower S_{gg} noise for the fast (high-frequency) RTS considering the same amount of time as for the slow (low-frequency) RTS process (Figure 5.5(b)). The slope or steepness of the g-factor dependence on the applied gate voltage is another important parameter that defines STP efficiency for biosensing applications. Figure 5.5(c) shows the gate-voltage dependencies of the g-factor with different slopes. As it follows from Equation 5.6, S_{gg} noise also strongly depends on g_g that is the slope of the g-factor curve. The results shown in Figure 5.5(d) confirm that S_{gg} can be, in fact, reduced by down to an order of magnitude due to the effect of the g-factor slope.

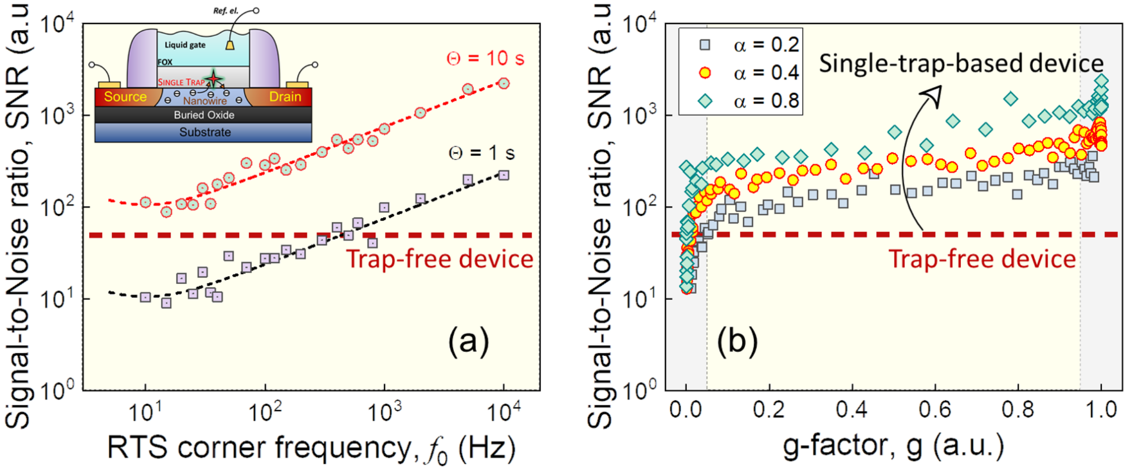


Figure 5.6: Boosting SNR in STP-based biosensors. (a) SNR of $5.9\ mV$ signal as a function of RTS corner frequency for the time windows $\Theta = 1\ s$ and $\Theta = 10\ s$ when $g = 0.5$. (b) SNR vs. g for different g-slopes and $\Theta = 10\ s$. The dashed horizontal line denotes the SNR level calculated for the Si NW FET biosensor with DP voltage noise of $1.4 \times 10^{-8}\ V^2/Hz$ at $10\ Hz$. The arrow indicates the SNR enhancement for the STP-based sensing approach.

Typically, for transistor-based biosensors monitoring a shift of the threshold voltage as a signal, the SNR can be calculated as:

$$SNR = \frac{\delta V_{th}}{\sqrt{\int_{f_1}^{f_2} S_{V_G} df}} \tag{5.7}$$

where S_{V_G} is the input-referred voltage noise, and δV_{th} is a threshold voltage shift caused by the target analyte attached to the surface of the classical FET-based biosensor.

Therefore, SNR for STP-based nanobiosensors can be defined similarly as:

$$SNR_{(STP-approach)} = \frac{\delta V_{th}}{\sqrt{\int_{f_1}^{f_2} S_{gg} df}} \tag{5.8}$$

SNR as a function of RTS corner frequency is presented in Figure 5.6(a) for the time windows $\Theta = 1\ s$ and $\Theta = 10\ s$ at $g = 0.5$. As can be seen in Figure 5.6(a), SNR considerably increases with increasing RTS frequency due to the increased number of trapping/detrapping events for the higher RTS rate ($\gamma = \pi f_0$), which results in smaller S_{gg} noise (see Figure 5.6(b)). SNR values calculated for STP with different g-factor slopes (see Figure 5.5(c)) are shown in Figure 5.6(b). The horizontal dashed line plotted in Figures 5.6(a) and 5.6(b) denote the SNR level for the trap-free device demonstrating only DP noise with the same gate capacitance as for the one demonstrating STP. As the input signal, we used the threshold voltage shift of $5.9\ mV$ caused by $0.1\ pH$ change in a gating solution in the case of the FET-based sensor showing a Nernstian-type response [18]. Therefore, the data presented in Figures 5.6(a) and 5.6(b) clearly show that under optimized conditions SNR indeed can considerably be increased even above the level of trap-free devices monitoring the threshold voltage shift as a signal. The obtained results shed light on relevant parameters required to optimize nanobiosensors exploiting STP.

5.4 Summary

Electrical noise in transistor biosensors is always considered as a limiting factor for the detection of small biological signals coming from the target analyte. Therefore, the physical mechanisms and effects leading to the reduction of the noise level in such devices have to be investigated and employed. In this chapter, we demonstrated and discussed a noise suppression mechanism offered by STP in nanoscale FETs. Unlike the usual nanotransistor-based biosensors, where the threshold voltage shift is the signal and voltage fluctuations are the noise, the signal in STP-based devices is a trap occupancy probability (g-factor). Therefore, the fluctuations of this parameter become the noise. To evaluate the g-factor noise, we proposed a method that allows obtaining g-factor fluctuations in time directly from RTS voltage fluctuations. The obtained results show that **low-frequency noise can, in fact, be suppressed even beyond the thermal limit** by monitoring the trap occupancy probability as a signal in an approach analog to the stochastic resonance effect used in biological systems. Under these conditions, we defined and calculated SNR for devices exploiting STP and demonstrated experimentally, numerically, and analytically that SNR can substantially be improved even beyond that of trap-free devices. The results are important for the optimization of advanced STP-based tools that could revolutionize the fields of biotechnology and personalized medicine.

STP FOR ADVANCED BIO- AND CHEMICAL SENSING

The development of advanced biosensing technologies for diagnosis and warning of various diseases and infections that continue to rapidly spread all over the world are urgently needed nowadays. To increase the chances for the successful recovery of patients and advance our understanding about a disease towards determining the best possible ways for the treatment and preventive healthcare, a disease has to be detected at the earliest possible stage. In this regard, the non-invasive diagnostic testing of disease-specific molecular biomarkers in biological samples is considered as one of the most promising strategies for disease management. However, the task is still very challenging and complex since the target biomarkers usually exist in very low concentrations, especially at the early stages of disease development. Therefore, there is a continuous need to develop reliable, accurate, and highly sensitive analytical devices for the high-effective biomarker-based medical diagnostics. In this chapter, we apply the single-trap phenomena approach for the label-free detection of target analytes in chemical and biological experiments. Our idea is to use RTS characteristic time constants as novel sensing parameters that are directly related to the signal of interest, i.e. a change of the surface potential due to biochemical reactions occurring on the sensors' surface. The obtained results prove the validity of the approach and demonstrate that STP in the novel Si TL NW FETs with advanced characteristic parameters can be effectively used to increase the sensitivity of nanosensors. We underline that the STP-based approach provides a noise-free amplification of sensor sensitivity since RTS is used as a signal. In this contribution, we report the successful experimental demonstration of sensitivity enhancement effect enabling ultra-sensitive bio- and chemical sensing at the nanoscale.

6.1 Analysis of pH response and ions sensitivity of TL NW FET biosensors

Measurement and control of the pH value of liquids are extremely important tasks in a wide variety of applications. Therefore, a pH measurement system has to be capable to provide good reliability, accuracy, and speed of pH measurement. The use of ISFETs is a relatively new and promising method in this regard. However, the sensitivity of such classical ISFETs is still limited to perform high-quality and high-accurate pH measurements. The use of dual-gate measurement configuration for the nanotransistor-based sensors in which a liquid-gate remains fixed and a back-gate is monitored has been recently proposed to boost the pH sensitivity of such devices even beyond the Nernst limit of $60\ mV/pH$ at room temperature [94]. However, one can still argue that this dual-gate approach not necessarily provides a larger signal-to-noise ratio as the noise is amplified exactly in the same manner as the signal. In this section, we employ STP in fabricated TL NW FETs as a novel approach to detect different pH values as well as variations in concentrations of different ions in gating solitons. The liquid-gate potential was applied to the FETs using a standard $Ag/AgCl$ reference electrode. All sensing experiments were performed at room temperature inside a metal Faraday cage to shield against external electromagnetic radiation and other parasitic disturbances.

pH sensing using the STP-based approach

Figure 6.1(a) shows a typical amplitude histogram plotted for different time traces measured on Si TL NW FET with $100\ nm$ width and $200\ nm$ length at different liquid-gate voltages. As can be seen in Figure 6.1(a), the histogram curves are composed of two Gaussian peaks reflecting a characteristic behavior of two-level RTS as a result of STP in the tested device. The ratio between peaks that correspond to capture and emission RTS states changes with varying liquid-gate potential suggesting a strong dependence of STP on surface potential controlled by the liquid gate. The extracted STP capture and emission times are shown in Figure 6.1(b) as a function of drain current. As can be seen, the register RTS demonstrated an enhanced capture kinetics behavior with a characteristic capture time slope of (-2.6) in the logarithmic scale that is far beyond the classical SRH model. The result suggests a very high sensitivity of RTS capture time as a novel biosensing parameter to be used for monitoring changes in surface potential caused by biochemical reactions on the surface of the TL NW sensor.

After RTS noise characterization, the liquid-gated TL NW structure demonstrating pronounced STP was employed for pH measurements. First, the pH response of the p-type NW FET sensor was measured using the standard approach by monitoring changes in drain current. Figure 6.1(c) shows a continuous-time trace of transistor drain current measured at constant $V_{DS} = 100\ mV$ when the device was liquid-gated at constant $V_{LG} = 2\ V$ in buffer solutions with different pH values. The back gate was grounded in this experiment. A commercially available ISMATEC tubing pump and the home-made PDMS microchannel were used for liquid delivery. As can be seen in Figure 6.1(c), the drain current increases gradually with increasing pH. The lower the pH value of the buffer solution, the more positively-charged hydrogen ions accumulate on the SiO_2 surface resulting in the depletion of holes as majority carriers in the $p^+ - p - p^+$ device. It should be noted that the measured pH response is in agreement with the results of I-V measurements under different pH conditions presented in Section 4.2.2 of this work. The data presented in Figure 6.1(c) was then used to determine the pH response of the sensor in terms of sensitivity:

$$S_{(I_D)} = \frac{I_D}{I_{D\_Max}} \tag{6.1}$$

where I_{D_Max} is the drain current of the transistor exposed to a buffer solution with a maximum pH value of 7.2 in this experiment at definite operational conditions.

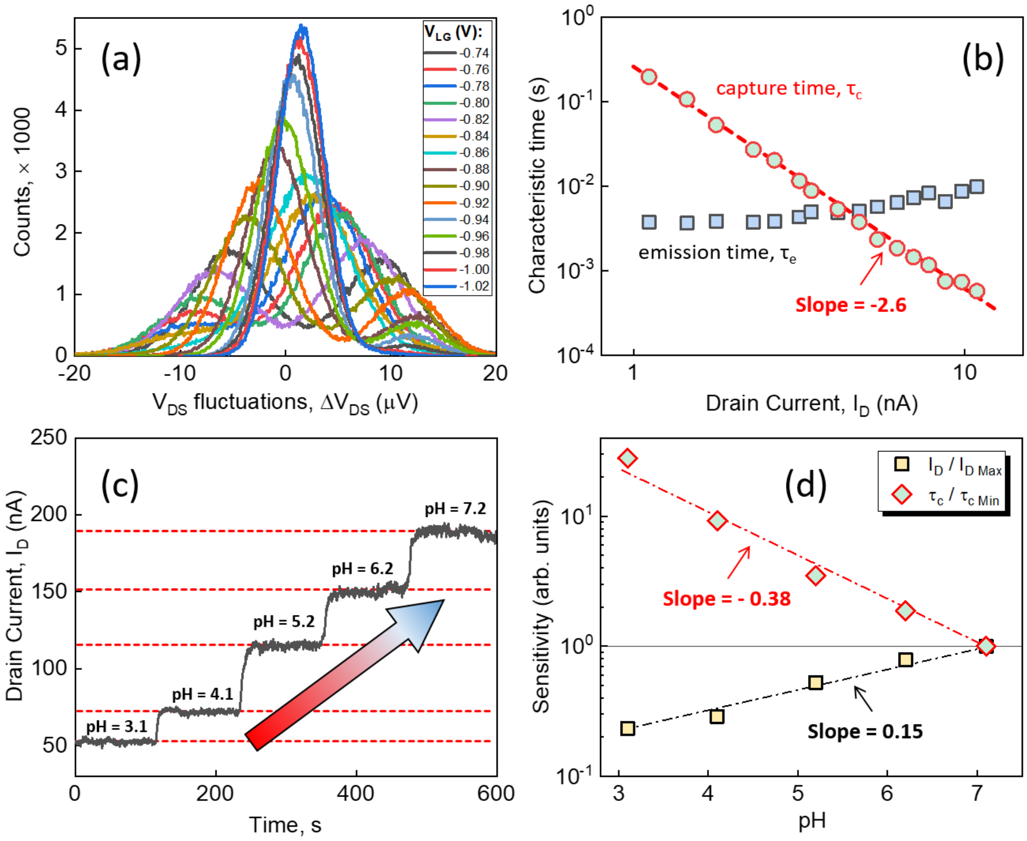


Figure 6.1: (a) Histograms of the voltage fluctuations confirming the two-level RTS switching behavior of the signal; (b) Capture and emission time constants vs. drain current extracted for the measured RTS time traces; (c) Time-resolved pH response of Si TL NW FET; (d) Responses of the NW sensor calculated for the standard $I_D - approach$ and a new $STP - approach$. The dot-dashed lines show linear fits with slopes indicated for both sensing approaches.

The same variations in pH values of the buffer solutions were then measured using the STP-based approach by monitoring RTS capture time as a signal. For this purpose, $40\ s-$long RTS time traces were recorded at constant $V_{DS} = 100\ mV$ and $V_{LG} = -0.8\ V$. Such operational conditions were applied to ensure that the single trap remains active in the whole range of the tested pH values taking into account that the drain current in p-type devices and therefore trap occupancy probability increases with pH (see Figure 6.1), which is equivalent to the increase of the liquid-gate potential. Thus, as protonation/deprotonation of SiO_2-covered TL NW surface changes the surface potential, the changes in RTS capture time at the definite working point were registered and analyzed in terms of sensitivity as:

$$S_{(\tau_c)} = \frac{\tau_c}{\tau_{c\_Min}} \tag{6.2}$$

where τ_{c_Min} is the RTS capture time measured for the case when the device is exposed to the solution with the highest in this experiment $pH = 7.2$ resulting in the highest drain current of the p-type sensor in this particular case.

In Figure 6.1(d) the experimental results are compared for two sensing approaches. An approximately linear dependence of the drain current change on pH with a slope of (0.15) in the semilogarithmic scale was obtained for the standard I_D-approach when the drain current was used as a sensory signal. At the same time, the RTS capture time constant used as a sensing parameter in the STP-based approach evolved the dependence on pH with a characteristic slope of (-0.38), which is at least $2.5\ times$ (or about $250\ \%$) larger compared to the standard I_D-approach. The result confirms that STP in the employed sensor is extremely sensitive to the changes in surface potential caused by the variation of the pH values in this specific case. Such a much stronger dependence of RTS capture time on the pH in comparison to the current change can be explained considering the enhanced RTS capture dynamic (see Figure 6.1(b)). It should be noted that within the measurement errors the revealed sensitivity gain of $2.5\ times$ approaches the value of the characteristic capture time slope of 2.6 (see Figure 6.1(b)), which reflects the trapping/detrapping dynamic behavior of the single trap. Therefore, the obtained results show that STP with enhanced characteristic parameters possesses a huge potential to be used for advanced biosensing.

Ion sensing using the STP-based approach

As proof of good reproducibility and working stability, the same NW FET sensor demonstrating pronounced RTS with advanced characteristics was further employed to detect different concentrations of KCl and $MgCl_2$ in solutions with constant pH value using both the standard I_D*-approach* and the new *STP-based approach*.

The results of the sensing experiments are shown in Figure 6.2(a). The solid lines “1” and “2” with the characteristic slopes (-0.09) and (-0.12) in the logarithmic scale denote the response of the sensor to variations in KCl and $MgCl_2$ concentration in DI water, respectively. In this case, the transistor drain current was monitored as a signal. It should be noted that a slightly higher response of the p-type sensor to Mg^{2+} compared to K^+ cations was observed in this case, which is consistent with the I-V measurement results presented and discussed in Section 4.2.2. At the same time, the solid lines “3” and “4” with the characteristic slopes (0.23) and (0.32) demonstrate the response of the device respectively to K^+ and Mg^{2+} ions in the approach based on STP when the RTS capture time was used as a sensing parameter. All the response curves “1-4” were obtained by fitting the normalized sensor responses with Equation 4.2. We consider the slope of the normalized response curves as device sensitivity to compare the efficiency and sensitivity of different approaches.

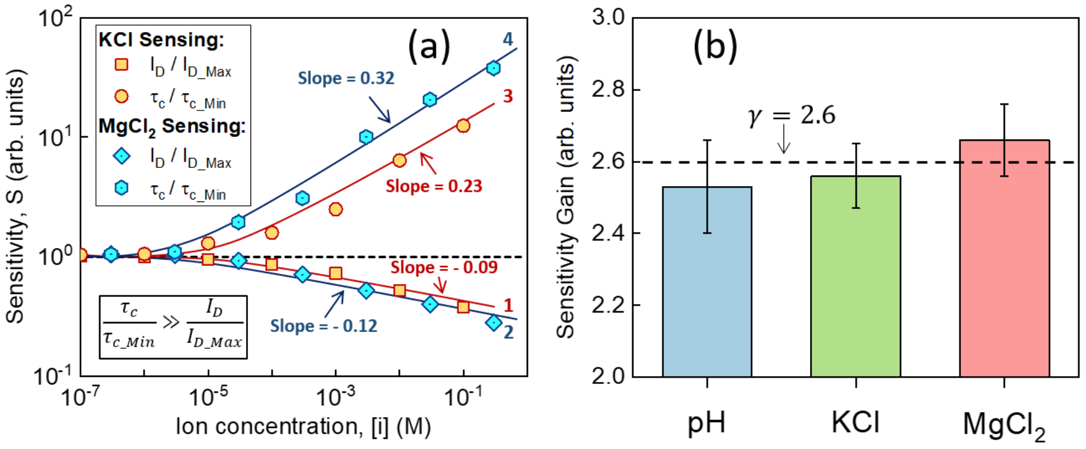


Figure 6.2: Demonstration of sensitivity enhancement to different chemical analytes for the NW sensor exploiting RTS capture time as a signal. (a) Responses of the sensor calculated for different sensing approaches: solid lines “1” and “2” show the responses of the device to the changes respectively in concentrations of K^+ and Mg^{2+} cations using the standard $I_D-approach$, while lines “3” and “4” denote the responses of the same sensor operating in the $STP-approach$; (b) The sensitivity amplification obtained by the same NW sensor monitoring the variations in concentrations of different chemical species using the STP-based approach. The dashed horizontal line reflects the capture dynamic slope $\gamma = 2.6$ (see Figure 6.1(b)) that was obtained for the measured RTS process which was further exploited for biosensing applications. Vertical error bars represent statistical errors calculated using the least square root method.

As can be seen in Figure 6.2(a) (line “3” and “4”), the RTS characteristic capture time changes more strongly in response to the change of ions concentrations compared to the changes of drain current (line “1” and “2”). This fact demonstrates that changes in surface potential due to the chemical adsorption of charged species such as K^+ and Mg^{2+} cations on the sensor’s surface can be registered with enhanced sensitivity by monitoring changes in capture time as a characteristic of STP in the liquid-gated nanoscale device. Figure 6.2(b) summarizes the amplification in sensitivity obtained experimentally to different chemical analytes for the NW sensor exploiting STP. We stress that the STP-approach provides a noise-free amplification in sensitivity since RTS was exploited as a sensory signal. As can be seen in Figure 6.2(b), the achieved sensitivity gain, which is the ratio between sensitivities for different approaches, in fact, corresponds to the exponent γ which reflects the RTS capture dynamic (see Equation 2.44). This result is a direct proof of the principle for the utilization of STP with enhanced capture dynamic for advanced biosensing with improved sensitivity.

6.2 Demonstration of STP for the enhancement in sensitivity to antioxidants

Antioxidants such as ascorbate (ascorbic acid) molecules play an important role in multiple biological functions and help to protect a biological system against harmful reactive oxygen species (ROS) released as a result of oxidative stress. Working as scavengers of oxidizing free radicals, antioxidants neutralize ROS molecules and therefore help a biological system to stop the toxic effect, repair the damage and restore the ROS-balanced state of the system disturbed by the oxidative stress. In this perspective, ascorbate is one of the most powerful non-enzymatic antioxidants as it rapidly and effectively reduces the toxic oxygen-derived species such as hydroxyl radicals, singlet oxygen, and hydrogen peroxide [103]. Therefore, it is important to develop a highly sensitive tool for the detection and monitoring of antioxidants like ascorbate that are involved in reduction-oxidation reactions of the ROS-balance-related biochemistry. It this section, we apply fabricated NW devices for sensing of ascorbate molecules as antioxidant-specific biomarkers using a novel STP-based approach. It should be noted that to the best of our knowledge, no attempts to measure changes in ascorbate concentration using NW-based sensors have been reported in the literature yet. In this study, we employed a p-type Si TL NW FET sensor with 400 nm long and 70 nm wide NW that is triangular in cross-section. A schematic view of the sensor including the measurement configuration is schematically illustrated in Figure 6.3. The home-made PDMS microchannel was used to deliver testing solutions. An $Ag/AgCl$ reference electrode was inserted into the outlet tube close to the microchannel to avoid any pollution of liquids pumped through the microfluidic channel.

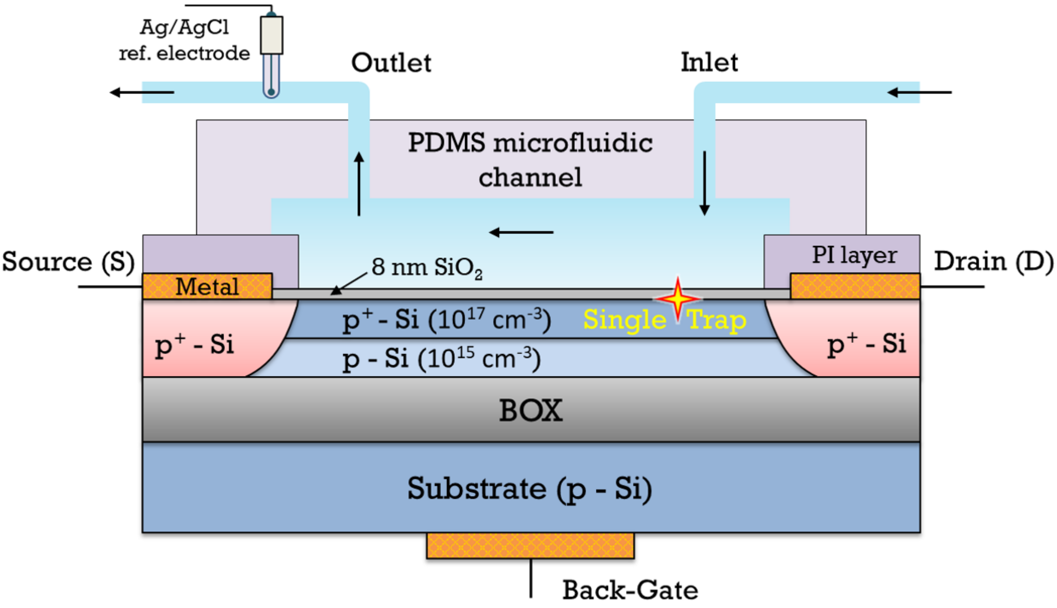


Figure 6.3: Schematic illustration of TL NW FET biosensor exploiting STP integrated with microfluidic (sectioning in the direction along NW) used for the delivery of gating solutions.

Sets of measured transfer and output I-V characteristics are shown in Figure 6.4(a) and 6.4(b), respectively. A physiological PBS solution with $pH = 7.4$ was used as the gating solution in this case. It should be noted that the device demonstrated leakage-free electrical performance while operating in a liquid environment. As can be seen in Figure 6.4(b), noticeable fluctuations in drain current were observed at high liquid-gate voltages. Such stepwise behavior registered at room temperature suggests the presence of a single trap in the front-gate oxide layer that randomly exchanges the charge carriers with the conductive channel of the NW FET.

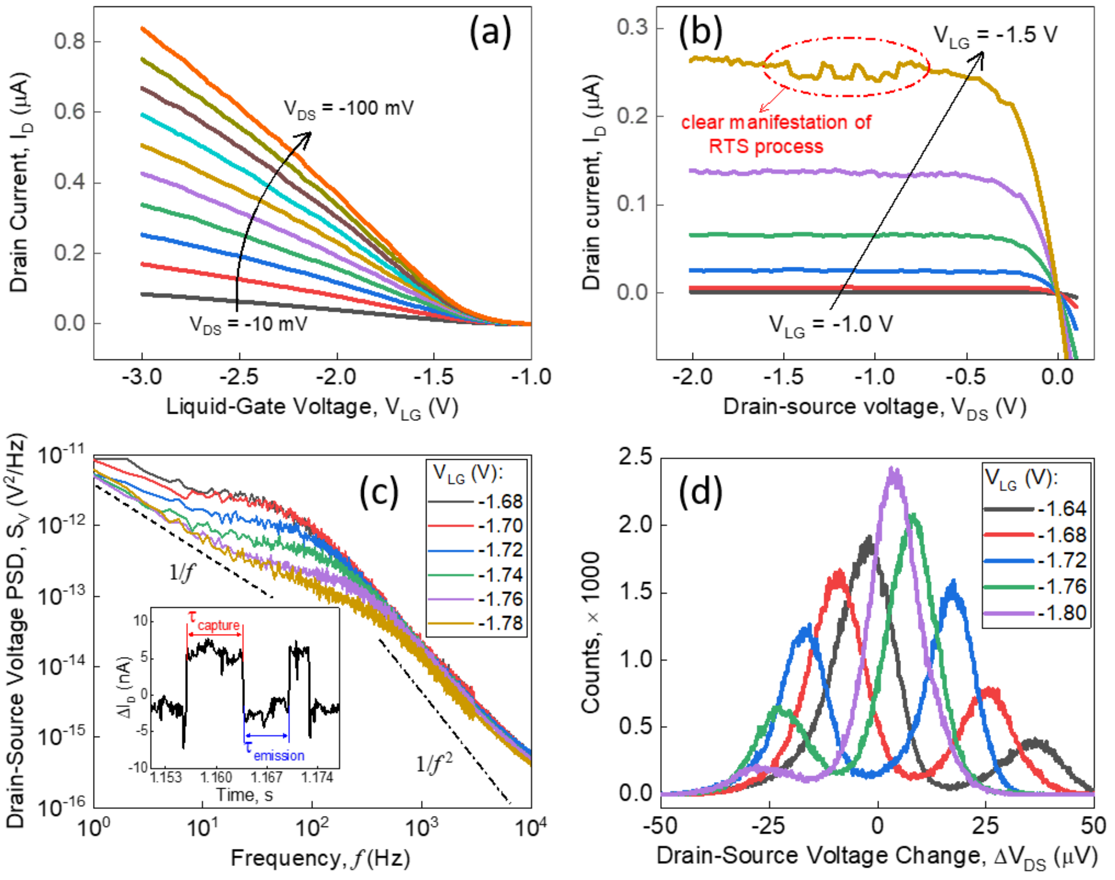


Figure 6.4: (a) Set of transfer I-V curves measured on the $400\ nm$ long and $70\ nm$ wide Si TL NW FET measured at different V_{LG} voltages: from $-10\ mV$ to $-100\ mV$ with a step size of $-10\ mV$; (b) Set of output I-V curves measured on the same device at different liquid-gate voltages that were varied in the range from $-1.0\ V$ to $-1.5\ V$ with a step size of $-0.1\ V$. A stepwise behavior observed at high liquid-gate voltages is indicative for STP in the device under study; (c) Drain-source voltage noise PSD spectra measured at different V_{LG} and a constant $V_{DS} = -100\ mV$. Inset: typical time-resolved RTS fluctuations of the transistor drain current measured at $V_{LG} = -1.70\ V$; (d) Amplitude histograms of measured time traces confirming two-level RTS fluctuations.

To investigate the observed fluctuation phenomena in detail, we performed the LF noise measurements. Figure 6.4(c) shows the voltage noise spectra measured for the same device at different liquid-gate voltages, while the back gate was grounded and the drain-source bias was kept constant at $-100\ mV$. As expected, the registered S_V spectra demonstrate Lorentzian-shaped noise behavior with the characteristic frequency shifting to a higher frequency range with increasing liquid-gate potential. The behavior is typical for the RTS noise as a result of STP in fabricated LG TL NW structures. The switching kinetic of the two-state RTS process is further confirmed in Figure 6.4(d) showing the amplitude histogram curves of measured V_{DS} time traces (see inset of Figure 6.4(c).

As can be seen in Figure 6.4(d), two Gaussian peaks can be well-resolved reflecting a probability of the trap to be in a certain RTS state: *capture* (trap is empty) or *emission* (trap is occupied by a charge carrier). The calculated average capture (τ_c) and emission (τ_e) time constants characterizing the registered RTS process are presented in Figure 6.5(a) as a function of the drain current controlled by the liquid gate. A relatively weak dependence on drain current, i.e. density of carriers, was experimentally revealed for τ_e in this specific case, while τ_c demonstrated a strong dependence on I_D with a characteristic slope of (-8.2) in the logarithmic scale. Such a strong behavior suggests that τ_c is an extraordinarily sensitive parameter to changes in surface potential and thus has to be used as a novel sensing parameter. Therefore, the tested device demonstrating the pronounced STP with advanced characteristics was further employed for the detection of different concentrations of ascorbate molecules diluted in the PBS solution with initial $pH = 7.4$ and ionic strength of $0.18\ M$.

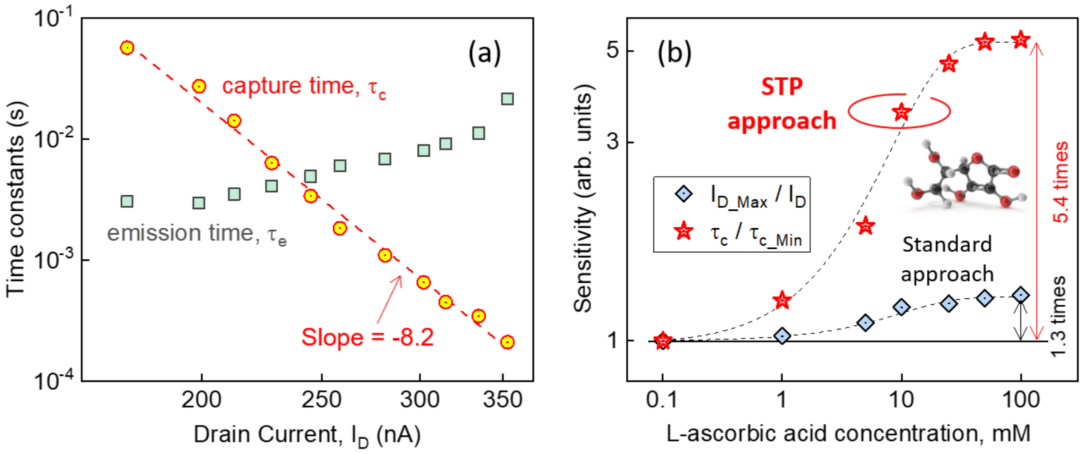


Figure 6.5: (a) RTS characteristic capture and emission time constants plotted as functions of drain current controlled by the liquid gate. The dashed red line with a slope of (-8.2) reflects a strong dependence of τ_c on I_D. (b) The response of the TL NW sensor to different concentrations of ascorbate molecules in terms of sensitivity calculated for different approaches: *standard approach* and *STP-based approach*. The dashed lines represent a visual aid.

In the sensing experiment, the current-voltage, as well as the LF noise measurements, were performed at defined operational conditions ($V_{DS} = -100\ mV$, $V_{LG} = -1.8\ V$), while the gating solutions with different concentrations of ascorbate molecules were subsequently supplied to the sensor through the microfluidic system (see Figure 6.3). The changes in both drain current (I_D) and RTS capture time (τ_c) were monitored and registered with an increasing concentration of ascorbate molecules until the concentration reaches approximately the value of $50\ mM$. At higher concentrations, no noticeable changes in neither I_D nor τ_c were further detected due to the saturation of the SiO_2-covered surface of the NW sensor. The results of the experiment are shown in Figure 6.5(b) for both the standard I_D-approach and the proposed STP-based approach using τ_c as a sensory signal. Both I_D and τ_c sensing parameters demonstrated a non-linear response to the changes in concentrations of target antioxidants. However, as it is evident in Figure 6.5(b), the RTS characteristic capture time constant varies much more strongly in response to the change of ascorbate concentration compared to I_D due to the enhanced RTS capture rate dynamic (see Figure 6.5(a)). The obtained result shows a clear advantage of the STP-based approach and confirms that fabricated TL NW structures demonstrating advanced STP characteristics can be effectively used as highly sensitive tools for monitoring the activity of antioxidant biomarkers such as ascorbate to measure oxidative stress in chemical, biochemical, or biological systems.

6.3 Ultrasensitive $fM-$detection of $A\beta$ peptides using STP-based approach

In this section, we report the successful demonstration of label-free and ultra-high-sensitive femtomolar (fM) detection of amyloid-beta ($A\beta$) peptides involved in Alzheimer's disease using fabricated biosensors. Alzheimer's disease (AD) is a severe neurodegenerative disorder in humans that progressively destroys brain cells which leads to irreversible loss of thinking skills and other mental abilities [104, 105]. In this regard, AD is considered a very serious health problem for mankind leading to lethal outcomes in most cases. Although research is still ongoing towards identifying risk factors and biochemical processes leading to the onset and development of AD, it has been revealed in many studies that extracellular aggregations of clustered $A\beta$ peptides ($A\beta$-plaques) and intracellular accumulations of neurofibrillary tangles consisted of altered tau proteins are direct hallmarks of AD [8, 9, 104].

The early diagnosis of AD is of extreme importance for the development of therapeutic drugs and personalized treatment of the progressive disease. This requires the development of appropriate detection and quantitation methods for $A\beta$ peptides as major suspects that initiate pathological changes leading to AD. Nowadays, the detection of AD biomarkers is mainly based on ELISA-based techniques including a method known as sFIDA (surface-based fluorescence intensity distribution analysis) assay, which has been developed to quantify $A\beta$ oligomers. The assay uses a sandwich-ELISA biochemical setup combined with high-resolution fluorescence microscopy and employs anti-$A\beta$ antibodies to capture all $A\beta$ species to a glass surface. Fluorescence-labeled anti-$A\beta$-antibodies are then involved to probe the captured peptides by optical measurements [106, 107]. Although such optical-based detection provides a lot of advantages such as high-sensitivity and high-specificity, there are many limitations, which make the tool labor-dependent, time-consuming, and expensive. One of the solutions to overcome these challenges is to use compact and label-free nanowire-based biosensors capable of performing highly efficient biosensing in real-time. As proof of concept, below we present the experimental results on the detection of ultra-low concentrations of the 40-amino-acid-long $A\beta$ peptides known as $A\beta40$ using newly fabricated TL NW sensors. To perform highly specific biosensing, the NW devices were functionalized with single-stranded deoxyribonucleic acid (ssDNA) aptamers specially developed to specifically capture the target $A\beta40$ sequence in a biological liquid. The development of $A\beta40$-specific ssDNA aptamers was based on a SELEX process using the biotinylated $A\beta40$ peptides as targets. Two control experiments involving Western blot analysis and an enzyme-linked oligonucleotide assay have been performed to validate the synthesized ssDNA aptamers as highly specific receptors for $A\beta40$ peptides [108]. Moreover, the field-effect capacitive technique exploiting electrolyte-insulator-semiconductor (EIS) structures was additionally employed before biosensing with NW sensors to confirm the high affinity and high specificity of developed aptamers to $A\beta40$ peptides. To enhance the sensitivity of the developed TL NW biosensors, the STP-based biosensing approach was used. As the result, highly specific, reliable, and label-free detection of $A\beta40$ peptides with sub-femtomolar sensitivity was demonstrated.

Detection of $A\beta40$ peptides using EIS-based biosensors

The field-effect capacitive technique is a widely used approach for biochemical sensing enabling label-free detection and monitoring of charged biomolecules in real-time. The technique is usually implemented using EIS structures consisting of only a few layers (see Figure 6.6(a)) which make them relatively simple and cost-efficient in fabrication. When the target biomolecule is selectively attached to the sensor's surface, the depletion or accumulation of charge carriers in the structure occurs depending on the type of the EIS structure. This results in the change of the capacitance characteristics of the sensor (see Figure 6.6(b)), which can be measured by the Impedance measurement unit as schematically depicted in Figure 6.6(a). As consequence, a shift in capacitive-voltage (C-V) characteristics can be then associated with the concentration of target molecules in the tested solution. Therefore, such a technique can be effectively used for the detection of target biomolecules such as $A\beta40$ peptides. For this purpose, we fabricated capacitive EIS structures using low-resistive n-doped silicon wafers with (100) orientation following the fabrication protocol reported in Ref. [54]. The EIS devices fabricated as $Al-n-Si-SiO_2$ structures were functionalized with $A\beta40$-specific ssDNA aptamers using the developed chemical functionalization protocol presented in *Appendix C* and employed for the detection of $A\beta40$ antigens dissolved in physiological PBS solution with $pH = 7.4$. The response of the EIS sensors was monitored as the concentration-dependent shift of the C–V characteristics caused by the attachment of target peptides to the sensor surface. The results of the sensing experiment are shown in Figure 6.7(a). The first curve shown in black corresponds to the reference C-V measurement performed in the pure $10\ mM$ PBS solution. The lateral shift of C-V curves in positive voltage direction was observed by introducing different concentrations of $A\beta 40$ peptides in the tested solution used as the liquid gate. The drop-cast method was used to prepare solutions with different concentrations of $A\beta 40$ molecules in this case.

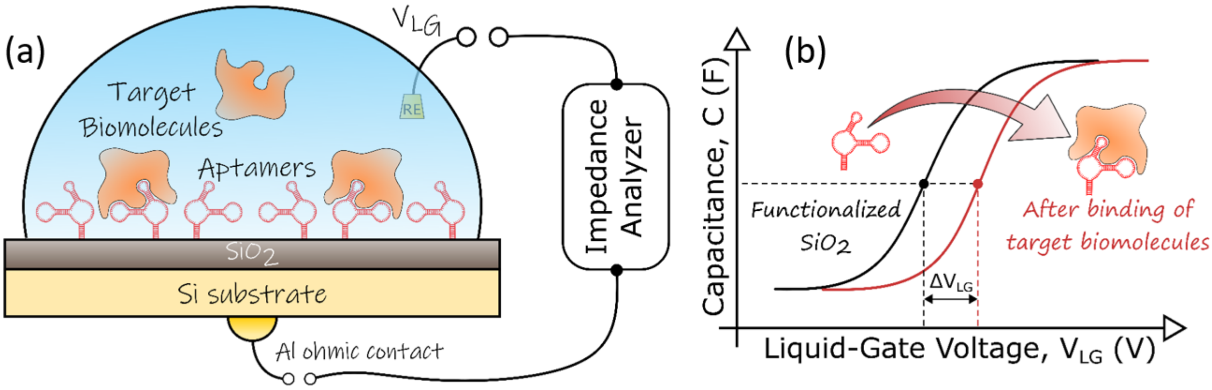


Figure 6.6: (a) Schematic demonstration of EIS sensor exploiting capacitive field-effect for the detection of the target biomolecules. The surface of the sensor is functionalized with aptamer receptors responsible for the recognition and capture of the targets; (b) A concentration-dependent shift of C-V curves caused by the specific binding of the targets to the surface of the EIS sensor.

The shift of C-V curves can be seen more clearly in the inset of Figure 6.7(a). Such behavior of C-V characteristics can be explained considering the electrostatic properties of target $A\beta 40$ biomolecules. Being dissolved in the buffer solution with pH = 7.4, $A\beta 40$ peptides with the isoelectric point value of 5.3 [109] possess a net negative electrical charge. Therefore, the attachment of negatively charged peptides to the surface of the n-type EIS sensor induces the depletion of electrons in the space-charge region close to the Si/SiO_2 interface, which results in a shift of flat band voltage to more positive voltage values due to a change in the surface potential. The response of the sensor to different concentrations of the target peptides is shown in Figure 6.7(b) in term of sensitivity calculated as:

$$S_{(EIS)} = \frac{V_{FB}}{V_{FB0}} \tag{6.3}$$

where V_{FB0} and V_{FB} are the flat band voltages of the functionalized sensor before and after the binding of target peptides, respectively. The flat band voltages were extracted using the slope of the linear part of $(1/C^2)$ curves obtained from the corresponding C–V characteristics in Figure 6.7(a). As can be seen from Figure 6.7(b), the EIS sensor demonstrated a logarithmic response upon the injection of the target $A\beta 40$ peptides in the wide concentration range from $0.1\ pg/ml$ to $1\ \mu g/ml$ due to the large sensing area of $0.37\ mm^2$ of the developed EIS sensors. At a high concentration range ($> 1\ \mu g/ml$), no further noticeable changes of C-V curves were registered due to the charge screening effect.

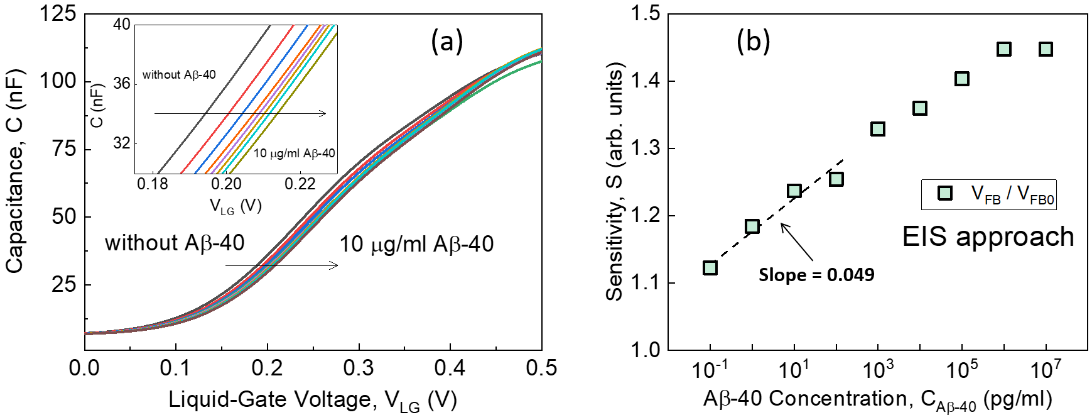


Figure 6.7: (a) C-V characteristics of the $Al-n-Si-SiO_2$ sensor measured at a frequency of $1\ kHz$ in the PBS solution with $pH = 7.4$ and different concentrations of $A\beta40$ peptides in physiological. The inset shows a pronounced shift of C–V curves upon increasing the target peptide concentration; (b) The response of the EIS sensor to different concentrations of the target $A\beta40$ peptides. The dashed line shows a linear fit of the response in a small concentration range $(0.1 - 100\ pg/ml)$ reflecting the sensitivity of the C-V-based approach.

Detection of $A\beta40$ *peptides using NW-based biosensors*

The highly sensitive and fast detection of the ultra-low concentrations of AD biomarkers such as $A\beta40$ peptides open prospects for the fast and reliable medical diagnosis of AD even at the early stages. Here, we experimentally demonstrate that the fabricated TL NW biosensors functionalized with $A\beta40$-specific ssDNA aptamers can be successfully assigned for this role when exploiting single-trap phenomena with advanced characteristics as a signal (see Figure 6.8(a)). For this purpose, we selected a p-type LG Si TL NW FET with a length of $100\ nm$ and a width of $100\ nm$ demonstrating pronounced RTS noise as a result of STP. The device was then functionalized with the synthesized ssDNA aptamers that are exclusively sensitive to the $A\beta40$ peptides.

Transfer curves measured for the NW sensor before and after the biofunctionalization procedure are shown in Figure 6.8(b). The shift of I-V curves registered after the functionalization step confirms the successful immobilization of the $A\beta40$-specific aptamers on the TL NW surface. It should be noted that the single trap in the tested nanosensor remained active after the functionalization resulting in the pronounced two-level RTS noise when the device was operating in the subthreshold working regime. Figure 6.9(a) shows a typical RTS time trace recorded for the same sensor at constant $V_{DS} = -20\ mV$ and $V_{LG} = -2.1\ V$. Two stable states of the measured RTS process can be well-resolved that correspond to the single trap in the gate oxide layer being empty or occupied by a charge carrier from the conductive channel.

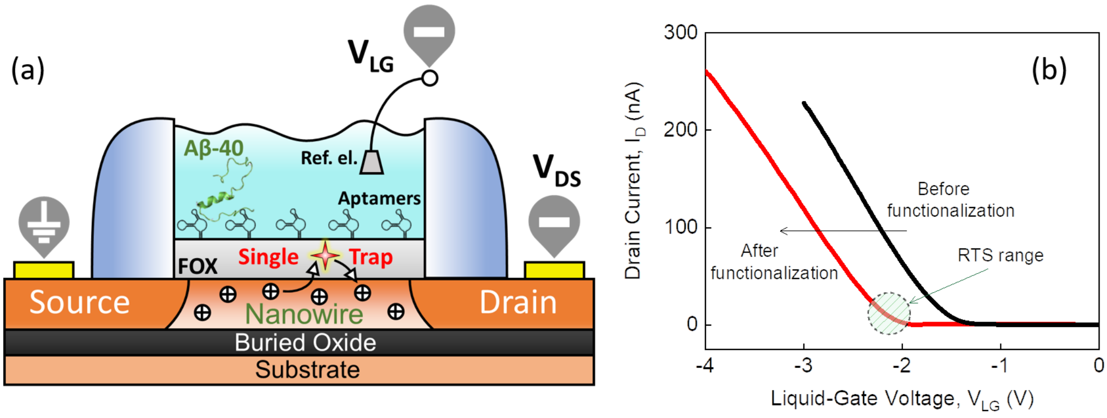


Figure 6.8: (a) A schematic view of the NW FET biosensor with a single trap in a gate oxide layer responsible for the random trapping/detrapping of charge carriers resulting in the RTS noise. The surface of NW is functionalized with $A\beta40$-specific ssDNA aptamers. (b) Transfer I-V characteristics of Si TL NW FET before and after the biofunctionalization step. The dashed area denotes the range of liquid-gate voltages at which the registered single trap was active.

Figure 6.9(b) presents the drain-source voltage noise PSD spectra measured at different liquid-gate voltages on the same device biased at a constant $V_{DS} = -20\ mV$. The spectra demonstrate Lorentzian-type shape with characteristic frequency shifting to a higher frequency range with increasing of liquid-gate potential, which is typical for the RTS noise in LG nanostructures. The registered two-level RTS process can be also evident from Figure 6.9(c) showing amplitude histograms at different V_{LG}. The histograms reveal two well-resolved Gaussian peaks confirming two stable states of the single trap in the tested device. The liquid-gate voltage and drain current dependencies of capture and emission times characterizing the measured RTS are shown in Figure 6.10(a) and 6.10(b), respectively.

As can be seen in Figure 6.10(a), the average emission time (τ_e) remains about constant in the range of the liquid-gate voltage applied, while the average capture time (τ_c) displays a superlinear dependence on V_{LG} in the semilogarithmic scale suggesting a strong dependence of the RTS capture dynamic on the surface potential controlled by the liquid gate. At the same time, the enhanced capture time dependence on the drain current with a slope of (-3.2) on the logarithmic scale can be evident in Figure 6.10(b). It should be noted that the RTS characteristic capture time in TL NW FETs demonstrates a much stronger dependence on I_D compared to the behavior with a slope of (-1) predicted by the classical SRH model. In this regard, the RTS capture dynamic appears to be very promising for the advanced biosensing considering τ_c as a sensory signal.

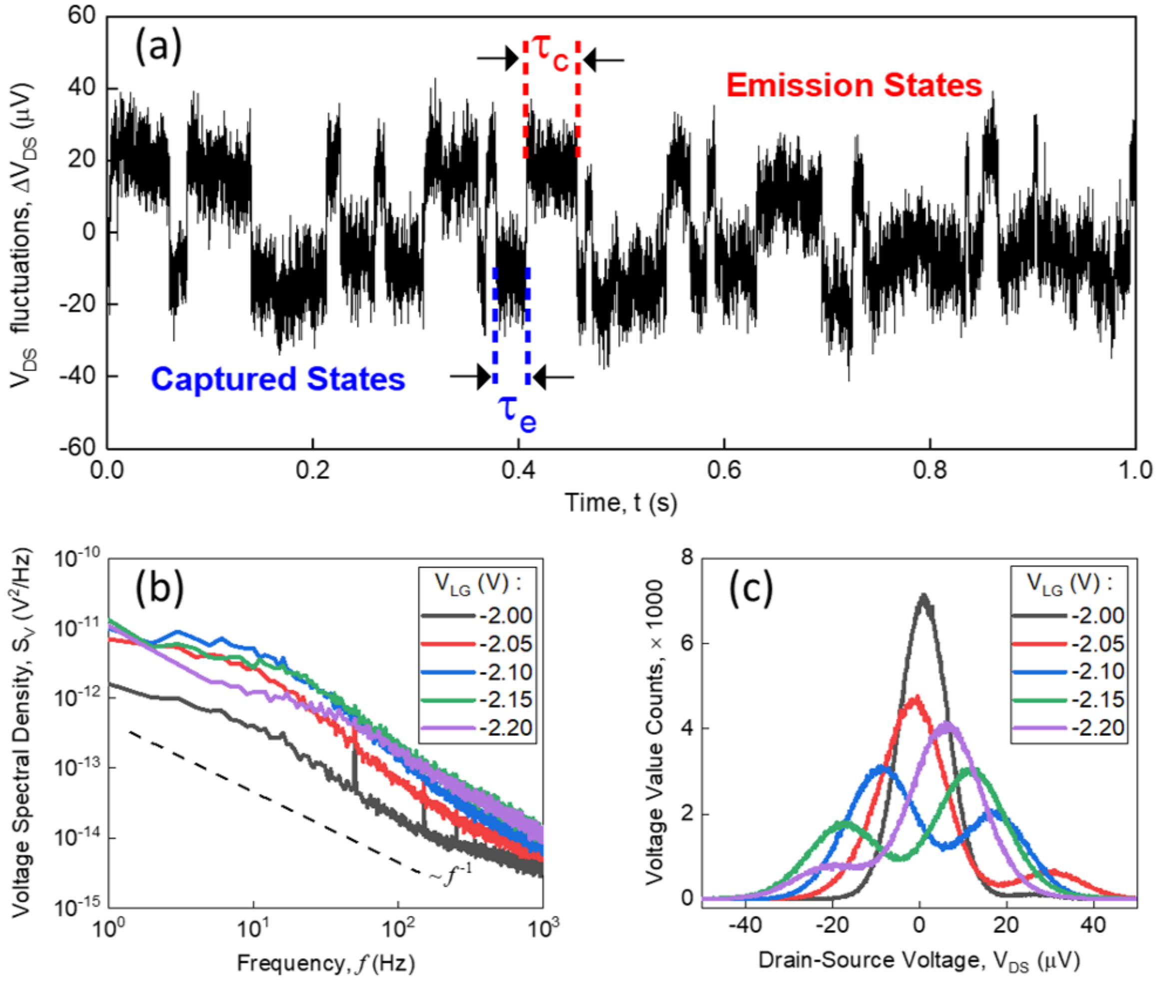


Figure 6.9: (a) Typical two-level RTS fluctuations of drain-source voltage measured on LG Si TL NW FET with NW width and length of $100\ nm$; (b) Voltage noise PSD spectra measured on the same device at different V_{LG}. The PSD curves reflect a Lorentzian behavior typical for the RTS noise; (c) Calculated amplitude histograms of the measured voltage fluctuations demonstrating two well-resolved Gaussian peaks.

After the characterization of RTS noise, the liquid-gated TL NW sensor functionalized with $A\beta40$-specific ssDNA aptamers was employed for the label-free sensing of the target $A\beta40$ peptides dissolved in the physiological PBS solution with $pH = 7.4$. The target analyte was detected by monitoring the modulation of the drain current (*standard approach*) as well as RTS characteristic capture time (*STP-based approach*) as the sensor was exposed to the PBS solutions containing different concentrations of $A\beta40$ peptides. For this purpose, a $40\ s-$long time traces were measured at constant $V_{DS} = -20\ mV$ and $V_{LG} = -2.05\ V$ for each concentration of the analyte. The RTS time traces were measured about $5\ min$ after introducing target peptides into the buffer solution to achieve an equilibrium state and thus reliable sensor output.

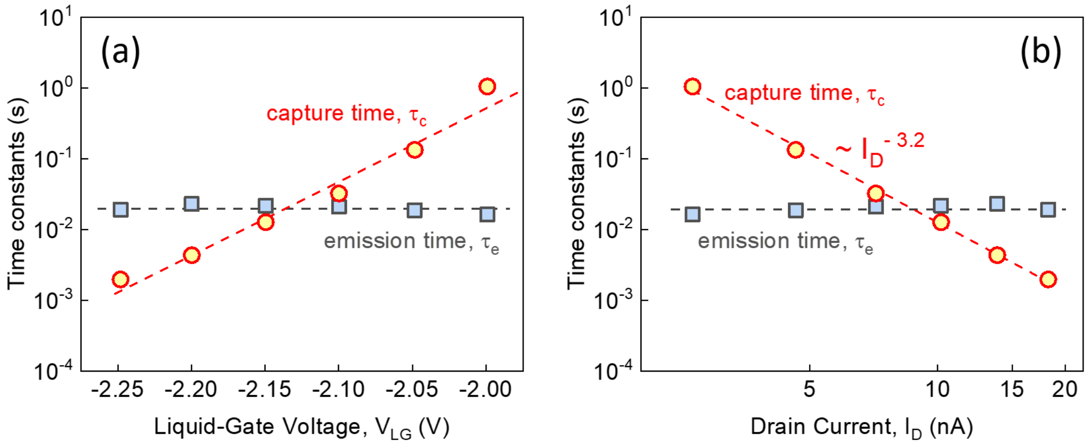


Figure 6.10: (a) Measured dependences of RTS characteristic time constants plotted as functions of (a) the liquid-gate voltage (V_{LG}) and (b) transistor drain current (I_D).

After the detailed analysis of the experimental data, the increase in the drain current, as well as the decrease in the RTS capture time upon increasing the concentration of $A\beta 40$ peptides, was revealed. The results are displayed in Table 6.1. Such behavior of the sensing parameters was expected for the p-type NW sensor taking into account that the $A\beta 40$ targets are negatively charged in the PBS solution with $pH = 7.4$ and therefore induce the accumulation of holes as majority carriers in the p-type device, which increases the probability of the single trap being occupied. As consequence, specific binding of negatively charged $A\beta 40$ peptides results in the increasing of drain current and decreasing of the RTS characteristic capture time with increasing $A\beta 40$ concentration.

Table 6.1: Sensing parameters of the TL NW sensor upon increasing the $A\beta 40$ peptides concentration.

#	$A\beta 40$ concentration (pg/ml)	Drain current, I_D (nA)	RTS capture time, τ_c (ms)
1	0	4.80	133.86
2	0.1	4.86	128.73
3	1	5.23	101.76
4	10	5.35	94.81

For the comparison purpose, the responses of the TL NW sensor in terms of the sensitivity calculated for both standard and STP-based approaches are shown in Figure 6.11. For the standard approach, the sensor response can be fitted as a linear function with a slope of (0.051). It should be noted that the sensitivity slope of (0.051) is only slightly higher in comparison with the slope (0.049) obtained for the capacitive EIS sensors (see Figure 6.7(b)). In contrast, for the STP-based approach, in which the RTS capture time was monitored as a sensory signal, the response of the sensor can be approximated as a linear function with a slope of (0.186). Such an enhanced value of the sensitivity slope confirms the superior sensitivity of the STP parameters such as RTS capture time to the surface potential changes due to the specific binding of target $A\beta 40$ peptides to the sensor surface. Therefore, in this specific case, the sensitivity of the new biosensing approach based on STP in nanobiosensors was at least 3 $times$ (or about 300 $\%$) higher for the specific and label-free $A\beta 40$ detection in comparison with the conventional approach based on the monitoring of drain current changes.

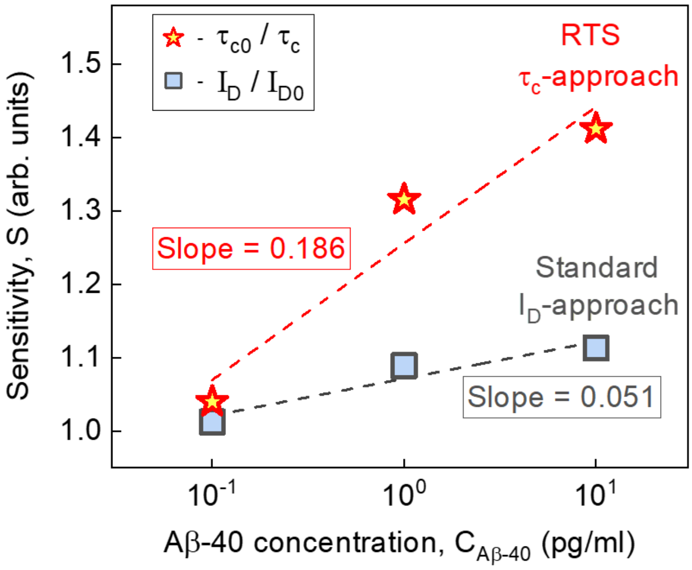


Figure 6.11: Measured responses of the TL NW FET biosensor in terms of sensitivity calculated for the *standard approach* and a new *STP-based approach*. The dashed lines show linear fits with slopes indicated for both sensing approaches.

It should be noted that for AD diagnosis at early stages the concentrations of target $A\beta 40$ biomarkers are usually in the range from dozens to several hundred picograms per milliliter [110]. For our developed TL NW sensors exploiting STP, the limit of detection defined as the minimum concentration of the target analyte that led to a response of the sensor was estimated to be ~ 20 fM. Therefore, our novel TL NW FET biosensors developed for the selective real-time detection of AD biomarkers such as $A\beta 40$ peptides with high sensitivity at concentrations as low as 20 fM open prospects to prevent AD at its early stage and thus increase the chances for the successful recovery of patients.

6.4 Summary

Sensitivity enhancement is an important aspect for the development of ultrasensitive biosensors aiming to detect low concentrations of the target analyte. In this chapter, we experimentally demonstrated that the proposed STP-based approach exploiting RTS noise as a signal allows the sensitivity to be **considerably enhanced** (up to $400\ \%$) for the nanoscale biosensors. In particular, we revealed that the change of the surface potential due to the change in pH or chemical composition of the gating solution (e.g., variations in concentrations of different ions or small chemical species like ascorbate molecules) can be monitored with the improved sensitivity owing to the enhanced RTS capture dynamic in fabricated TL NW FET biosensors. Furthermore, about 300% enhanced sensitivity compared to the standard biosensing approaches were achieved for the selective real-time detection of the target $A\beta$ peptides using the STP-based approach in fabricated devices. The result is important for the prospects of fast and reliable medical diagnosis of Alzheimer's disease at the early stages. Therefore, the performed experiments provide clear evidence of the effectiveness of the new biosensing strategy based on STP in LG nanostructures. The achieved results open up prospects for the label-free sensing of target chemical and biological markers with enhanced sensitivity, which is promising to bring clinical diagnosis, treatment, and personalized healthcare into the next level.

CONCLUSIONS AND OUTLOOK

The high demand for compact and reliable point-of-care devices stimulate and motivate the biosensors industry to grow rapidly nowadays. Although several promising prototypes of nanobiosensors for the sophisticated in vivo sensing applications have been recently reported, the biosensor community is still searching for the advanced biosensing technology that will boost personalized healthcare and transform the future of medical services in the forthcoming years. For these challenges, the usual concepts and conventional biosensing approaches have to be redefined and redesigned. As the result, it is expected that the new technology will release innovative, user-friendly, high-sensitive, and high-quality products capable to assist in guiding personalized medicine and delivery of health care in a high-speed, reliable, and relatively inexpensive manner. In this regard, miniaturized nanobiosensors attract much attention toward the implementation of such a complete "lab-on-chip" biosensing platform as a new paradigm for disease early diagnosis and monitoring of human health state.

In this thesis, we defined a new class of nanobiosensors exploiting **single-trap phenomena (STP) in nanoscale transistors as a signal**. Instead of the traditional view of STP as the most important issue for the miniaturized electronic devices, we proposed to consider a single trap in liquid-gated (LG) nanowire (NW) field-effect transistors (FETs) as a novel transducer principle which offers a unique possibility to detect small signals from the target analyte with enhanced sensitivity and improved signal-to-noise ratio compared to the standard biosensing approaches. The idea beyond this is to use the STP parameters that are directly related to the signal of interest (i.e., a change of the surface potential as the result of biochemical reactions on the sensors' surface) as a sensory signal carrying a useful chemical or biological information. For this purpose, **we designed and fabricated unique two-layer (TL) silicon (Si) NW FETs** consisting of two Si layers with different concentrations of boron dopants: the first layer is a low-doped Si with impurity concentration of 10^{15} cm^{-3}, while the second layer is a highly doped Si with doping concentration of 10^{16} cm^{-3} or 10^{17} cm^{-3} that was epitaxially grown on top of silicon-on-insulator (SOI) wafers. The main idea was to introduce the high-doped top Si layer with advanced properties to achieve enhanced random telegraph signal (RTS) switching kinetics of single traps in LG nanostructures. The devices configured as either p-channel or n-channel LG TL NW FETs were fabricated using a CMOS-compatible top-down approach. The fabrication protocol was optimized toward leakage reduction and better stability of the liquid-gated NW devices. In total, more than 10 thousand individual NW FETs with the NW lengths varying from 100 nm to 4 μm and widths in the range from 70 nm to 500 nm were fabricated. The devices can be operated by applying the voltage to the gating solution surrounding NW or to the highly doped Si substrate of SOI wafer acting as a back-gate electrode.

The TL NW FETs demonstrate **excellent scaling abilities, reproducible I-V characteristics, and stable operation in liquid without leakage currents**. The extracted values of the subthreshold swing were close to the ideal value of about $60\ mV/dec$ for the transistors measured in the liquid-gate configuration. At the same time, the typical mean values of field-dependent mobility were calculated to be $43\ cm^{-2}\cdot V^{-1}\cdot s^{-1}$ and $92\ cm^{-2}\cdot V^{-1}\cdot s^{-1}$ respectively for the $p^{+}-p-p^{+}$ devices with $10^{16}\ cm^{-3}$ and $10^{17}\ cm^{-3}$ doping concentrations, while for the structures configured as $n^{+}-p-n^{+}$ FETs with $10^{17}\ cm^{-3}$ concentration of dopants in the channel, this parameter approaches the value of $240\ cm^{-2}\cdot V^{-1}\cdot s^{-1}$. The measured characteristics and extracted parameters confirm the high-quality and high-level performance of the fabricated TL nanostructures.

The noise properties were studied for TL NW FETs with different NW geometries and device gate area. The fabricated TL NW devices generally show **the low-noise performance**. The analysis of the measured LF noise spectra revealed that mobility fluctuations due to the scattering and interactions of charge carriers with traps in the gate oxide layer are the main noise source in the p-type TL NW FETs with the gate area $A > 1\ \mu m^2$, while the n-type devices with similar dimensions demonstrate the number fluctuation noise mechanism. At the same time, RTS noise as a result of STP was revealed as a dominant noise source in $sub-\mu m$ LG TL NW FETs. The noise features investigated at low temperatures allowed us to **identify the origin of the single traps responsible for the RTS noise** in fabricated samples. The values of activation energy and the capture cross-section of the single trap extracted to be $290\ meV$ and $2.22\times10^{-18}\ cm^2$, respectively, indicate that the origin of the trap can be **attributed to a vacancy-boron complex**. Moreover, at temperatures below $200\ K$, the back-gated TL NW devices demonstrate clear generation-recombination noise with PSD proportional to $1/f^{3/2}$. Such noise behavior is characteristic of the diffusion-assisted transport processes in nanoscale devices confirming the contribution of the highly doped Si layer to the transport and noise properties of the TL nanostructures.

To reveal the high sensing capabilities of fabricated NW sensors, the devices were employed for the detection of various chemical and biological species of interest using the standard biosensing approach when a shift of transistor drain current or threshold voltage was used as a signal. In particular, NW FETs with different concentrations of dopants in the channel and covered only with $8\ nm$ thin bare SiO_2 as a sensing surface demonstrated $35\ mV/pH$ sensitivity. The obtained result is consistent with data reported for the state-of-the-art SiO_2-covered FET-based sensors. At the same time, the fabricated devices showed a good response to the chemical adsorption of K^{+} and Mg^{2+} cations on the sensors' surface at constant pH value. In particular, $48\ mV/log[i]$ sensitivity was obtained to variations in the concentration of **monovalent** K^{+} ions dissolved in deionized water, while the same sensors demonstrated the sensitivity as high as $64\ mV/log[i]$ upon changing the concentration of **divalent** Mg^{2+} ions. Notably, such an enhanced response of the tested sensors to variations in the concentration of Mg^{2+} exceeds the Nernst-limited sensitivity. The result can be explained considering ion-specific surface interactions yielding SiO_2 surface that is highly sensitive especially to multivalent cations like Mg^{2+}. In the future, the next step will be to check the sensitivity of the developed sensors to other multivalent ions and complex chemical species as well as perform sensing in multi-ion solutions. It should be also emphasized that our sensors start to respond as early as the concentration of ions reaches the value of $1\ \mu M$. Remarkably, such a **low detection limit is two orders of magnitude lower** than that reported for Al_2O_3-covered NW sensors. Interestingly, the performed sensing experiments reveal that the sensitivity of fabricated TL NW devices to different ions scales corresponding to a reversed Hofmeister series reported in the literature.

The fabricated biosensors demonstrated excellent capability for highly sensitive, highly selective, and label-free biosensing of **several biological targets such as cTnI and CRP cardiac biomarkers** in real-time. For the specific detection of target proteins, the surface of the sensors was functionalized with target-specific receptor molecules: DBCO-linked troponin-specific aptamers and CRP-specific monoclonal antibodies. The corresponding biofunctionalization protocols were developed and used. As the result, label-free specific detection of both cardiac biomarkers at picomolar concentrations with high sensitivity has been successfully demonstrated using developed biosensors. The efficient attachment of target biomarkers to the sensing area of Si NWs was confirmed by atomic force microscopy (AFM) measurements. Moreover, NW sensors of different sizes allowed us to detect target proteins in a wide concentration range (**from 1 pg/ml to 1 $\mu g/ml$**) which **covers** CRP and cTnI elevation levels during the development of heart diseases such as **acute myocardial infarction**. The obtained results open prospects to the development of high-sensitive assays for the rapid and accurate detection and monitoring of elevated cardiac biomarkers in real-time which is essential for the diagnosis of heart diseases at early-stages increasing the chances for successful recovery of patients.

Although promising biosensing results using fabricated NW biosensors have been achieved, the sensing capabilities of developed devices can be further extended considering STP as extremely sensitive effects enabling to enhance the knowledge of chemical and biological processes even at the molecular level. For this purpose, single trap dynamics in LG TL NW FETs with different concentrations of dopants in the channel were studied in detail. **A significant effect of the channel doping concentration on the single-trap dynamic was revealed in fabricated samples**. In particular, we registered the considerably enhanced RTS capture dynamic with increasing concentration of dopants in the TL NW channel compared to the behavior predicted by classical SRH theory. Remarkably, a superlinear RTS capture time behavior with **characteristic slope γ approaching even the value of** 10 was measured for some single traps in highly doped p-type devices. To understand and accurately explain the mechanism behind the enhanced RTS capture dynamic in highly doped nanostructures, we **developed an analytical model** considering the additional energy barrier that charge carriers have to overcome to be captured by a single trap. The derived model shows a good agreement with the measured data.

A strong modulation effect of the RTS capture dynamic with effectively tuned parameters was registered by applying a back-gate potential to the liquid-gated TL NW FETs. **A significant gate-coupling effect** between the liquid gate and the back gate revealed in the fabricated TL nanostructures enables the distribution of charge carriers to be intentionally changed in a well-controlled way allowing a precise modification of STP parameters including RTS characteristic capture time constant. The obtained experimental results were **supported also by TCAD simulations**. Therefore, as was experimentally demonstrated, the revealed effect allows the sensitivity to be fine-tuned for the sensors exploiting STP parameters as a signal. At the same time, the possibility to control single-carrier dynamic in nanoscale devices without any mechanical or chemical treatment opens up prospects for future nanotechnologies including the development of novel single-trap-based electrical switches and innovative logic elements.

Except for the sensitivity enhancement, STP in LG nanotransistors offer a unique possibility for the **low-frequency noise suppression** by monitoring the trap occupancy probability in an approach analog to the **stochastic resonance effect**. Unlike the classical transistor-based biosensors, where a shift of the threshold voltage is the signal and voltage fluctuations are the noise, the signal in STP-based biosensors is a trap occupancy probability (i.e., g-factor) and fluctuations of this parameter are the noise. To evaluate the g-factor noise, we proposed a method that allows g-factor fluctuations to be obtained directly from the RTS time trace. For the first time, we demonstrated that low-frequency noise can be suppressed even **beyond the thermal limit** by monitoring the trap occupancy probability as a signal. For this to happen, mainly three STP-related parameters have to be optimized: measurement time window Θ, RTS corner frequency f_0 (i.e., trap operation frequency), and a slope of the g-factor dependence on the gate voltage applied (g_g). The increase of the first two parameters leads to the increased number of transition events between the trap-states allowing a more accurate evaluation of g-factor and thus lower g-factor noise. The third parameter has a strong impact on the input-referred g-factor noise and determines the efficiency of the STP-based approach for biosensing applications. Moreover, **signal-to-noise ratio (SNR) for the devices exploiting STP was also defined and calculated**. We demonstrated experimentally, numerically, and analytically that under the optimized conditions, SNR can substantially be improved even beyond that of trap-free devices. The obtained results emphasize the importance of STP for biosensing applications.

The fabricated LG TL NW FETs were used to experimentally demonstrate the applicability and efficiency of the proposed STP-based approach for real biosensing. The first successful utilization of STP with advanced RTS capture dynamic in TL NW sensors was demonstrated for pH sensing. In this specific case, about **250% enhanced sensitivity compared to the standard approaches was achieved** for the detection of pH change in tested buffer solutions. The successful measurements exploiting STP have been also performed to detect changes in the surface potential due to the chemical adsorption of various chemical species like **ions or ascorbate molecules**. The results of the sensing experiments reveal that the RTS characteristic capture time used as a signal in the STP-based approach changes much more strongly compared to the transistor drain current in response to the change in concentration of chemical analytes. As a result, a considerable **amplification** (up to 400 %) in sensors' sensitivity was experimentally achieved and demonstrated. Moreover, the real advantage of the STP-based approach was shown for selective, label-free, and real-time biosensing. In this contribution, we successfully demonstrated that the developed TL NW sensors functionalized with specially synthesized $A\beta40$-specific ssDNA aptamers and demonstrating advanced STP with enhanced RTS capture dynamic can be effectively used as highly sensitive tools to specifically detect **$A\beta40$ peptides at concentrations as low as $20\ fM$. A new strategy exploiting STP in TL NW biosensors allows achieving about 300% improved sensitivity** compared to the standard detection approaches based on the measurements of capacitive-voltage or current-voltage characteristics. The obtained results open up new opportunities for **the early diagnosis of Alzheimer's disease** that will potentially enable termination of the disease development and further cerebral metabolism before these processes become irreversible. Thus, the performed sensing experiments provide clear evidence of the effectiveness of pronounced STP in nanoscale biosensors for advanced biosensing applications and show how the novel STP-based approach can assist in the detection and monitoring low concentrations of relevant biomarkers with enhanced sensitivity. This provides a unique and unprecedented opportunity to boost the quality of disease diagnosis at early stages and thus improves the confidence of decision-making in clinical practice. We believe that the results presented and discussed in this thesis can be used to conceptualize and produce **new robust, reliable, and extremely sensitive STP-based biosensing tools**.

To further investigate the potential of single traps in LG NW FETs for biosensing applications, the correlation effects between different traps in NW devices should be considered. We expect that the investigation of a strong coupling between individual charged traps or trap states (e.g., a strongly interacting cluster of localized electronic trap states) in the gate dielectric layer would enable observing new effects allowing the enhanced transducing of the signal coming from the target analyte due to the activation of several correlated traps simultaneously. Furthermore, the derived in this thesis analytical model for the enhanced STP dynamics in LG NW FETs can be further extended by considering quantum tunneling and strain effects which impact the capture and emission processes in nanoscale devices. The understanding and consideration of such effects may bring insights into the sensitivity enhancement of nanoscale devices exploiting STP. From the STP-based devices characterization point of view, the development and assembling of the **portable noise measurement setup** will allow performing of the low-frequency noise measurements labor-independently. The setup will enable the characterization of nanobiosensors exploiting STP-approach more effectively. We expect that the proposed roadmap of such future investigations will therefore strengthen the novel STP-based biosensing strategy proposed in this work and pave the way for the development of remarkably powerful, highly effective, and commercially-ready **single-trap-based devices** for personalized healthcare services in the nearest future.

APPENDIX A: Si TL NW FETs fabrication protocol

Here we present the final optimized process for the fabrication of **the novel Si Two-Layer NW FET-based biosensors** using CMOS-compatible top-down approach.

#	**Process**	**Parameters and Materials**
1	**Epitaxial growth of doped Si layers**	
	• High-temperature bake	1 min @ 1000 °C in H_2 atmosphere
	• Oxide removal	HF vapor treatment for 2 min
	• Silicon epitaxy	Reduced-Pressure CVD @ 800 °C using Si_2H_6 and B_2H_6 dopant precursors
2	SiO_2 **hard-mask formation**	
	• Full RCA cleaning:	
	▷ Piranha	$H_2O_2 : H_2SO_4 = 2 : 1$ for 10 min $DI\ H_2O$ for 10 min or 14 $M\Omega$ conductivity 1 $\%$ HF for 10 s $DI\ H_2O$ for 10 min or 14 $M\Omega$ conductivity
	▷ SC-1	$NH_4OH : H_2O_2 : DI = 1 : 4 : 20$ for 10 min $DI\ H_2O$ for 10 min or 14 $M\Omega$ conductivity 1 $\%$ HF for 10 s $DI\ H_2O$ for 10 min or 14 $M\Omega$ conductivity
	▷ SC-2	$HCl : H_2O : H_2O_2 = 1 : 20 : 1$ for 10 min $DI\ H_2O$ for 10 min or 14 $M\Omega$ conductivity 1 $\%$ HF for 10 s $DI\ H_2O$ for 10 min or 14 $M\Omega$ conductivity drying with N_2 gun
	• Thermal oxidation	40 min @ 1000 °C for 20 nm SiO_2

3	**Definition of alignment markers**	
	• Applying photoresist:	$\underline{AZ^{\circledR}nLOF\ 2020}$
	▷ Dehydration bake	5 min @ 180 °C
	▷ Adhesion treatment	HMDS @ 130 °C
	▷ Spin-coating	spin-coat approx. $4\ ml$ of $AZ^{\circledR}nLOF$ 2020 @ 4000 rpm with pre-acceleration
	▷ Soft bake	1 min @ 110 °C
	• Exposure	MA-IV @ 40 $mJ \cdot cm^{-2}$ (contact mode)
	• Post-exposure bake	1 min @ 110 °C
	• Development	developer $AZ^{\circledR}MIF$ 326 for 45 s $DI\ H_2O$ for 10 min or 14 $M\Omega$ conductivity drying with N_2 gun
	• Reactive ion etching	O_2 : 30 $sscm$ for 3 s, RF power CHF_3/Ar : $50/50$ $sscm$ for 40 s, RF power SF_6/O_2 : $100/8$ $sscm$ for 21 s, RF power CHF_3/Ar : $50/50$ $sscm$ for 7 min, RF power O_2 : 30 $sscm$ for 3 min, RF + ICP power
	• Cascade cleaning	Acetone for 2 min Isopropanol (IPA) for 1 min drying with N_2 gun
4	**E-beam lithography**	
	• Applying PMMA e-beam resist:	$\underline{AR-P\ 649.04\ K}$
	▷ Dehydration bake	5 min @ 180 °C
	▷ Adhesion treatment	HMDS @ 130 °C
	▷ Spin-coating	spin-coat approx. $4\ ml$ of $AR-P$ 649.04 K with pre-acceleration
	▷ Hard bake	5 min @ 180 °C
	• E-beam writing	270 $\mu C \cdot cm^{-2}$ and 5 nm step @ 500 pA
	• Development	developer $AR-P$ $600-55$ for 1 min IPA for 1 min drying with N_2 gun
	• Reactive ion etching	O_2 : 30 $sscm$ for 3 s, RF power

		CHF_3/Ar : 50/50 $sscm$ for 40 s, RF power
		O_2 : 30 $sscm$ for 2 min, RF + ICP power
5	**Mesa structure definition**	
	• Cascade cleaning	Acetone for 2 min
		IPA for 1 min
		drying with N_2 gun
	• Applying photoresist:	$\underline{AZ^{\circledR}5214E}$
	▷ Dehydration bake	5 min @ 180 °C
	▷ Adhesion treatment	HMDS @ 130 °C
	▷ Spin-coating	spin-coat approx. 4 ml of $AZ^{\circledR}5214E$ @ 4000 rpm with pre-acceleration
	▷ Soft bake	1 min @ 110 °C
	• Exposure	MA-IV @ 75 $mJ \cdot cm^{-2}$ (contact mode)
	• Development	developer $AZ^{\circledR}MIF$ 326 for 1 min
		$DI\ H_2O$ for 10 min or 14 $M\Omega$ conductivity
		drying with N_2 gun
	• Reactive ion etching	O_2 : 30 $sscm$ for 3 s, RF power
		CHF_3/Ar : 50/50 $sscm$ for 40 s, RF power
		O_2 : 30 $sscm$ for 3 min, RF + ICP power
6	**Wet etching of NW FET structures**	
	• Strip native oxide	1 % HF for 30 s
		$DI\ H_2O$ rinse for 30 s
	• Anisotropic wet etching	5 % TMAH for 20 s @ 80 °C
		$DI\ H_2O$ for 10 min or 14 $M\Omega$ conductivity
		drying with N_2 gun
7	**Protective oxidation**	
	• Full RCA & Hard mask removal:	
	▷ Piranha	$H_2O_2 : H_2SO_4 = 2 : 1$ for 10 min
		$DI\ H_2O$ for 10 min or 14 $M\Omega$ conductivity
		1 % HF for 3 min
		$DI\ H_2O$ for 10 min or 14 $M\Omega$ conductivity

	▷ SC-1	$NH_4OH : H_2O_2 : DI = 1 : 4 : 20$ for 10 min $DI\ H_2O$ for 10 min or 14 $M\Omega$ conductivity 1 $\%$ HF for 10 s $DI\ H_2O$ for 10 min or 14 $M\Omega$ conductivity
	▷ SC-2	$HCl : H_2O : H_2O_2 = 1 : 20 : 1$ for 10 min $DI\ H_2O$ for 10 min or 14 $M\Omega$ conductivity 1 $\%$ HF for 10 s $DI\ H_2O$ for 10 min or 14 $M\Omega$ conductivity drying with N_2 gun
	• Thermal oxidation	12 min @ 950 °C for 5 nm SiO_2
8	**Source/drain contact implantation**	
	• Applying photoresist:	$\underline{AZ^{\circledR}5214E}$
	▷ Dehydration bake	5 min @ 180 °C
	▷ Adhesion treatment	HMDS @ 130 °C
	▷ Spin-coating	spin-coat approx. 4 ml of $AZ^{\circledR}5214E$ @ 4000 rpm with pre-acceleration
	▷ Soft bake	1 min @ 110 °C
	• Exposure	MA-IV @ 75 $mJ \cdot cm^{-2}$ (contact mode)
	• Development	developer $AZ^{\circledR}MIF$ 326 for 1 min $DI\ H_2O$ for 10 min or 14 $M\Omega$ conductivity drying with N_2 gun
	• Ion implantation:	
	▷ for $p^+ - p - p^+$ FETs	Boron, energy = 6 keV, dose = 1×10^{15} cm^{-2}
	▷ for $n - p - n$ FETs	Arsenic, energy = 8 keV, dose = 5×10^{14} cm^{-2}
	• Acetone cleaning	Acetone: overnight Acetone for 2 min IPA for 1 min, drying with N_2 gun
9	**Post-implantation RTP annealing**	

	• Full RCA cleaning:	
	▷ Piranha	$H_2O_2 : H_2SO_4 = 2 : 1$ for 10 min $DI\ H_2O$ for 10 min or 14 $M\Omega$ conductivity 1 $\%$ HF for 10 s $DI\ H_2O$ for 10 min or 14 $M\Omega$ conductivity
	▷ SC-1	$NH_4OH : H_2O_2 : DI = 1 : 4 : 20$ for 10 min $DI\ H_2O$ for 10 min or 14 $M\Omega$ conductivity 1 $\%$ HF for 10 s $DI\ H_2O$ for 10 min or 14 $M\Omega$ conductivity
	▷ SC-2	$HCl : H_2O : H_2O_2 = 1 : 20 : 1$ for 10 min $DI\ H_2O$ for 10 min or 14 $M\Omega$ conductivity 1 $\%$ HF for 10 s $DI\ H_2O$ for 10 min or 14 $M\Omega$ conductivity drying with N_2 gun
	• RTP annealing of dopants	
	▷ for $p^+ - p - p^+$ FETs	RTP @ 1000 °C for 5 s in N_2 atmosphere
	▷ for $n - p - n$ FETs	RTP @ 950 °C for 30 s in N_2 atmosphere
10	**Gate oxidation**	
	• Strip native oxide	1 $\%$ HF for 1 min $DI\ H_2O$ for 10 min or 14 $M\Omega$ conductivity
	• Thermal oxidation	45 min @ 850 °C for 8 nm SiO_2
11	**Back-gate opening & Strip of gate oxide from mesa pads**	
	• Applying photoresist:	$\underline{AZ^{\circledR}5214E}$
	▷ Dehydration bake	5 min @ 180 °C
	▷ Adhesion treatment	HMDS @ 130 °C
	▷ Spin-coating	spin-coat approx. 4 ml of $AZ^{\circledR}5214E$ @ 4000 rpm with pre-acceleration

	▷ Soft bake	1 min @ 110 °C
	• Exposure	MA-IV @ 75 $mJ \cdot cm^{-2}$ (contact mode)
	• Development	developer $AZ^{\circledR}MIF$ 326 for 1 min $DI\ H_2O$ for 10 min or 14 $M\Omega$ conductivity drying with N_2 gun
	• Hard bake	2 min @ 120 °C
	• Wet chemical etching	BOE ($HF : NH_4F = 1 : 7$ for 2 min $DI\ H_2O$ for 10 min or 14 $M\Omega$ conductivity drying with N_2 gun
	• Resist mask removal	Acetone for 2 min IPA for 1 min drying with N_2 gun
	• Deep Piranha cleaning	$H_2O_2 : H_2SO_4 = 2 : 1$ for 10 min $DI\ H_2O$ for 10 min or 14 $M\Omega$ conductivity
12	**Metallization of contacts**	
	• Applying photoresist:	$AZ^{\circledR}nLOF$ 2020
	▷ Dehydration bake	5 min @ 180 °C
	▷ Adhesion treatment	HMDS @ 130 °C
	▷ Spin-coating	spin-coat approx. 4 ml of $AZ^{\circledR}nLOF$ 2020 @ 4000 rpm with pre-acceleration
	▷ Soft bake	1 min @ 110 °C
	• Exposure	MA-IV @ 40 $mJ \cdot cm^{-2}$ (contact mode)
	• Post-exposure bake	1 min @ 110 °C
	• Development	developer $AZ^{\circledR}MIF$ 326 for 1 min $DI\ H_2O$ for 10 min or 14 $M\Omega$ conductivity drying with N_2 gun
	• Strip native oxide	1 $\%$ HF for 30 s $DI\ H_2O$ for 10 min or 14 $M\Omega$ conductivity

		drying with N_2 gun
	• Metallization	sputtering of 5 nm TiN / 200 nm Al metal stack
	• Lift-off	Acetone: overnight Acetone for 2 min IPA for 1 min drying with N_2 gun
	• Plasma cleaning	O_2 plasma cleaning for 3 min
	• RTP annealing of metal contacts	RTP @ 450 °C for 10 min in forming gas atmosphere $N_2 : H_2 = 5 : 5$
13	**Passivation**	
	• Applying adhesion promoter:	$\underline{VM\ 652}$
	▷ Dehydration bake	30 min @ 180 °C
	▷ Spin-coating	spin-coat approx. 3 ml of VM 652 @ 3000 rpm with pre-acceleration
	▷ Soft bake	1 min @ 110 °C
	• Applying polyimide:	$\underline{PI\ 2545}$
	▷ Spin-coating	spin-coat approx. 10 ml of PI 4525 @ 5000 rpm with pre-acceleration
	▷ Soft bake	6 min @ 140 °C
	• Applying photoresist:	$\underline{AZ^{\circledR}nLOF\ 2020}$
	▷ Spin-coating	spin-coat approx. 4 ml of $AZ^{\circledR}nLOF$ 2020 @ 5000 rpm with pre-acceleration
	▷ Soft bake	1 min @ 110 °C
	• Exposure	MA-IV @ 40 $mJ \cdot cm^{-2}$ (contact mode)
	• Post-exposure bake	1 min @ 110 °C
	• Development	developer $AZ^{\circledR}MIF$ 326 for 30 s $DI\ H_2O$ for 10 min or 14 $M\Omega$ conductivity drying with N_2 gun

	• Resist mask removal	Acetone for 2 min IPA for 1 min drying with N_2 gun
	• Plasma cleaning	O_2 plasma cleaning for 2 min
	• Hard bake in a process furnace	30 min @ 350 °C under N_2 flow
14	**Protective coating and cutting of processed wafers**	
	• Applying PMMA e-beam resist:	$\underline{AR - P\ 649.04\ K}$
	▷ Dehydration bake	5 min @ 180 °C
	▷ Spin-coating	spin-coat approx. 4 ml of $AR - P$ 649.04 K with pre-acceleration
	▷ Soft bake	2 min @ 110 °C
	• Cutting wafers with dicing saw	
	• Chips arranging into boxes	Acetone/IPA cleaning

APPENDIX B: RTS noise simulation procedure

RTS noise was simulated for the system schematically depicted in Figure 7.1(a) with the additional consideration of dielectric polarization noise. A single trap that induces two-level fluctuations of transistor drain current is located at the distance d_{trap} in the front-gate dielectric layer with a thickness of t_{ox}. To evaluate the probabilities of electrons to be captured or emitted to/from the single trap we utilized a method previously described in Ref. [100]. The capture and emission rates were defined using the following formulas:

$$R_c = R_0 \cdot exp\left[-\frac{q}{kT}\gamma(E_{trap} - \alpha V_g)\right] \tag{7.1}$$

$$R_e = R_0 \cdot exp\left[-\frac{q}{kT}(1-\gamma)(E_{trap} - \alpha V_g)\right] \tag{7.2}$$

where q is the elementary charge, T is the absolute temperature, k is the Boltzmann constant, γ is the charge transfer coefficient (please note, in this case γ is not RTS capture rate slope as defined and used in this thesis), E_{trap} is the energy of the trap, V_G is the liquid-gate voltage applied, and α is the ratio between the trap depth, d_{trap} and the dielectric thickness, t_{ox} (see Figure 7.1). The charge transfer coefficient γ is equal to 1 if the emission rate does not depend on the gate voltage applied.

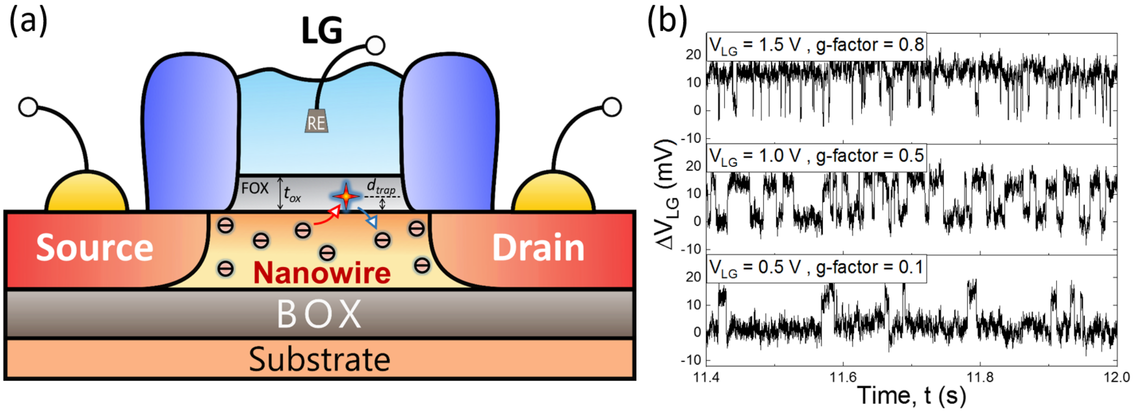


Figure 7.1: (a) Schematic illustration of a LG nanotransistor with a single trap located at d_{trap} in the gate oxide layer with a thickness of t_{ox}; (b) Typical RTS voltage fluctuations simulated at different liquid-gate voltages.

The probability of the electron transfer (capture or emission) at time t since the last transition is calculated using formulas:

$$P_{c,e} = 1 - exp\left[-\frac{t}{\tau_{c,e}}\right] \tag{7.3}$$

The random telegraph process is implemented in the following way. At each time step defined by the time trace sampling frequency (typically $100\ kHz$), the transition probability is calculated for a certain discrete state (emission or capture) and compared to the uniformly generated random number between 0 and 1. If the number is larger than the probability value, the transition event occurs and trap state changes. Otherwise, the trap state is kept unchanged and the transition event does not occur. Such a procedure results in the random fluctuations of the signal between two levels that correspond to the capture and emission states of the single trap. To be able to compare simulation and experimental results, the RTS process is generated as fluctuations referred to the gate of a nanotransistor. Therefore, RTS amplitude is calculated using the formula [12]:

$$\Delta V_G = \frac{q^*}{C_G} \tag{7.4}$$

where q^* is effective trap charge and C_G is a gate capacitance of a nanotransistor.

Dielectric polarization (DP) noise with $1/f$ characteristic behaviour is simulated as a stochastic process by generating first the noise coefficients in spectral space. The phases are simulated randomly, while the amplitude of the coefficients (the amplitude of DP noise) is calculated using Equation 2.15 to follow $1/f$ spectrum in frequency domain. The stochastic signal in the time domain is then obtained via an inverse Fourier transform. Finally, the simulated RTS time traces are gathered by adding DP noise with pure two-level RTS fluctuations with amplitude ΔV_G. For the simulated RTS datasets, the number of events in the given time interval follows Poisson distribution, while the times between the transition events are independent and follow exponential distribution as it is expected for a typical RTS process. Typical RTS time traces generated at different liquid-gate voltages are presented in Figure 7.1(b). The simulated RTS datasets were further used to evaluate g-factor noise. The corresponding results are presented and discussed in Sections 5.2 and 5.3. The programs for simulation of RTS time traces as well as for extraction and analysis of the g-factor noise have been developed and realized using technical computing system *Wolfram Mathematica* (version 12.1).

APPENDIX C: Developed functionalization protocols

To implement a high-selectivity and an exclusive specificity of transistor-based biosensors to the target analytes, the sensing surface of the transducers has to be modified with the special linker molecules and analyte-specific receptors such as antibodies, DNA, aptamers, etc. Typically, such a bio-recognition layer consisting of linker and receptor molecules is assembled onto the sensors' surface using electrostatic or covalent functionalization methods. This step plays a crucial role in determining the performance of the biosensor whose detection principle is based on the "lock and key" model of receptor–analyte interactions. To date, silane-based chemistry is traditionally involved in surface functionalization of Si NWs covered with SiO_2. However, open questions still remain concerning optimal functionalization protocols to facilitate the efficiency of charge transfer within the supramolecular architecture of the bio-recognition layer and thus to improve the signal-to-noise ratio of such Si NW FET-based biosensors. Below, we describe the developed functionalization protocols which allow robust and uniform covalent functionalization of the receptor molecules onto the SiO_2 surface of the fabricated sensors.

cTnI-specific aptamers functionalization protocol

To selectively detect cardiac troponin I proteins, the fabricated NW FET structures were functionalized with novel dibenzocyclooctyne (DBCO)-linked troponin-specific aptamers. The ss-DNA aptamers were specifically designed and synthesized in collaboration with *Dr. Marcus Menger* (*Fraunhofer Institute for Cell Therapy and Immunology, Germany*). The functionalization protocol was developed with the help of *MSc. Dmytro Yehorov* and *Dr. Jie Li*. The main functionalization steps are schematically shown in Figure 7.2. The functionalization procedure is the following:

1. **Cleaning and surface activation.** Before the modification of the Si NW structures, the devices are cleaned with pure ethanol for $1\ min$ and thoroughly dried using N_2 flowing gas. Then, the surface of the nanowires is activated using oxygen plasma ($0.8\ mbar$, $80\ W$) for $3\ min$ to make it more hydrophilic with hydroxyl groups terminating SiO_2.

2. **Immobilization of azide-terminated linkers.** The chips with nanowire structures are then immersed for $1\ hour$ in (3-azidopropyl)triethoxysilane solution, which is diluted in 100%-ethanol solution. After that, the devices are thoroughly rinsed with $1\ M$ acetic acid, sonicated for $5\ min$ in a pure ethanol solution, dried with flowing nitrogen gas, and annealed for $10\ min$ at $120°C$. Such a procedure results in a self-assembled uniform monolayer of azide-terminated linkers on the nanowire surface.

3. **DBCO-linked troponin-specific aptamers.** Nanowire devices are then immersed for $2\,hours$ in the PBS buffer solution $(10\,mM, pH = 7.4)$ containing $1\mu g/ml$ concentration of troponin-specific aptamers modified with the dibenzocyclooctyne (DBCO) terminals to immobilize the aptamers on the NW surface. It should be noted that this novel DBCO surface functionalization technique performed under physiological conditions without cytotoxic $Cu(I)$ catalyst yields the highly selective reaction of DBCO groups with the trimethylsilyl azide-modified NW surface. To remove unlinked aptamer molecules, the devices are washed twice with buffer solution before the sensing experiment.

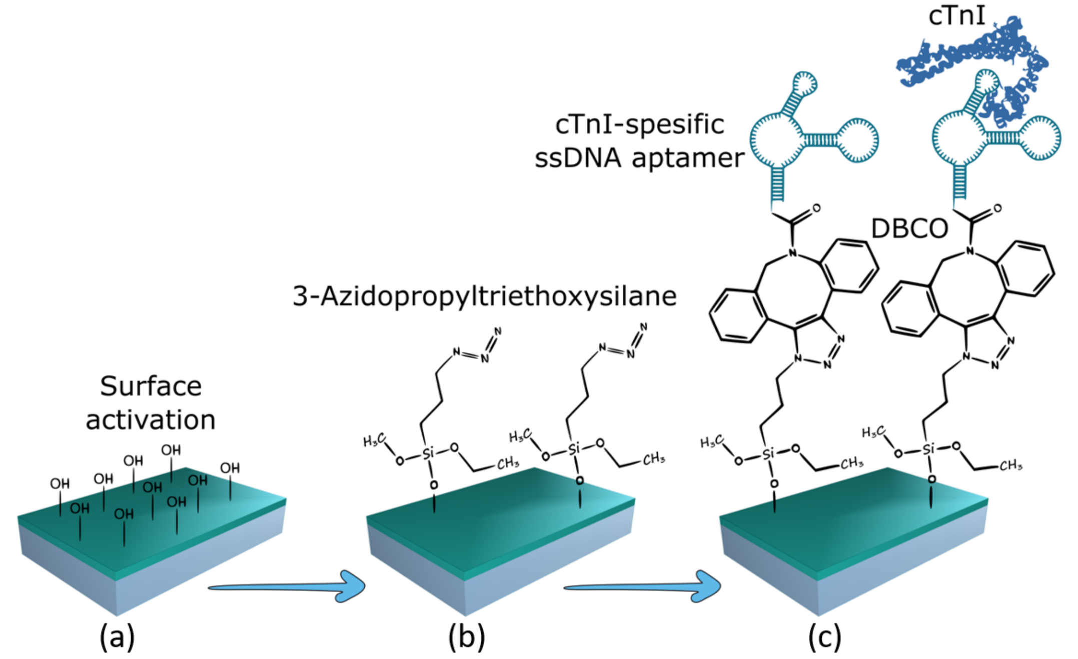


Figure 7.2: Schematic illustration of functionalization protocol for immobilzation of cTnI-specific DBCO-linked aptamers onto SiO_2-covered NW surface: (a) cleaning and plasma activation of SiO_2 surface, (b) immobilization of the azide-terminated linkers and (c) attachment of DBCO-linked troponin-specific aptamers on the NWs.

The successful immobilization of DBCO-linked cTnI-specific aptamers onto the NW surface has been confirmed by X-ray photoelectron spectroscopy measurements and validated during performed biosensing experiments described in this thesis. Thus, the developed functionalization protocol allows fast, non-toxic, and robust immobilization of cTnI-specific receptor molecules onto NW biosensors aiming to detect low concentrations of cTnI proteins.

Anti-CRP antibodies functionalization protocol

The functionalization procedure of the NW sensors with anti-CRP antibodies consists of the following steps:

1. **Cleaning and surface activation.** Firstly, the devices are cleaned and plasma-activated in the same way as described in the protocol above.
2. **APTES silanization.** The nanostructures are functionalized with (3-aminopropyl) - triethoxysilane (APTES) molecules by deposition from the gas phase in a desiccator (2 $hours$ at 5 $mbar$ pressure). The process is performed in an argon atmosphere inside a glove box. To remove unreacted APTES molecules, the devices are rinsed several times with pure ethanol and dried using nitrogen gas flow. Then, the devices are annealed for 5 min at $110°C$ to improve the bonding strength of APTES on the nanowire surface.

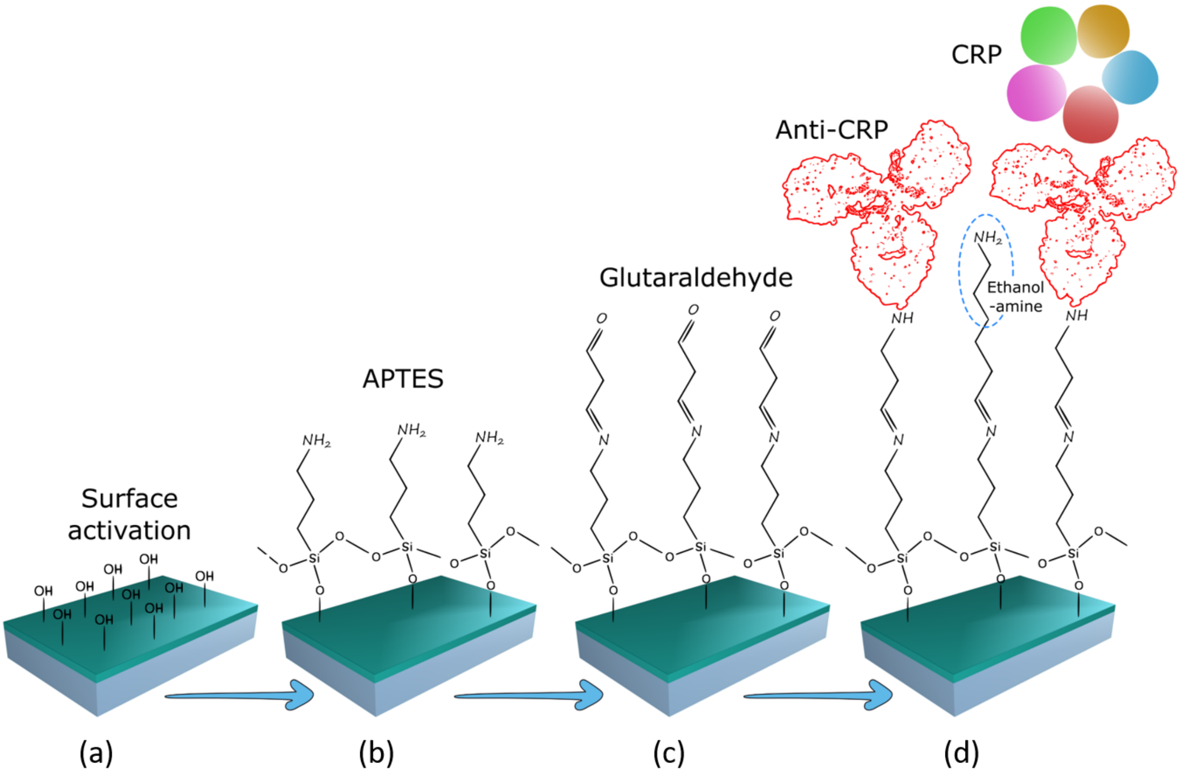


Figure 7.3: Schematic representation of CRP functionalization protocol: (a) cleaning and plasma activation of SiO_2-covered samples, (b) surface treatment with APTES molecules, (c) immobilization of the glutaraldehyde linkers and (d) anti-CRP antibodies to specifically detect CRP antigens.

3. **Treatment with glutaraldehyde.** The amine-terminated surface of the nanowires is exposed to $2.5\%-$glutaraldehyde solution for 1 $hour$ at room temperature.

4. **Immobilization of anti-CRP antibodies.** Finally, monoclonal anti-CRP antibodies are immobilized on the surface of the nanostructures and incubated for 2 $hours$ at room temperature.

5. **Ethanolamine blocking.** To passivate unreacted aldehyde groups on the nanowire surface and prevent nonspecific bindings, devices are thoroughly rinsed with 5%-ethanolamine solution. Functionalized samples can be stored at $4°C$ and thoroughly washed with the PBS buffer solution before the sensing experiments.

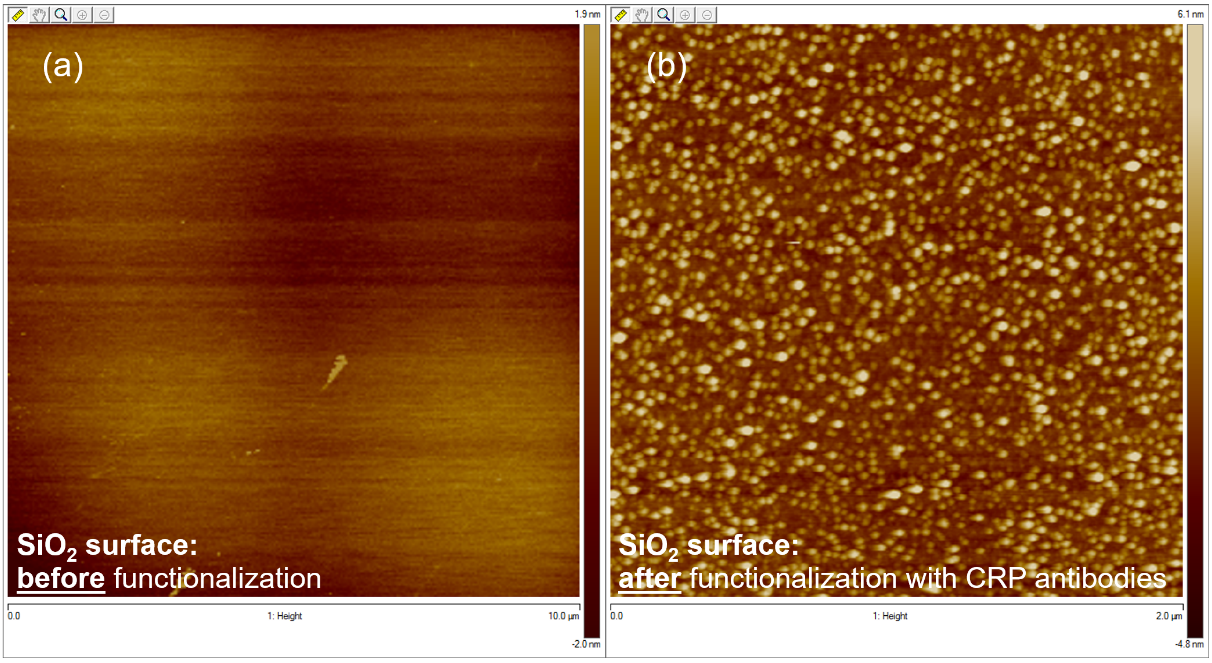


Figure 7.4: Typical AFM micrographs of a SiO_2-covered surface (a) before and (b) functionalization with anti-CRP antibodies. The roughness of the surface increased after functionalization procedure confirming the efficient binding of proteins to the sensing area. The AFM characterization was performed in our group by Dr. Jie Li.

The functionalization steps are schematically shown in Figure 7.3. In order to confirm the efficient attachment of anti-CRP antibodies onto the NW surface covered with SiO_2, a profile imaging using atomic force microscopy (AFM) has been performed. The imaging was conducted using a diving cantilever with silicon probes. Typical 2D AFM micrographs of the SiO_2 surface before and after the functionalization procedure are shown in Figures 7.3(a) and 7.3(b), respectively. As can be seen from Figures 7.4(a), the roughness of the bare SiO_2 surface was around 2 nm. The same sample was then functionalized with anti-CRP antibodies according to the above-described protocol. As can be seen from Figure 7.3(b), after the functionalization, the roughness of the surface has been increased to 6 nm which is comparable with the dimensions of the anti-CRP molecules. This confirms the efficient binding of receptors to the SiO_2 surface.

$A\beta 40$-specific aptamers functionalization protocol

The functionalization procedure of the SiO_2-covered sensors with $A\beta 40$-specific aptamers is the following:

1. **Cleaning and surface activation.** Structures covered with the SiO_2 layer are thoroughly washed with ethanol, further cleaned with isopropanol, and dried using N_2 gas. The devices are then treated with oxygen plasma ($0.8\ mbar$, $50\ W$) for $3\ min$ to activate the SiO_2 surface (see Figure7.5(a)).

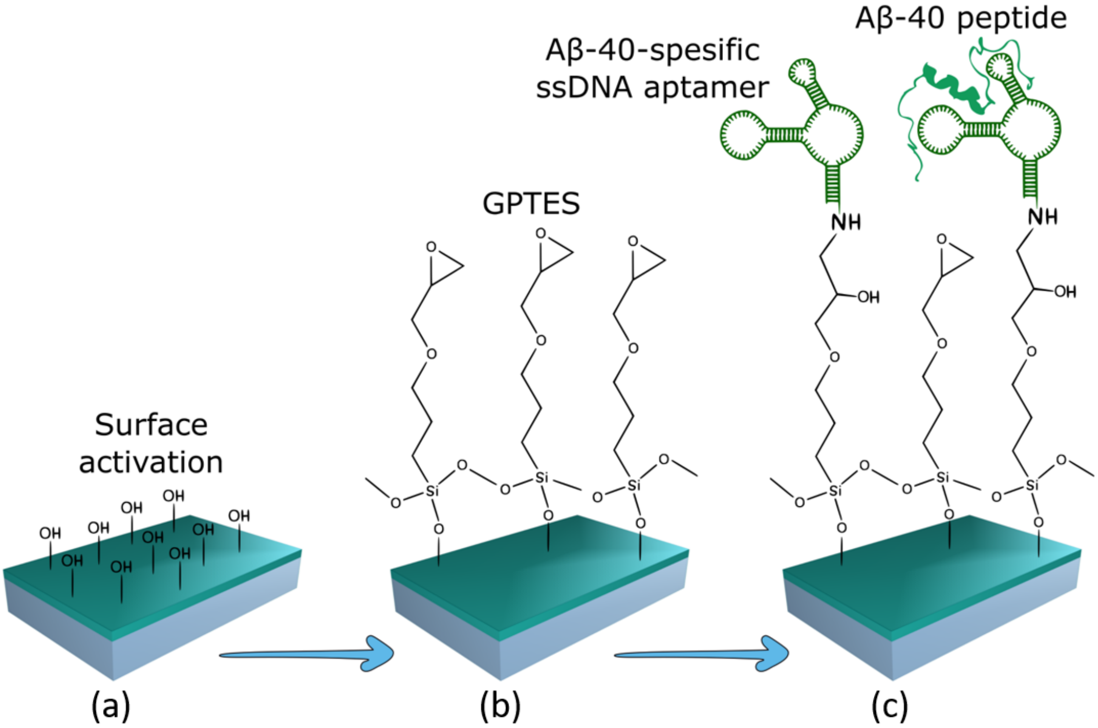


Figure 7.5: Schematic representation of functionalization protocol for immobilzation of $A\beta 40$-specific amino-modified ssDNA aptamers onto SiO_2-covered NW surface: (a) cleaning and plasma activation of NWs, (b) immobilization of the GPTES linkers and (c) anchoring of $A\beta 40$-specific aptamers on the SiO_2 surface.

2. **Immobilization of GPTES linkers.** Immediately after plasma treatment, the structures are salinized for $1\ hour$ in argon atmosphere ($5.2\ mbar$) with 3- glycidyloxypropyltrimethoxysilane (GPTES) molecules (see Figure 7.5(b)) in a desiccator. The devices are thoroughly rinsed with the 100%-ethanol solution to wash away unbound GPTES molecules and annealed at $100°C$ to increase the strength of the molecular bonds.

3. **Immobilization of $A\beta40$-specific amino-modified ssDNA aptamers.** Chips are immersed in a PBS solution containing a $50\ nM$ concentration of $A\beta40$-specific amino-functionalized single-stranded deoxyribonucleic acid (ssDNA) aptamers (see Figure7.5(c)), and incubated for $2\ hours$ at room temperature. To wash away unreacted aptamers, the surface of the sensors is rinsed twice with buffer solution ($10\ mM$, $pH = 7.4$). The devices should be measured immediately after the aptamer immobilization step or can be stored at $4°C$ until use.

The functionalization protocol has been developed with the help of Dr. Hanna Hlukhova. The amino-modified ssDNA aptamers that are capable of selective detection of the target $A\beta40$ sequence were specifically designed and synthesized in a collaboration with Dr. Marcus Menger (*Fraunhofer Institute for Cell Therapy and Immunology, Germany*). The efficiency of the developed protocol has been successfully confirmed by using the electrolyte–insulator–semiconductor as well as nanowire transistor biosensors covered with SiO_2. The detection of ultra-low concentrations of the target peptides has been achieved as demonstrated in this thesis.

Thus, the developed functionalization protocols described here allow fast and reliable assembling of receptor molecules onto the surface of SiO_2-covered biosensors aiming to detect low concentrations of target biomolecules. The experimental results shown in this thesis confirm the validity of the developed and used functionalization protocols.

LIST OF ABBREVIATIONS

AEB additional energy barrier

APTES 3-aminopropyl-triethoxysilane

BOE buffered oxide etch

BOX buried oxide

CMOS complementary metal-oxide-semiconductor

CRP C-reactive protein

cTnI cardiac troponin I

DBCO dibenzocyclooctyne

DUT device under test

ELISA enzyme-linked immunosorbent assay

FET field-effect transistor

FFT Fast Fourier transform

FZJ Forschungszentrum Jülich GmbH

GCE gate-coupling effect

HMDS hexamethyldisilazane

HNF Helmholtz Nanoelectronic Facility

IPA isopropanol

LF low-frequency

LG liquid-gated

MOSFET metal-oxide-semiconductor

NW nanowire

PBS phosphate-buffered saline

PDMS polydimethylsiloxane

PEB post-exposure bake

PECVD plasma-enhanced chemical vapor deposition

PI polyimide

PMMA poly(methyl methacrylate)

POC point-of-care

PSD power spectral density

RIE reactive ion etching

RP-CVD reduced-pressure chemical vapor deposition

SDA simultaneous data acquisition

SELEX systematic evolution of ligands by exponential enrichment

Si Silicon

SIMS secondary ion mass spectrometry

SMU source-measurement unit

SNR signal-to-noise ratio

SOI silicon-on-insulator

SR stochastic resonance

ssDNA single-stranded deoxyribonucleic acid

STP single-trap phenomena

TL two-layer

TMAH tetramethylammonium hydroxide

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PERSONAL PUBLICATION LIST

Peer-Reviewed Journals

[1] **Y. Kutovyi**, N. Boichuk, I. Zadorozhnyi, J. Lie, M. Petrychuk, and S. Vitusevich, “Boosting the Performance of Liquid-Gated Nanotransistor Biosensors Using Single-Trap Phenomena”, **Advanced Electronic Materials**, *2000858*, 1-10 (**2021**) DOI:10.1002/aelm.202000858

[2] **Y. Kutovyi**, I. Madrid, N. Boichuk, K. Soo Hyeon, F. Teruo, J. Laurent, A. Offenhausser, S. Vitusevich and N. Clement, “Single-trap phenomena stochastic switching for noise suppression in nanowire FET biosensors”, **Japanese Journal of Applied Physics**, *60, SBBG03*, 1-5 (**2021**) DOI:10.35848/1347-4065/abdc87

[3] **Y. Kutovyi**, I. Madrid, I. Zadorozhnyi, N. Boichuk, K. Soo Hyeon, F. Teruo, J. Laurent, A. Offenhausser, S. Vitusevich and N. Clement, “Noise suppression beyond the thermal limit with nanotransistor biosensors”, **Nature Scientific Reports**, *10(1)*, 1-11 (**2020**) DOI:10.1038/s41598-020-69493-y

[4] J. Li, **Y. Kutovyi**, I. Zadorozhnyi, N. Boichuk, and S. Vitusevich, “Monitoring of Dynamic Processes during Detection of Cardiac Biomarkers Using Silicon Nanowire Field-Effect Transistors”, **Advanced Materials Interfaces**, *2000508*, 1-11 (**2020**) DOI:10.1002/admi.202000508

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[7] I. Zadorozhnyi, H. Hlukhova, **Y. Kutovyi**, V. Handziuk, N. Naumova, A. Offenhaeusser, and S. Vitusevich, “Towards Pharmacological Treatment Screening of Cardiomyocyte Cells Using Si Nanowire FETs", **Biosensors and Bioelectronics**, *137*, 229-235 (**2019**) DOI:10.1016/j.bios.2019.04.038

[8] M. Petrychuk, I. Zadorozhnyi, **Y. Kutovyi**, S. Karg, H. Riel, and S. Vitusevich, “Noise Spectroscopy to Study the 1D Electron Transport Properties in InAs Nanowires", **Nanotechnology**, *30*(305001) (**2019**) DOI:10.1088/1361-6528/ab175e

[9] **Y. Kutovyi**, I. Zadorozhnyi, V. Handziuk, H. Hlukhova, N. Boichuk, M. Petrychuk, and S. Vitusevich, “Temperature-Dependent Noise and Transport in Silicon Two-Layer Nanowire FETs”, **Physica Status Solidi (B)**, *256*(6) (**2019**) DOI:10.1002/pssb.201800636

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Articles in Conference Journals

[1] **Y. Kutovyi**, I. Zadorozhnyi, S. H. Kim, T. Fujii, A. Offenhäusser, S. Vitusevich, and N. Clement, “Noise in single-trap punctual nanobiosensors", *25th International Conference on Noise and Fluctuations* (**ICNF-2019**) DOI:10.5075/epfl-ICLAB-ICNF-269281

[2] **Y. Kutovyi**, I. Zadorozhnyi, N. Naumova, N. Boichuk, M. Petrychuk, and S. Vitusevich, “Ascorbate detection using single trap phenomena in two-layer Si NW FETs", *25th International Conference on Noise and Fluctuations* (**ICNF-2019**) DOI:10.5075/epfl-ICLAB-ICNF-269314

[3] V. Handziuk, **Y. Kutovyi**, H. Hlukhova, I. Zadorozhnyi, N. Boichuk, M. Petrychuk, and S. Vitusevich, “Nanoimprint Technology for Liquid-Gated Si Nanowire FET Biosensors: Noise Spectroscopy Analysis", *25th International Conference on Noise and Fluctuations* (**ICNF-2019**) DOI:10.5075/epfl-ICLAB-ICNF-269199

[4] N. Boichuk, **Y. Kutovyi**, N. Lobato-Dauzier, A. Genot, T. Fujii, A. Offenhaeusser, S. Vitusevich, and N. Clément, “$1/f$ DNA Hydrogen-Bond Energy Noise”, *25th International Conference on Noise and Fluctuations* (**ICNF-2019**) DOI:10.5075/epfl-ICLAB-ICNF-269285

[5] M. Petrychuk, I. Zadorozhnyi, Y. Kutovyi, S. Karg, H. Riel, and S. Vitusevich, "Lorentzian Noise Approach for 1D Transport Studies", *25th International Conference on Noise and Fluctuations* (**ICNF-2019**) DOI:10.5075/epfl-ICLAB-ICNF-269198

[6] I. Zadorozhnyi, H. Hlukhova, **Y. Kutovyi**, M. Petrychuk, V. Sydoruk, V. Handziuk and S. Vitusevich, "Analysis of charge states in GaN-based nanoribbons using transport and noise studies" *IEEE Conferences: 2017 International Conference on Noise and Fluctuations* (**ICNF-2017**) DOI: 10.1109/ICNF.2017.7985995

[7] **Y. Kutovyi**, I. Zadorozhnyi, H. Hlukhova, M. Petrychuk, and S. Vitusevich, "Low-Frequency Noise in Si NW FET for Electrical Biosensing," *IEEE Conferences: 2017 International Conference on Noise and Fluctuations* (**ICNF-2017**) DOI:10.1109/ICNF.2017.7986024

[8] I. Zadorozhnyi, **Y. Kutovyi**, H. Hlukhova, M. Petrychuk, S. Vitusevich, "Hooge's parameter in Si NW FET with different widths", *IEEE Conferences: 2017 International Conference on Noise and Fluctuations* (**ICNF-2017**) DOI:10.1109/ICNF.2017.7985991

[9] **Y. Kutovyi**, R. Dybovskyi, I. Gavrilchenko, V. Skryshevskii, Y. Milovanov, Y. Skryshevskii, O. Vakhnin, "Surface modification of mesoporous silicon for nanoelectronics applications," *IEEE Conferences: 35th International Conference on Electronics and Nanotechnology* (**ELNANO-2015**) DOI:10.1109/ELNANO.2015.7146836

Conference Proceedings

[1] N. Boichuk, **Y. Kutovyi**, J. Lie, G. Beltramo, V. Weihnacht, and S. Vitusevich, "High-Performance of Liquid-Gated Silicon Nanowire Field-Effect Transistors Covered with Ultrathin Layers of Diamond Like Tetrahedral Amorphous Carbon", *51st IEEE Semiconductor Interface Specialists Conference* (**IEEE SISC 2020**)

[2] **Y. Kutovyi**, I. Madrid, N. Boichuk, K. Soo Hyeon, F. Teruo, J. Laurent, A. Offenhäusser, S. Vitusevich and N. Clement, "Combining Stochastic Resonance and Single-Trap Phenomena for Noise Suppression Beyond the Thermal Limit with Nanotransistor Biosensors", *International Conference on Solid State Devices and Materials 2020* (**SSDM-2020**)

[3] **Y. Kutovyi**, J. Li, I. Zadorozhnyi, V. Handziuk, H. Hlukhova, N. Boichuk, D. Yehorov, and S. Vitusevich, "High-sensitive and fast detection of C-reactive protein and cardiac troponin biomarkers using liquid-gated single silicon nanowire biosensors", *Materials Research Society Fall Meeting 2019* (**MRS-2019**)

[4] H. Hlukhova, **Y. Kutovyi**, M. Menger, A. Offenhäusser, and S. Vitusevich, "Label-Free Aptamer-Based Detection of Amyloid Beta Proteins on SiO_2 Covered Silicon Structures", *Materials Research Society Fall Meeting 2019* (**MRS-2019**)

[5] **Y. Kutovyi**, I. Zadorozhnyi, V. Handziuk, N. Boichuk, H. Hlukhova, M. Petrychuk, and S. Vitusevich, "Single-Electron Dynamics in Liquid-Gated Two-Layer Silicon Nanowire Structures: Towards Biosensing with Enhanced Sensitivity," *International Conference on Solid State Devices and Materials 2018* (**SSDM-2018**)

[6] **Y. Kutovyi**, I. Zadorozhnyi, V. Handziuk, H. Hlukhova, M. Petrychuk, and S. Vitusevich, "Temperature-dependent noise and transport in two-layer silicon nanowire FETs," *34th International Conference on the Physics of Semiconductors 2018* (**ICPS-2018**)

[7] **Y. Kutovyi**, I. Zadorozhnyi, V. Handziuk, H. Hlukhova, M. Petrychuk, and S. Vitusevich, "The impact of biomolecules binding on low-frequency noise in Si NW FET biosensors," *8th International Conference on Unsolved Problems on Noise 2018* (**UPoN-2018**)

[8] M. Petrychuk, I. Zadorozhnyi, **Y. Kutovyi**, S. Karg, H. Riel, and S. Vitusevich, "1D electron transport in InAs nanowires," *8th International Conference on Unsolved Problems on Noise 2018* (**UPoN-2018**)

[9] **Y. Kutovyi**, I. Zadorozhnyi, V. Handziuk, H. Hlukhova, M. Petrychuk, N. Boichuk and S. Vitusevich, "Nanowire field-effect transistor structures for the detection of cardiac biomarkers: troponin and C-reactive protein," *Deutsche Physikalische Gesellschaft Spring Meeting 2018* (**DPG-2018**)

Attended Schools & Invited Talks

[1] ICS-8 Summer School on topic «Bioelectronics: from in vitro to in vivo applications», Kleinwalsertal, Austria, July $7 - 11^{th}$, **2019**. Talk presented: "*FET-based devices for electrical cell recordings*".

[2] "*Nanotransistor biosensors: Single-trap phenomena approach for braking thermal limits*», invited talk at LIMMS/CNRS Seminar, IIS, The University of Tokyo, Japan, January 21^{st}, **2019**

[3] ICS-8 Winter School on topic «State-of-the-art implant technology & in vivo monitoring and stimulation», Kleinwalsertal, Austria, March $17-22^{nd}$, **2018**. Talk presented: "*Spinal cord probes and Implants: Neuroprosthetics for paralysis*".

Awards

[1] *DAAD Research Award 2016-2020*

[2] *Innovation Award of RWTH Aachen University as part of RWTH transparent 2016*