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ORIGINAL RESEARCH

An inertia-emulation-based cooperative control strategy and parameters design for multi-parallel energy storage system in islanded DC microgrids

Gang Lin[1] | Jiayan Liu[1] | Yang Zhou[1] | Yong Li[2] | Christian Rehtanz[1] | Shaoyang Wang[2] | Pengcheng Wang[3] | Wei Zuo[4]

[1]Institute of Energy Systems, Energy Efficiency and Energy Economics, TU Dortmund University, Dortmund, Germany

[2]College of Electrical and Information Engineering, Hunan University, Changsha, China

[3]College of Electrical Engineering, Zhejiang University, Hangzhou, China

[4]College of Electrical Engineering, University of Leeds, Leeds, UK

Correspondence
Gang Lin, Institute of Energy Systems, Energy Efficiency and Energy Economics, TU Dortmund University, Dortmund 44227, Germany.
Email: 1287937851@qq.com

Yong Li, College of Electrical and Information Engineering, Hunan University, Changsha, China.
Email: yongli@hnu.edu.cn

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Abstract

This paper proposes an inertia-emulation-based cooperative control strategy for the multi-parallel energy storage system (ESS) to meet the requirements of state-of-charge (SoC) balance, inertia enhancement and zero-steady-state voltage deviation. The inertia emulation loop (IEL) is constructed by analogy with DC motors to dampen voltage oscillation, while the secondary voltage recovery loop is derived from the circuit equivalence of an inductor to indicate the system stiffness. Moreover, to equalize SoCs of energy storage units (ESUs) dynamically, a SoC self-balance algorithm is developed. The redefined SoC mismatch degree and balance speed adjustment factor k are introduced into the droop resistance, adjusting the SoC self-balance rate and eliminating the SoC deviation among ESUs. The dynamic performance of the SoC self-balance algorithm is analyzed and the small signal model of the DC microgrid (DC-MG) with proposed strategy is established. Based on eigenvalue analysis and step response, the system stability is assessed, and the influence of control parameters on transient characteristics and stability margin is investigated. Considering power constraint, voltage deviation constraint and dynamic stability constraint, the optimal design method of k is given. Finally, simulation and experiment verify that the proposed control, without modifying hardware, performs better dynamic and static characteristics and can equalize SoC among ESUs in charge and discharge mode.

1 | INTRODUCTION

In terms of seamless integration of renewable energy generation and multi-parallel energy storage systems (ESS) into industrial applications, such as electric vehicle (EV) charging stations and smart buildings, dc microgrid (DC-MG) is a promising architecture, due to its high power conversion efficiency, flexibility and reliability, and no concern on power angle stability [1, 2]. Interface converters replace conventional rotating machines and normally adopt droop control and dual loop control with response time in microseconds or milliseconds, and thus cannot provide sufficient damping and inertia for DC-MG. The inherent capacitor inertia is much smaller than rotating inertia, making DC-MG an inertia-less system [3]. During the random variation of load and/or REG, DC voltage fluctuates dramatically, damaging sensitive loads and multi-parallel ESS [4]. Besides, the energy storage units (ESU) forming multi-parallel ESS might be in inappropriate operation mode, such as over-charge/-discharge and state of charge (SoC) imbalance, degrading their lifespans [5]. Hence, the major issues in multi-parallel ESS of DC-MGs are to achieve SoC balance and improve the dynamic voltage stability, which will be solved simultaneously in this article.

Compared with connecting capacitors which bring extra power loss and are restrained by certain application scenarios with limited space, such as ship electric systems, inertia

emulation is a creditable method to maintain the voltage stability. Virtual inertia control (VIC) and its improved control algorithm originally concentrate on AC systems to improve frequency regulation by simulating output characteristics of synchronous generators [3, 6], and only a few studies focus on the VIC application in DC systems to improve the voltage stability [7–12]. VIC for bidirectional grid-connected converter (BGC) is proposed in [7], and thus the DC-MG inertia is enhanced and the voltage fluctuation is restrained by the energy from the utility grid. In [8], virtual synchronous generator control damping dc voltage oscillation is presented, and its working mechanism in different modes is analysed thoroughly. In DC-MG lacking BGC, auxiliary power (i.e. inertia and damping power) alleviating voltage fluctuation is from ESU connecting to DC bus via bidirectional DC converter (Bi-C) [4, 9]. An inertia and damping control is proposed, making the external characteristic of converter consistent with the charge/discharge process of capacitor [8], and based on the DC machine model and its speed regulation theory, a virtual DC machine (VDCM) control is introduced in [4]. Still, the controller design is complicated, increasing the difficulty of its practical application. In [24], power-loop-free VDCM is proposed to eliminate the calculation of torques by using power measurements, reducing required resources for implementation. Different from the above methods realizing inertia emulation by analogy with machine or adding extra inertia loop, inertia response in [10] results from the fast droop-curve swing related to the voltage variation. However, damping improvement is ignored. Reference [11] proposes a VIC method, and a feedback analytical approach is presented to identify the motion of DC voltage intuitively and comprehend the stability principle deeply. In [23], an adaptive coordinated control scheme that can provide adaptive virtual inertia and virtual governor-gain support is proposed to enhance the stability of the networked AC/DC MGs while keeping power sharing among these MGs. The low-frequency oscillation mechanism in DC-MGs is revealed and the potential instability factors are identified in [25] to design a related improved loop. It is worth noting that the SoC balance issue, ignored in [7–11, 23–25], is considered in [12] where SoC is integrated into the droop coefficient of VDCM to enhance inertia and balance SoC simultaneously. VDCM in [12, 13, 24] possesses the same structure as that in [11], but lacks a fast-response inner voltage controller, degrading voltage tracking ability, even worse, bringing negative impacts for stability maybe.

To ensure the voltage stability of DC-MG, the voltage support ability of multi-parallel ESS should be fully utilized [14]. However, SoC imbalance might occur among battery cells or ESUs, reducing the overall performance of multi-parallel ESS. Most studies ignore the voltage support capabilities of ESS to improve system inertia and stability while balancing the SoC, which is another focus of this paper. For instance, a battery management system has been developed for the SoC balancing of battery cells connected in series inside ESU [15]. But, the SoC balancing of ESUs deserves attention to avoid unexpected hazards, for instance, over-heat and explosion. Hierarchical control is presented in [16] to equalize SoC at both cell level and ESU level by its modulation scheme for the duty cycle of switches. Reference [17] adds SoC information into current deviation factor to modify current reference and balance SoC, degrading current regulation ability. The droop coefficient is adjusted by a proportional-integral (PI) controller according to SoC level to achieve SoC balance, but the extra controller complicates the parameter design [18]. The above methods make the control complex and increase their difficulty in practical application. An improved SOC balancing strategy based on low bandwidth communication is proposed in [26] where the SOC balancing efficiency is improved and the current deviation is removed by using the SOC slope-adjusting and current-shifting approaches simultaneously. Besides, SoC information can be incorporated into the droop coefficient in other forms, such as the difference between ESU SoC and the average SoC (SoC_{av}) [5], the degree of SoC unbalance [12], and SoC^n [19, 20], to redistribute power and remove SoC divergence. Solutions have been developed for SoC unbalance, but these methods have theoretical incompleteness, lacking parameter optimization design method considering various constraints for example. Reference [27] proposed a local-distributed and global-decentralized SoC balancing method for hybrid series-parallel ESS to achieve global SoC balancing and power sharing of ESUs. In [28], an adaptive control algorithm is proposed to balance the SOCs for a series-connected battery system using the current-SOC droop concept. Furthermore, the state-of-health status of battery cells is accounted in the SoC balancing method [29]. Few studies describe the association of the SoC balance and inertia enhancement, except [12], but lacking inner voltage controller leads to poor voltage tracking ability. Besides, the optimal selection method of balance speed adjustment factor, considering variable and stability constraints, is less proposed. Therefore, there is no suitable method to simultaneously solve the SoC imbalance and stability problems of multi-parallel ESS.

To address the aforementioned issues, focusing on the SoC self-balance among ESUs and system stability enhancement, this paper proposes an inertia emulation-based cooperative control strategy. The inertia emulation loop (IEL) is derived from the physical model of motors. Moreover, according to the real-time SoC information, SoC-integrated droop resistance is redefined as adaptive droop coefficient, and the SoC self-balance algorithm can dynamically adjust delivered power to eliminate SoC divergence. Compared with integrator-based SoC balance methods, the proposed strategy has better extensibility because of its simpler parameter design and bandwidth coordination. Different from [11–13], the internal dual loop control structure ensures fast and accurate voltage tracking capability. The SVR loop is constructed based on the circuit equivalence of inductor, to reflect the system stiffness and expand the selecting range of k in the scenario of larger ΔSoC. Control principle and implementation, stability analysis of each loop and parameter design considering various constraints are presented in detail. Simulation and hardware in loop (HIL) experiment verify the performance of the proposed control method.

Compared with previous studies that only pay attention to the series-connection structure, ignore the combination of SoC balance and IEL, do not deal with the contradiction between SoC balance speed and system stability, or lack parameter

optimization selection method, an inertia-emulation based cooperative control strategy is proposed in this paper to solve both the SoC imbalance and voltage deviation problems during steady-state operation, and the voltage stability problem caused by inertia-less in the transient process. Besides, the contradiction between SoC balancing speed and maintaining system stability is addressed. System stability and influences of parameters on dynamics are investigated by time-domain modelling and analysis. The major innovation and contributions of this work are

1. A cooperative control strategy is proposed to balance the SoC of the multi-parallel ESS of DC-MGs. The defined SoC mismatch degree and balance speed adjustment factor k are incorporated into the redefined droop resistance by SoC self-balance algorithm to balance SoC dynamically and adjust the balance rate, which is the main innovation different from previous research.
2. The contradiction between SoC balancing speed and maintaining system stability is addressed by the reconstructed SoC-based droop resistance function, which is not considered in previous literatures.
3. The optimal design method of k is given considering variable constraints and dynamic stability constraint, ensuring SoC self-balance algorithm will not affect stability. This optimal design method has not been involved before.
4. IEL is proposed to enable multi-parallel ESS to provide virtual inertia to Bi-C, and to improve the voltage stability. Different from previous inertia control, this IEL is designed based on the detailed DC motor model, giving all the control parameters a clearer physical meaning. And the rated value of output voltage is added into the IEL, thus, the proposed IEL only acts in the transient process with a better control performance and would not affect the static characteristic (i.e. voltage regulation and power sharing).
5. Based on the circuit equivalence of inductors, SVR is constructed to achieve zero steady-state voltage deviation by short-circuiting droop resistor and the system stiffness is improved, which is not involved in previous literatures.

2 | PRINCIPLE OF IEL AND SOC SELF-BALANCE ALGORITHM

2.1 | Circuits of Bi-C and DC motor

The two-port network of Bi-C is shown in Figure 1a. The front end is connected with ESU (battery usually) and the back end is linked to DC bus via DC cable. v_{in} and v_{out} are the input and output voltages of Bi-C; i_b and i_{out} are the input and output currents. L_s, R_s and C_{out} are the filter inductance, resistance, and output capacitor, respectively. The physical model of DC motor is shown in Figure 1b. U_0 is the input voltage of motor and E is armature winding induced potential. R_a is armature winding resistance and R_{rs} is the speed regulating resistance. M is the mechanical inertia of DC motor, representing the role of rotor kinetic energy in the dynamic process. T_m is the load torque and P_m is the introduced electrical power to simulate the mechanical

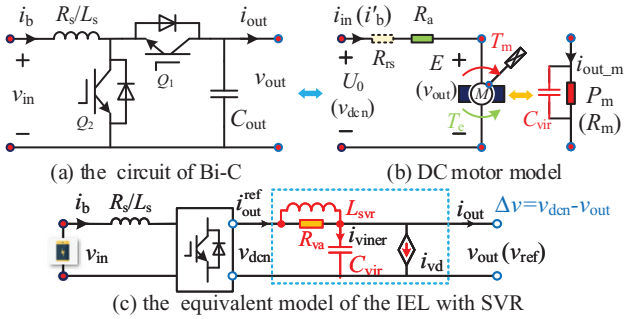


FIGURE 1 Mapping between Bi-C and DC motor, and *RLC* model for virtual inertia

TABLE 1 Analogy between DC motor/inductor and Bi-DC converter

Physical meaning	DC motor and Inductor	*RLC* model of IEL
Moment of inertia	Rotor (M)	ESS (J_{vir})
Damping source	The friction (D_{damp})	i_{vd} (D_d)
Stiffness	L_{svr}	i_{svr}(k_s)
Droop characteristic	R_a+R_{rs}	R_{va}
Input voltage	U_0	v_{dcn}
Output voltage	E	v_{out}
Load	T_m (P_m)	P_{out}
Input current	i_{in}	$i$ref out (i'_b)

power with respect to T_m. At this time, an additional resistance R_m and a virtual capacitor C_{vir} storing inertia energy are added to achieve power balance. The circuit and power balance equations are in (1). The stored kinetic energy can effectively restrain voltage fluctuation caused by power imbalance. With M (C_{vir}) increasing, the rate of voltage change becomes smaller.

$$\begin{cases} E = U_0 - i_{in}\,(R_a + R_{rs})\ \text{(a)} \\ P_e - P_m = \dfrac{\omega M}{C_T \Psi}\dfrac{dE}{dt} \approx \dfrac{\omega_{on} M}{C_T \Psi}\dfrac{dE}{dt} = C_{vir}\dfrac{dE}{dt}\ \text{(b)} \end{cases} \quad (1)$$

From (1a), the DC motor can change its operation point and output power through speed regulation resistance R_{rs} featuring (self-adaptive) droop characteristics, as shown in (2).

$$P_m = E\, i_{out\_m} = U_0^2 R_m / (R_{rs} + R_a + R_m)^2 \quad (2)$$

2.2 | The design of IEL and SVR loop

Based on Figures 1a and 1b, the analogy between DC motor and Bi-C is in Table 1. On this basis, the IEL equation can be obtained as in (3) and (4) and its concept model is in Figure 1c. Its essence is systematic coordination of virtual capacitor, active damping and virtual resistance by exploring the auxiliary power in ESU properly to perform inertia and droop features.

$$i'_{\mathrm{b}} - i_{\mathrm{out}} - i_{\mathrm{vd}} + i_{\mathrm{svr}} \approx \frac{\omega_{\mathrm{on}} M}{v_{\mathrm{dcn}} C_{\mathrm{T}} \Psi} \frac{\mathrm{d}v_{\mathrm{ref}}}{\mathrm{d}t} = \frac{1}{J_{\mathrm{vir}}} \frac{\mathrm{d}\left(v_{\mathrm{ref}} - v_{\mathrm{dcn}}\right)}{\mathrm{d}t} = i_{\mathrm{viner}} \quad (3)$$

$$\begin{cases} i'_{\mathrm{b}} = i_{\mathrm{out}}^{\mathrm{ref}} = \left(v_{\mathrm{dcn}} - v_{\mathrm{out}} + \Delta v_{\mathrm{svr}}\right) / R_{\mathrm{va}} \ (a) \\ i_{\mathrm{vd}} = D_{\mathrm{d}} \left(v_{\mathrm{ref}} - v_{\mathrm{out}}\right) \ (b) \\ i_{\mathrm{svr}} = \left[k_{\mathrm{s}} \int \left(v_{\mathrm{dcn}} - v_{\mathrm{out}}\right) \mathrm{d}t \right] / R_{\mathrm{va}} = \Delta v_{\mathrm{svr}} / R_{\mathrm{va}} \ (c) \end{cases} \quad (4)$$

where v_{dcn} is the rated value of v_{out}. i'_{b} is actually the output reference $i_{\mathrm{ref\,out}}$, which mainly includes i_{vd} (the virtual damping current), i_{viner} (the virtual inertia current), i_{svr} (the virtual inductor current), and i_{out}. The physical significance of i'_{b} is to represent energy supply and mimic i_{in}. v_{ref} is the virtual internal potential emulating E. R_{va} is the virtual droop resistance in series on the Bi-C output side, making the Bi-C present droop feature. Consequently, $i$ref out is obtained by the droop feature, as shown in (4a). J_{vir} and D_{d} are the introduced virtual inertia and damping coefficient, respectively. The introduced J_{vir} can be equivalent to the virtual (static) rotor, virtual capacitor C_{vir} actually, of Bi-C, mitigating voltage oscillation by supplying or absorbing power mismatch. Damping current i_{vd} is added to prevent voltage from deviating its rated value; thus, it is defined in proportional to the voltage deviation as shown in (4b). i_{vd} is provided till the voltage returns to its reference value.

Based on the circuit equivalence that inductors behave as short circuits at a long-time limit while open circuits at a short-time limit, virtual-inductor-based SVR is developed as shown in Figure 1c. L_{svr} refers to the virtual inductor. The control law is 4(c) and k_{s} is the stiffness coefficient, revealing the voltage recovery speed. At a long-time limit, the virtual inductor short-circuits R_{va} and i_{out} are transferred from R_{va} to L_{svr}, thus the voltage deviation Δv is eliminated. The control diagram is shown in Figure 2a.

It can be observed from Table 1 that the inertia and damping power of Bi-C originate from ESS instead of the rotational kinetic energy. i_{viner} will be produced, when the voltage oscillates, to provide inertia to suppress voltage fluctuation, and more inertia current will be produced if oscillation frequency increases. Note that the oscillation frequency declines as J_{vir} increases in the scenario requiring the same inertia current. i_{vd} is generated when voltage deviates from its reference value, indicating voltage deviation is dependent on D_{d}. In order to attain better performance, larger D_{d}, leading to smaller voltage deviation, is preferred. The proposed strategy enables Bi-C to have inertia and damping features, and (self-adaptive) droop characteristics. Its detailed control diagram is in Figure 2a.

2.3 | Principle of SoC self-balance algorithm

In order to promote SoC equalization, multi-parallel ESS should operate in the manner that the ESS with higher SoC should release more power in discharge mode and absorb less power in charge mode than the one with lower SoC, as illustrated in Table 2. Thus, the $\Delta\mathrm{SoC}_{\mathrm{ij}}$ ($\Delta\mathrm{SoC}_{\mathrm{ij}} = \mathrm{SoC}_{\mathrm{i}} - \mathrm{SoC}_{\mathrm{j}}$) would

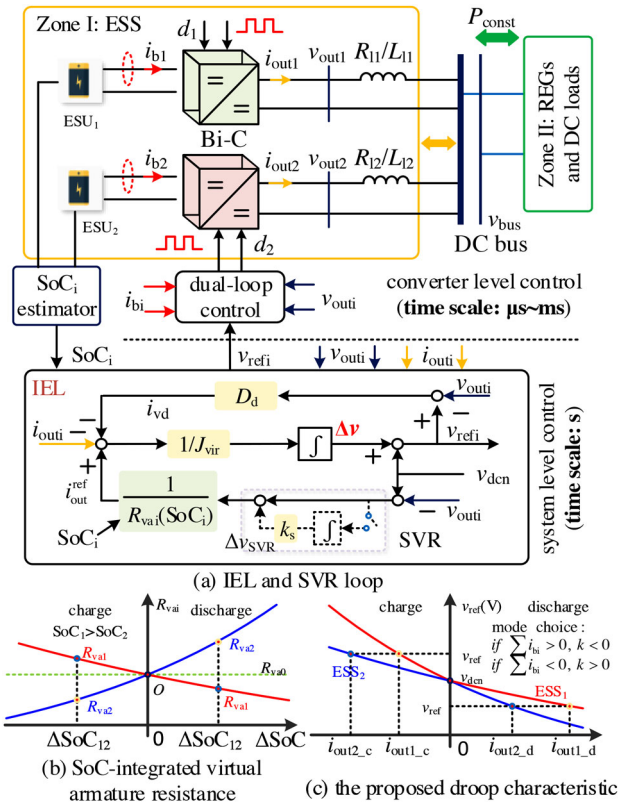


FIGURE 2 The diagram of DC-MG with the proposed control strategy

TABLE 2 Design principle of droop resistance

Mode	RoCoV	Action of ESS	Droop resistance
Charging mode	Negative	Reduce input ↓	Increase ↑
	Positive	Increase input ↑	Reduce ↓
Discharging mode	Negative	Increase output ↑	Reduce ↓
	Positive	Reduce output ↓	Increase ↑

RoCoV, rate of change of voltage.

be removed, avoiding uneven use and expanding their lifespan. Subscripts 'i' and 'j' are the ESU identifier index.

Learning from the speed regulation of DC motor, a SoC-integrated droop resistance $R_{\mathrm{vai}}(\mathrm{SoC_i})$ is redefined in the SoC self-balance algorithm, as shown in (5). Thus, power would be redistributed to balance SoC in charge and discharge modes. R_{va0} is the initial value of R_{vai} and is designed based on traditional droop methods [17]. k is the SoC equalization speed adjustment factor and selected to be negative in discharge mode and positive in charge mode, affecting the SoC balance speed. It is worth noticing that λ_i is a time-varying parameter indicating the SoC mismatch degree among $\mathrm{SoC_i}$ and the $\mathrm{SoC_{av}}$, and also affects the SoC balance speed according to the time-varying $\mathrm{SoC_i}$, which is a novel contribution of this paper. It can be observed from (5) that R_{vai} will return to R_{va0} and power distribution will become equal, as λ_{i} gradually converges to 0. Note that k and λ_{i} affect the balance speed as exponent forms. The

droop control is shown in (6)

$$\begin{cases} R_{\mathrm{vai}} = R_{\mathrm{va0}}\mathrm{SoC}_{\mathrm{i}}^{-k\lambda_{\mathrm{i}}},\ i = 1, 2, \ldots, n \\ \lambda_{\mathrm{i}} = \mathrm{SoC}_{\mathrm{i}} - \mathrm{SoC}_{\mathrm{av}},\quad \mathrm{SoC}_{\mathrm{av}} = \sum_{i=1}^{n} \mathrm{SoC}_{\mathrm{i}}/n \end{cases} \tag{5}$$

$$v_{\mathrm{refi}} = v_{\mathrm{dcn}} - R_{\mathrm{vai}} i_{\mathrm{outi}} \tag{6}$$

3 | DIAGRAM OF DC-MG WITH PROPOSED STRATEGY

Based on (3)–(6), the diagram of DC-MG with the proposed strategy is in Figure 2, including IEL and SVR part, SoC self-balance algorithm and dual loop control. A benchmark DC-MG composed of renewable energy generations, constant power load (CPL) and multi-parallel ESS is considered.

IEL and SVR link: The IEL consists of virtual inertia loop and damping loop, which enable Bi-C to compensate power mismatch by using the energy in ESS, improving the inertia of DC-MG and restraining the voltage fluctuation. The virtual inductor of the SVR loop acts as a short circuit of R_{va} at a steady state, and i_{out} is transmitted through the virtual inductor instead of R_{va}. Hence, Δv is eliminated. SVR loop is activated selectively, which will be explained in Section 5.

SoC self-balance algorithm: SoC evaluator calculates the $\mathrm{SoC_i}$, according to the coulomb counting method, as shown in (7). C_{e} is the capacity of ESU, d_{i} is the duty cycle. SoC should be within the constraint range in (8) to ensure the service life. $\mathrm{SoC_{min}}$ and $\mathrm{SoC_{max}}$ are the minimum and maximum values, respectively. Then a central controller is required for $\mathrm{SoC_{av}}$. Each ESU calculates their R_{vai} according to (5), regulating their delivered power according to the $\mathrm{SoC_i}$ to achieve SoC balance.

$$\mathrm{SoC_i} = \mathrm{SoC_{i,\ t=0}} - \frac{1}{C_{\mathrm{e}}}\int i_{\mathrm{bi}}\mathrm{d}t = \mathrm{SoC_{i,\ t=0}} - \frac{1}{C_{\mathrm{e}}}\int \frac{i_{\mathrm{outi}}}{1-d_{\mathrm{i}}}\mathrm{d}t \tag{7}$$

$$\mathrm{SoC_{min}} \le \mathrm{SoC_i} \le \mathrm{SoC_{max}} \tag{8}$$

For the sake of simple analysis, taking the multi-parallel ESS composed of two ESUs as an example, the relation between R_{vai} and $\Delta\mathrm{SoC_{ij}}$, and the droop characteristic are in Figures 2b and 2c, respectively. In the discharge mode with $k < 0$, $\mathrm{ESU_1}$ with higher $\mathrm{SoC_1}$ would supply more power at $i_{\mathrm{out1\_d}}$ than $\mathrm{ESU_2}$ with lower $\mathrm{SoC_2}$ does at $i_{\mathrm{out2\_d}}$ because of $R_{\mathrm{va1}} < R_{\mathrm{va2}}$. This implies that the SoC values of each ESU will move closer to each other to eliminate $\Delta\mathrm{SoC_{12}}$ till $\lambda_{\mathrm{i}} = 0$. Then, all ESUs would charge or discharge at the same rate, maintaining $\lambda_{\mathrm{i}} = 0$. Consequently, the SoC self-balance algorithm equalizes the SoC gradually and can perform well in SoC-unbalanced and SoC -balanced scenarios.

Dual loop control: Dual loop control consists of voltage loop tracking v_{ref} accurately and current loop controlling the voltage indirectly, improving the control performance.

From Figure 2, the IEL and SoC self-balance algorithm are at the system level because the droop feature is from the redefined R_{va}. Therefore, the bandwidth of each loop can be coordinated better and easier, enhancing the voltage tracking ability. The time scale of system level control is second, while the time scale of converter level control is microsecond or millisecond. $\mathrm{SoC_i}$ need not be updated fast and its update cycle is 0.01 s, due to its slow variation. The impact of communication delay (microseconds usually) is also ignored, because it is much smaller than the inertia emulation part [21].

Normally, the resistance of DC cable is very small in DC-MG; thus, the voltage droop across transmission cable can be ignored as (9) [20]. Consequently, the power sharing relation among ESUs with the same capacities is in (10).

$$v_{\mathrm{out1}} \approx v_{\mathrm{out2}} \approx \ldots \approx v_{\mathrm{outn}} \tag{9}$$

$$\begin{aligned} i_{\mathrm{out1}} : i_{\mathrm{out2}} : \ldots : i_{\mathrm{outn}} &\approx i_{\mathrm{b1}} : i_{\mathrm{b2}} : \ldots : i_{\mathrm{bn}} \\ &\approx \mathrm{SoC}_1^{k\lambda_1} : \mathrm{SoC}_2^{k\lambda_2} : \ldots : \mathrm{SoC}_{\mathrm{n}}^{k\lambda_{\mathrm{n}}} \end{aligned} \tag{10}$$

The above analysis is for ESUs with the same capacity. When the ESU capacities differ significantly, R_{va0} is chosen according to their capacity ratio, ensuring that the charge and discharge powers can be allocated reasonably. Thus, this SoC self-balance algorithm is also suitable for ESUs with different capacities.

4 | DYNAMIC PERFORMANCE AND STABILITY ANALYSIS

Taking multi-parallel ESS with two ESUs as an example, SoC balance speed regulation, stability analysis of SoC self-balance algorithm and small-signal stability analysis of IEL are presented.

4.1 | SoC balance speed adjustment

$$\mathrm{SoC_i} = \mathrm{SoC_{i,\ t=0}} - \frac{i_{\mathrm{load}}}{C_{\mathrm{e}}}\int \mathrm{SoC}_{\mathrm{i}}^{k\lambda_{\mathrm{i}}} / \sum_{i=1}^{n} \mathrm{SoC}_{\mathrm{i}}^{k\lambda_{\mathrm{i}}}\mathrm{d}t \tag{11}$$

Combining (7) and (10), it yields (11). Selecting $C_{\mathrm{e}} = 3$ Ah, $i_{\mathrm{load}} = 6$ A, $\mathrm{SoC_{1,\ t=0}} = 50\%$, $\mathrm{SoC_{2,\ t=0}} = 40\%$ and $R_{\mathrm{va0}} = 2$, the numeric solution of (11) in discharge mode is obtained as in Figure 3a. The delivered power and R_{vai} are shown in Figures 3b and 3c. The related data is in Table 3 when $t = 800$ s. It is shown that, under the same $\Delta\mathrm{SoC_{12}}$, a larger k would enlarge the differences of R_{vai} and i_{outi}, balancing SoC in a shorter time. At $t = 800$ s, $\Delta\mathrm{SoC_{12}}$ is 0.9%, 2.360% and 4.812% when k is –10, –6 and –3, respectively. From Figures 3b and 3c, the delivered power is inversely proportional to R_{vai}. R_{va1} of $\mathrm{ESU_1}$ with higher SoC would be smaller to release more energy. As a result, $\mathrm{SoC_1}$ and $\mathrm{SoC_2}$ balance dynamically, then R_{vai} return to R_{va0}.

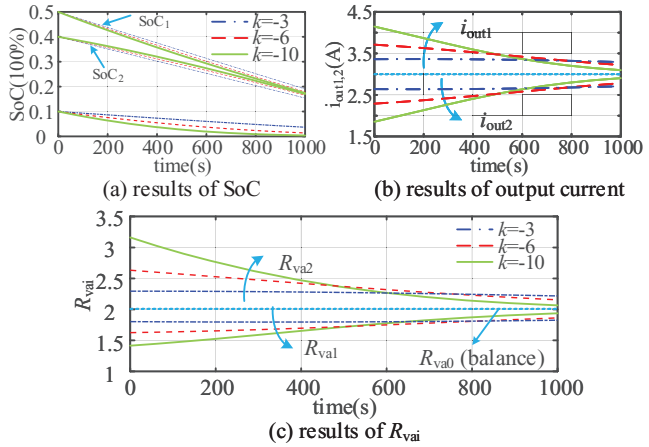


FIGURE 3 SoC balance speed regulation with different k

TABLE 3 Numeric solution of SoC balance regulation when $t = 800$ s

K	$\Delta SoC_{12,\ t=800}$	R_{va1}	R_{va2}	i_{out1}	i_{out2}
–10	0.900%	1.868	2.146	3.208	2.792
–6	2.360%	1.808	2.229	3.313	2.687
–3	4.812%	1.811	2.243	3.320	2.680

4.2 | Stability analysis of the SoC self-balance algorithm

The stability of the SoC self-balance algorithm is evaluated by small signal analysis. Since the bandwidth of dual loop control is much higher than the SoC self-balance algorithm, a unity gain block represents the closed-loop gain of dual loop control. Perturbing (6), there is

$$\frac{-\Delta v_{outi}}{v_{dcn}-v_{outi}}=\frac{-k_{dci}}{i_{outi}}\Delta SoC_i+\frac{\Delta i_{outi}}{i_{outi}},\quad i=1,2 \tag{12}$$

$$k_{dc1}=ki_{out1}\left[(SoC_1-SoC_2)/SoC_1+\ln(SoC_1)\right] \tag{13a}$$

$$k_{dc2}=ki_{out2}\left[(SoC_2-SoC_1)/SoC_2+\ln(SoC_2)\right] \tag{13b}$$

Linearizing (7), it yields (14).

$$\Delta SoC_i=-\frac{\Delta i_{bi}}{sC_e}=-\frac{v_{outi}}{sv_{bi}C_e}\Delta i_{outi}=-\frac{\Delta i_{outi}}{sC_e'} \tag{14}$$

Combining (11) and (14), (15) and (16) can be obtained. For zone II, the simplified model is shown in (17). Based on KCL, the power balance equation is derived in (18).

$$\Delta i_{out1}=-2si_{out1}C_e'\Delta v_{out1}/\left[(v_{dcn}-v_{out1})\left(2sC_e'+k_{dc1}\right)\right] \tag{15}$$

TABLE 4 System parameters of the studied DC-MG

	Items	Value
Zone I	Input voltage v_s	100 V
	Input filter inductor L_s/R_s	5 mH/0.01 Ω
	Capacitance C_{out}	3000 μF
	Line impedance R_{li}/L_{li}	0.01 Ω/0.1 mH
	Initial value of R_{vai}/R_{va0}	2 Ω
	Sample frequency	10 kHz
Zone II	Bus voltage rating v_{dcn}	300 V
	Net power P_{const} (R)	2900 W
	Equivalent load R_{const}	30 Ω
Variable limitation	Δv_{out_max}	10 V
	Δi_{outi_max}	5 A
	Δi_{bi_max}	14 A

$$\Delta i_{out2}=-2si_{out2}C_e'\Delta v_{out2}/\left[(v_{dcn}-v_{out2})\left(2sC_e'+k_{dc2}\right)\right] \tag{16}$$

$$\begin{cases} i_{load}=v_{bus}/R_{load}, \text{discharge mode } (a) \\ i_{load}=P_{const}/v_{bus}, \text{charge mode } (b) \end{cases} \tag{17}$$

$$\sum_{i=1}^{n}\Delta i_{outi}=\Delta i_{load} \tag{18}$$

The characteristic equation can be derived from (15) to (18).

$$As^2+Bs+C=0 \tag{19}$$

$$\begin{cases} A=4\cdot C_e'^2\cdot(i_{out1}+i_{out2}+I_{det}) \\ B=2\cdot C_e'\cdot(i_{out1}k_{dc2}+i_{out2}k_{dc1}+I_{det}(k_{dc1}+k_{dc2})) \\ C=k_{dc1}\cdot k_{dc2}\cdot I_{det} \\ I_{det}=(v_{dcn}-v_{outi})/R_{load} \quad \text{discharge mode} \\ I_{det}=P_{const}(v_{dcn}-v_{outi})/v_{bus}^2 \quad \text{charge mode} \end{cases} \tag{20}$$

From (19), the dominant poles of SoC self-balance algorithm with different SoC and exponent k in charge and discharge modes are presented by using the parameters in Table 4, as shown in Figure 4. Usually, the SoC self-balance algorithm is an overdamped system; thus, only one dominant pole is left.

Figures 4a and 4c show the influences of SoC_1 varying from 0.3 to 0.7 with $SoC_2 = 50\%$ and $|k| = 1$ in discharge and charge modes. The increasing of SoC_1 leads to the pole moving away from the imaginary axis first, and then towards the imaginary axis, which indicates that the stability is first improved and then weakened. When the SoC of two ESUs is close, the stability is approximately the strongest. Figures 4b and 4d show the influences of $|k|$ varying from 0.1 to 10 in discharge and charge modes. With the increase of $|k|$, the pole moves away from

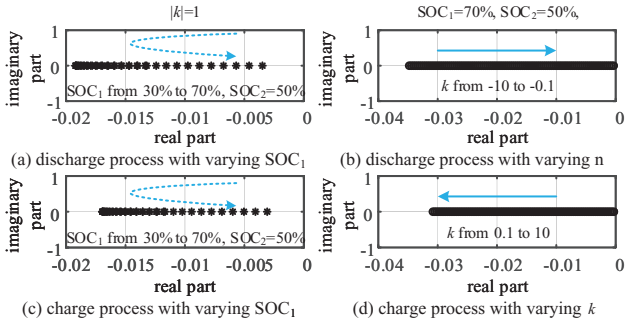


FIGURE 4 The dominant pole distribution of SoC self-balance algorithm

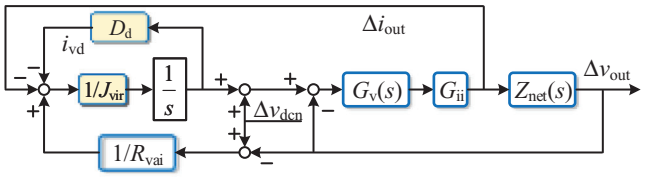


FIGURE 5 Small signal model of DC-MG with the proposed IEL

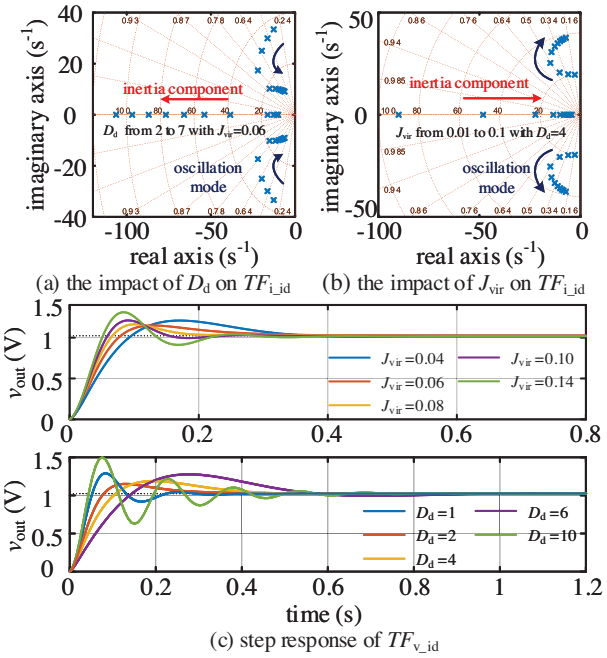


FIGURE 6 Dynamic stability analysis of DC-MG with the IEL

the imaginary axis, improving the stability, because a larger $|k|$ makes SoC balance faster. But the current difference between ESUs is also greater and ESU_1 undertakes most of the load and is closer to its critical state; therefore, an upper limit of $|k|$ is necessary and introduced later. In Figure 4, the pole is always on the left half plane, so stability of SoC self-balance algorithm is guaranteed.

4.3 | Small signal stability analysis of IEL

Ignoring the power loss, (21) is derived from power balance.

$$V_s \Delta i_s = (I_{out} + s \times 2 \times C_{out} V_{out}) \Delta v_{out} + V_{out} \Delta i_{out} \quad (21)$$

Therefore, the relation between Δi_{out} and Δi_b can be obtained when virtual-inductor-based SVR is not connected.

$$G_{ii} = \Delta i_{out} / \Delta i_b = V_s / V_{out} \quad (22)$$

The closed-loop gain of current loop is equivalent to unity gain block. Based on (21), (22) and Figure 2a, the small-signal model of IEL is established in Figure 5. G_v(s) is the voltage PI regulator. $Z_{net}(s)$ is the small-signal impedance of Zone II and lines. The relation between Δv_{out} and Δi_{out} is in (23) and its physical significance is to reflect the dynamic response of v_{out} when i_{out} changes suddenly. The transfer function of Δv_{out} and Δv_{dcn} is in (24), reflecting the voltage tracking ability.

$$TF_{i\_id} = \frac{\Delta v_{out}}{\Delta i_{out}} = \frac{-G_v \times G_{ii} \times Z_{net}}{sJ_{vir} + D_{damp} + G_v \times G_{ii} \times Z_{net}(1/R_{vai} + sJ_{vir})} \quad (23)$$

$$TF_{v\_id} = \frac{\Delta v_{out}}{\Delta v_{dcn}} = \frac{(1/R_{vai} + sJ_{vir}) \times G_v \times G_{ii} \times Z_{net}}{sJ_{vir}(1 + G_v G_{ii} Z_{net}) + D_{damp} + G_v \times G_{ii} + G_v G_{ii} \times Z_{net}/R_{vai}} \quad (24)$$

The pole distribution of $TF_{i\_id}(s)$ and step response of $TF_{v\_id}(s)$, with varying D_d and J_{vir}, are presented, as in Figure 6. From Figures 6a and 6b, remarkably, the DC-MG with IEL can be simplified to a third-order system approximately, including a negative real root (representing the inertia component) and a pair of negative conjugate complex roots (representing low-frequency oscillation mode). In Figure 6a, with D_d increasing from 2 to 7, the poles of oscillation mode move to real axis, and the damping increases first and then decreases. At about $D_d = 4$, the damping is maximum. Besides, the time constant T_{iner} of the inertia component decreases with D_d increasing, indicating that system inertia is weakened. The opposite movement trend of poles, with J_{vir} increasing, can be observed in Figure 6b. The damping of oscillation mode is first increased and then decreased, and the poles move away from real axis and oscillation frequency increases. The poles are always on the left half plane, confirming the stability of inertia emulation part.

In Figure 6c, with the increase of J_{vir} and D_d, the oscillation damping first increases and then decreases, which is consistent with Figures 6a and 6b.

5 | PARAMETERS DESIGN GUIDANCE

In the SoC self-balance algorithm, the exponent k changes the SoC balance speed by adjusting the power allocation. In this

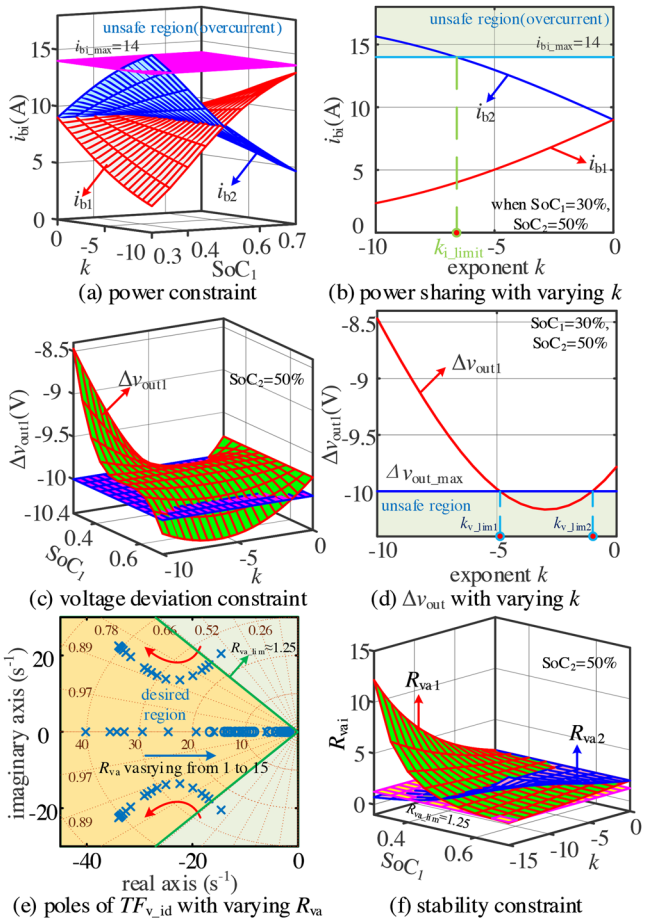


FIGURE 7 Different constraints for exponent k

process, R_{vai} will be dynamically adjusted according to k and SoC, which would affect i_{outi}, v_{outi} and transient performance. Therefore, power constraint, voltage constraint and dynamic stability constraint should be considered while selecting k. Two ESUs in discharge mode are taken as an example. SoC$_1$ changes from 30% to 70% and $|k|$ changes from 0 to 10 with SoC$_2$ = 50%.

5.1 | Power constraint

The sharing of P_{const} can be derived from (10), as shown in (25), which is not only related to k but also related to the ΔSoC_{ij} of ESU. The output/injected current of Bi-C and ESU should not exceed their maximum value, that is, i_{outi_max} and i_{bi_max}.

$$\begin{cases} i_{outi} = \left(SoC_i^{k\lambda_i} \Big/ \sum_{i=1}^{n} SoC_i^{k\lambda_i} \right) i_{load} \le i_{outi\_max} \text{ (a)} \\ i_{bi} = \left(SoC_i^{k\lambda_i} \Big/ \sum_{i=1}^{n} SoC_i^{k\lambda_i} \right) \dfrac{v_{outi}}{v_{si}} i_{load} \le i_{bi\_max} \text{ (b)} \end{cases} \tag{25}$$

Figure 7a shows how the power sharing would be affected by SoC$_i$ and k. The larger k, with the same ΔSoC_{ij}, enlarges the power allocation difference between ESUs, which might cause the ESU power to exceed its maximum though balancing SoC faster. The relation between i_{outi} and k, when $\Delta SoC_{12} = -20\%$, is in Figure 7b. It can be found that the power released by ESU$_2$ exceeds its acceptable power rating when k exceeds $k_{i\_limit} \approx 6.5$, degrading its lifespan. Power constraint is an upper limit to k.

5.2 | Voltage deviation constraint

The maximum voltage deviation Δv_{outi} caused by droop feature is another constraint of k. $R_{va0} = 2$ can be obtained from (26). Combining (10) and (25), the quadratic equation of Δv_{outi} can be derived from (4a), as shown in (27). Δv_{outi} can be acquired by solving (27), as shown in (28). The other solution of (27) is rejected because it exceeds v_{dcn}. From (28), Δv_{outi} is affected by SoC$_i$, k and P_{const}, and their relationship is shown in Figure 7c. When $|\Delta SoC_{12}|$ is large, there would be a set of k making v_{outi} exceed its constraint value. Figure 7d shows the relation between Δv_{outi} and k, when $\Delta SoC_{12} = -20\%$. Δv_{outi} would locate in the unsafe region when $k \in [k_{v\_lim1}, k_{v\_lim2}]$, degrading power quality. Therefore, Equation (28) provides a regional limit for k.

$$R_{va0} = \Delta v_{out\_max} / \Delta i_{out\_max} \tag{26}$$

$$\Delta v_{outi} = -\frac{R_{va0} i_{load}}{\sum_{i=1}^{n} SoC_i^{k\lambda_i}} = -\frac{R_{va0}}{\sum_{i=1}^{n} SoC_i^{k\lambda_i}} \frac{P_{const}}{v_{outi} + \Delta v_{outi}} \tag{27}$$

$$|\Delta v_{outi}| = \left| \left(-v_{dcn} + \sqrt{v_{dcn}^2 - 4 \frac{R_{va0} P_{const}}{\sum_{i=1}^{n} SoC_i^{k\lambda_i}}} \right) / 2 \right| \le \Delta v_{out\_max} \tag{28}$$

5.3 | Dynamic stability constraint

As mentioned before, R_{vai} is regarded as a virtual impedance connected in series on the Bi-C output side, affecting the system damping ξ. According to (24), the influence of R_{vai} on the system dynamic characteristics is shown in Figure 7e. Note that ξ first increases and then decreases with R_{vai} increasing. To ensure a good dynamic response, ξ should not be less than 0.707, thus from Figure 7e, R_{vai} should not be less than $R_{va\_lim} = 1.25$. Considering (6), the dynamic stability constraint is in (29).

$$R_{vai} = R_{va0} SoC_i^{-k\lambda_i} \ge R_{va\_lim} \tag{29}$$

Figure 7f shows the influences of SoC and k on R_{vai}. The difference in R_{vai} becomes larger with the increase of k, resulting in larger power allocation difference and accelerating the SoC balance speed. However, the ESU releasing more power is with a smaller R_{vai}, degrading the system damping and deteriorating dynamic characteristic. Hence, the dynamic stability constraint provides an upper limit for k.

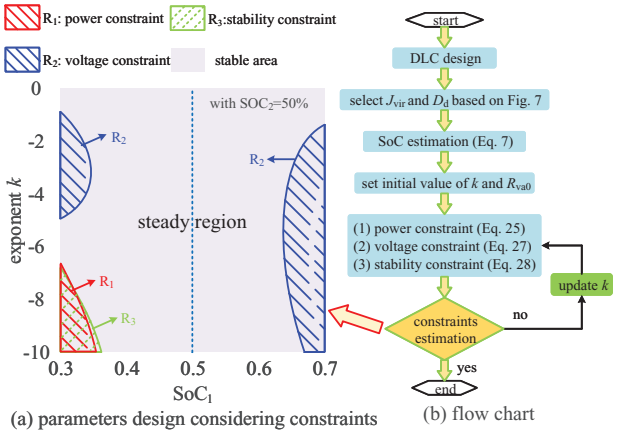


FIGURE 8 Constraint estimation and parameter optimization flow chart

Considering these three constraints, constraints estimation is performed, as shown in Figure 8a. Lower limit of $|k|$ is not required. The power is equally distributed among ESUs when $R_{vai} = R_{va0}$ and $k = 0$. From Figure 7f, the dynamic stability is ensured because R_{va0} is within the acceptable range. Power and voltage deviation constraints would also be obeyed, when ESUs with $R_{vai} = R_{va0}$ supply power within rated range. Hence, the above three constraints are upper and region limitations.

The flow of control parameter design and optimized selection range is shown in Figure 8b. The specific process is as follows:

1. PI controllers of dual-loop control are designed according to the requirements of phase margin and amplitude margin [13].
2. As shown in Figure 6, J_{vir} and D_d are selected based on the standards of dynamic performance (ξ and T_{iner}). Note that the impact of oscillation mode should not be ignored.
3. Set R_{va0} from Equation (26); choose the initial value of k according to the SoC balance speed (Figure 3).
4. Draw Figure 8a based on Equations (25), (28) and (29) for constraint estimation. If these constraints are met, it indicates that the selected k is reasonable, if not, an appropriate k should be chosen according to Figure 8a.

6 | SIMULATION AND EXPERIMENT VERIFICATION

Simulation and dSPACE-based HIL experiment is conducted to validate the effectiveness of the proposed control strategy. The islanded DC-MG system similar to Figure 2 is tested and P_{const} is changed suddenly to imitate the power disturbance. The parameters are in Tables 4 and 5.

6.1 | Simulation result

In order to verify the inertia effect and voltage regulation ability of the proposed strategy, it is compared with the droop control and VDCM control [12, 13]. The results are shown in Figures 9 and 10. The voltage oscillates severely under droop control, indicating that DC-MG lacks damping and inertia.

It can be seen from Figure 9b that the dynamic performance is improved significantly when IEL or VDCM works, and v_{out} can move to steady state without oscillation. Since the proposed

TABLE 5 Control parameters of different control

Control Strategy	Item	Value
Dual loop control	Droop coefficient R_a	2 Ω
	Voltage loop $k_{vp} + k_{vi}/s$	$1 + 10/s$
	Current loop $k_{ip} + k_{ii}/s$	$5 + 1/s$
VDCM control	Droop coefficient R_a	2 Ω
	Virtual armature resistance	1.2 Ω
	Voltage loop $k_{vp} + k_{vi}/s$	$0.1 + 50/s$
	Virtual inertia J_{vir}	2 F
	Virtual damping D_{damp}	10
Inertia emulation loop	Virtual inertia J_{vir}	0.06
	Virtual damping D_d	4
	droop resistance R_{va0}	2 Ω
	Voltage loop $k_{vp} + k_{vi}/s$	$0.1 + 50/s$
	SVR k_s	1
	$SoC_{1,\,t=0}$ / $SoC_{2,\,t=0}$	80%/70%

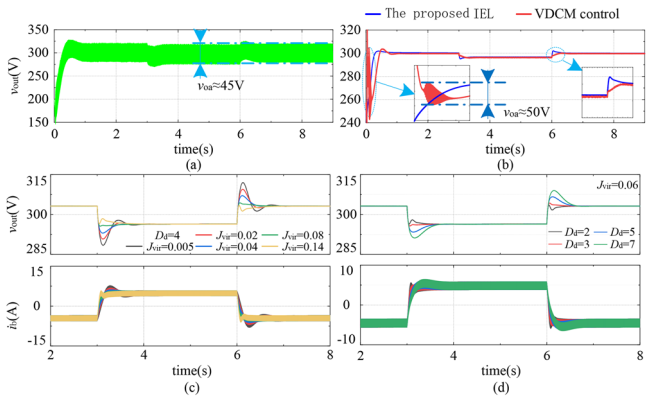


FIGURE 9 Comparison of different control strategies

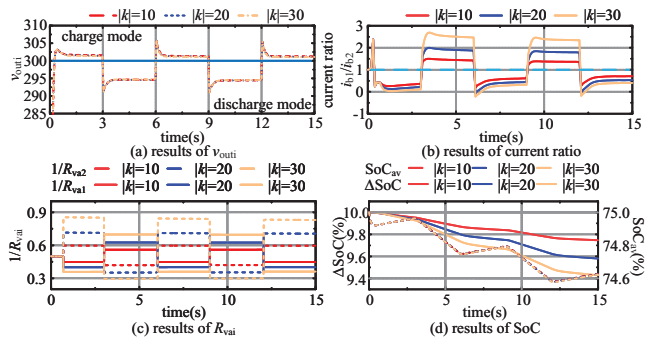


FIGURE 10 The influence of k on SoC balance speed

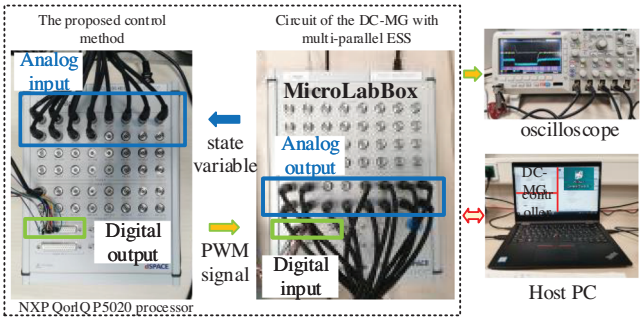


FIGURE 11 The HIL experimental platform

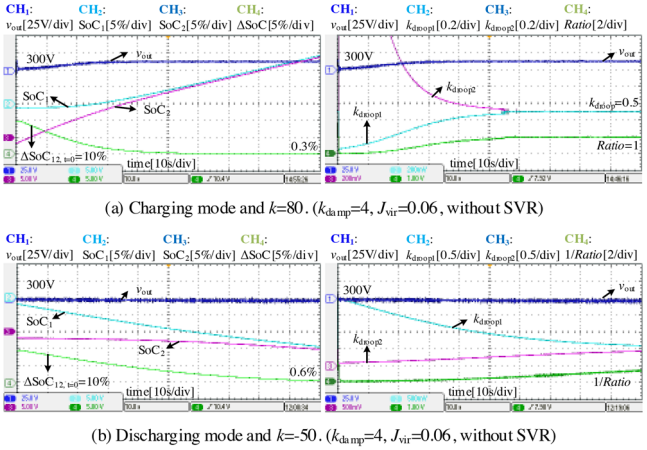


FIGURE 12 The SoC balance in different mode, when $SoC_{1,\,t=0} = 60\%$ and $SoC_{2,\,t=0} = 50\%$

IEL is in the system level control, it does not destroy bandwidth coordination, and thus can eliminate voltage oscillation in the initial stage. The transient behaviour is improved and the voltage-tracking ability at the startup phase is enhanced, compared with droop control and previous VDCM control. The influences of J_{vir} and D_d are shown in Figures 9c and 9d, respectively. When J_{vir} or D_d selects a small value, v_{out} would achieve stability after a short period of oscillation. The oscillation will be better suppressed and a good transient behaviour would be acquired when larger J_{vir} or D_d is chosen. The damping of oscillation mode would decrease with the increase of J_{vir} or D_d, which is consistent with Figure 6. Therefore, ξ and T_{iner} should be considered together when selecting J_{vir} and D_d.

P_{const} and the operation mode are changed every 3 s. When $t \in [0, 0.5\ s]$ (the startup stage), the SoC balance algorithm does not work. After $t = 0.5$ s, the SoC self-balance algorithm is activated. The simulation results are in Figure 10. From Figures 10b and 10c, R_{va1} of ESU_1 with a larger SoC is smaller in discharge mode, and thus the output current is larger. In the charge mode, R_{va1} is larger and the injected current is smaller. As a result, ΔSoC_{12} is decreased to 0. It can be concluded from Figure 10d that, after a same time period, the final ΔSoC_{12} with a higher $|k|$ becomes smaller, indicating that the SoC equalization rate is enhanced. Meanwhile, although different k would change the SoC balance speed, it would hardly bring a difference in SoC_{av}, indicating that changing k will not affect the overall efficiency of ESS.

6.2 | HIL experiment result

The dSPACE-based HIL platform is built, as shown in Figure 11, to verify the performance of the proposed inertia-emulation-based cooperative control strategy under different working conditions which include different operation modes (charging and discharging modes) and their switching, different power levels (light load and heavy load, i.e. changed operation points), the different levels of disturbance power, and the influences of control parameters. The DC-MG is built in the power electronics simulation software MATLAB and simulated by compact prototyping unit MicroLabBox with a time step of 100 μs. The discrete control algorithm is implemented in the NXP QorlQ P5020 processor to generate the gate signals of all IGBTs and the sampling frequency is 10 kHz. The analog signals and digital signals (state variables and pulse width modulation (PWM) signals) are transferred through I/O interfaces and cables.

This dSPACE-based HIL experiment has the following advantages similar to physical experiment platform:

1. Uncertain measurement disturbances in the HIL experiment (similar to sensors);
2. Unknown harmonics caused by capacitors or inductors of the signal transmission cables and MicroLabBox;
3. Digital signal processor, NXP QorlQ P5020, is adopted in this HIL experimental platform and the sampling frequency is 10 Hz. Its high performance, high-efficiency core and integration make it very well suited as a control processor.
4. Considering time delay of discrete control, sampling and signal transmission.

Therefore, based on the above advantages similar to the whole physical experiment, this HIL experiment is sufficient to verify the theoretical analysis in this article.

6.2.1 | Case *I*: Performance of the SoC self-balance algorithm in different operation modes of ESS

Case I validates the effectiveness of the SoC self-balance algorithm when ESS operates in different modes. And the current sharing coefficient $k_{droopi} = 1/R_{vai}$ and current ratio between ESUs $Ratio = i_{s1}/i_{s2}$ are defined.

In Figure 12a, ESS operates in charging mode with $P_s = 5$ kW and $P_{const} = 1$ kW, as well as k is selected as 80. In Figure 12b, ESS operates in discharging mode with $P_s = 5$ kW and $P_{const} = 6$ kW, and k is changed to -50. The initial SoCs of ESUs are 60% and 50%. It can be observed from Figure 12a that ESU_1 with a larger SoC is allocated less power than ESU_2 in the charging mode, because k_{droop1} is smaller than k_{droop2} and

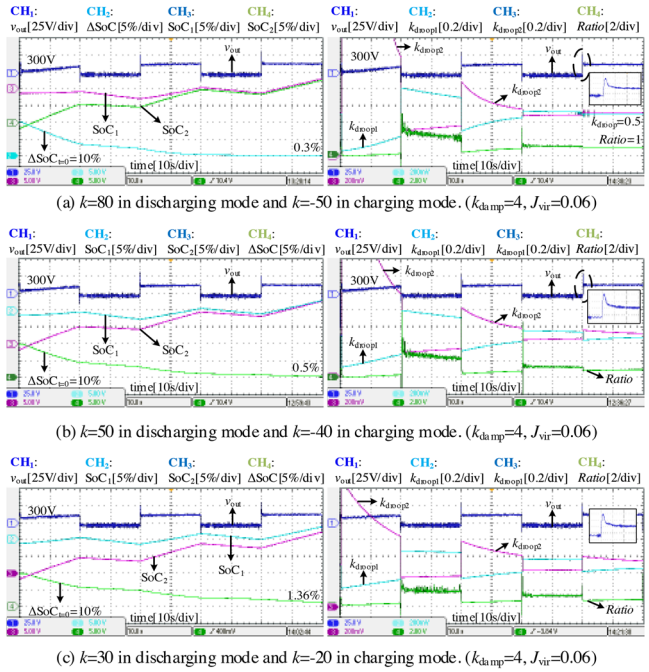


FIGURE 13 The effect of k on the SoC balance speed, when $SoC_{1,\,t=0}$ = 60% and $SoC_{2,\,t=0}$ = 50% (without SVR)

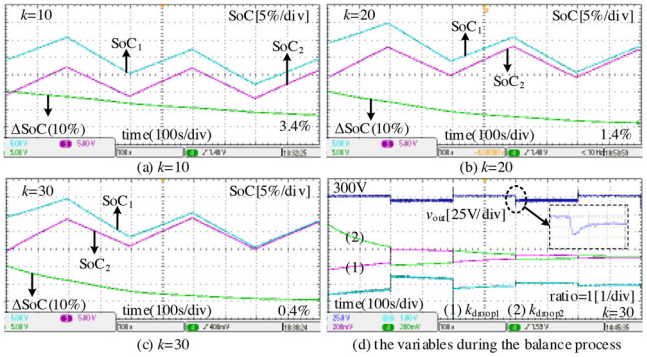


FIGURE 14 The effect of k on the SoC balance when SoC_1 = 80% and SoC_2 = 70%

the injected current is smaller. As a result, SoC_1 and SoC_2 tend to balance, and ΔSoC_{12} drops from 10% to 0.3%. Finally, the delivered current and the current sharing coefficient of ESUs become equal (i.e. *Ratio* = 1).

On the other hand, it can be found from Figure 12b that ESU_1 with a larger SoC delivers more power in the discharging mode due to that k_{droop1} of ESU_1 is larger than k_{droop2}. Thus ΔSoC_{12} converges from 10% to 0.6% and 1/*Ratio* gradually approaches 1. Therefore, the proposed SoC self-balance algorithm can maintain good performance in the dual-quadrant operation.

6.2.2 | Case *II*: Performance of the SoC self-balance algorithm with different k and sudden power fluctuation

In case II, the SoC balance effect of the proposed strategy in case of power fluctuation is validated and the influence of SoC equalization speed adjustment factor k on the convergence speed is investigated. P_s is constant at 5 kW. The initial power of P_{const} is 1 kW, which suddenly increases or decreases by 5 kW every 20 s to change the operation mode of ESS. The initial SoC of ESUs are 60% and 50%. The result is shown in Figure 13. k_{droop1} of ESU_1 with a larger SoC is larger in discharge mode, and thus the output current is larger, while k_{droop1} becomes smaller and the injected current is smaller in the charge mode. As a result, ΔSoC_{12} converges from 10% to 0.3% (i.e. the activation threshold), 0.8% and 1.36%, respectively, as shown in Figure 13. Note that, after ΔSoC_{12} is converged to 0.3%, the SoC self-balance algorithm will stop working, and ESUs will share the power according to the initial value of the droop coefficient $R_{0\,vai}$, that is, k_{droopi} is equal to 0.5 and the current ratio *Ratio* becomes 1, as shown in Figure 13a.

Hence, it can be concluded that the proposed SoC self-balance algorithm is still valid under varying load conditions and can realize the free switch between double-quadrant operations. Besides, it can be observed that faster dynamic power sharing equalization can be achieved with larger $|k|$, which obviously accelerates the SoC equalization speed. This is in accordance with the theoretical analysis.

The experimental waveform with varying k is shown in Figure 14, when P_s = 3 kW and P_{const} = 2 kW. P_{net}(= P_{const} − P_s) is disturbed by 2 kW every 200 s and the operation mode of ESS is thus changed. The initial SoCs of these ESUs are 80% and 70%. In discharge mode, v_{out} of ESU is lower than v_{dcn}, and v_{out} is higher than v_{dcn} in charge mode, as shown in Figures 14a to 14c. k_{droop1} of ESU_1 with a larger SoC is larger than k_{droop2} in discharge mode, and thus the output current is larger. In the charge mode, k_{droop1} of ESU_1 is smaller than k_{droop2} and the injected current is smaller. As a result, ΔSoC_{12} converges to 0. From Figure 14, the final ΔSoC_{12} with a higher $|k|$ becomes smaller after a same time period. $\Delta SoC_{12,\,t=1000}$ is 3.4%, 1.4% and 0.4% when $|k|$ is 10, 20 and 30. The SoC equalization rate is enhanced by a higher $|k|$. These experiment results agree with those of the simulation.

It can be concluded by comparing Figures 13 and 14 that the SoC self-balance algorithm can achieve the dynamic SoC self-balance under varying loading conditions, different power disturbance conditions and various initial SoC of ESUs.

Moreover, the experimental waveform of three ESUs in parallel is shown in Figure 15. P_{net}(=P_{const} − P_s) is disturbed by 2 kW every 20 s and the operation mode of ESS is thus changed. The initial SoCs of these ESUs are 55%, 50% and 45%. Similar to the result in Figure 14 (two ESUs in parallel), the ESUs regulated by the proposed SoC self-balance algorithm also operate in the manner that the ESU with higher SoC should release more power in discharge mode and absorb less power in charge mode than the one with lower SoC. T he SoC unbalance can be removed much faster when choosing a larger $|k|$.

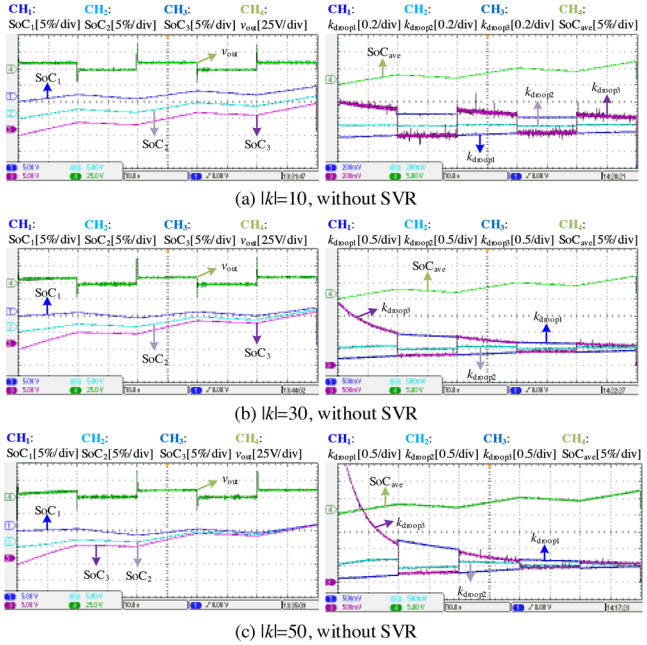


FIGURE 15 The effect of the SoC balance algorithm on multi-parallel ESUs when $SoC_1 = 55\%$, $SoC_2 = 50\%$ and $SoC_3 = 45\%$

6.2.3 | Case *III*: Performance of the proposed SoC self-balance algorithm for ESUs with different capacities

In case III, different ESU capacities condition is considered to test the SoC balance ability of the proposed SoC self-balance algorithm. P_s is constant at 5 kW, and the initial value of P_{const} is 1 kW which increases or decreases by 5 kW every 20 s to change the operation mode of ESS. The initial SoCs are 60% and 50%. The experimental results are shown in Figures 16 and 17. The rated capacities are selected as $ESU_1 = 1.4$ Ah and $ESU_2 = 2.8$ Ah in Figure 16, and $ESU_1 = 2.8$ Ah and $ESU_2 = 1.4$ Ah in Figure 17. Correspondingly, the initial value of the droop coefficient will be selected according to their capacities, that is, $R_{0\,va1} = 4$ and $R_{0\,va2} = 2$ in Figure 16, and $R_{0\,va1} = 2$ and $R_{0\,va2} = 4$ in Figure 17.

It can be concluded from Figures 16 and 17 that the proposed SoC self-balance algorithm still can dynamically balance the SoC and eliminates the SoC difference although the ESUs capacities are different. And similarly, the ΔSoC_{12} converges to 0 much faster with k increasing. After achieving SoC balance, the current ratio *Ratio* becomes 0.5 in Figure 16 ($k_{droop1} = 0.25$ and $k_{droop2} = 0.5$) and 2 in Figure 17 ($k_{droop1} = 0.5$ and $k_{droop2} = 0.25$), respectively, due to that the current is allocated according to the inverse proportion of the initial values of droop coefficients.

6.2.4 | Case *IV*: Performance of IEL

Case IV verifies that the system stability has been significantly improved by the proposed inertia-emulation-based cooperative

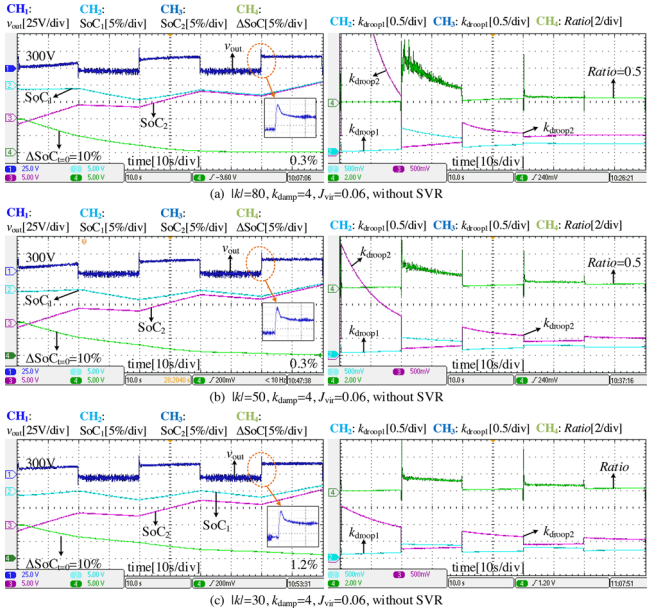


FIGURE 16 Performance of the SoC balance algorithm for $ESU_1 = 1.4$ Ah and $ESU_2 = 2.8$ Ah, when $SoC_{1,\,t=0} = 60\%$ and $SoC_{2,\,t=0} = 50\%$

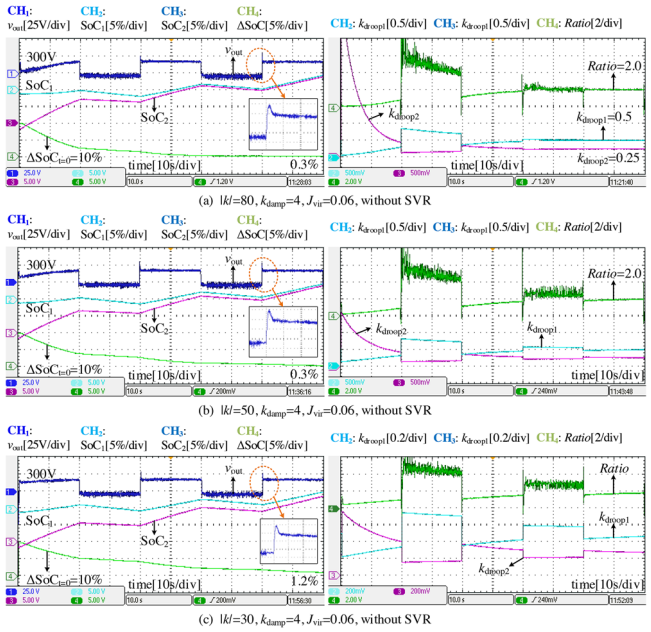


FIGURE 17 Performance of the SoC balance algorithm for $ESU_1 = 2.8$ Ah and $ESU_2 = 1.4$ Ah, when $SoC_{1,\,t=0} = 60\%$ and $SoC_{2,\,t=0} = 50\%$

control strategy while the SoC can be dynamically balanced. P_s is constant at 3 kW, and the initial value of P_{const} is 1 kW which increases or decreases by 5 kW every 4 s. Figures 18 and 19 present the waveform under varying control parameters.

It can be observed from Figure 18 that the IEL controlled Bi-C can be equivalent to a third-order system approximately and the dynamic process can be decomposed into a superposition of a first-order inertia component and an oscillation mode [22]. As J_{vir} increases, the time constant of the inertia component gradually increases, indicating that the system inertia is enhanced.

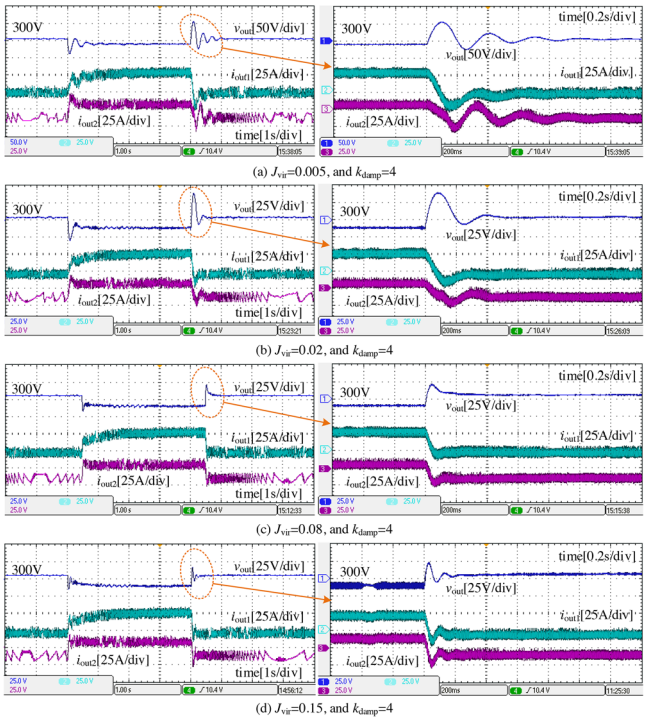


FIGURE 18 The influence of J_{vir}, when ignoring SVR loop

The influence of J_{vir} on the oscillation mode is relatively complicated. The oscillation frequency of oscillation mode gradually increases with J_{vir} increasing, and its oscillation amplitude is well suppressed first, and then increases (compare Figures 18c and 18d), implying that the damping increases first and then decreases. The experiment result of J_{vir} is consistent with the analysis of Figure 6b.

With k_{damp} increasing, a different trend from Figure 18 can be observed in Figure 19 [22]. As k_{damp} increases, the time constant of the inertia component gradually decreases, indicating the reduced inertia. Also, the oscillation frequency of the oscillation mode gradually decreases. In addition, the oscillation amplitude of the oscillation mode first decreases (compare Figures 19a and 19b) and then gradually increases, indicating that the system damping first increases and then decreases. The experiment results of k_{damp} agree with the analysis of Figure 6a.

6.2.5 | Case *V*: Performance of SVR loop

Case V verifies the impact of SVR loop, as shown in Figure 20. P_s is constant at 3 kW. The initial value of P_{const} is 2 kW, which increases or decreases by 2 kW every 4 s. Comparing Figures 20a and 20b, SVR can eliminate steady-state error and ensure better voltage quality. In the transient process, SVR increases the oscillation amplitude, and as k_s increases, the oscillation becomes more severe because of the interaction between SVR and IEL which form a second-order oscillation loop. Thus, k_s should not be too large. In this article, $k_s = 1$.

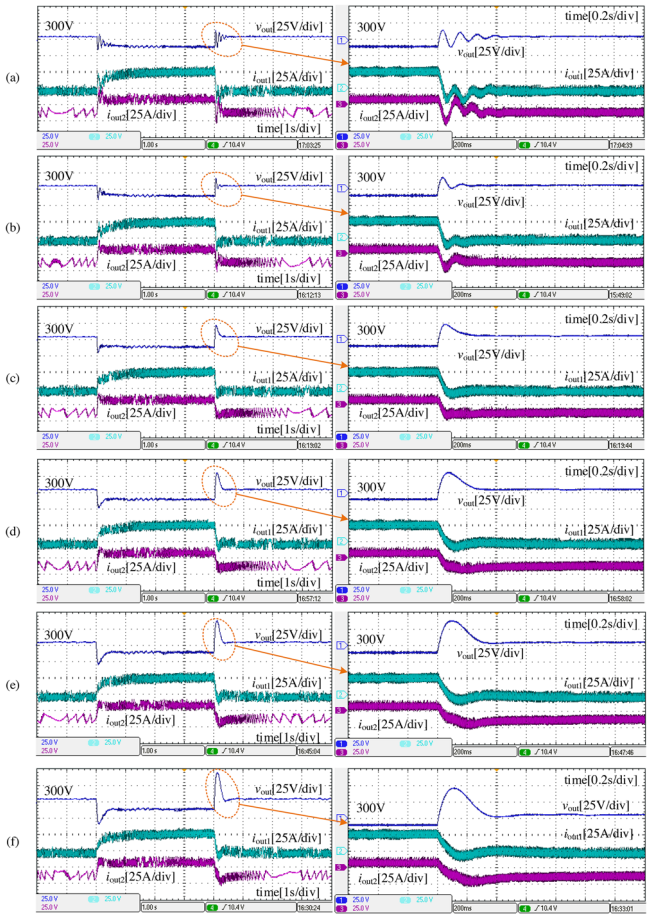
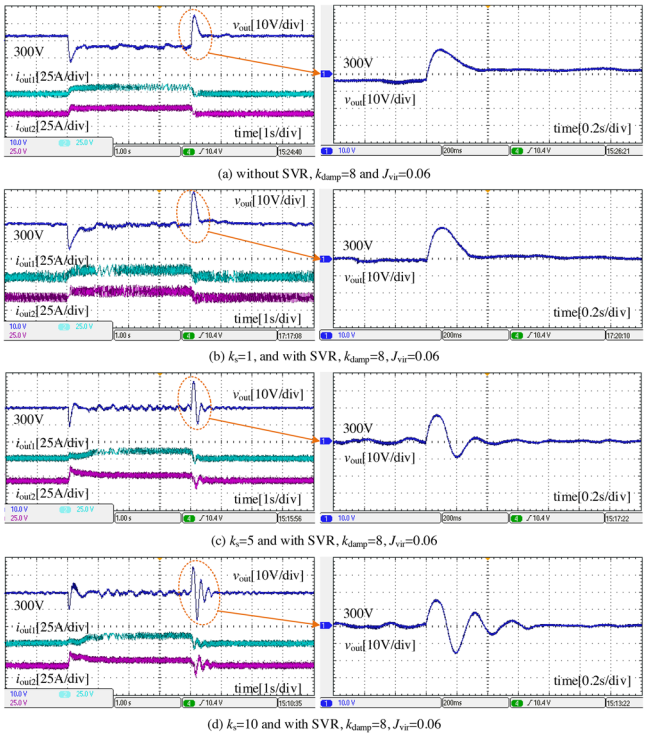


FIGURE 19 The influence of k_{damp}, when ignoring SVR loop. (a) $k_{damp} = 1, J_{vir} = 0.06$. (b) $k_{damp} = 2, J_{vir} = 0.06$. (c) $k_{damp} = 4, J_{vir} = 0.06$. (d) $k_{damp} = 6, J_{vir} = 0.06$. (e) $k_{damp} = 8, J_{vir} = 0.06$. (f) $k_{damp} = 10, J_{vir} = 0.06$

6.2.6 | Case *VI*: Comparison analysis with the double-quadrant SoC-based droop control method

In order to verify the superiority of the proposed inertia-emulation-based cooperative control strategy, it is compared with the double-quadrant SoC-based droop control method of [19, 20]. Note that the control effect of IEL has been compared with the traditional droop control and verified by simulation; thus, only the performance of SoC self-balance algorithm is compared with [19, 20] when the IEL is added into the method of [19, 20] for a fair comparison. P_s is constant at 5 kW. The initial value of P_{const} is 1 kW, which increases or decreases by 5 kW every 20 s. The initial SoCs of ESUs are 60% and 50%. The HIL experiment results of these two methods are shown in Figures 21 and 22. It can be concluded that the proposed method can balance the SoC more quickly under the condition of ensuring a smaller voltage deviation.

It can be seen from Figure 21 that although the convergence rate of SoC can be sped up by increasing k, a larger k will also lead to a larger steady-state voltage deviation with the double-quadrant SoC-based droop control method. By contrast, it can be observed from Figure 22 that the proposed SoC self-balance algorithm can not only improve the system



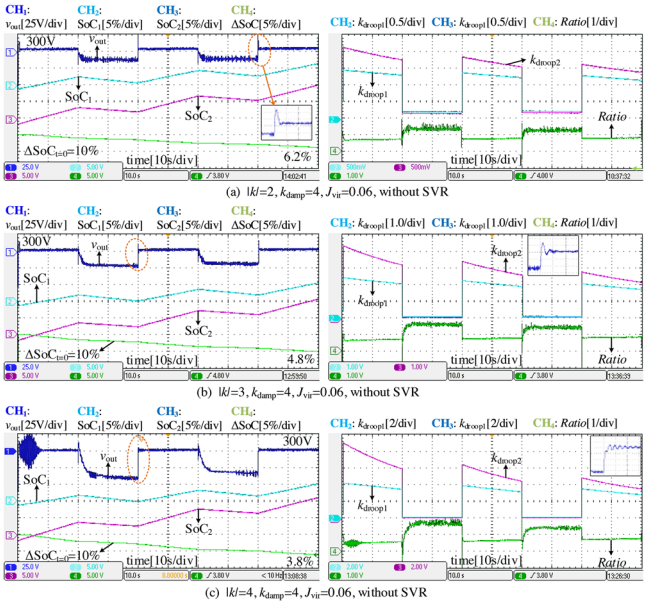
(a) without SVR, k_{damp}=8 and J_{vir}=0.06

(b) k_s=1, and with SVR, k_{damp}=8, J_{vir}=0.06

(c) k_s=5 and with SVR, k_{damp}=8, J_{vir}=0.06

(d) k_s=10 and with SVR, k_{damp}=8, J_{vir}=0.06

FIGURE 20 The influence of SVR loop



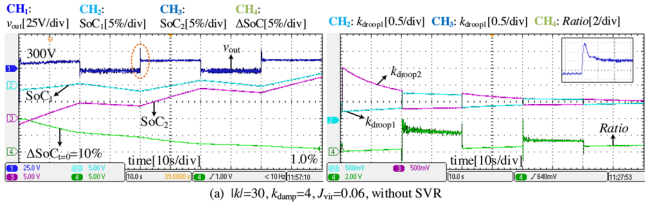
(a) $|k|$=2, k_{damp}=4, J_{vir}=0.06, without SVR

(b) $|k|$=3, k_{damp}=4, J_{vir}=0.06, without SVR

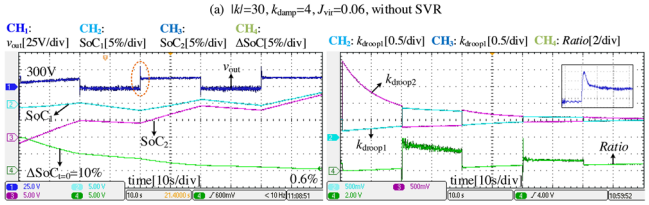
(c) $|k|$=4, k_{damp}=4, J_{vir}=0.06, without SVR

FIGURE 21 Performance of the double-quadrant SoC-based droop control method of [13, 14]

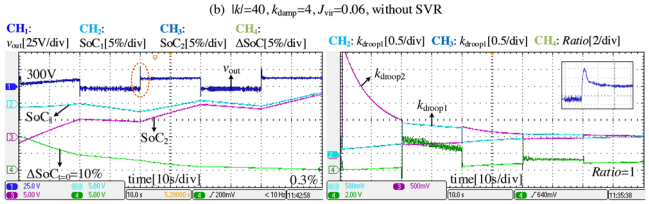
stability, but also realize the dynamic balance of SoC among ESUs faster under the requirement of a smaller steady-state voltage deviation, indicating obvious advantages compared with the double-quadrant SoC-based droop control method. Different from [19, 20], the SoC can be converged more quickly by the proposed inertia-emulation-based cooperative control strategy with a smaller steady-state voltage deviation. Besides,



(a) $|k|$=30, k_{damp}=4, J_{vir}=0.06, without SVR



(b) $|k|$=40, k_{damp}=4, J_{vir}=0.06, without SVR



(c) $|k|$=50, k_{damp}=4, J_{vir}=0.06, without SVR

FIGURE 22 Performance of the proposed inertia-emulation-based cooperative control strategy

the SVR loop can be activated to achieve secondary voltage recovery, when a larger value of k, which might cause a larger voltage deviation, is necessary to balance the SoC quickly. The combination of SoC balance, secondary voltage management and dynamic stability improvement is realized by the proposed inertia-emulation-based cooperative control strategy.

7 | CONCLUSION

An inertia-emulation-based cooperative control strategy is proposed to address the SoC imbalance and voltage deviation problem during steady-state operation and the voltage stability problem caused by inertia-less in the transient process in multi-parallel ESS of DC-MGs, which includes SoC self-balance algorithm, IEL, and virtual-inductor-based SVR loop. Different from previous work, the combination of SoC balance and inertia enhancement is realized, the contradiction between SoC balance speed and system stability is solved and the corresponding optimal parameter selection method is given in this paper.

Specifically, SoC mismatch degree is defined and the power distribution is regulated by integrating this SoC mismatch degree into virtual droop resistance to achieve dynamic SoC balance. Thus, the contradiction between SoC balancing speed and maintaining system stability is addressed by this redefined SoC-based droop resistance function. The SoC convergence speed depends on the introduced adjustment factor k. Besides, IEL and SVR loop are developed based on DC motor model and circuit equivalence of inductors, respectively, to improve the dynamic stability and eliminate the steady-state voltage error. The dynamic performance analysis demonstrates that the larger exponent $|k|$ accelerates balance speed. Moreover, SoC self-balance algorithm is a second-order system and the IEL can be simplified to a third-order system. Thus, appropriate J_{vir} and

D_d could be selected based on the requirements of ξ and T_{iner}. The steady region of k is discussed considering the boundaries of various constraints estimation, and the parameter optimal design process is presented.

To validate the correctness of the theoretical analysis, simulation and dSPACE-based HIL experiment are conducted under various working conditions, including different operation modes of ESS and their switching, different power levels (i.e. different operation points), the different levels of disturbance power, and the influences of control parameters. It is demonstrated that fast SoC balance, inertia effect and stiffness can be simultaneously ensured in multi-parallel ESS with the proposed method.

NOMENCLATURE

Subscript 'i' the ESU identifier index, $i = 1, 2, 3,\ldots$

EV	electric vehicle
SoC	state-of-charge
ESU	energy storage unit
ESS	energy storage system
Bi-C	bidirectional DC converter
VIC	virtual inertia control
SVR	secondary voltage recovery
IEL	inertia emulation loop
v_{in} and v_{out}	input and output voltage of Bi-C
d_i	duty cycle of ith Bi-C
i_b and i_{out}	input and output current of Bi-C
v_{dcn}	the rated value of v_{out}
P_{net}	net power of load subsystem (Zone II)
L_s (R_s)	filter inductance and its resistor of Bi-C
C_{out}	output capacitor of Bi-C
ΔSoC_{ij}	SoC difference between ith and jth ESU
R_{vai} (R_{va})	SoC-integrated droop resistance of ith Bi-C
U_0 and E	input voltage and armature winding induced potential of motor
$i_{ref\ out}$	reference value of i_{out}
$R_{0\ vai}$	the initial value of R_{vai}
R_a	armature winding resistance of DC motor
R_{rs}	speed regulating resistance
R_a	armature winding resistance of DC motor
ω (ω_{vir})	angular velocity of (virtual) rotor
C_{Tm} (C_T)	(virtual) torque coefficient
ψ_m (ψ)	(virtual) magnetic flux
T_m (P_m)	load torque (related electrical power)
J_{vir}	virtual inertia coefficient of IEL
D_d	virtual damping coefficient of IEL
k_s	stiffness coefficient of IEL
kSoC	SoCequalization speed adjustment factor
λ_i	time-varying parameter indicating the SoC mismatch degree
C_{vir}	virtual capacitor of IEL
L_{svr}	virtual inductor of IEL
i_{vd}	virtual damping current of IEL
i_{viner}	virtual inertia current of IEL
i_{svr}	virtual inductor current of IEL
'Δ'	the small-signal components
Δv	the voltage deviation from the rated value

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CONFLICT OF INTEREST

We declare that we have no financial and personal relationships with other people or organizations that can inappropriately influence our work, there is no professional or other personal interest of any nature or kind in any product, service and/or company that could be construed as influencing the position presented in, or the review of, the manuscript entitled, 'An Inertia-Emulation based Cooperative Control Strategy and Parameters Design for Multi-parallel ESS in Islanded DC-MG'.

DATA AVAILABILITY STATEMENT

Data sharing not applicable to this article as no datasets were generated or analysed during the current study.

ORCID

Gang Lin https://orcid.org/0000-0002-5214-6891
Yong Li https://orcid.org/0000-0002-1183-5359

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