Alexander Gumprich

Fabrication of Steep Slope Carbon Nanotube Transistors on Novel Multi-Gate Substrates

Cover images:
Boxes, left to right: (1) Micrograph of a buried graphene triple gate sample. (2) SEM Micrograph of a contacted carbon nanotube on a buried multi gate sample. (3) 80-degree SEM Micrograph of a buried graphene heterostructure. (4) Sample with five probing needles on a temperature controlled vacuum chuck.
Background: 3D plot of the dispersion relation of graphene made with open source visualizer 3dmath

Cover design by A. Gumprich

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Fabrication of Steep Slope Carbon Nanotube Transistors on Novel Multi-Gate Substrates

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Vorwort / Preface

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Danke Euch Allen!

Dortmund, im September 2023
Alexander Gumprich

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Glossary (List of Acronyms)

AFM	Atomic Force Microscopy
ALD	Atomic Layer Deposition
BJT	Bipolar Junction Transistor
BMG	Buried Multi Gates
BTBT	Band-to-band Tunneling
BTG	Buried Triple Gates
CAD	Computer Aided Drawing
CG	Center Gate
CIE	Commission Internationale De L'Éclairage
CMP	Chemical Mechanical Polishing
CNT	Carbon Nanotube
CNTFET	Carbon Nanotube Field Effect Transistor
CSAR	Poly(α-Methyl Styrene-Co-α-Chloroacrylate Methylester)
CVD	Chemical Vapor Deposition
DEP	Dielectrophoresis
DIBL	Drain Induced Barrier Lowering
DI-Water	De-Ionized Water
DSG	Drain Side Gate
EBL	Electron Beam Lithography
eDIPS	Enhanced Direct Injection pyrolytic Synthesis
EDX	Energy-dispersive X-ray Spectroscopy
EF-FET	Energy Filtering Field Effect Transistor
FEM	Finite Elements Method
HS	Heterostructure
IC	Integrated Circuit
IPA	Isopropyl Alcohol
IRDS	International Roadmap for Devices and Systems
LOCOS	Local Oxidation Of Silicon
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MWCNT	Multi-walled Carbon Nanotube
NW	Nanowire
OM	Optical Microscope
PECVD	Plasma Enhanced Chemical Vapor Deposition
PMMA	Poly(Methyl Methacrylate)
PVD	Physical Vapor Deposition
RIE	Reactive Ion Etching
rPECVD	Remote Plasma Enhanced Chemical Vapor Deposition
S/D	Source/Drain
SB-MOSFET	Schottky Barrier Metal Oxide Semiconductor Field Effect Transistor
SEM	Scanning Electron Microscope
SOI	Silicon-on-insulator
SSG	Source Side Gate
SST	Steep Slope Transistor

SWCNT	Single-walled Carbon Nanotube
TEM	Transmission Electron Microscope
TFET	Tunnel Field Effect Transistor
TG	Triple Graphene
TGA	Thermo Gravimetric Analysis
TMAH	Tetramethylammonium Hydroxide
TMD	Transition Metal Dichalcogenide
UV-vis-NIR	Ultraviolet Visible Near-infrared Spectroscopy
VLS	Vapor-Liquid-Solid
VLSI	Very Large Scale Integration
VSS	Vapor-Solid-Solid
WCD	Weighted Color Difference
WF	Writefield
WKB	Wentzel-Kramers-Brillouin (approximation)

Glossary (List of Molecular Formulae)

Al	Aluminum
Al_2O_3	Aluminum Oxide
AlGaAs	Aluminum Gallium Arsenide
Au	Gold
C_2H_2	Acetylene
C_2H_4	Ethylene
C_2H_6O	Ethanol
CH_4	Methane
CO	Carbon Monoxide
$FeCl_3$	Iron(III) Chloride
GaAs	Gallium Arsenide
H_2SO_4	Sulfuric Acid
h-BN	Hexagonal Boron Nitride
HF	Hydrofluoric Acid
HNO_3	Nitric Acid
InAs	Indium Arsenide
MoS_2	Molybdenum Disulfide
$MoSe_2$	Molybdenum Diselenide
Si	Silicon
SiO_2	Silicon Dioxide
Ti	Titanium
TiN	Titanium Nitride
WO_3	Tungsten Oxide
WS_2	Tungsten Disulfide
WSe_2	Tungsten Diselenide

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Chapter I
Introduction

The assimilation of electronic circuits into every day life has been shaping modern civilization for many decades. From cars to refrigerators, from dishwashers to smartphones; today, almost everything is electronically enhanced and controlled. Naturally, this technological development did not appear over night. Instead, it is the result of an evolution that has been going on for nearly a century now. The idea to create logic gates from electrical switches is the fundamental base of computing in any manifestation. Although already invented in the 1920s, the field effect transistor had to surrender to electron tubes since actual manufacturing of transistors was not feasible at the time. Electron tubes managed to be used as the switch needed for logic gates for many years until, finally, in 1947 the bipolar junction transistor was invented. From there, the electronic evolution accelerated and instead of bulky tubes, extremely small semiconducting devices took over. Integrated circuits (ICs) containing thousands of transistors became the heart

of electronic computing. Almost two decades later, the field effect transistor eventually made its appearance as a device called the MOSFET which stands for metal-oxide-semiconductor field-effect transistor. The working principle of MOSFETs was the key to integrated low-power complementary logic called CMOS technology. In 1965, it was Gordon Moore, a co-founder of Intel Cooperation, who asserted that the density of transistors in integrated circuits will double every two years, which is commonly known as Moore's Law [1]. His famous prediction turned out to be astonishingly accurate and integration density in modern ICs surpassed 10^{10} transistors/cm^2 as of today [2]. This was possible due to one specific measure: Scaling the geometry of the transistor and the supply voltage by a factor of $1/\alpha$ leads to a higher density of transistors proportional to α^2 and an increase of computing speed proportional to α while the power consumption stays constant. In the meantime, the semiconductor industry has grown in sales from \$1 billion in 1970 to \$20 billion in 1984 and to \$439 billion in 2020 [3]. Over the years, this long-term scaling reached tremendous difficulties due to quantum mechanical and short channel effects, such as drain induced barrier lowering [4]. One approach to mitigate these effects are FinFET devices [5], which were successfully scaled down in the sub 22 nm regime. As of 2022, leading semiconductor companies like IBM introduced 2 nm technology nodes, with typical gate lengths of 14 nm and a 44 nm pitch, extensively pushing the limits for Moore's law. According to the International Roadmap for Devices and Systems (IRDS) the MOSFET has fully reached its limitations [6]. As a replacement for the MOSFET and for silicon based technology in general, the IRDS proposes a number of emerging research devices, such as spin based atomic switches and III-V semiconductor based transistors.

For several years now, the demand for mobile applications has significantly increased and has shifted transistor development towards a point where minimizing power dissipation is more important than maximizing performance. A simple solution is, of course, the further reduction of the supply voltage. However, bound to approximately 1 V in minimum supply voltage due to its limited inverse subthreshold slope, that is 60 $^{\mathrm{mV}}/_{\mathrm{dec}}$, the conventional MOSFET is rendered unfit for future demands in any aspect. In fact, every device which relies on injecting carriers from the thermally broadened Fermi distribution is bound by this so-called thermionic limit. Consequently, novel and redesigned low power devices are subject to industrial and academic research. Here, the key challenge is to maintain sufficient electrostatic gate control for small gate lengths while decreasing the power. The solution is to redesign device architecture inasmuch that the channel material and geometry are fundamentally different from state of the

art transistors [7–9]. Materials like nanowires (NWs) and carbon nanotubes (CNTs) exhibit extraordinary properties and offer new design opportunities [9–11]. These one-dimensional materials enable excellent gate control and extreme scalability. Examples of novel low power devices include steep slope transistors (SSTs), such as tunneling field effect transistors (TFETs) and superlattice energy-filtering transistors (EF-FETs) [12–18].

With awareness of the imminent end of Moore's law, the present thesis addresses the fabrication and characterization of TFET and EF-FET devices using CNTs. Since the operation of such transistors demands very different requirements than MOSFETs, the fabrication process is fundamentally different as well. For instance, a dynamic electrostatic doping landscape is required which becomes feasible by burying multiple gate electrodes into a substrate covered by a dielectric. The fabrication of such substrates is also part of this thesis. The so-called buried triple gate (BTG) architecture uses individually addressable and mutually insulated graphene films as integrated gate electrodes separated by an intermediate dielectric. In another variation - a BTG heterostructure - a combination of thin metal layers and graphene films is deployed. As the name is suggesting, the presented BTG platform only provides three gate electrodes in order to fabricate TFET devices. However, the mentioned EF-FET is based on energy filtering through periodic potentials. Thus, an entire set of electrodes in close proximity is necessary in order to generate this potential pattern. On buried multi gate (BMG) substrates, provided by Thomas Grap of RWTH Aachen University, EF-FETs with carbon nanotubes were manufactured.

Outline

Apart from introduction and summary, the thesis is divided into six main chapters: Chapter II introduces the fundamentals of transistors, from MOSFET technology towards SSTs. Since only CNTs are used for the devices fabricated in this work, chapter III is dedicated entirely to their electrical and structural properties. Besides, the chapter elaborates the synthesis of CNTs and discusses Schottky-barriers at the interfaces. An overview of methodology for the fabrication process is given by chapter IV. Thereafter, the BTG and BMG platforms are introduced in chapter V. Including details about the design, manufacturing, assessment and finite element simulations of the architectures. The presented devices are completed after CNT deposition and the fabrication of contact terminals which is discussed in chapter VI. Finally, chapter VII reports on electrical measurements of the devices to ascertain their characteristics with regard to subthreshold slope and on-/off-currents.

Chapter II

Fundamentals of Nanoscale Transistors

In order to understand steep slope nanoscale transistor research, the fundamentals of MOSFET devices should be discussed beforehand. The **m**etal-**o**xide-**s**emiconductor **f**ield-**e**ffect **t**ransisitor is the best example to show how transistors work and why improvement was feasible. Modern MOSFET architectures have been scaled down to a remarkable extent within only a few nanometers. In this chapter the basic working principle of the MOSFET will be introduced, as well as its properties and limits for modern computing. In addition, this chapter goes beyond MOSFET technologies, presenting alternatives and new developments concerning steep slope transistors and alternative channel materials.

2.1 The MOSFET

Since manufactured for the first time in the 1960s, the MOSFET has become the most commonly produced electronic device ever in history [19]. Simple in structure and inexpensive in production, it can be easily arranged in a complementary architecture. With all that, the MOSFET has a huge advantage over the bipolar junction transistor (BJT) which was state of the art at the time.[1] Progress in research and development eventually made it possible to implement the very large scale integration (VLSI), the foundation of modern electronics. For example, latest high-end microprocessors contain up to 114 billion MOSFETs on a single chip produced within a 5 nm technology node for very short channel lengths [2]. However, to explain how the MOSFET works, it is easier to focus on long channel devices first. Afterwards, section 2.1.3 describes how characteristics change if the channel length is reduced.

2.1.1 Ideal Working Principle

In microprocessors the MOSFET is generally used as a switch, thus being the building block of any logic circuit. In contrast to the BJT, the MOSFET's distinguished feature is the MOS capacitor, which controls the carrier transport. Thus, apart from the displacement current there is no secondary current necessary in order to control the primary current. Instead, the MOSFET can be switched on only by applying a gate voltage causing the capacitor to charge. Eventually, the resulting electric field manipulates a doped channel region at the substrate's surface [20]. For the sake of simplicity, in this section only the n-channel MOSFET will be explained as shown in Figure 2.1.

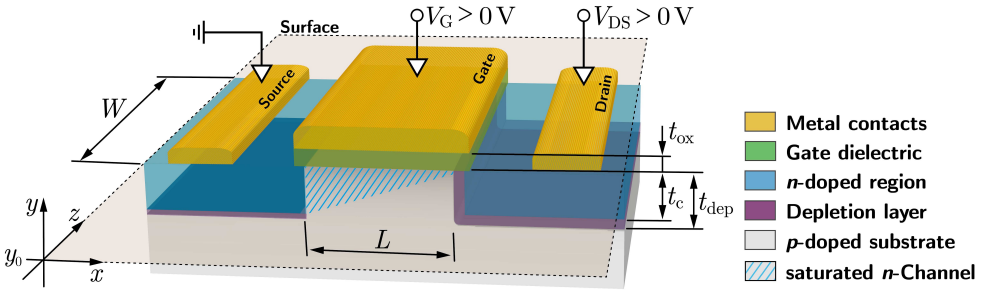

Figure 2.1: Schematics of the n-channel MOSFET: L is the channel length and W is the channel width. The thickness of the gate dielectric is given by t_{ox}. The full thickness of the channel is given by t_{ch}. Disregarding the depletion layer, t_c fits the depth of the n-region. V_G and V_{DS} relates to the source terminal which is usually grounded and/or connected to the bulk substrate.

[1] Although the idea of field effect transistors is actually older, the BJT was the first to replace electron tubes since production of the MOSFET was not feasible at the time.

The highly n-doped source and drain regions are blue colored in the figure. In-between is a weakly p-doped channel region (colored in light gray), thus forming pn-junctions to source and drain. The gate electrode at the top of the channel is insulated by the gate dielectric. Applying a positive gate voltage V_G creates an electrical field in y-direction moving both valence and conduction band towards source level. Therefore, a depletion of positive charge carriers occurs at the p-doped channel surface. Constantly increasing the gate voltage V_G and going above the threshold voltage V_th, moves the conduction band closer and the valence band further apart to the Fermi level. This reduces the barrier for negative charge carriers in the n-regions and leads to the injection of carriers into the channel in such a way that electrons now become majority carriers underneath the gate. An additional sufficiently high voltage V_DS between the source and drain region will move the Fermi level at the drain E_F^D far away from the Fermi level at source E_F^S. The probability for electrons occupying free states in the channel increases drastically. Now, charge carrier transport from source to drain eventually emerges in x-direction. Figure 2.2 shows the band structure depending on the gate and drain-source voltage in an ideal scenario. The characteristics can be best described by the so-called Gradual Channel Approximation [21]: Initially, when the drain-source voltage V_DS is lower than $V_\mathrm{G} - V_\mathrm{th}$, the drain current almost increases linearly within the first half of a parabola given by

$$I_\mathrm{D} = \mu_\mathrm{eff} C_\mathrm{ox} \frac{W}{L} \left[(V_\mathrm{G} - V_\mathrm{th}) V_\mathrm{DS} - \frac{V_\mathrm{DS}^2}{2} \right] \quad \begin{matrix} \text{for } V_\mathrm{G} - V_\mathrm{th} \geq V_\mathrm{DS} \\ \text{(linear regime)} \end{matrix} \quad [3]. \tag{2.1}$$

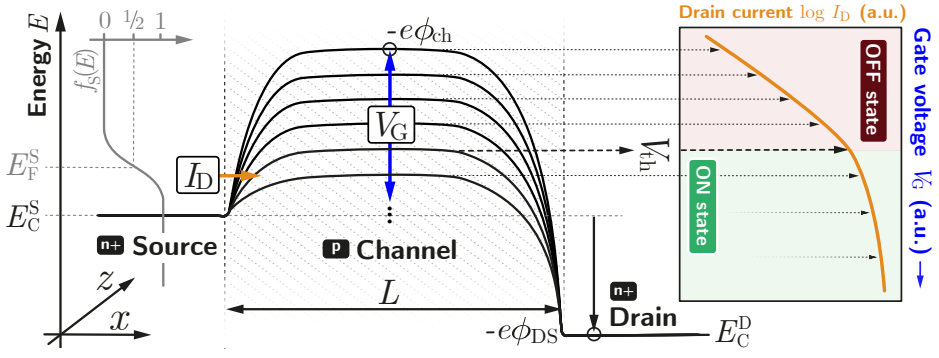

Figure 2.2: Illustration of the ideal n-channel MOSFET's conduction band as a function of V_G with static V_DS [22]: Initially, the high barrier of the p-channel does not allow any carrier transport from source to drain. The conduction band (same applies to the valence band) bends down by applying a gate voltage V_G lowering the barrier. Exceeding ($V_\mathrm{G} > V_\mathrm{th}$) leads to carrier injection from source into the channel. By applying a sufficiently high drain-source voltage V_DS, carriers eventually flow from source to drain. Note that the band structure refers to ideal conditions at the interface between channel and gate oxide.

Besides the already known parameters, equation 2.1 contains the effective carrier mobility μ_{eff} and the gate capacitance C_{ox} (or the MOS capacitor for that matter). After exceeding the gate voltage by $V_{\text{DS}} > V_{\text{G}}$, superposition of both voltages comes into effect. V_{DS} increases along the x-direction and decreases the effective gate voltage V_{G} at the channel region. Therefore, the length of the active channel varies along its expanse. Eventually, the channel will be pinched off and ideally any further increase of the drain current I_{D} stops [22]. This behavior can be observed in the output characteristics illustrated in figure 2.3a. The drain current I_{D} rises within the linear regime and stays unchanged in the saturation regime after V_{DS} exceeds $V_{\text{G}} - V_{\text{th}}$. At this point, I_{D} does not depend on changes in V_{DS} any more:

$$I_{\text{D}} = \mu_{\text{eff}} C_{\text{ox}} \frac{W}{2L} (V_{\text{G}} - V_{\text{th}})^2 \quad \begin{matrix}\text{for } V_{\text{DS}} \geq V_{\text{G}} - V_{\text{th}} \\ \text{(saturation regime)}\end{matrix} \text{ [3].} \tag{2.2}$$

Figure 2.3b shows the transfer characteristic describing the drain current I_{D} as a function of the gate voltage V_{G}. The log scale depiction of an arbitrary MOSFET characteristic visualizes how the the on-state is delimited from the off-state by the threshold voltage V_{th}. The off-state is defined by the electric potential barrier of the channel for $V_{\text{G}} < V_{\text{th}}$. Moving the barrier towards the thermally broadened Fermi distribution, the maximum slope of the current is restricted below V_{th} at the so-called thermionic limit. The steeper the slope, the faster the transition to the on-state can be enforced.

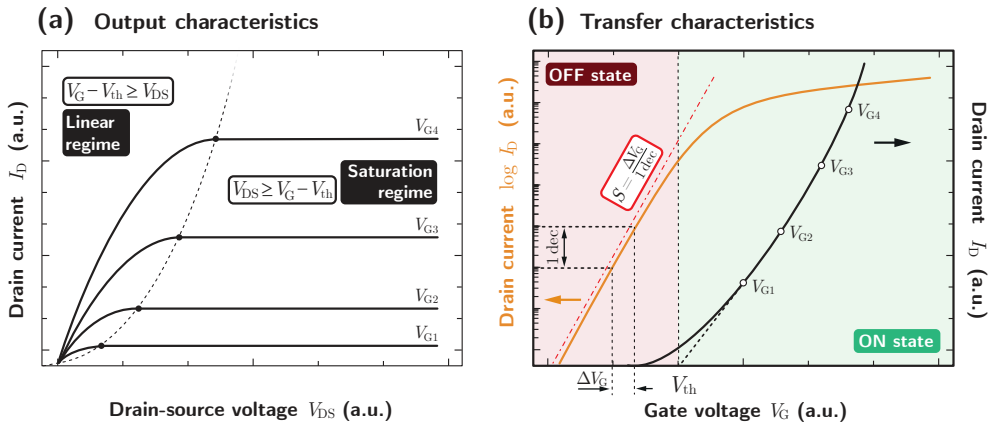

Figure 2.3: I-V characteristic of the ideal n-channel MOSFET: (a) Output characteristics for the drain current I_{D} as a function of the drain-source voltage V_{DS} with four arbitrary incrementing gate voltages $V_{\text{G,1-4}}$. The dashed line marks the transition from the linear (ohmic) regime to the saturation regime. (b) Transfer characteristic with logarithmic (left) and linear axis (right) for the drain current I_{D} as a function of the gate voltage V_{G}. The threshold voltage V_{th} separates the on-state from the off-state. Below V_{th} the (subthreshold) slope is only graphically visible on the logarithmic scale.

2.1.2 Limitations and non-ideal Characteristics

Beyond the ideal description, one will find a lot of research on alternatives to the MOSFET implying that there must be some limitations in its use. As mentioned at the end of the previous section, the slope of I_D is restricted below the threshold V_th. This off-state limitation is particularly interesting, because it determines how abrupt the transition to the on-state will be. Consequently, the sharper the transition, the lower the operating voltage has to be. This characteristic is known as the subthreshold slope and is also illustrated in figure 2.3b. More commonly used though is the inverse subthreshold slope S to stress the required voltage in relation to the log-scale current, which is defined as

$$S\,[\mathrm{mV/dec}] = \left(\frac{\partial\ \log I_\mathrm{D}}{\partial\ V_\mathrm{G}}\right)^{-1} = \ln 10 \left(\frac{\partial I_\mathrm{D}}{\partial V_\mathrm{G}} \frac{1}{I_\mathrm{D}}\right)^{-1} \quad [3, 21]. \tag{2.3}$$

In the interest of finding a more meaningful expression for S and with the assumption that the drain-source potential ϕ_DS is constant, the drain-current can then be expressed by[2]

$$I_\mathrm{D} = \frac{4}{\pi\hbar} \int_{-e\phi_\mathrm{ch}}^{\infty} f_\mathrm{S}(E)\mathrm{d}E \ \ [21]. \tag{2.4}$$

As discussed in section 2.1.1, the gate potential - or more specific the channel potential - is still far away from the Fermi level of the source region E_F^S for the off-state. This allows replacing the Fermi distribution by the simpler Boltzmann approximation[3] $f_\mathrm{S}(E) \approx \exp\left((E_\mathrm{F}^\mathrm{S}-E)/k_\mathrm{B}T\right)$, where k_B is the Boltzmann constant and T the temperature [21]. Doing so, the integral from 2.4 is approximated to

$$I_\mathrm{D} \approx \frac{4}{\pi\hbar} \int_{-e\phi_\mathrm{ch}}^{\infty} \exp\left(\frac{E_\mathrm{F}^\mathrm{S} - E}{k_\mathrm{B}T}\right) \mathrm{d}E = \frac{4k_\mathrm{B}T}{\pi\hbar} \cdot \exp\left(\frac{E_\mathrm{F}^\mathrm{S} + e\phi_\mathrm{ch}}{k_\mathrm{B}T}\right). \tag{2.5}$$

Inserting I_D from equation 2.5, the partial derivative $\partial I_\mathrm{D}/\partial V_\mathrm{G}$ in equation 2.3 is solved by applying the chain rule and yields

$$\frac{\partial I_\mathrm{D}}{\partial V_\mathrm{G}} = e \cdot \frac{I_\mathrm{D}}{k_\mathrm{B}T} \cdot \frac{\partial \phi_\mathrm{ch}}{\partial \phi_\mathrm{G}}\ . \tag{2.6}$$

Next, to find a solution for the partial derivative $\partial\phi_\mathrm{ch}/\partial\phi_\mathrm{G}$ an equivalent circuit will be of help [24]. This way the junctions at the source-channel transition and the drain-channel transition can be interpreted as capacitors C_s and C_d,

[2] To avoid exceeding the scope of the thesis, the complete deduction of I_D was dismissed. It can be found in [21] and [23].

[3] Because the Boltzmann approximation applies to the high-energetic part of the Fermi distribution, it is usually called the *Boltzmann tail*.

respectively (which they basically are). They both are connected to the channel which in turn is connected to the gate capacitor C_{ox}. At this node, they all share the same channel potential ϕ_{ch} (cf. figure 2.4).

From an ideal perspective, the gate potential ϕ_{G} and the channel potential ϕ_{ch} should be nearly identical, which is synonymous to perfect gate control. In reality, the channel potential also depends on the drain-source potential ϕ_{DS} and additional non-ideal capacitances, namely the inversion capacitance C_{inv}, the depletion capacitance C_{dep}, the dielectric interface capacitance C_{if}, and obviously C_{d} and C_{s}. However, since the source terminal is usually set to ground, C_{s} can be neglected.

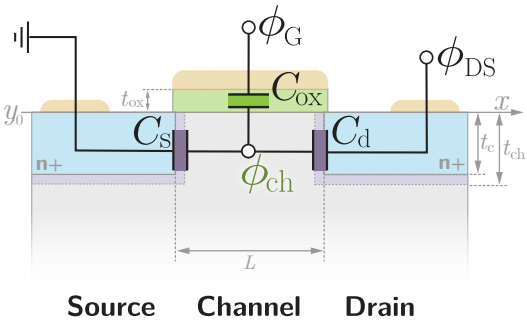

Figure 2.4: For the ideal MOSFET the energy bands within the channel will exactly follow the gate potential ϕ_{G}. However, the real perspective reveals that the channel potential ϕ_{ch} differs from the gate potential ϕ_{G} and is shared amongst the three capacitors C_{ox}, C_{s} and C_{d}.

With that in mind, the relative change of ϕ_{ch} can then be written as a potential divider:

$$\partial\phi_{\mathrm{ch}} = \partial\phi_{\mathrm{G}}\frac{C_{\mathrm{ox}}}{\Sigma C_{\square}} + \partial\phi_{\mathrm{DS}}\frac{C_{\mathrm{d}}}{\Sigma C_{\square}} \quad [21], \tag{2.7}$$

with $\Sigma C_{\square} = C_{\mathrm{ox}}+C_{\mathrm{inv}}+C_{\mathrm{dep}}+C_{\mathrm{if}}+C_{\mathrm{d}}$. For the sake of simplicity, $C_{\mathrm{inv}}, C_{\mathrm{dep}}, C_{\mathrm{if}}$ and C_{d} are condensed to $C_{\text{non-ideal}}$ for now. The partial derivative $\partial\phi_{\mathrm{ch}}/\partial\phi_{\mathrm{G}}$ in equation 2.6 can then be extracted from equation 2.7. Knowing that the drain-source potential is constant, hence $\partial\phi_{\mathrm{DS}} = 0$, equation 2.7 is simplified to

$$\frac{\partial\phi_{\mathrm{ch}}}{\partial\phi_{\mathrm{G}}} = \frac{C_{\mathrm{ox}}}{C_{\mathrm{ox}} + C_{\text{non-ideal}}}\,. \tag{2.8}$$

Using equation 2.8, the inverse subthreshold slope may be written as

$$S = \ln 10\left(\frac{\partial I_{\mathrm{D}}}{\partial V_{\mathrm{G}}}\frac{1}{I_{\mathrm{D}}}\right)^{-1} = \frac{k_{\mathrm{B}}T}{e}\ln 10\cdot\left(\frac{C_{\mathrm{ox}} + C_{\text{non-ideal}}}{C_{\mathrm{ox}}}\right) \quad [3, 21]. \tag{2.9}$$

Assuming that $C_{\mathrm{ox}} \gg C_{\text{non-ideal}}$, the lowest achievable inverse subthreshold slope is $60\,\mathrm{mV/dec}$ at room temperature ($T = 300\,\mathrm{K}$). This very specific value marks the limit in performance for every conventional MOSFET at this temperature. Besides that, the on-/off-ratio is also an important criteria for favorable switching behavior. The difference in current between those two

states should be as high as possible. As a recommendation by the International Roadmap for Devices and Systems (IRDS) a MOSFET should maintain an on-/off-ratio of at least six decades (10^6) [6]. Therefore, a slope limitation of $60\,\mathrm{mV/dec}$ implies that a gate voltage of at least 360 mV will be necessary in order to switch from the off-state to the on-state. However, this is of course the most optimistic switching behavior possible. In reality, gate control is far from optimum and all parts of $C_{\text{non-ideal}}$ contribute to a bigger inverse subthreshold slope, demanding for a much higher gate voltage. Unfortunately, a higher gate voltage also implies a higher supply voltage. Equation 2.10 shows how the dynamic and static power dissipates from the MOSFET:

$$P \propto f C_{\text{ox}} V_{\text{DD}}^2 + I_{\text{leak}} V_{\text{DD}} \text{ [23].} \tag{2.10}$$

I_{leak} is the off-state leakage current and V_{DD} is the supply voltage. The gate charging frequency or the circuit clock frequency f for that matter is defined by the gate delay τ as

$$\tau \leq \frac{1}{f} := \frac{C_{\text{ox}} W L V_{\text{G}}}{I_{\text{D}}} = \frac{2L^2}{\mu} \cdot \frac{V_{\text{G}}}{(V_{\text{G}} - V_{\text{th}})^2} \text{ [23],} \tag{2.11}$$

where I_{D} is the on-state drain current within the saturation regime from equation 2.2. Considering that the gate voltage can only be as high as the supply voltage V_{DD}, V_{G} might as well as be replaced by V_{DD}. In general, the gate delay τ serves as a good criteria for the on-state performance of the MOSFET. Obviously, it is desirable to increase the frequency while simultaneously reducing power losses. Equation 2.11 offers four approaches to do so: Reducing the channel length L. Increasing the carrier mobility μ. Decreasing the supply voltage V_{DD}. Reducing the threshold voltage V_{th}. By looking closer to those options, the MOSFET again does reveal its limitations: Decreasing V_{th} is actually not an option, because it would massively increase the off-state leakage current as exemplified in [21]. The carrier mobility is practically a constant of the material and is therefore set by silicon and the dopant concentration. Aggressively reducing the supply voltage would be an option, however, the mentioned limit in S requires for at least 360 mV.[4] The only option left is to reduce the channel length while maximizing gate control. To accomplish this it is necessary to reevaluate equation 2.7. Considering the case that the MOSFET is in the on-state, i.e. $\partial\phi_{\text{DS}} \neq 0$, the drain-source potential must be somehow detached from equation 2.7. This is achieved by assuming $C_{\text{ox}} \gg C_{\text{d}}$ and that the donor

[4] Note that in real applications a so-called overdrive voltage adds to the 360 mV, which is usually around $\times$ 1-2 the threshold voltage, ultimately limiting the supply voltage to $\sim$1 V.

concentration is usually very high which results in very thin depletion layers around the n-regions. It follows that the channel thickness t_{ch} can be roughly considered being equal to the depth of the n-regions t_{c} (cf. figure 2.1). Next, dismembering C_{ox} and C_{d} yields:

$$\underbrace{\epsilon_0 \epsilon_{\mathrm{ox}} \frac{WL}{t_{\mathrm{ox}}}}_{C_{\mathrm{ox}}} \gg \underbrace{\epsilon_0 \epsilon_{\mathrm{ch}} \frac{W \cdot t_{\mathrm{ch}}}{L}}_{C_{\mathrm{d}}} \quad [23]. \tag{2.12}$$

Now, condition 2.12 can finally be rearranged for L, resulting in:

$$L \gg \sqrt{\frac{\epsilon_{\mathrm{ch}}}{\epsilon_{\mathrm{ox}}} t_{\mathrm{ox}} t_{\mathrm{ch}}} \equiv \lambda_{\mathrm{ch}} \quad [23]. \tag{2.13}$$

Here, the right term of statement 2.13 can be interpreted as the gate geometry factor λ_{ch}. In general, this factor can be considered as a screening length for the electrical field inside the channel.[5] Evidently, a channel length L much longer than λ_{ch} will sufficiently screen the channel potential from the drain-source potential [21]. This is of course inconsistent to the first mentioned option of maximizing performance, that is reducing the channel length L. Nevertheless, changing the MOSFET's geometry, i.e. reducing L, is still the only option left. The implications are discussed next.[6]

2.1.3 Impact of Short Channel Geometries

So far, the focus primarily lied on the so-called long channel MOSFET. Over the last decades however, the demand for highly integrated and also highly performing transistors has vastly increased. As a consequence, the geometry has been scaled down far below sub-100 nm dimensions [25]. Unfortunately, the steady reduction of the MOSFET's channel prompted new problems.

Although the basic working principle has not changed, a much shorter channel will make the device more elaborate and difficult to control. The primary reason for this are the depletion zones around source and drain. Their relative expanse in comparison to the channel cannot be neglected anymore. Since the drain-source voltage V_{DS} usually refers to ground potential of source, it is the depletion zone around the drain region which is expanding with rising V_{DS}. If the expanse takes up significantly more space within the relatively short channel, the gate potential will be shielded and effectively reduced (cf. equation 2.13). A more general approach is described

[5] Comparable to the Debey-length λ_{D} in doped semiconductors.

[6] Note that for MOSFETs the channel is made from silicon ($\epsilon_{\mathrm{ch}} = \epsilon_{\mathrm{Si}}$). However, this approach is valid for all gate-controlled devices and is not unique to silicon. Further references on that matter are therefore addressed just as "channel material".

by Yan et al. [26] using the channel's electrostatics: Starting with Poisson's differential equation, Yan et al. simplify the potential of the channel $\phi(x, y)$ by applying three boundary conditions so that the equation is left with the sole potential at the surface: $\phi(x, y_0) := \phi(x)$:

$$\frac{\mathrm{d}^2\phi(x)}{\mathrm{d}x^2} - \frac{\phi(x) - \phi_\mathrm{G}}{\lambda_\mathrm{ch}^2} = \frac{eN_\mathrm{A}}{\epsilon_0\epsilon_\mathrm{ch}} \quad [26]. \tag{2.14}$$

The equation contains the gate potential ϕ_G, the doping concentration inside the channel region N_A (p-substrate) and the permittivity of the channel material $\epsilon_0\epsilon_\mathrm{ch}$. The key value is the channel geometry factor λ_ch, because it determines the solution for $\phi(x)$ which is proportional to $\exp(\pm x/\lambda_\mathrm{ch})$. As a reminder, λ_ch can be considered as a screening length for the potential inside the channel. For planar gate geometries like the MOSFET, $\lambda_\mathrm{ch} = \sqrt{\frac{\epsilon_\mathrm{ch}}{\epsilon_\mathrm{ox}} t_\mathrm{ox} t_\mathrm{ch}}$. In case of impurity doping, λ_ch will be influenced by the depletion zones of source and drain, because their expanse determines the channel thickness t_ch.

Figure 2.5a illustrates the problem of the expanding depletion zone from the drain region into the channel. The length of the channel L can be expressed by units of λ_ch. For $L \leq \lambda_\mathrm{ch}$ the depletion zones will overlap and there is no way to pinch off the channel any more. The energy bands at the surface for $L = 4\lambda_\mathrm{ch}$ and $L = 8\lambda_\mathrm{ch}$ are shown in figure 2.5b: The closer the channel length is to λ_ch, the less influence the gate potential has and the energy barrier towards the channel is lowered, implying that more electrons will be

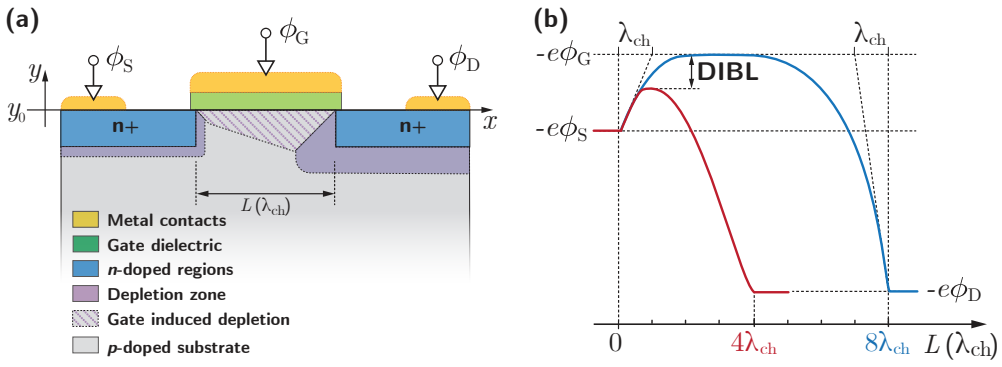

Figure 2.5: The length of the channel L can be described by using the gate geometry factor λ_ch as a natural scale of screening. The cross-section in (a) illustrates how the depletion zones of the source, drain and channel region interact with each other. (b) depicts the energy bands at the surface y_0 for their respective electric potentials as a function of λ_ch. As an example, for $L = 4\lambda_\mathrm{ch}$ the barrier from source towards the channel is lowered and DIBL occurs. Increasing L to $8\lambda_\mathrm{ch}$ the gate potential gains more influence and DIBL can be avoided [27, 28]. For simplicity ratios for L have been chosen arbitrarily.

injected into the channel region. This effect is called drain induced barrier lowering (DIBL) and has a negative impact on the transfer characteristic of the transistor, because it results in higher leakage currents.[7] The inverse subthreshold slope increases and it is more difficult to control the device. An analytical expression of DIBL affecting S is given by:

$$S \approx \frac{k_\mathrm{B}T}{e}\ln 10 \cdot \left[1 - 2 \cdot \exp(-\frac{L}{2\lambda_\mathrm{ch}})\right]^{-1}, \ \mathrm{DIBL} = \frac{\partial\phi_\mathrm{ch}}{\partial\phi_\mathrm{DS}} \approx \exp(\frac{-L}{2\lambda_\mathrm{ch}}) \ [21]. \tag{2.15}$$

Note that the expanse of the depletion zones of source and drain into the channel λ_S and λ_D, respectively, are omitted, because they only depend on the doping concentrations (λ_S, $\lambda_\mathrm{D} \propto (N_\mathrm{A,D})^{-1/2}$), which should to be very low in order to maintain control over the channel via the gate.

After all, if DIBL has to be avoided but L is desired to be extremely short anyway, λ_ch has to be minimized. The most practical way to do so is by using very thin gate dielectrics with high relative permittivity[8]. Provided the channel thickness t_ch is independent from impurity doping, a thin body layout will also work in favor. Additionally, the device layout can be implemented as a double gate or even as a cylindrical gate-all-around geometry to increase control over the channel [30–32]. For the latter λ_ch changes to

$$\lambda_\mathrm{ch} = \sqrt{\frac{1}{8}\frac{\epsilon_\mathrm{ch}}{\epsilon_\mathrm{ox}} t_\mathrm{ch}^2 \cdot \ln\left(1 + \frac{t_\mathrm{ox}}{t_\mathrm{ch}}\right)} \ [31], \tag{2.16}$$

yielding much smaller values for λ_ch when compared to equation 2.13. Silicon-on-insulator (SOI)- and nanowire-MOSFET technologies with gate-all-around geometry yield an inverse subthreshold slope very close to $60\,\mathrm{mV/dec}$ [30,32–35].

2.2 Novel Transistor Technologies

Although, the mentioned gate-all-around MOSFETs show improved gate control, they still cannot overcome the limit of $S = 60\,\mathrm{mV/dec}$. In fact, every field effect transistor which relies on injecting carriers from the thermally broadened Fermi distribution is bound by that thermionic limit. Of course technological development did not stop there. The need for denser integration and lesser power consumption motivated research and boosted inventions. Extremely sophisticated fabrication technologies enabled new possibilities and

[7] Note that besides DIBL there are numerous other short channel effects [29], such as channel length modulation or hot carrier degradation which are omitted here.

[8] In common literature the term high-κ dielectric is used very often. Note that in this thesis the symbol for the relative permittivity in a mathematical context is always ϵ_ox.

gave birth to new transistor architectures, that are indeed able to overcome the limit of $S = 60\,\mathrm{mV/dec}$. [36–43]. Motivated by this growing field of new transistor research, the main subject of this thesis is the fabrication and characterization of transistors having silicon replaced by carbon nanotubes. To justify this choice, three criteria have to be fulfilled: First, the device should obviously exhibit an inverse subthreshold slope below $60\,\mathrm{mV/dec}$ (subsections 2.2.1 and 2.2.2). Second, the device geometry must be designed in a way to achieve maximum gate control (subsection 2.2.3). And third, the properties of alternative channel materials must show distinct advantages over silicon (subsection 2.2.4). The next sections cover all of the three requirements, showing how they actually contribute to the development of transistors being superior to the MOSFET.

2.2.1 Tunnel FETs

As mentioned before, every field effect transistor which relies on injecting carriers from the Boltzmann tail of the Fermi distribution has a limited inverse subthreshold slope of $60\,\mathrm{mV/dec}$ at $300\,\mathrm{K}$. Being able to go steeper than this natural limitation is the sought objective of modern transistor research, hence the term steep slope transistor (SST).

Basically, the objective of any SST is to inhibit the carrier injection from the Boltzmann tail thus suppressing the thermal leakage current. Figure 2.6 supplements the MOSFET energy bands by an imaginary Boltzmann filter. Consequently, the drain current only increases from injection of the low energetic part of the Fermi distribution with an incredibly steep slope far below $60\,\mathrm{mV/dec}$. The question at hand is how to realize this filtering. One prominent way is the so-called Tunnel-FET or TFET for short.

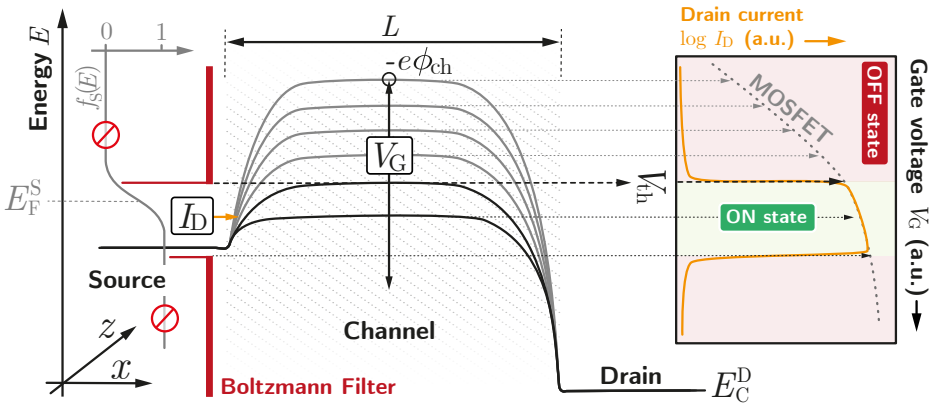

Figure 2.6: Principle of SSTs: Preventing thermal injection from the Boltzmann tail leads to an extremely steep transition from the off-state to the on-state.

A TFET device is based on band-to-band tunneling (BTBT). By using either asymmetrical *n-i-p* impurity or electrostatic doping, the valence band in the intrinsic channel can be positioned very close to and also above the conduction band of the *n*-doped source region. The probability for quantum tunneling between the two bands then vastly rises. Naturally, BTBT is not bound to occur only at the source-channel transition. If the channel conduction band drops below the valence band in drain, tunneling also starts to occur at the channel-drain transition (unfortunately, this ambipolarity gives room for more off-state current leakage [28], which is omitted for now).

Figure 2.7 shows the valence and conduction band of a TFET device. The Fermi levels are fully aligned with the respective bands of source and drain. This is actually the ideal case, because in this scenario the conduction band of the source is nearly empty (this matter will be discussed later in this section). Since source and drain are of opposite doping and the channel is kept intrinsic, the channel potential ϕ_{ch} can push the channel valence band above the conduction band of the source [44]. At the transition BTBT with the probability $T(E)$ occurs. The resulting drain current is

$$I_{\mathrm{D}} = \frac{e}{\pi\hbar}\int_{-\infty}^{\infty} T(E)(f_{\mathrm{S}}(E) - f_{\mathrm{D}}(E))\,\mathrm{d}E \quad [21], \tag{2.17}$$

where $f_{\mathrm{S}}(E)$ and $f_{\mathrm{D}}(E)$ are the Fermi distributions of source and drain region, respectively. The energy difference from the conduction band of source to the valence band of the channel $E_{\mathrm{C}}^{\mathrm{S}} - E_{\mathrm{V}}^{\mathrm{ch}}$ determines the energetic window in which BTBT becomes possible (light green strip). Under the assumption that $E_{\mathrm{C}}^{\mathrm{S}} = 0$, the window's height matches the channel valence band at $-e\phi_{\mathrm{ch}}$. Thus, the limits for the integral in equation 2.17 can be chosen accordingly, i.e. from 0 to $-e\phi_{\mathrm{ch}}$.[9] The difference of $f_{\mathrm{S}}(E)$ and $f_{\mathrm{D}}(E)$ is visualized on the left side in figure 2.7 (hatched green area). When solving the integral within the given limits, the resulting function F will only depend on the channel potential ϕ_{ch}. For the ideal scenario of perfect gate control ($\phi_{\mathrm{G}} = \phi_{\mathrm{ch}}$), F might as well be expressed as a function of the gate potential $F(\phi_{\mathrm{G}})$. The energetic window for BTBT can therefore be manipulated by the external gate voltage. A helpful tool to solve the tunnel probability $T(E)$ is linearizing the band curvature at the transition and using the Wentzel-Kramers-Brillouin (WKB) approximation. By applying this method, $T(E)$ can be expressed as

$$T(E) \approx T_{\mathrm{WKB}}(E) = \exp\left(\frac{-4(\lambda_{\mathrm{S}} + \lambda_{\mathrm{ch}})\sqrt{2m^*}\,E_{\mathrm{g}}^{3/2}}{3\hbar(E + E_{\mathrm{g}})}\right) \quad [45], \tag{2.18}$$

[9] Note that in this simple approach off-state current leakage due to minor thermal carrier injection from above the conduction band and also from below the valence band is omitted.

with $\lambda = \lambda_S + \lambda_{ch}$ being equal to the tunnel barrier distance. The band gap E_g and the effective carrier mass m^* are given by the channel material and the maximum energy E is equal to $-e\phi_{ch}$, deducing $T_{WKB}(E)$ also becomes a function of the gate potential: $T_{WKB}(\phi_G)$. By using $F(\phi_G)$ and $T_{WKB}(\phi_G)$ equation 2.17 can be approximated as:

$$I_D \approx \frac{-e}{\pi\hbar} T_{WKB}(\phi_G)\, F(\phi_G) \quad [45]. \tag{2.19}$$

Based on equation 2.3, the inverse subthreshold slope can be calculated by inserting the drain current for the TFET from equation 2.19, which gives

$$S = \ln(10)\frac{1}{e}\left(\frac{\partial T_{WKB}(\phi_G)}{\partial\phi_G \cdot T_{WKB}(\phi_G)} + \frac{\partial F(\phi_G)}{\partial\phi_G \cdot F(\phi_G)}\right)^{-1} \quad [21, 23]. \tag{2.20}$$

Two cases have to be considered here: First, if the tunnel probability $T_{WKB}(\phi_G)$ is low but rapidly changes as a function of the gate potential, the inverse subthreshold slope breaks down to

$$S \approx \ln(10)\frac{1}{e} \cdot \frac{3\hbar(-e\phi_G + E_g)}{4(\lambda_{ch} + \lambda_S)\sqrt{2m^*}\, E_g^{3/2}} \quad [21]. \tag{2.21}$$

Second, if $T_{WKB}(\phi_G)$ is very high (i.e. close to one) but does not change as a function of the gate potential, it will no longer be important and S will become a simple function of the gate potential only:

$$S \approx \ln(10) \cdot \phi_G \quad [21]. \tag{2.22}$$

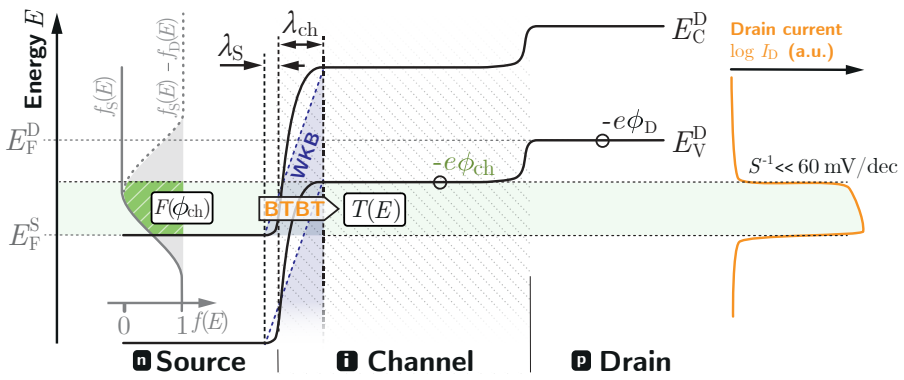

Figure 2.7: Band configuration of a TFET device for the on-state: The mutual proximity of the valence band of the channel and the conduction band of the source region enables BTBT. The blue triangles represent the potential barrier approximating the WKB tunneling probability $T_{WKB}(E)$. $F(\phi_{ch})$ is illustrated on the left as a result of the integral of $f_S(E) - f_D(E)$ from equation 2.17 (hatched green area). Note that in this illustration the Fermi level of source is equal to the hight of the conduction band.

In both cases S becomes independent from thermal carrier injection offering the possibility of much steeper slopes. Carrier injection into the channel can only occur within the energetic tunneling window applied on the Fermi distribution. The Boltzmann tails at both ends of the function are almost cut off, so that the window is in fact operating as band-pass filter. [21]

To enforce the case in which equation 2.22 is dominant, two criteria have to be met for obtaining a very steep subthreshold slope: First, the BTBT probability $T_{\mathrm{WKB}}(\phi_{\mathrm{G}})$ must come as close to one as possible. When considering equation 2.18 it is obvious that the expanse of the depletion zone of the source and the channel geometry factor $\lambda_{\mathrm{ch}} + \lambda_{\mathrm{S}}$ must be rather small in order to get $T_{\mathrm{WKB}}(\phi_{\mathrm{G}})$ towards one. This can be achieved by applying the same optimization methods for λ_{ch} as discussed in subsection 2.1.3. λ_{S} can be decreased by an extremely high doping concentration in the source region. The higher the concentration, the smaller the expanse of the depletion zone. Furthermore, a material with a very low effective carrier mass m^* is of help as well as a small band gap. Although, a (too) small band gap may increase leakage current. Second, the doping of the source region must be kept low, which is of course contradicting to the just mentioned statement. However, a lower doping concentration leads to a source conduction band being almost empty, allowing all electrons to tunnel from the channel valence band to the vacant states in the source conduction band. Only then the Fermi level lies at the conduction band edge and the Boltzmann tails will be cut off (cf. figure 2.8a). However, as mentioned earlier, a low doping concentration increases

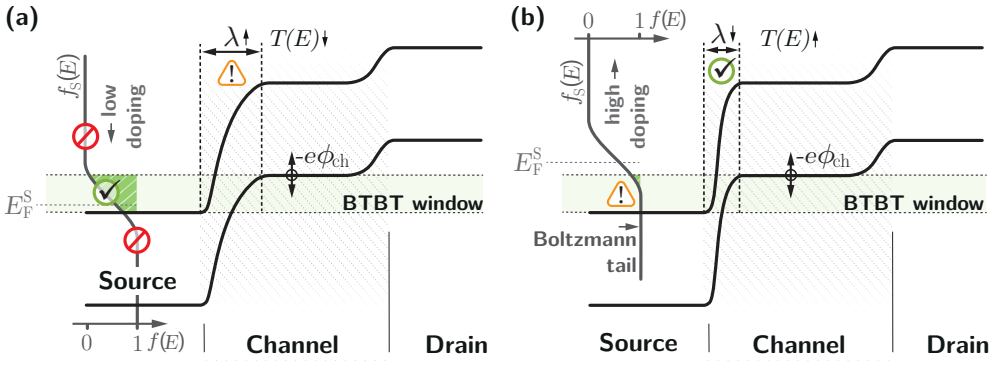

Figure 2.8: Electronic band structure of a TFET device for different source doping profiles. (a) A low doping concentration leads to band-pass filtering of the Fermi distribution and the Boltzmann tail gets cut off. At the same time $\lambda = \lambda_{\mathrm{S}} + \lambda_{\mathrm{ch}}$ becomes larger, thus increasing the tunneling distance which also decreases the BTBT probability $T(E)$. (b) A high doping concentration has the reverse effect. $T(E)$ will be closer to one while on the downside the energetic BTBT window applies partially or entirely on the Boltzmann tail of the Fermi distribution. [23, 46]

the expanse of the depletion zone, that in turn will again decrease $T_{\mathrm{WKB}}(\phi_{\mathrm{G}})$. On the other hand, a too high doping concentration moves the Fermi level away from the conduction band leading to a low $F(\phi_{\mathrm{G}})$ and to an energetic window being applied to the Boltzmann tail of the Fermi distribution (instead of cutting off the Boltzmann tail, cf. figure 2.8b). In this case the device does not behave like a TFET but rather like a conventional transistor not being able to overcome the limit of $60\,\mathrm{mV/dec}$. [21, 23, 46]

Fabricating a TFET requires the channel to be split up into three different gates. One gate is needed for device control (main gate) and two additional gates for implementing the doping. Adjusted individually, these gates allow for different band configurations along the channel region satisfying the mentioned conditions in order to configure a TFET device. Obviously, standard doping by implanting impurities will not provide the necessary scope for dynamically adjusting gate potentials, therefore the gates must be implemented as mutually insulated electrodes [11]. In this case, the energy bands will be controlled by the electrical field from each electrode.[10] Chapter V elaborates on the so-called buried triple gate (BTG) architecture, which was fabricated within the scope of this thesis. Its purpose is to provide the necessary electrostatic doping landscape for TFET devices.

2.2.2 Energy Filtering FETs

Despite its name, the part being responsible for the steep slope of a TFET is not the tunneling per se. However, the band-to-band tunneling determines the filtering function and is not easy to control. In fact, not being able to setup the configuration properly the TFET will operate even worse than latest MOSFET designs. Only by achieving energy filtering, the TFET exhibits a very steep subthreshold slope. Nonetheless, this major downside can be bypassed by creating an actual energy filter without the involvement of BTBT. One exemplary application is the Superlattice-FET or simply energy filtering FET (EF-FET).

Similar to the TFET architecture multiple gates can be used to control the EF-FET: Implementing a certain setup of a reconfigurable gate landscape can work as a bandpass filter, too. The gates must be switched in alternating sequence in order to create periodic potential barriers. If the physical distance between the potential barriers is small enough, an energetic superlattice emerges, comparable to the periodic potentials in solid state crystals. Within the superlattice, injection through the barriers becomes possible and

[10] Noteworthy theoretical and experimental research on TFET architectures can be found in [12, 13, 28, 31, 43, 47].

generates a cosine-shaped miniband. Therefore, a specific energetic window with a non-zero density of states enables carrier transport inside this window. When applied on the low energy part of the source Fermi distribution, the miniband is able to function as a band-pass filter for the high energetic Boltzmann tail. The distance between the potential barriers generating the superlattice is anti-proportional to the miniband's width. To reach sufficiently high currents, the tunneling distance must be very small. Unfortunately, for higher energies additional minibands will develop. If the barrier distance will be too small, not only the first miniband will grow larger but the second miniband, too, increasing mutual proximity. Obviously, the energetically higher placed second miniband will contribute to thermal leakage current due to carrier injection from the Boltzmann tail. This way, the EF-FET cannot yield an inverse subthreshold slope below $60\,^{\mathrm{mV}}/_{\mathrm{dec}}$. The only way to avoid unfavorable minibands - while still yielding sufficient carrier transport - is by finding a trade-off solution with appropriate barrier lengths. In order to function as a transistor, the energy filter has to be combined with a FET channel (cf. figure 2.9). For a current-less off-state, the channel potential ϕ_{ch} must be carefully placed above the first miniband but still below the second miniband to avoid injection from the Boltzmann tail. Only the filter within the first miniband prevents carrier injection from the Boltzmann tail. Eventually, when the channel potential energetically drops below the filter itself, carrier injection quickly rises for a steep transition to the on-state.

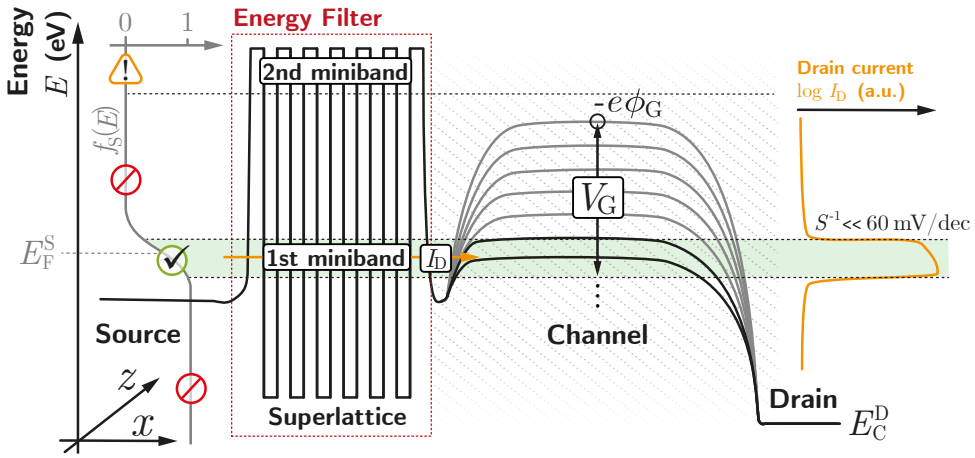

Figure 2.9: Conduction band of an EF-FET [21, 48]: The alternating potentials at the gates create a superlattice which leads to a miniband along the gate cluster. The carrier injection from source into the channel comes from the non-thermally broadened part of the Fermi function, thus only within a filtering window. Injected carriers can then tunnel throughout the tunable miniband. If the band in the FET channel will be pushed inside the filtering window, the device can transit to the on-state with S far below $60\,^{\mathrm{mV}}/_{\mathrm{dec}}$.

Once the on-current has been reached, the current is restricted and its density j stays constant even with further lowering of the channel potential. This is due to the continuity equation, in which the density of carriers n decreases for lower channel potentials but at the same time carrier velocity ν must increase ($j = en \cdot \nu = \text{const.}$) [21]. Note that this transistor architecture also comes with a major disadvantage: By deploying multiple gates in a lateral system, scaling down the device becomes quiet difficult. Thus, possible applications will focus on low-power devices rather than on increased integration density.[11] The buried multi gate (BMG) architecture fabricated by Grap et al. [16, 48] is designed for such energy filter applications (providing up to 17 gates for each device in the latest version). Alongside the buried triple gates, the buried multi gates serve as a fundamental platform for developing steep slope transistors in this thesis and will be introduced in chapter V.

2.2.3 One-Dimensional Channel Geometries

Section 2.1.3 describes how gate control can be increased by deploying small values for λ_{ch}. Wrapping the gate around the channel i.e. having a concentric cylinder capacitor for C_{ox}, λ_{ch} can be minimized even further (eq. 2.16). The equation for λ_{ch} derived from the condition $C_{\text{ox}} \gg C_{\text{d}}$, ignoring the non-ideal capacitances inside the FET channel C_{inv}, C_{dep} and C_{if} as seen in equation 2.7 and 2.8. However, for the overall desire for perfect gate control, <u>all</u> non-ideal capacitors have to be decisively smaller than C_{ox}, so that the channel potential eventually can be expressed by this linear term:

$$\phi_{\text{ch}}(\phi_{\text{G}}) = \phi_{\text{G}} + \text{const.} \quad [48]. \tag{2.23}$$

This state is called the quantum capacitance limit and allows for the channel potential to linearly change with the gate potential without any losses, i.e. perfect gate control. [8, 21, 48]

To be brief, a superior field effect transistor must be designed to minimize the non-ideal capacitors, so that $C_{\text{ox}} \gg C_{\text{non-ideal}}$. Condition $C_{\text{ox}} \gg C_{\text{dep}}$ can be achieved by decreasing the channel thickness or the depletion length, respectively. $C_{\text{ox}} \gg C_{\text{if}}$ is satisfied when incorporating extremely high quality dielectrics with low interface states, which of course demands for a native oxide or extraordinary deposition techniques. Both of the mentioned criteria are important and complex in their own way, but the last condition $C_{\text{ox}} \gg C_{\text{inv}}$ deserves some attention in particular: For an increasing channel potential, 2D sub-energy bands begin to develop inside the inversion layer

[11] Noteworthy theoretical and experimental research on superlattice architectures can be found in [17, 18, 49–52].

below the gate dielectric, in turn increasing the carrier density at this point. Inside the channel region, the 2D density of states effectively becomes a 3D density of states being proportional to

$$D_{3D}(E) \propto \sqrt{E_F - e\phi_{ch}} \quad [53]. \tag{2.24}$$

Note that C_{inv} linearly depends on $D_{3D}(E)$, meaning that an increasing effective gate potential ϕ_{ch} unfortunately also increases C_{inv}. An EF-FET device with several gates could not be controlled with a quickly rising inversion capacitance C_{inv}. The connection between C_{inv} and the density of states inside the channel region can be beneficial nonetheless. The channel dimensions can be altered, so that the calculation model for the density of states differs from bulk geometries. For 1D materials the 1D density of states is proportional to

$$D_{1D}(E) \propto \frac{1}{\sqrt{E_F - e\phi_{ch}}} \quad [53]. \tag{2.25}$$

Different from Equation 2.24, here the effective gate potential ϕ_{ch} is in the denominator, thus increasing it, actually minimizes the inversion capacitance. Therefore, replacing the bulk-channel with 1D materials, such as nanowires or carbon nanotubes, noticeably contributes to enhanced gate control. [10, 48]

2.2.4 Alternative Channel Materials

Materials of lower dimensions, such as one-dimensional materials like nanowires (NWs) or carbon nanotubes (CNTs), and two-dimensional graphene or transition metal dichalcogenides (TMDs) could potentially replace bulk silicon transistor channels [9–11, 54]. These materials allow to drive relatively high currents despite their almost atomically constrained geometry. As discussed in the previous section, these low-dimensional channel materials enable excellent gate control and extreme scalability. There are a number of 1D and 2D materials that exhibit very small bandgaps and high carrier mobilities. Equation 2.11 shows that a high carrier mobility actually reduces gate delay turning these materials into ideal candidates for novel low-power transistor devices [23, 28]. Another important group of materials are the III-V semiconductors[12]. Examples like indium arsenide (InAs) or gallium antimonide (GaSb) also exhibit high carrier mobilities and small bandgaps well below 1 eV. In fact, they would massively increase performance in bulk MOSFET devices. Unfortunately, they do not come with a native oxide for gate insulation like silicon does. An oxide layer must be deposited

[12]That is a compound of elements from the boron group (third main group) and the nitrogen group (fifth main group).

separately, leading to trapped charges and a high density of states at the interface. However, many III-V semiconductors are well-suited to be fabricated in 1D geometries. Some studies present FET devices based on nanowires made from indium arsenide (InAs-NWs) showing excellent performances [16, 55–57]. The 2D carbon modification, better known as graphene, also performs extremely well in transistor applications. Once the graphene is modified to exhibit a small band gap, the effective mass becomes very low, making it an excellent choice for TFET devices [28]. However, graphene has more and more become very unattractive as channel material since this mandatory band gap engineering turned out to be rather difficult and complex.

The main focus in this thesis is directed towards another important carbon modification, CNTs. Depending on the application, they provide even better properties than III-V materials and seem ideal alternative channel materials for steep slope transistor devices [43, 58–61]. Table 2.1 provides a short comparison on relevant electronic properties of CNTs, InAs-NWs, graphene and bulk-silicon. InAs has a very high electron mobility, but only a slightly higher hole mobility than silicon. Carbon nanotubes come with even higher values. The highest carrier mobility however, still belongs to graphene, which is only surpassed by AlGaAs/GaAs heterostructures [62].

	CNTs	Graphene	InAs-NWs	Bulk-silicon
μ_n (cm^2/Vs)	∼79,000[a] [63]	∼200,000[a] [64]	≤40,000 [65]	≤1,400 [65]
μ_p (cm^2/Vs)	∼79,000[a] [63]	∼200,000[a] [64]	≤500 [65]	≤450 [65]
n_i (cm^{-3})	10^{18} [66]	10^{11} [b] [67]	$\sim 10^{15}$ [65]	$\sim 10^{10}$ [65]
m_e^* (m_0)	0.099 [66]	0.088[c] [28]	0.023 [65]	0.98[d], 0.19[f] [65]
E_g (eV)	0.135 - 2.089 [66]	none[f]	0.354 [65]	1.12 [65]

Table 2.1: Electrical properties of relevant alternative channel materials. [a]Carrier mobility for pristine graphene or CNTs, respectively. In device applications mobility is usually restricted well below 10,000 cm^2/Vs due to strong scattering effects and a high defect density [68]. [b]Valid for unmodified graphene at 300 K, unit is cm^{-2}; [c]valid for a band gap of 0.1 eV; [d]longitudinal; [e]transverse; [f]only through band gap engineering via nanoribbons a band gap emerges. m_0 is the mass of an electron $m_e = 9.1094 \cdot 10^{-31}$ kg. Values for CNTs are the highest measured in [66].

Chapter III
Carbon Nanotubes

Single-walled carbon nanotubes (SWCNTs) have been discovered in 1993 by Sumio Iijima [69]. Later in 1996 it was possible to fabricate SWCNTs with a controlled and stable procedure by laser vaporization [70]. In the beginning, only a few SWCNTs could be produced in parallel. Over the years production methods improved and higher quantities with higher quality could be made. In this work SWCNTs are used as alternative channel material for SST devices on the previously mentioned BTG and BMG platforms. Chapter III is dedicated to a comprehensive description of the structure, electrical properties, synthesis and applications for SST devices.

3.1 Fundamentals of Carbon Nanotubes

Within the allotropy of carbon there are many different types of how the carbon atoms can be arranged. A single layer of graphite, called graphene, consists of sp^2-hybridized carbon atoms shaped in a hexagonal 2D-structure. A rolled-up sheet of graphene is called a carbon nanotube and comes usually as a single-walled type meaning there are no other layers of carbon inside the tube. These single-walled carbon nanotubes (SWCNTs) are in the focus of this work, therefore the multi-walled types are not given the same significance as their single-walled siblings in this chapter.[13] For simplicity, the term carbon nanotubes (CNTs) implies that they are in fact SWCNTs unless it is explicitly said otherwise in this thesis.

3.1.1 Structural Properties

CNTs exhibit exceptional properties in terms of electrical conductivity and semiconductivity [72]. Due to the σ-bonds between the carbon atoms, CNTs also have a very high tensile strength [73]. Their diameter can vary from 2.35 Å (the thinnest tube possible) to approximately 1.5 nm depending on the synthesis method [74]. Compared to that, the average length is by far greater; in fact within several micrometers. Although impressive yet not suitable for transistor applications, the longest CNT ever produced so far was almost 550 mm long [75].

Since CNTs are based on graphene, the same structural properties apply. One of the four valence electrons of carbon is delocalized, contributing to a two-dimensional electron gas and can commit to π-bonds weakly stacking other layers of graphene. It is also the reason why graphene exhibits extremely high electron mobility. The remaining three valence electrons bond uniformly within 120° giving graphene its hexagonal shape [76]. Figure 3.1 shows the unit vectors inside the graphene lattice. A symmetrical pattern comes every 30° and reveals the two basic formations: The zig-zag and the armchair configuration.

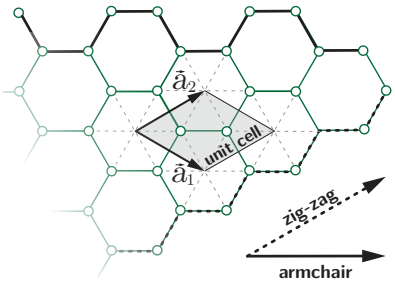

Figure 3.1: Unit vectors of graphene $\vec{a}_1$ and $\vec{a}_2$, which span the unit cell. The dashed line marks the rim of the zig-zag configuration and the bold line the rim of the armchair configuration.

[13] Multi-walled carbon nanotubes (MWCNTs) are mostly composed of one single-walled tube with slightly smaller tubes nested inside and bound by van der Waals forces. Because of the entangled tubes' proximity, electronic properties differ a lot from SWCNTs'. [71]

The unit vectors $\vec{a}_1$ and $\vec{a}_2$ as shown in figure 3.1 are defined in Cartesian coordinates as

$$\vec{a}_1 = \frac{a}{2}\left[\sqrt{3}, 1\right]^{\mathrm{T}}, \quad \vec{a}_2 = \frac{a}{2}\left[\sqrt{3}, -1\right]^{\mathrm{T}} \quad [74], \tag{3.1}$$

where $a = |\vec{a}_1| = |\vec{a}_2| = \sqrt{3} \cdot a_0 = 2.46\,\text{Å}$ with $a_0 = 1.42\,\text{Å}$ being the natural bond length of two carbon atoms inside a sp^2-hybridized graphene lattice.

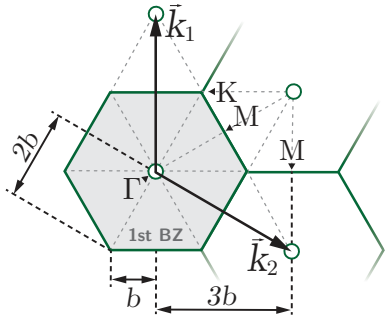

Figure 3.2: 1st Brillouin zone of graphene with high symmetry points Γ, *M*, *K* and the reciprocal lattice vectors $\vec{k}_1$ and $\vec{k}_2$ [74].

After introducing the unit cell the reciprocal lattice vectors $\vec{k}$ and the Brillouin zone can be determined. Figure 3.2 shows the reciprocal lattice with the high symmetry points Γ, M, and K. The distances between these points are a multiple of $b = {}^{2\pi}/_{3a}$ [74]. By definition, the center of the first Brillouin zone (BZ) is marked as Γ. Because of the symmetry the primitive hexagonal lattice and its properties can be fully described by that first Brillouin zone. Regarding CNTs, an additional vector $\vec{k}_3$ applies. [22]

In Cartesian coordinates the lattice vectors $\vec{k}$ are:

$$\vec{k}_1 = \frac{4\pi}{\sqrt{3}a}\,[0, 1]^{\mathrm{T}}, \quad \vec{k}_2 = \frac{4\pi}{\sqrt{3}a}\left[\frac{1}{2}\sqrt{3}, \frac{-1}{2}\right]^{\mathrm{T}} \text{ and } |\vec{k}_3| = \frac{2\pi}{a}, \tag{3.2}$$

whereas $|\vec{k}_3|$ corresponds to the translational period a and points towards the z-direction i.e. the axis of rotation. As the tube is regarded as infinitely long, $\vec{k}_3$ is continuous. [74]

3.1.2 Configurations and Chirality

Because of its relation to graphene, the same lattice notation can be applied to CNTs. When graphene is rolled-up, the lattice vector $\vec{c} = n\vec{a_1} + m\vec{a_2}$ is called the chiral vector and its length is equivalent to the circumference. The integers n and m define the chirality or achirality, respectively. Depending on the angle of $\vec{c}$ with respect to $\vec{a_1}$ (named chiral angle ϑ) different electronic properties emerge, which are discussed later in section 3.1.3. Since the carbon atoms inside the graphene sheet are hexagonal shaped, the maximum angle is 60° before the pattern repeats. If the six-fold symmetry of the pattern is also taken into account, the actual chiral angle that has to be considered is only 30°. Within this span every CNT can be described as a set of n, m integers, which therefore is known as the (n,m)-notation.

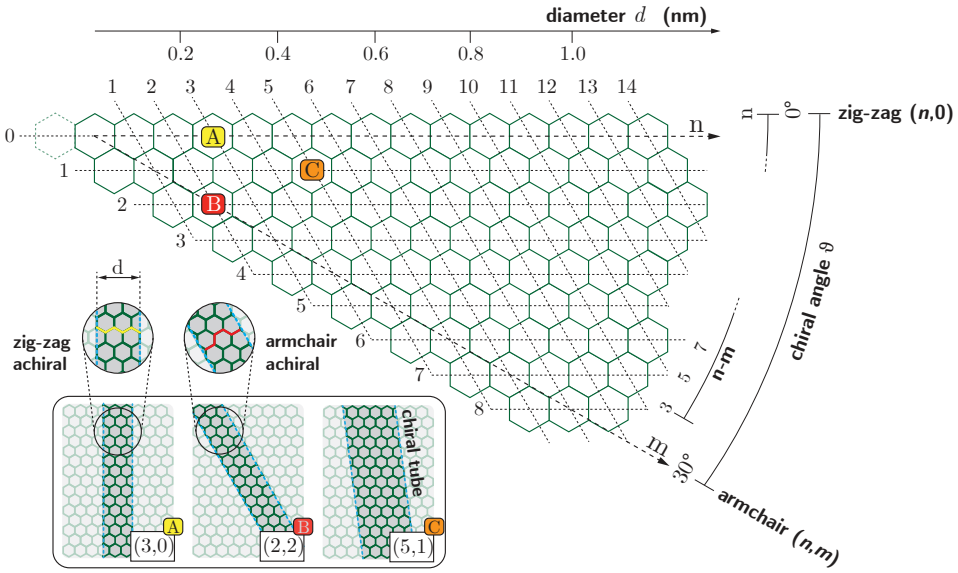

Figure 3.3: (n,m)-notation for the CNT chirality [77]: The maximum chiral angle ϑ can be 30° (considering symmetry) before the pattern repeats. The figure shows three examples for possible chiralities: The $(3,0)$ type is the narrowest zig-zag tube possible while the $(2,2)$ is the narrowest armchair tube possible. The $(5,1)$ example is a chiral tube and shows how n and m influence the chiral angle. The three examples are marked with A, B and C inside the (n,m)-notation scheme.

Figure 3.3 shows in detail how the (n,m)-notation works. A given set of n and m describes the shape of the specified CNT: The chiral angle ϑ can then be calculated from

$$\cos\vartheta = \Lambda^{-1/2}\left(n + \frac{m}{2}\right) \quad [74], \tag{3.3}$$

where $\Lambda = n^2 + nm + m^2$. With $|\vec{c}|$ being equal to the circumference, the diameter of the tube d is given by

$$d = \frac{|\vec{c}|}{\pi} = \Lambda^{1/2} \cdot \frac{a}{\pi} \quad [74]. \tag{3.4}$$

For $\vartheta = 0°$ the CNT is set in the zig-zag configuration, which corresponds to $(n,0)$. With $\vartheta = 30°$ the CNT is in the armchair configuration or (n,n). Both are not chiral, hence called achiral. However, every possible n,m-combination in-between $0° < \vartheta < 30°$ is in fact a chiral configuration. For the achiral configurations Λ can be simplified to

$$\Lambda_\mathrm{A} = 3n^2 \;|_\mathrm{armchair} \quad \text{and} \quad \Lambda_\mathrm{Z} = n^2 \;|_\text{zig-zag}\,. \tag{3.5}$$

3.1.3 Electronic Behavior Near the Fermi Level

In order to understand the electrical behavior of CNTs it is necessary to get acquainted with the energetic band structure of graphene. As discussed earlier only three of the four valence electrons of the carbon atoms are involved in the valence σ-bonding. This means the remaining electrons from the overlapping $2p_z$-orbitals of adjoining atoms form a bonding π-band and an anti bonding π^*-band (i.e. valence and conduction band). Since the π-electrons are the only ones being able to move through the lattice, they determine the relevant electronic band structure. According to the tight-binding approximation [78], the two-dimensional dispersion relation E_{2D} as a function of the wave vector $k = (k_x, k_y)$ around $E_F = 0\,\text{eV}$ can be written as

$$E_{2D}(k_x, k_y) = \pm\gamma_0 \left[1 + 4\cos\left(\frac{\sqrt{3}k_x a}{2}\right)\cos\left(\frac{k_y a}{2}\right) + 4\cos^2\left(\frac{k_y a}{2}\right)\right]^{1/2} \quad [78]. \tag{3.6}$$

The opposing signs represent the π-band or the π^*-band respectively. a is the in-plane lattice constant as introduced in equation 3.1 and γ_0 is the hopping energy, which is used to define the overlap to the adjoining atom. The entire function is visualized in figure 3.4 demonstrating that both bands actually touch at the K-points of the first Brillouin zone. Integrating over the Fermi distribution in the 2D-plane results in a zero density of states at these points. Since both bands touch at the K-points, graphene does not exhibit a band gap and therefore does not show any semiconducting behavior. Furthermore,

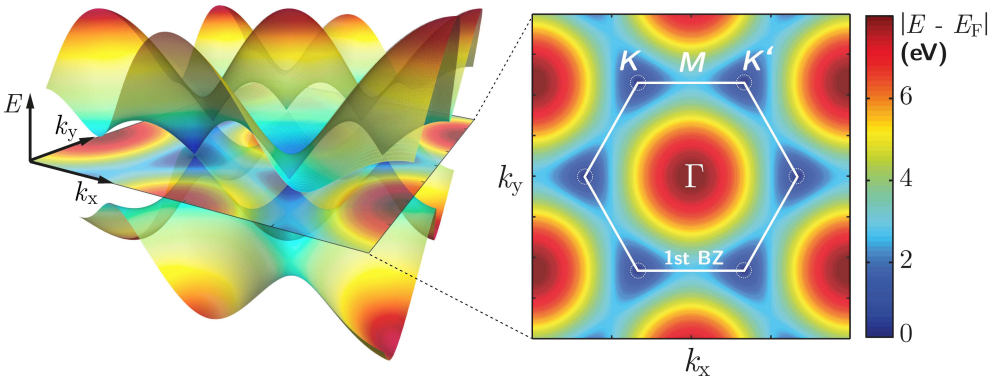

Figure 3.4: 3D (left) and 2D (right) visualization the dispersion relation of graphene as a function of k_x and k_y from equation 3.6. The plot is normalized for the the Fermi level to be in the middle at 0 eV. Both the π- and the π^*-band are symmetric and touch each other at the K-points of the first Brillouin zone (BZ) with no band gap.

when approaching the K-points the energy dispersion approximates to a linear function and electrons will behave like massless Dirac particles rather than fermions. This is expressed by a very low effective mass, resulting in an extremely high mobility, which is beneficial for many applications. Although this high mobility is very desirable for transistor devices as well, the lack of an actual band gap makes graphene rather unsuitable here[14].

Considering CNTs, which expand relatively large along their axis but very little along the circumference, the density of states is very different for those directions. While there are many possible states along the axis, the low number of atoms around the perimeter is keeping the density of possible states in the circumferential direction very low. When the graphene sheet rolls up along the chiral vector $\vec{c}$ to form a CNT, boundary conditions limit the density of states creating integer 1D-states on periodic modes propagating along the axis [79]. The periodic behavior is described by

$$\vec{c} \cdot \vec{k} = [n\vec{a_1} + m\vec{a_2}] \cdot \vec{k} = 2\pi j \ , \quad j \in \mathbb{Z} \quad [79]. \tag{3.7}$$

Considering the armchair configuration, that is $n = m = Z$, the x-direction of the wave vector points towards the CNT's axis while the circumference

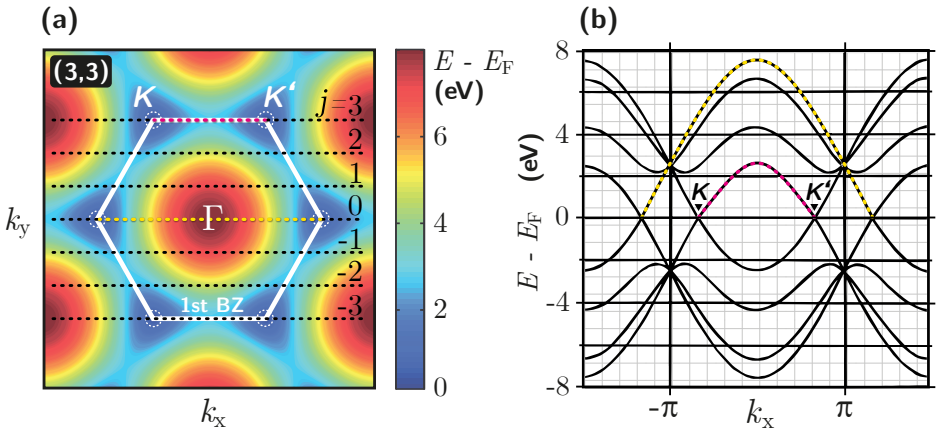

Figure 3.5: 2D-dispersion relation and band structure for an armchair $(3,3)$-CNT [79]. (a) 2D-dispersion relation for the first Brillouin zone Γ with projected states (dashed black lines). Obviously allowed states match with all K-points. (b) Corresponding band structure: Valence and conduction band meet at the K-points and since all K-points are allowed states the CNT exhibits metallic behavior. The dashed yellow and red line mark the corresponding states for $j = 3$ and $j = 0$ in (a) and (b).

[14] However, there is a lot of research concerning band gap engineering with graphene. In fact, it is possible to either cool down the system near to 0 K for confining all electrons into the π-band, or the graphene can be shaped into so-called nanoribbons. In this case graphene actually does exhibit a small band gap and registers as a semiconductor [28, 79–81].

corresponds to the y-direction. In this case, allowed states for the wave vector appear periodically based on equation 3.7 as

$$k_{\mathrm{y,j}} = \frac{2\pi j}{Z\sqrt{3}a} \quad [79]. \tag{3.8}$$

Inserting equation 3.8 into equation 3.6 the allowed states become lines crossing the dispersion relation $E(\vec{k})$. Figure 3.5a illustrates these lines for the first Brillouin zone of a $(3,3)$-armchair tube. The lines obviously cross the K-points, thus, making them available states. Since both π-bands touch each other at the K-points there is no band gap in-between and the $(3,3)$-CNT exhibits metallic behavior.

For the zig-zag configuration $(n = Z, m = 0)$ or $(n = 0, m = Z)$ equation 3.7 can be written as

$$k_{\mathrm{x,j}} = \frac{2\pi j}{Za} \quad [79], \tag{3.9}$$

now in which k_{x} points towards the circumferential direction. Considering equation 3.7 in case of $|n - m|$ being 0 or a multiple of 3, the lines of allowed states will always meet the K-points, and will thus, always lead to metallic behavior. For this reason, one third of all possible CNT configurations is in fact metallic (including all armchair configurations). [79]

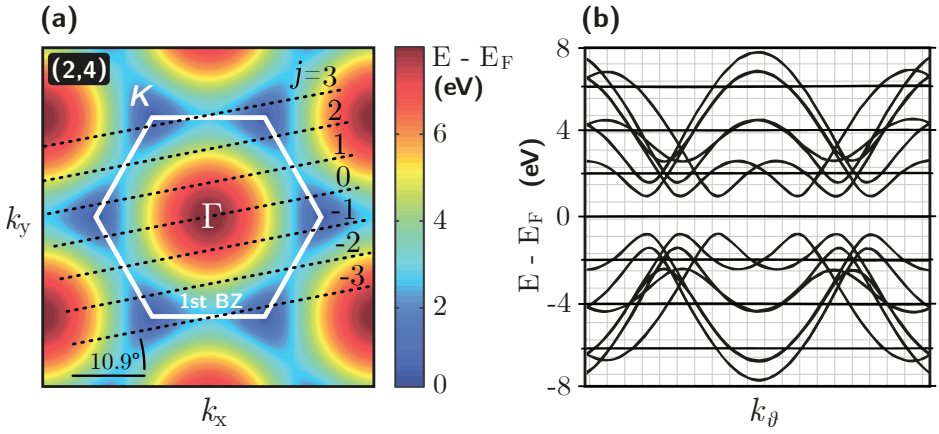

Figure 3.6: 2D-dispersion relation and band structure for a chiral $(2,4)$-CNT [66, 79]: (a) Projected lines of allowed states within the 2D-dispersion relation. In this chiral configuration there are no allowed states along the K-points. (b) Resulting band structure for this chiral configuration. In contrast to the armchair CNT in figure 3.5 a band gap does exist. Here, k_ϑ represents the direction of the wave vector along the chiral angle $\vartheta = 10.9°$ (since it does not match with neither k_{x} or k_{y}).

For the remaining two thirds of all possible configurations, electronic characteristics are decisively different. Figure 3.6 shows how allowed states fall into place for chiral CNTs. In this case the dispersion relation and band structure of a $(2, 4)$-configuration is illustrated (analogous to figure 3.5). Using equation 3.3 the chiral angle ϑ in this example is $\sim$10.9° and allowed states do not meet with the K-points. As a consequence, the lines of allowed states correspond to 1D-cutouts of the dispersion relation, where both valence and conduction band maintain a specific band gap at any time, hence the semiconducting behavior. [66, 79]

The size of the band gap E_g for chiral CNTs depends on its diameter d as $1/d$. Note that simulations and analytical data sometimes do not perfectly match with empirical measurements. Different models may lead to slightly different results: Niranjan et al. [82] calculated the band gap for a large number of possible tube configurations. They compare numerical self-consistent tight binding simulations and ab-inito density functional methods in order to calculate the band gaps. As expected, they receive small deviations in results for the two models. Alternatively, applying the analytical approach by unfolding the full tight binding calculations (as done by [21]), the band gap is eventually given by

$$E_\mathrm{g} = \gamma \left| j - \frac{2n+m}{3} \right| \cdot \frac{2\sqrt{3}a}{d} \quad [21]. \tag{3.10}$$

For calculating the gap from the first conduction band to the first valence band, i.e. the regular band gap, j must be the nearest integer of $\frac{2n+m}{3}$ and the hopping energy γ must be $\gamma_0 = 2.8\,\mathrm{eV}$ [28, 78]. The results from this equation are very close to the data from Niranjan. In fact, the values can always be found in-between the two results Niranjan et al. calculated with their mentioned models. From the same analytical origin explicated in [21], the effective carrier mass m^* can be calculated by

$$m^* = \gamma^{-1} \left| j - \frac{2n+m}{3} \right| \cdot \frac{1}{\sqrt{3}ad} \cdot 4\hbar^2 \quad [21]. \tag{3.11}$$

Note that CNTs possess a symmetric band structure, thus identical effective carrier masses in the valence and conduction band [21]. Table 3.1 compares the effective carrier mass m^*, the intrinsic carrier density n_i and the band gap E_g for selected diameters. With larger diameters, electrical properties of CNTs are getting more interesting for transistor applications. However, extremely large diameters should be avoided, because leakage current increases with small E_g. Reported carrier mobilities are in the range of 10^3 to $79{\cdot}10^4\ \mathrm{cm^2/Vs}$ being notably high compared to silicon and other alternative channel materials [63, 83, 84].

	(5,0)	(4,2)	(5,1)	(7,3)	(9,2)	(11,3)
d (Å)	3.94	4.17	4.39	7.01	8.00	10.07
m_e^* (m_0)	0.408	0.271	0.159	0.116	0.099	0.108
n_i (cm^{-3})	$\sim 10^5$	$\sim 10^7$	$\sim 10^8$	$\sim 10^{13}$	$\sim 10^{14}$	$\sim 10^{15}$
E_g (eV)	1.821	1.721	1.635	1.024	0.897	0.713

Table 3.1: Electrical properties of selected CNTs (n, m) [66]. Obviously the small-diameter CNTs are not particularly beneficial when compared to silicon. However, CNTs of larger diameters as the $(9, 2)$-configuration for example, exhibit smaller band gaps, have significantly low effective electron masses and show much higher concentrations of intrinsic carrier densities. (m_0 is the mass of an electron $9.1094 \cdot 10^{-31}$ kg.)

3.2 The Schottky Barrier at the CNT-Metal Interface

Given the information from this chapter thus far, transistors made from CNTs seem to be an ideal choice. However, one issue remains that has not yet been addressed and needs to be discussed: Since the goal of this work is the actual fabrication and characterization of carbon nanotube transistors, the need to somehow contact the device is very obvious. Therefore, a metallic layer has to be deposited directly onto the carbon nanotube. In case of metallic tubes one should consider that carrier transport at the CNT- metal interface is non-ballistic and is dominated by carrier backscattering events. This includes scattering from impurities, phonon scattering and electron-electron scattering depending on the operating temperature.[15] More important however are observations regarding a metal interfacing with semiconducting nanotubes. At a conventional 3D-semiconductor to 3D-metal interface a Schottky barrier ϕ_{SB} will suppress carrier injection to the semiconducting material. The height of the barrier usually depends on the difference of the work function of the metal and the electron affinity of the semiconductor. This means the height can vary depending on doping and the element or alloy being used as contact material and eventually the barrier can be exceeded (barrier-free MOSFET). For 1D materials like carbon nanotubes some older studies assume that high work function materials such as nickel or gold enables hole injection to the valence band, thus, eventually overcoming the barrier as well [85, 86]. When using carbon nanotubes with small circumferences a very high carrier injection through the Schottky barrier occurs, which lead to misinterpreting the results of these early studies. The implications of that are discussed later in this section.

[15] The details on that matter go far beyond the scope of this thesis. Nevertheless, measuring the intrinsic conduction of a metallic tube (which could also be unintentionally when it is unclear to the operator which type of CNT is in use) might lead to false results due to changes in contact resistance caused by the backscattering events [79].

Despite the mentioned studies claiming that a Schottky barrier can be neglected under some circumstances, a simple CNTFET can actually be best described by assuming that it does in fact behave like a Schottky barrier (SB)-MOSFET: Figure 3.7 shows the conduction band in the presence of a Schottky barrier (following the Schottky-Mott rule). For a gate potential above the barrier the transistor will act like any conventional MOSFET. If the gate potential moves the conduction band of the channel below $-e\phi_{\mathrm{SB}}$, carrier injection occurs by tunneling through the barrier (with transmission probability $T(E)$). At this point, transfer characteristics aggravate and the inverse subthreshold slope increases above $60\,\mathrm{mV/_{dec}}$. According to [21], the easiest way to describe the drain current I_{D} of the SB-MOSFET is by introducing an effective Schottky barrier:

$$\phi_{\mathrm{SB}}^{\mathrm{eff}} = (\phi_{\mathrm{SB}} - \phi_{\mathrm{G}}) \exp\left(\frac{d_{\mathrm{t}}}{\lambda_{\mathrm{ch}}}\right) + \phi_{\mathrm{G}} \quad [21], \tag{3.12}$$

where ϕ_{G} is the gate potential (representing the position of the conduction band at ideal conditions), d_{t} is the tunneling distance and λ_{ch} is the channel geometry factor as initially introduced in equation 2.13. Skipping the calculation done in [21] and looking at the result, the drain current I_{D} is expressed as being proportional to $\exp\left(-\phi_{\mathrm{SB}}^{\mathrm{eff}}/k_{\mathrm{B}}T\right)$. Naturally, this also affects the inverse subthreshold slope S, which consequently, for a SB-MOSFET is:

$$S = \left(\frac{\partial\, \log I_{\mathrm{D}}}{\partial\, V_{\mathrm{G}}}\right)^{-1} \overset{\lambda_{\mathrm{ch}} > d_{\mathrm{t}}}{\approx} \frac{k_{\mathrm{B}}T}{e}\ln(10)\left(\frac{1}{2} + \frac{\lambda_{\mathrm{ch}}}{d_{\mathrm{t}}}\right) \quad [21]. \tag{3.13}$$

Now, having λ_{ch} being a part of equation 3.13 it becomes evident that the SB-MOSFET's performance heavily depends on the transistor geometry. As a reminder λ_{ch} is equal to $\sqrt{\frac{\epsilon_{\mathrm{Si}}}{\epsilon_{\mathrm{ox}}} t_{\mathrm{ox}} t_{\mathrm{ch}}}$, deducing that the gate thickness t_{ox} will have a strong influence on S. The same dependence can be observed when characterizing CNTFETs with back-gate configurations [31, 87]. In addition, a CNTFET also exhibits ambipolarity just like any conventional SB-MOSFET.

To avoid limitations for S by the Boltzmann part $k_{\mathrm{B}}T$, SST architectures - as discussed in section 2.2 - must be implemented. However, not all observations concerning the CNTFET-contact can be applied to SB-MOSFET behavior. Some data show that differences in drain current of CNT devices are higher for some contact materials than for others [88]. This behavior is most pronounced for tubes with large band gaps (i.e. tubes with small diameters). Similar nanotube devices with band gaps above 1 eV have been contacted with different materials and showed significant deviations from SB-MOSFET transfer characteristics. However, it is reported by Tersoff [89] that the wave

function significantly attenuates in radial direction due to a very high potential barrier (>10 eV) at the metal-tube interface. Although this barrier is very high, it is extremely thin and can be ascribed to the Van-der-Waals distance between the two materials. For small band gaps (i.e. tubes with larger diameters), the distance eventually leads to the suppression of Fermi level pinning, acting like a so-called depinning layer. With this in mind, the Schottky-Mott rule for CNT transistors is fully sufficient. In addition, tunneling is a fundamental part of the CNTFETs characterized within the experimental part of this thesis. That alone will substantially limit the current inside the channel, inasmuch that any given contact-related issues will be of secondary concern. [21, 90]

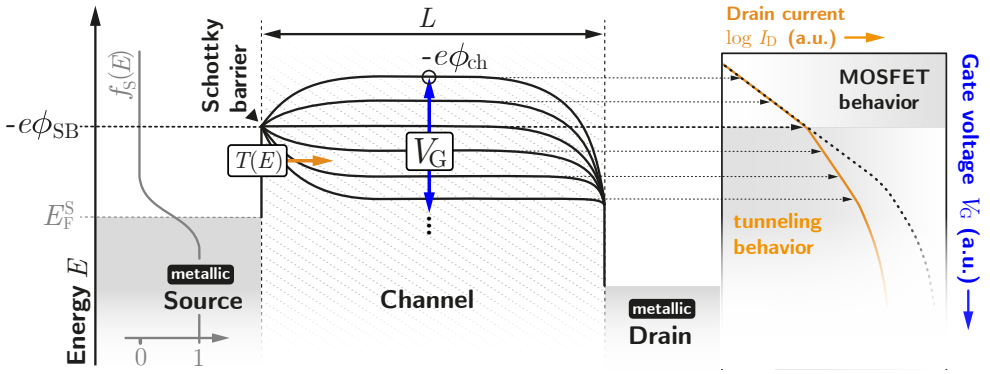

Figure 3.7: Conduction band of the SB-MOSFET [21, 22]: As long as the gate potential is higher than the Schottky barrier (SB), the device behaves like a conventional MOSFET at ideal conditions. Below the SB, carriers have to tunnel (with transmission probability $T(E)$) through the barrier in order to maintain injection into the channel region. For low values of $T(E)$, S will drift above 60 $^{mV}/_{dec}$ aggravating off-state performance.

3.3 Large Scale Synthesis

There are numerous methods for synthesizing CNTs that can be found in the respective literature [91–98]. A chemical vapor deposition (CVD) technique is the most significant method in terms of being the most suitable for large scale production, albeit there are two methods worth mentioning beforehand: In 1991, CNTs have been accidentally discovered in soot on graphite electrodes after an arc discharge occurred [71]. After experimental research on this matter, it soon became the first stable method to synthesize CNTs [93]. Operating within a temperature range of over 1,700 °C, the technique causes the CNTs to have few structural defects and impurities [99]. Nevertheless, the process turned out to be not very practical and produced CNTs were almost exclusively multi-walled. They exceeded 50 µm in length in most cases [100], which is less attractive for electronic devices. A few years later in 1996, T. Guo et

al. discovered a novel laser technique. They used a pulsed laser to vaporize graphite inside a high-temperature chamber. The carbon atoms mixed with an inflow of argon gas and formed nanotubes on the cooler surfaces of the chamber [101]. Because this method produced primarily MWCNTs, Guo et al. later improved the process by introducing metal catalysts such as cobalt and nickel into the process. In consequence, they managed to yield at least a 70 % production of SWCNTs where the tube diameter is controlled by the reaction temperature [70]. Although this method is highly productive it is yet too expensive to be profitable [100].

3.3.1 Synthesis via CVD Processes

Over the past years, the CVD process has become the most commonly used procedure for CNT production [102]. Within the field of CVD processes there are many ways to serve the same purpose. However, they all achieve material deposition by the chemical decomposition of gases and then using the components to create new solid materials.[16] A common CVD technique for the growth of CNTs is the so-called vapor-liquid-solid process (VLS).

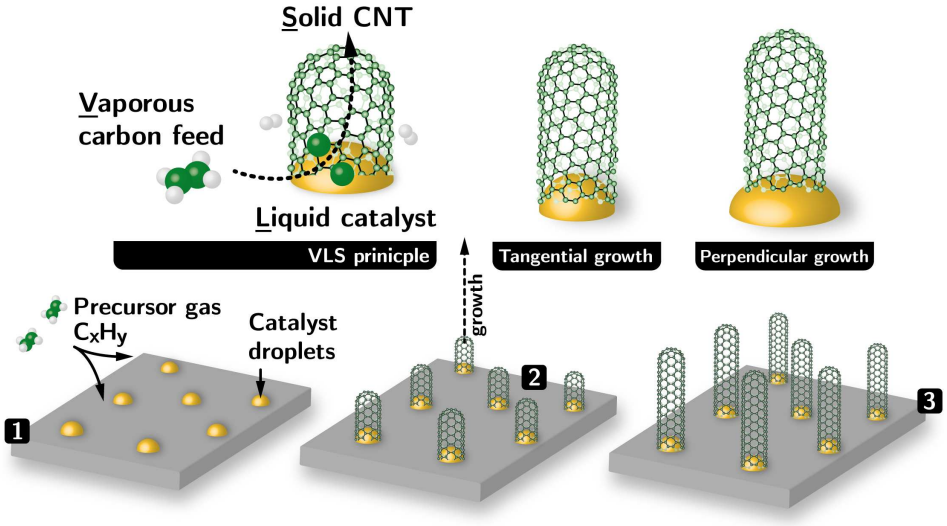

Figure 3.8: CVD-VLS process [91]: First, metal catalysts are deposited onto a substrate and heated to their melting point. Second, a carbon-based precursor gas is supplied and dissolves inside the catalysts forming a carbon-metal alloy. Third, when the catalysts are fully saturated with carbon, the carbon atoms emerge at the catalyst droplet's surface beginning to grow a carbon nanotube. The tubes can either grow in a tangential mode or in a perpendicular mode with respect to the surface.

[16] Usually the energy for the reaction is drawn from high temperature. Some processes use ionized gas making the reaction occur at much lower temperature. In this case the change of phase will be from plasma to solid.

As shown in figure 3.8, the VLS process uses metal catalysts such as nickel, cobalt, copper, gold, combinations of such and in some cases iron-manganese alloys [91, 103, 104]. Small nanoparticles of these catalyst materials are getting deposited onto large substrates for heat conditioning. When they change phase from solid to liquid a carbon-based precursor gas is added to the process. At high temperature the gas will diffuse inside the liquid catalysts, reacting to form a carbon-metal compound. If the catalyst becomes highly saturated with carbon, a catalytic fission leads to carbon accumulation at the surface creating small caps. Subsequently, these caps extrude to form CNTs once additional caps become energetically unfavorable due to curvature strain [105–109]. In their research Fiawoo et al. [110] describe that there are two possible modes for the tube to grow; tangential growth or perpendicular growth with respect to the catalyst's surface (cf. figure 3.8). When growing tangentially, the circumference of the tube is nearly of the same size as of the catalyst droplet. However, the perpendicular growth causes the circumference to be smaller and independent from the size of the catalyst. During the process, these two types of the so-called nucleation compete with each other. Fiawoo et al. reported that the perpendicular growth occurs when the process conditions are not at the local thermodynamic equilibrium. To enforce this, they propose to add nitrogen [111–113] or sulfur [114] to the carbon feed because the hetero-atoms might interact with the catalyst's surface. Since the catalyst is liquid in the process, interaction between catalysts and the tube edges tend to limit progress in having a selective growth.

According to Yang et al. [115] catalysts with very high melting points are more suitable for a selective growth. In this case the catalyst stays in its solid crystalline structure and the CNT begins to grow in a more controlled manner, thus enhancing selectivity. By the use of high melting point-catalysts the technique is then renamed vapor-solid-solid process (VSS). Although the VSS process is considered to be more beneficial it is quite a challenge to find catalysts matching the correct requirements. Li et al. [91] recommend using tungsten-based alloys such as W_6Co_7.

3.3.2 Selective Growth Mechanisms

As discussed in section 3.1.3 the electrical properties of CNTs depend on their chirality. The achiral armchair configurations always show metallic behavior, meaning they are unsuitable for transistor devices. Thus, previous discussions on synthesis have to be supplemented by methods of how a certain selectivity towards preferable chiral angles can be realized. Molecular dynamic simulations by Ding et al. [116] as well as other theoretical and experimental studies [117–120] show that it is of energetic advantage for

SWCNTs to grow with large chiral angles or even to grow entirely achiral. Additionally, Artyukhov et al. found that chiral tubes are more likely to grow faster [121]. These two observations are not contradictory and manifest in enriched growth near armchair configurations $(n, n-1)$ such as (9,8) or (6,5). For the VLS process, roughly one-third of the tubes grow in the achiral armchair configuration. Attempting to avoid armchair CNTs[17] all along, the focus lies on the VSS process in which catalysts remain solid state. In this case, selective growth will then be accomplished by adjusting the interaction between nanotube edges and catalysts through the selection of different metals. Further, Gomez et al. discuss the effects of special metal substrates for keeping the crystalline structure of the metal catalyst at high temperature, thus limiting the diffusion of carbon atoms into the tube [122]. This way a favorable growth can be chosen by the metal surface. It is suggested that the deposition of the catalyst should be done by epitaxy. If done so, atoms of the catalyst could match the edge of the tube specifically enough to eventually determine the growth for a specified chirality [123]. Obviously the making of matching catalysts is a complete study on its own

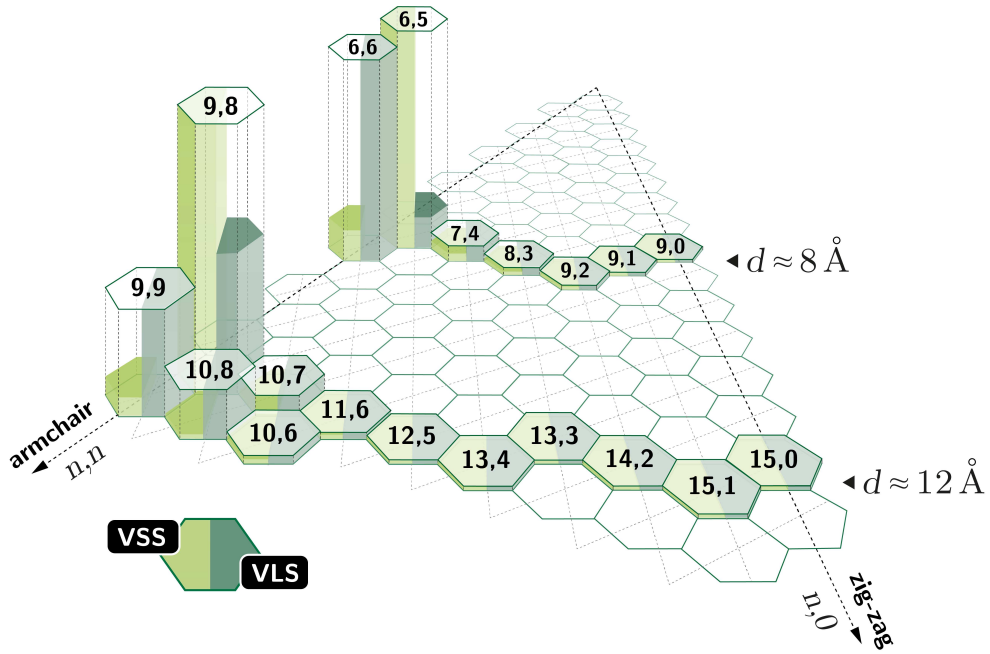

Figure 3.9: Simulated chirality distribution [116]: The molecular dynamics study of Ding et al. handle catalysts for CNT diameters of ∼8 Å and ∼12 Å. Growth via the VLS process causes more CNTs to be in undesired (n, n) armchair configurations. The VSS process on the other hand creates mostly chiral $(n, n-1)$-CNTs. The advantage clearly emphasizes for the 8 Å set.

[17] SWCNTs in armchair configuration exhibit metallic properties, see section 3.1.3.

and would go far beyond the scope of this work.[18] Figure 3.9 shows how Ding et al. simulates the growth with two sets of diameters. It turns out that chiral CNTs with a high chiral angle ϑ are more likely to arise from the VSS process. In this case a majority ($\geq 80\,\%$) of all CNTs is distributed within a $(n, n-1)$ configuration.

Besides the catalyst, reaction conditions must be perfectly adjusted as well. Although research in this field has extensively increased, there are still no universal guidelines to obtain the best growth conditions. Temperature, chamber pressure and carbon feed are very critical elements when it comes to selective chirality and diameters. Table 3.2 shows how temperature affects the diameter during the process. Based on their experiments, Zoican et al. [124] and He et al. [125] find that with higher temperatures larger tube diameters will occur. The choice of the medium providing the carbon is also highly important since basically all of the qualified carbon sources are combined with other elements such as hydrogen or oxygen. In the form of aggressive radicals those by-products do play an important role in the assembly of the CNTs [126, 127]. Most used sources are ethanol (C_2H_6O), carbon monoxide (CO), methane (CH_4), acetylene (C_2H_2) and ethylene (C_2H_4) [128–131].[19]

T (°C)	6.8 Å	8.8 Å	10.8 Å	12.8 Å	14.8 Å	T (°C)	(6,5)	(7,5)	(8,4)	(7,6)
600	66.6 %	31.6 %	7.69 %	33.3 %	0 %	600	47.6 %	9.09 %	6.66 %	12.5 %
700	16.6 %	42.1 %	38.4 %	33.3 %	0 %	750	33.3 %	45.4 %	46.6 %	37.5 %
800	16.6 %	26.3 %	53.8 %	33.3 %	100 %	800	19.1 %	45.4 %	46.6 %	50.0 %

Table 3.2: Process temperature affecting the CNT's diameter: Left: Relative distribution of diameters of grown tubes (measurements taken from Zoican et al. [124]). The higher the temperature the larger the diameter. Tubes with greater diameters than 14.8 Å only occur at temperatures around 800 °C. In this setup a CoMn–MCM-41 bimetallic catalyst was used. Right: Relative distribution of photoluminescence emission intensities corresponding to shown chiralities (measurements taken from He et al. [125]). Higher temperatures might also increase the probability for near 30°-chirality angles. Here a MgO supported FeCu catalyst is used.

In 2008 an efficient floating-catalyst method named enhanced direct injection pyrolytic synthesis (eDIPS) was developed [133]. It uses two kinds of hydrocarbons with different decomposition properties. Because of its high efficiency and productivity, the eDIPS is one of the most suitable processes

[18] Note that Li et al. [91] published a comprehensive article on that subject covering all important aspects of catalysts and chirality-selective growth in general.

[19] The thermodynamic stability strongly varies among these sources. The decomposition of methane requires higher temperatures, while the use of acetylene, ethylene, and ethanol is easier to implement since they decompose exothermally at atmospheric pressure [132].

for large scale production of CNTs [134]. The advantage comes from conditioning multiple carbon sources for a high diameter-controlled assembly. As demonstrated in figure 3.10, eDIPS using ethylene as additional carbon source allows the diameters to be very well controlled. Opposing to intuition a higher flow rate of an additional carbon precursor does not lead to wider tubes. Instead, a 100 % increase in flow rate caused 30 % shorter diameters on average [135].

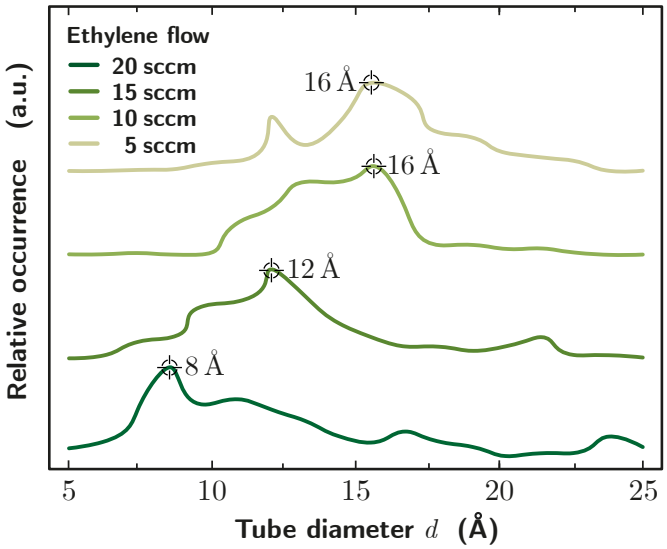

Figure 3.10: Influence of ethylene flow as additional carbon source on the eDIPS process [135]: By adjusting the ethylene flow the tube's diameter can be tuned within a range of a few Ångströms: Increasing the flow will cause slightly shorter diameters.

3.3.3 Extraction and Purification

Obviously the production process does not end with CNTs fully grown to their desired lengths. As emphasized in subsection 3.3.2, most CNT synthesis methods use metal catalysts in the process. When the carbon atoms emerge at the catalyst surface they entangle at the interface. This causes the CNTs to be attached to the metal, which has to be removed in post processing (among other impurities). The entanglement is even more pronounced when the growth originated from tangential nucleation [136]. Besides metal removal the extraction and purification procedure includes identifying and sorting out CNTs with structural defects. Impurities which are neither defects nor residues of catalysts can be avoided by using high CVD process temperatures to begin with. The assessment of impurities is usually done by scanning- and transmission electron microscopy (SEM, TEM), thermo gravimetric analysis

(TGA) and Raman spectroscopy [137]. The TGA process is a very fast and effective method to determine the amount of metal and carbonaceous impurities by simply oxidizing the CNT samples. A high temperature is always related to less defective and purer CNTs [138]. Because of the strong correlation between impurities and temperature the TGA process can be used as a relatively precise tool in a repeating control routine. A brief review of several assessment tools is given in table 3.3.

Tool	Carbonaceous impurities	Metal impurities	Structural defects	Conductivity features	Advantage
SEM/ TEM	HQ	HQ	Q	NQ	Direct Observation
TGA	Q	Q	NQ	NQ	Direct assessment of level of impurification
Raman	HQ	NQ	HQ	Q	Diameter, quality and conductivity features
UV-vis-NIR[a]	Q	NQ	NQ	Q	Quality and conductivity features
EDX[b]	NQ	Q	NQ	NQ	Elemental resolution, best for tiny residues

Table 3.3: Comparison of important purification assessment tools by Hou et al. [137]. HQ: Highly qualified, Q: Qualified, NQ: Not qualified. ([a]Ultraviolet visible near-infrared spectroscopy; [b]Energy-dispersive x-ray spectroscopy.)

Once the quality is determined, the actual purification takes place. There are basically two categories for this process; chemical and physical purification. The chemical based process is subdivided into a selective oxidation process, in which carbonaceous impurities will be oxidized more aggressively and therefore faster than the CNT itself. Afterwards, in a second chemical process, the metallic impurities or metallic residues respectively are dissolved by strong acids. A major disadvantage of the chemical treatment lies in the inevitable impact on the structure of CNTs. In every oxidation process - despite all possible precautions - the carbon of the tube will eventually react with the oxygen leading to undesired carbon modifications. [137]

The physical purification process sorts out impurities based on individual characteristics such as size, molecular weight, aspect ratio or magnetic properties. The separation process is done without any invasive tools and keeps the CNTs undamaged. However, a physical based purification is rather laborious as well as time consuming and expensive. In their research, Hou et al. propose to use a combination of both chemical and physical purification in order to combine advantages and avoid disadvantages [137].

Chapter IV
Experimental Methodology

MANUFACTURING of carbon nanotube transistors and affiliated substrates includes some typical optimization procedures for many steps during the process. Therefore, it is important to understand the fundamentals of the methods itself in order to change parameters on educated decisions. This chapter provides detailed information about the experimental methods used for this work. This includes state of the art material deposition methods, lithography procedures and setups for electrical characterization.

4.1 Deposition Methods

Material deposition in semiconductor technology requires the reproducible generation of homogeneous, particle-free layers that have high electrical quality and a low concentration of impurities. It is desirable to deposit these layers without strain and at the lowest possible temperature on arbitrary substrate surfaces. The deposition methods developed for this purpose can be divided into chemical and physical deposition techniques. Monocrystalline, polycrystalline and amorphous layers can be applied to a substrate surface using vapor deposition. The methods to be discussed are thermal evaporation and sputtering, which belong to the group of physical vapor depositions (PVD). In general, PVD is widely used for the application of metallic layers, however, dielectric materials are possible as well. Furthermore, this section also introduces plasma enhanced chemical vapor deposition (PECVD), which can only be used for non-metallic materials.

4.1.1 Thermal Evaporation

To achieve deposition by thermal evaporation, a solid material in a so-called boat source is heated in a high vacuum chamber to such an extent, that its atoms transitions to the gaseous phase. They then distribute in the chamber and deposit over the entire surface on the substrates attached inside the chamber. Since the source and the substrates are spatially distant from each other and only very few scattering processes take place due to the high vacuum, the evaporating particles move in a straight line and hit the surface perpendicularly. Consequently, the even coverage i.e. conformity[20] of the process is very low. Heating of the source is achieved by applying electrical current to the source, which is usually made from high-melting metals, such as tungsten or tantalum. The target material quickly melts in the boat and then vaporizes with increasing temperature. Alternatively, an electron beam is deflected onto the source to heat the target material. Since the power of the electron beam can be controlled very fast and precisely, the evaporation rate can be controlled more precisely than with thermal evaporation. However, for the processes in this work only the electrically heated evaporation type were used. The pressure inside the chamber during the process normally settles around $4.0{\cdot}10^{-5}$ mBar. Materials that qualify for thermal evaporation are primarily metals because of their lower melting points. Widespread used materials are aluminum, gold and titanium. Dielectric materials often exhibit considerably higher melting points and are not suitable for thermal evaporation. However, some exceptions are tungsten oxide or molybdenum dioxide. The latter has a melting point of only 795 °C. [139, 140]

[20] Conformity is defined as the ratio of horizontal deposition to vertical deposition [139].

4.1.2 Sputtering

In this process, accelerated ions inside a vacuum chamber collide with atoms or molecules from a mounted target, which in the simplest case consists of the material of the layer to be applied. Ejected atoms or molecules disperse with an energy of roughly 1-10 eV in the vacuum of the chamber and accumulate everywhere in the chamber including the substrate's surface. Compared to thermal evaporation, the process takes place at higher ambient pressures around $7.0{\cdot}10^{-3}$ mBar, so that the mean free path of the particles is only a few millimeters. Consequently, the molecules experience some changes in direction as a result of collisions with the residual gas in the chamber. They do not spread in a straight line, but hit the substrate's surface at any angle and accumulate on both vertical and horizontal surfaces.

In most cases the ions come from an argon feed since it is a non-reactive noble gas. Using DC-sputtering, the target is charged generating a static electrical field, which accelerates the ions towards its surface transferring their momentum. Since the target must be able to discharge, only conductive materials can be used as target with this deposition method. Sputtering non-conductive materials demands for a high-frequency (HF) setup with an alternating voltage (cf. figure 4.1). Due to the different mobility of the electrons and the argon ions in the plasma, the target is charged negatively because the electrons migrate to the target during the positive half-wave of the HF and charge the target, but cannot leave during the negative half-wave since the energy does not exceed the work function of the electrode. The argon ions are thus subject to the electrical field on average over time, which results from the negative charging of the target. The efficiency of both techniques is extremely low at a maximum of 1 %, so that the power loss has to be dissipated by a cooling system. To increase efficiency and deposition

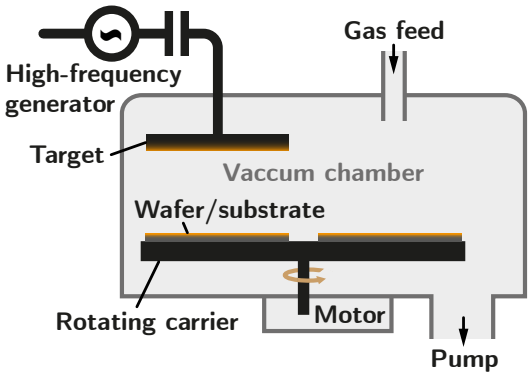

Figure 4.1: Sketched layout of a high-frequency sputtering system with a rotating carrier disk for multiple wafers. Such systems can also contain multiple targets.

rate, built-in permanent magnets in state of the art systems do deflect the plasma above the target (magnetron-sputtering). As a result, the electrons inside the chamber move in circular paths around the target and increase the ion impact density at the target's surface. This causes an increased material removal, so that the process is suitable for high-rate coatings.

Another subtype is the so-called reactive-sputtering, where a reaction gas is added to the inert gas. A chemical reaction takes place between the sputtered material and the molecules in the gaseous phase. As a result, insulating materials, such as aluminum oxide can be deposited by using an aluminum target and an additional oxygen feed. Sputtering a titanium target combined with a nitrogen feed will produce the commonly used titanium nitride metal. The conformity of sputtering is about 0.7, being significantly higher than the conformity of thermal evaporation, which is almost zero. [139, 140]

4.1.3 Plasma Enhanced Chemical Vapor Deposition

The plasma enhanced chemical vapor deposition (PECVD) process typically operates at temperatures around 250-350 °C. Thus, the thermal energy is not sufficient for pyrolysis, which means that gases injected to the vacuum chamber need to be additionally excited and decomposed by high-frequency ionization for the gases to react on the surface of the substrate (usually in a parallel plate reactor). Due to the low process temperature, PECVD is used in particular for passivation of surfaces or for intermediate insulation purposes after metal deposition. Conductive layers of amorphous silicon can be deposited as well. Although related processes with higher operating temperatures, such as low pressure CVD (LPCVD), produce significantly denser and electrically more stable insulators (oxides), the high temperatures lead to critical expansion of integrated metal layers, that might damage the substrate. [139]

Common oxides produced by PECVD are silicon dioxide (SiO_2) and silicon nitride (Si_3N_4). SiO_2 is deposited by using a combination of silicon precursor gases like monosilane (SiH_4) and oxygen precursors, such as pure oxygen or nitrogen dioxide (NO_2), typically at pressures ranging from a few millitorr to a few torr. Si_3N_4 is produced from monosilane and ammonia (NH_3) or nitrogen and is usually composed in a dual-frequency reactor applying both high and low frequencies in an alternating sequence to avoid intrinsic stress [141]. The PECVD process has a relatively low impurity density and can achieve very high deposition rates of up to $500\,^{\mathrm{nm}}/_{\mathrm{min}}$ with a conformity of > 0.5. However, the overall outlay on equipment and gas throughput of the entire process are relatively high.

4.2 Lithography Processes

The function of an exposure process (i.e. lithography) is to create a soluble pattern in a radiation sensitive film, called the photoresist. The exposed parts of the photoresist can then be removed with a liquid developer. Afterwards, the pattern can then be permanently transferred into the wafer/substrate via any number of subsequent processes like metalization or etching. With respect to the type of exposure, lithography can be divided into three methods: optical lithography (UV-lithography), electron beam lithography and X-ray lithography. The latter is a highly sophisticated operation, that is almost entirely reserved to industrial fabrication and can be neglected here. The multi-gate platforms, as presented in this work, are manufactured by using UV-lithography. The subsequent fabrication of carbon nanotube transistors on these platforms makes use of electron beam lithography with much higher resolution capabilities.

4.2.1 Optical Lithography

In order to expose the photoresist on a silicon wafer, optical lithography requires a mask (reticle) as a pattern template, which is usually a transparent quartz plate with a patterned chromium coating. Light with a characteristic UV spectrum (typically 365 nm, i-line) is then projected in an optical system through the mask onto the wafer. The exposed photoresist becomes solvable by a developer, while photoresist under the chromium does not receive any light exposure and remains intact after developing. The result is the pattern template of the mask replicated within the photoresist.

There are several projection and lens systems available for the desired result. However, in this work the preferred method is contact lithography, which does not utilize any lenses or light projection. The wafer has either unforced direct contact to the mask (soft contact) or is pushed against the mask by pressurized air (hard contact). Note that due to the constant contact between wafer and mask, enclosed particles may introduce defects and strain into the process. Moreover, the mask must be frequently cleaned in order to prevent particle deposition. The resolution of contact lithography is limited by the diffraction effects at the structure edges, so that, depending on the wavelength and photoresist used, minimum structure widths of $\sim$0.8 µm for 436 nm wavelengths down to $\sim$0.4 µm for 248 nm wavelengths are possible [142]. Alignment limitations for procedures on existing structures (overlay lithography) are given by the wafer-to-mask displacement mechanics and by the focus capabilities of the observing microscope. In general, a restricted alignment scope as high as 0.5-1 µm is realistic.

4.2.2 Electron Beam Lithography

Instead of UV-light exposure, a focused beam of electrons can depolymerize a special resist, which then becomes solvable. This high-resolution alternative technique is referred to electron beam lithography (EBL, or e-beam lithography). The patterning masks for EBL are created with CAD software using the GDS format, which is extremely fast to implement and easy to modify. Unlike optical lithography, masks for EBL are inverted, because a surface element in the CAD-mask is not shielding the resist from light, but indicating where to actually exposure the resist with electrons. The theoretical resolution limit is marked by the de Broglie wavelength, that is, 0.12 Å at 10 kV accelerating voltage. In practice, the resolution is determined by the degree of focal precision and electron scattering in the resist (and in the sample) also known as proximity effect. Ultimately, the maximum resolution for the smallest pattern is about 3 to 10 nm [143].

A research-EBL system is usually based on a SEM-column with additional control units. It consists of an electron source (the filament), a complex apparatus of electrostatic and magnetic lenses, one or more electron detectors and an interferometric stage to control the substrate position (cf. figure 4.2). In contrast to optical lithography, the exposure cannot be done at once. The focused beam has to be deflected by the lenses in order to create a two-dimensional pattern on the resist according to the CAD-mask. The EBL operator software generates a writing line model for any polygon to be

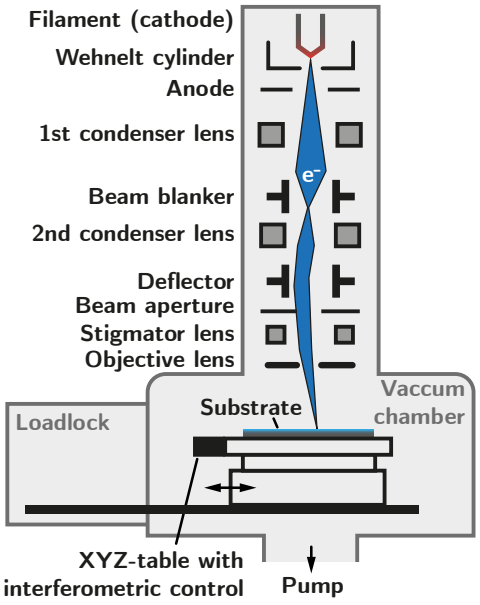

Figure 4.2: Sketched layout of the beam column of an e-beam lithography system. The beam passes multiple stages of lenses and deflection units until it is focused onto the substrate. To gain highest mean free path of the electrons, an ultra-high vacuum is provided. Note that usually an EBL system is combined with electron detectors to implement a scanning electron microscope (SEM), which is not shown in the figure. Also note that column technology differs from kind to kind. The shown lens configuration is exemplary.

scanned by the beam. This time-consuming line-by-line scanning is the largest disadvantage of EBL. However, EBL is capable of creating extremely small structures with ultra high alignment accuracy at relatively low labor. The EBL system used for this work is a Raith Pioneer machine relying on a Zeiss Gemini SEM column with a maximum accelerating voltage of 30 kV.

4.3 Electrical Characterization

The used measurement setup accessible at the lab consists of an Everbeing probe station with an Agilent 4156C parameter analyzer equipped with four source measuring units (SMUs) and two voltage source units (VSUs). The analyzer is operated in the so-called sweep mode, where one cycle consists of a sweep of one variable (e.g. gate voltage) and the full measurement is composed by several sweeps under variation of a second parameter (e.g. drain-source voltage). Figure 4.3a shows a sample in a typical configuration with five probing needles touching the contact pads. Since the majority of samples had gold contact pads, the used needles were also made from gold to minimize the risk of scratching or damaging the pads. The sample resides on a vacuum chuck, which is temperature controlled and can be heated up to 423 K (150 °C). Both the probing needles and the chuck are *xyz*-adjustable. In order to be able to address more than five contacts at the same time, an additional setup at RWTH Aachen University was used involving a chip carrier and ultrasonic bonding. The carrier distributes every bonded wire to outgoing triaxial BNC plugs split over two parameter analyzers for a sufficient amount of SMUs (Keysight B1500A with 8 SMUs and Agilent 4156C with 4 SMUs). Figure 4.3b shows the chip carrier with 14 wires connecting two devices on one sample.

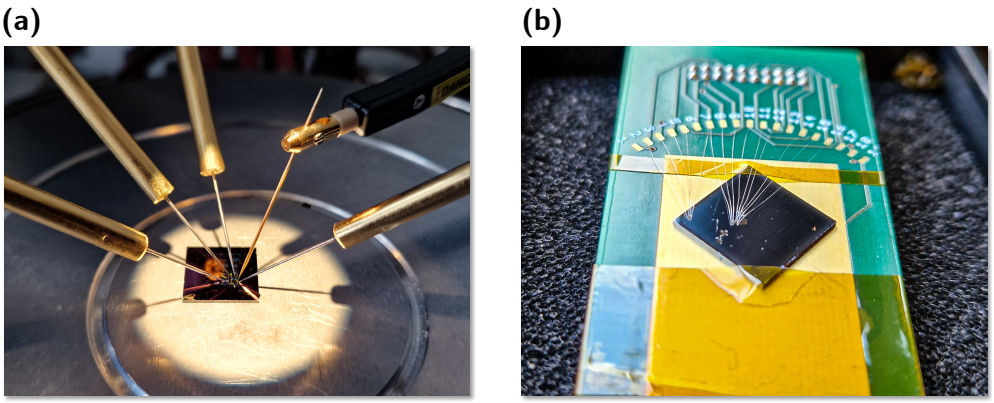

Figure 4.3: Measurement setups: (a) Sample with five probing needles on a temperature controlled vacuum chuck. (b) A customized chip carrier for a sample with several bonded wires connecting the chip with the measurement equipment.

Chapter V
Introducing Buried Gate Architectures

In order to fabricate steep slope transistors by using electrostatic doping, multiple gate electrodes are necessary. This chapter introduces two different platforms based on buried electrodes, which can be used to implement an arbitrary potential landscape. The platforms can then be used to fabricate transistors with low-dimensional materials. The first design to be introduced is the **b**uried **t**riple **g**ate architecture. The concept is based on previous works by Müller et al. [15, 28, 81] and has been fundamentally redesigned within the scope of this thesis. Instead of a lateral triple electrode configuration like in the design by Müller et al., the new BTG substrates are built with vertically stacked graphene-based gate electrodes separated by an intermediate oxide. The platform enables the electrostatic doping profile for TFET devices.

The second design to be introduced is the **b**uried **m**ulti **g**ate architecture. This unique platform accommodates up to 17 mutually insulated buried gates on a sub-10 nm node. The substrates were provided by Grap et al. and are designed for transistors with 1D materials [16, 48]. Due to its individually addressable multi gate landscape the BMG platform is used for EF-FET configurations in this thesis.

5.1 The Buried Triple Gate Substrates

The BTG substrates fabricated by Müller et al. [15, 28, 81] are designed to offer a universal platform for deposition of any 1D or 2D material including an integrated electrostatic doping system. The main purpose of the platform shifted towards being the target substrate for precise transfers of 2D materials, such as graphene or tungsten diselenide. Meander-shaped gates, covering as much of the surface as possible, were buried inside a silicon-on-insulator (SOI) substrate. This maximizes the probability for any material to be aligned perfectly along the gates. Figure 5.1 shows the schematic of the original BTG. The lateral design of the platform contains buried v-shaped aluminum center gate electrodes (brown-colored) enclosed by n-doped silicon side gate electrodes (blue-colored). Atomic layer deposition is used to deposit aluminum oxide on top serving as gate dielectric (light green-colored). CNTs or any other 1D or 2D nano-objects could then be transferred onto the surface. In the case of graphene, TFET devices were fabricated by dry-etching the material into nanoribbons with subsequent metal contact deposition (the figure exemplifies a contacted 1D CNT instead of a 2D material). The colors in the background indicate the electrostatic doping zone for the source side gate (SSG, orange), drain side gate (DSG, blue) and the center gate (purple), respectively. Fabrication is based on labor intensive methods such as impurity doping for the side gates and chemical mechanical polishing for the required planarization of the surface. Moreover, the v-shaped center gate electrodes are prepared by anisotropic wet-chemical etching, limiting the lateral dimensions. Besides technical challenges during fabrication, a major drawback of the architecture is that the layout does not allow for a perfect overlap of the buried electrodes, which restricts the steepness of the electrostatic doping profiles. Apart from the well-designed concept, the original BTGs neither provided reliable gate-to-gate nor gate-to-source insulation due to fabrication faults.

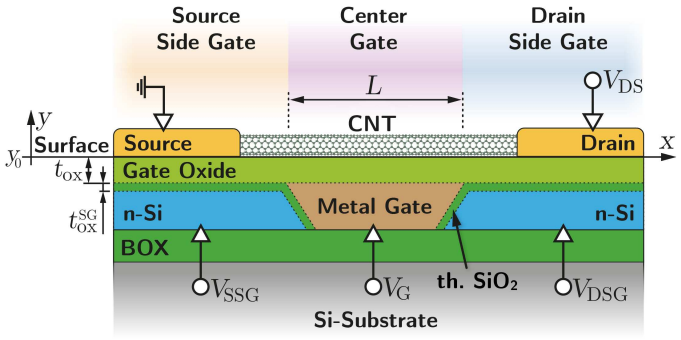

Figure 5.1: Cross-section of the original BTG platform by Müller et al. [15, 28, 81] with an exemplary contacted CNT on top of the surface.

To eliminate the issues with the existing BTG concept, two graphene-based alternative platforms have been developed for this thesis. The fundamental principle of both platforms, however, is very similar and is based upon the same lithography masks and almost the same fabrication cycle. The new BTG implements a vertical approach with side gate electrodes and slightly overlapping center gate electrodes separated by an intermediate oxide. The center gate electrode is then buried by another top oxide. The first platform only includes graphene layers for all three gates and is named triple graphene (TG) design. The concept aims to exhibit an almost planar surface without the need of sophisticated planarization processes, due to the atomically thin graphene layers. However, the transfer of graphene is extremely susceptible to failure in the fabrication process. The second design accounts for this by replacing the graphene side gates by embedded titanium making it a metal/graphene heterostructure (HS). Only having one layer of graphene to process makes fabrication much simpler and allows for wafer-scale substrate production for the side gates and the intermediate oxide with a planar surface. To illustrate an application of a CNTFET, figure 5.2 shows the cross-section of both designs with source and drain contact terminals connecting to a CNT laying over all three gates. The figure uses the same color scheme as in figure 5.1 to indicate the electrostatic doping zones.

The silicon substrates were thermally oxidized to provide insulation to the electrodes (dark green-colored). The fabrication of intermediate and top oxide (light green-colored) is a critical process since the oxide must not damage the graphene layers. Oxide deposition must be very reproducible and needs to provide high electrical integrity in terms of preventing any leakage current between the gates.

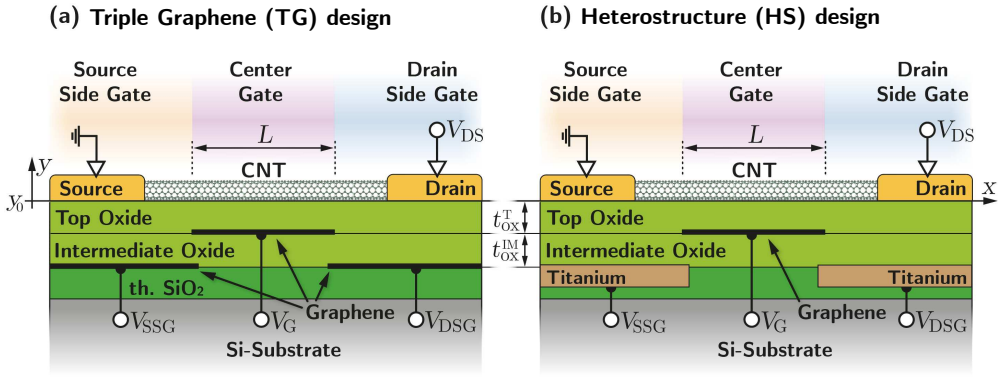

Figure 5.2: The newly designed BTG architecture. (a) Triple graphene design, and (b) heterostructure design replacing the graphene side gates by embedded titanium side gates. Both designs are shown with a contacted CNT on top.

5.1.1 Design and Simulation of the new BTGs

As discussed in chapter 2.2.1, band-to-band tunneling depends on the energetic position of the source (or drain) conduction band and the channel valence band (cf. equation 2.18). This requires a very sharp potential barrier in order to adjust the energy bands accordingly. This means, the steeper the potential transition, the higher the gate control for the device. This will be achieved by electrostatic doping along the electrode landscape of the platform. The influence on the gate control is determined by the screening length λ. The λ-value itself is heavily influenced by the geometry of the gate architecture (e.g. oxide thickness, cf. equation 2.13), which is subject to the development of the new BTGs. The goal is to minimize λ in order to maximize gate control.

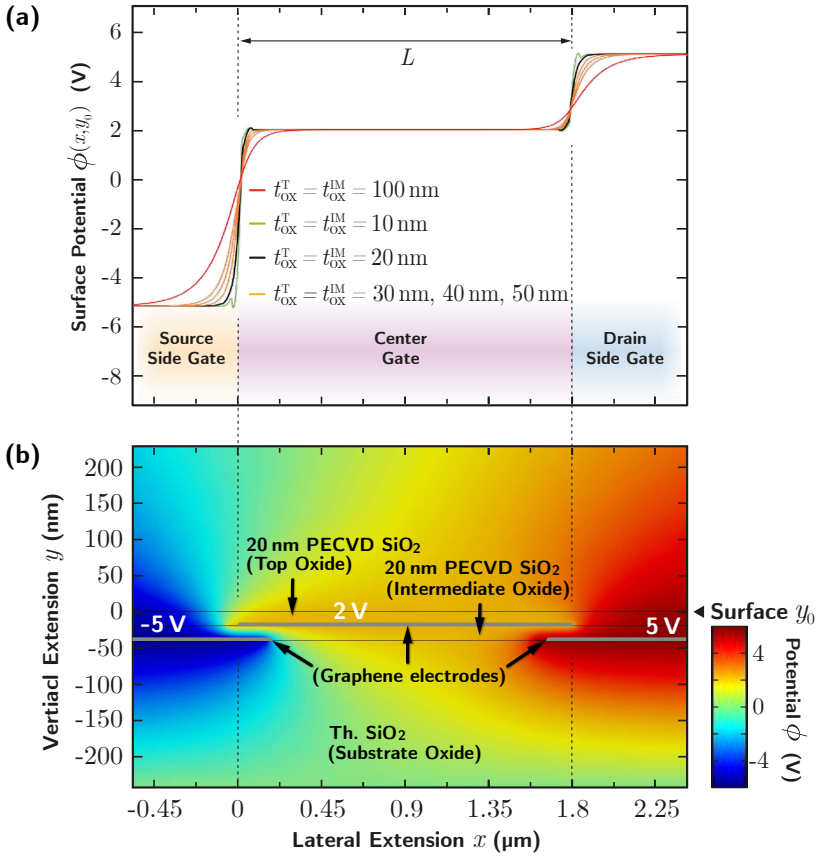

Figure 5.3: (a) Finite element simulations of the potential with different oxide thicknesses at the surface y_0 (equal increment for intermediate and top oxide). Voltages are chosen arbitrarily since they only scale the curves but do not affect the potential characteristic. (b) 2D finite element simulations of the potential distribution including the cross-section of the TG platform. The buried gate electrodes are drawn as gray bars.

The electric potential distribution along the new BTG architecture has been investigated by finite element simulations using Comsol Multiphysics. Figure 5.3a shows the surface potential distribution along all three gates with different oxide thicknesses t_{ox}, respectively. Potential profiles are plotted in y-direction beneath the surface for t_{ox} = 10 nm, 20 nm, 30 nm, 50 nm and 100 nm (identical increment for intermediate and top oxide), respectively.[21] Figure 5.3b illustrates the 2D surface potential with the corresponding electrodes (gray-colored). Voltages are arbitrarily chosen and depend on the channel material. As expected, the sharpness of the potential decreases for greater vertical distances of the electrodes, thus weakening the band transitions. Therefore, the electrostatic doping gradients depend significantly on the oxides' thickness and should be as thin as possible.

Since the electrodes are not arranged laterally but stacked vertically, alignment and horizontal shift are critical for the total potential distribution. Ideally, transition from one potential to the other proceeds instantaneously. However, fabrication of two layers of structured electrodes (metal or graphene) is bound to alignment limitations in the lithography process. Figure 5.4 shows the simulated lateral potential shifts for possible misalignments during lithography.

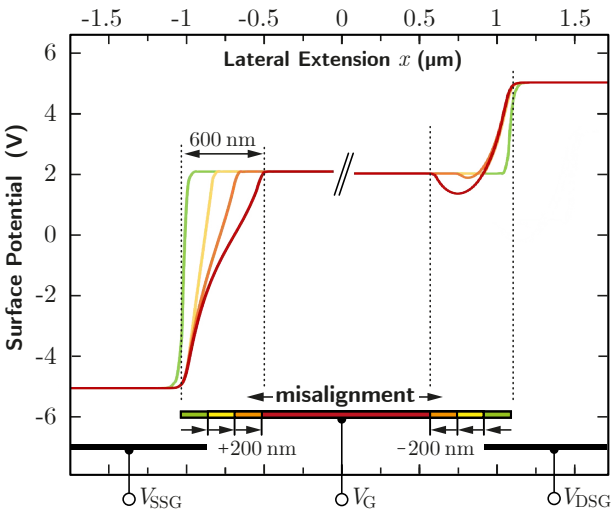

Figure 5.4: Deviations of the surface potential from lithography misalignments: The greater the shift of the center gate to either side, the weaker the potential steepness. The green curve indicates perfect alignment, the other colored curves show the surface potential for a ±200 nm shift each.

[21] Note that the graphene electrodes had been substituted by 1 nm thick metal pads in the simulations. Furthermore, the simulation reached its limits (within reasonable time) in terms of mesh optimization, hence the overshoot effects for the 10 nm thickness curve.

The simulation makes clear that the most important part for alignment is avoiding any gaps between center and side gates. While the potential is still rising up when bridging a gap between source side gate and center gate, the potential will collapse for a lower voltage difference such as from center gate to drain side gate. This makes the alignment process even more critical. On the one hand an electrode overlap leads to a screening of the electric potential blurring the doping profile at the center gate to side gate transition. On the other hand a gap between the electrodes weakens the potential flank or even lets the potential collapse. For achieving perfect electrode alignment at any time, electron beam lithography could be applied. However, for a proof of concept and to be able to fabricate on wafer-scale, UV-lithography is used, thus, accepting possible misalignments.

Figure 5.5 compares the simulation of the surface potential with the original platform. Due to the lateral structure used by Müller et al. the electrode line-up is discontinuous. The simulation showed that a lateral formation of electrodes does not provide as much steepness as overlapping electrodes with an intermediate oxide. The width of the transition (10 % to 90 %) between SSG and center gate are 6 nm and 13 nm for the new platform (for 10 nm and 20 nm oxide thickness, respectively). Although equipped with relatively

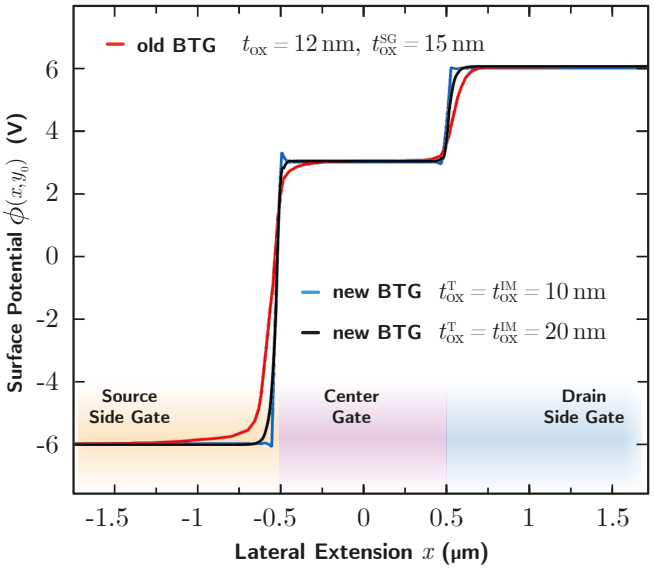

Figure 5.5: The simulated surface potential of both new and the old BTGs: The blue and the black curve are the potentials for the new BTGs with side and center gate thicknesses of 10 nm and 20 nm, respectively. The red curve is the potential for the old BTG in the standard process with 15 nm side gate oxide and 12 nm top oxide (redrawn with permission by Marcel Müller [28]).

thin oxides of 15 nm on the side gates and 12 nm on the center gate, the transition width for the old BTG platform is 37 nm, being significantly wider than for the new BTG. The reason for this is the unique geometry of the old BTG architecture which becomes clearer by looking at figure 5.6. The sketch depicts the meeting point of side gate and center gate (for ideal etching profiles). As long as the oxide layer has a high conformity, i.e. isotropic thickness distribution, a displacement d_0 among center gate and side gate will always occur. For a given side gate thickness t_{ox}^{SG} the miss-match d_0 can be calculated as $d_0 = t_{ox}^{SG}/\tan\vartheta$. The angle ϑ comes from TMAH etching and is 54.7° for {100}-silicon. Consequently, there will always be a drop of the surface potential at this specific position. In case of the fabricated substrates with a side gate thickness of 15 nm, the drop will extend over ~10 nm. Thus, the new BTG concept allows for inherently steeper electrostatic doping profiles. For the latest version of the old BTG a LOCOS[22] process had been used to overcome this issue. However, avoiding the oxide growth on top of the side gates does not change the geometry. The oxide right at the edge of the side gate does actually grow a bit slower but the issue in general remains. Therefore, a vertical stack of overlapping electrodes will always be superior to a lateral line-up. Another disadvantage of Müller's platform is that it relied on n-doped silicon side gates. Being a semiconducting electrode, the side gate exhibits a depletion zone for positive voltages adding to the issue of discontinuous potential transitions (similar to the polysilicon depletion effect in MOS transistors [144]).

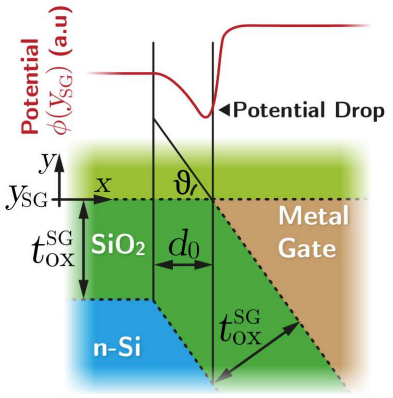

Figure 5.6: Gate geometry of the old BTG (clipping from fig. 5.1): The surface potential slightly collapses at the descending edge of the side gate.

Based on the results of the potential distribution simulation, UV-lithography masks determine the design of the new platform. Core element is the BTG-cell, which is 1.4 mm x 1.4 mm in size. Every BTG substrate sample contains 16 BTG-cells and several alignment marks. Each BTG-cell has a pair of side gate electrodes and one center gate electrode structure. Figure 5.7 shows the final lithography mask of a single BTG-cell. The orange and blue layers are the side gates forming an interlocking comb-like architecture.

[22] Local oxidation of silicon: A silicon nitride hard mask prevents unwanted oxide growth at protected areas. Advantages include better conformity and reduced electromigration [139].

The purple layer is the main gate or center gate. Layers for etching and metalization are displayed by the white and black dashed lines, respectively. Local alignment marks are arranged on a 50 µm grid consisting of 255 fields. Experiments showed that within the entire lithography process the resolution was limited to 1.4 µm. The lithography process itself is definitely capable of resolutions around 600 nm for small structures. However, the side gate electrodes occupy a very large area in close proximity. A distance between the side gates below 1.4 µm showed increased issues in the patterning and metal deposition leading to short-circuits rendering the cell useless. With this in mind, the mutual distance of the side gates was chosen to be 1.4 µm. As suggested by the simulations, the overlap of the center gate is 200 nm in both directions resulting in an overall gate length $L = 1.8\,\text{nm}$. The layout illustrated in the figure is used for both the triple graphene design and the heterostructure. Just like the old BTG architecture the new platform aims to provide as much gate area as possible around the surface. This ensures that randomly deposited CNTs have a high chance finding themselves fully aligned along all three gates after.

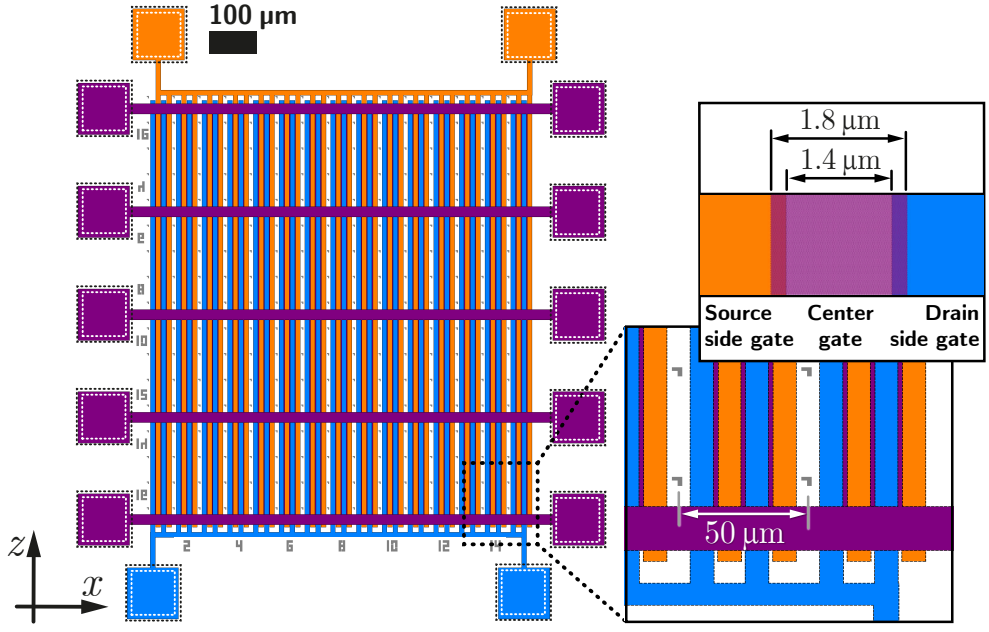

Figure 5.7: UV-lithography mask layout of a BTG-cell used for both the triple graphene design and the heterostructure. The orange layer corresponds to the source side gate (SSG), the blue layer corresponds to the drain side gate (DSG) and the purple layer corresponds to the center gate. Contact pads are manufactured redundantly at all sides. Layers for etching and metalization are displayed by the white and black dashed lines, respectively. Local alignment marks are arranged on a 50 µm grid consisting of 255 fields.

5.1.2 Fabrication of Triple Graphene Substrates

Besides improved gate geometry and improved surface potential distribution, the idea behind the new BTG layout is to simplify the fabrication process and to allow for wafer-scale production. The manufacturing process only requires optical lithography, reactive ion etching (RIE), oxide- and metal-deposition methods and a graphene transfer. This section describes the fabrication process of the triple graphene (TG) design based on the illustrations shown in figure 5.8. The specific parameters used in every process are documented in appendix 9.1.

Fabrication of the TG samples starts with wet-thermal oxidation of a 4-inch silicon wafer (a). Optical visibility of graphene layers atop depends on the SiO_2-thickness and was targeted to 250 nm. Subsection 5.1.5 explains the importance of that matter in detail. To save time and resources the triple

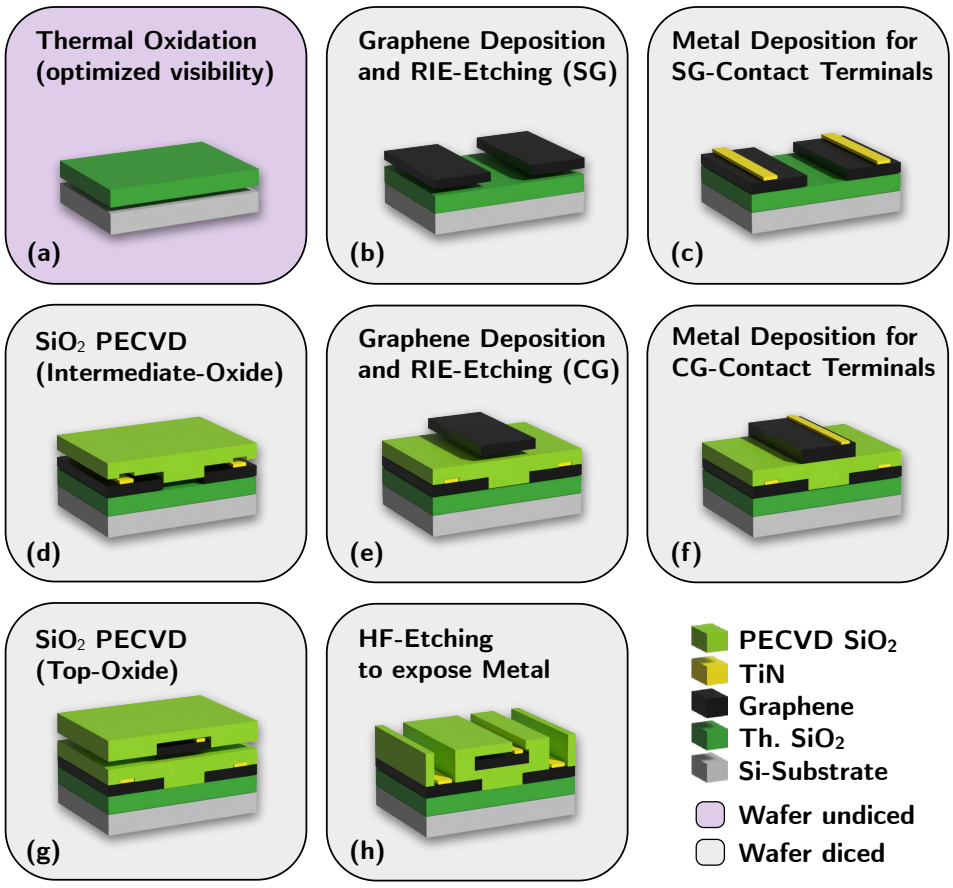

Figure 5.8: Process flow of the triple graphene (TG) design. Detailed explanations are given within the text of this section.

gate and the heterostructure design share the first wafer-scaled lithography (i-line, $\lambda = 365\,\text{nm}$) with a positive photoresist. For the TG substrates it is the initial lithography step to structure the alignment marks for subsequent lithography procedures including electron beam lithography for the CNT devices (cf. chapter 6.2). Metal deposition was done via titanium sputtering with a subsequent lift-off in acetone. After that the wafer was diced into 1.2 cm x 1.2 cm-sample substrates. The dimensions were chosen in accordance to the follow-up wet-transfer method of the graphene layer. The transfer is based on studies by Li et al. and Deokar et al. [145, 146], but with some modification which is discussed in section 5.1.4. The deposited graphene sheet was then structured by UV-lithography and an argon/oxygen RIE-etching to become side gate electrodes (b). Thereafter, another UV-lithography and a titanium nitride (TiN) sputtering deposition with subsequent lift-off are used for structuring contact pads for the graphene side gates (c). Titanium was previously chosen for the embedded metal because it exhibits a very low thermal expansion coefficient ($8.5\,10^{-6}/\text{K}$), which is comparable to the thermal expansion coefficient of the surrounding silicon dioxide ($5.1\,10^{-6}/\text{K}$), thus preventing any damage of the substrate at high temperatures. This is extremely important because the forthcoming intermediate oxide is deposited by a plasma enhanced chemical vapor deposition (PECVD) at 350 °C (d). Note that during the experimental phase of this thesis, there were three different materials from three different deposition methods available: Aluminum oxide (Al_2O_3) by Atomic Layer Deposition (ALD), silicon dioxide (SiO_2) by plasma-enhanced chemical vapor deposition (PECVD) and tungsten oxide (WO_3) by thermal evaporation. Section 5.1.6 compares the

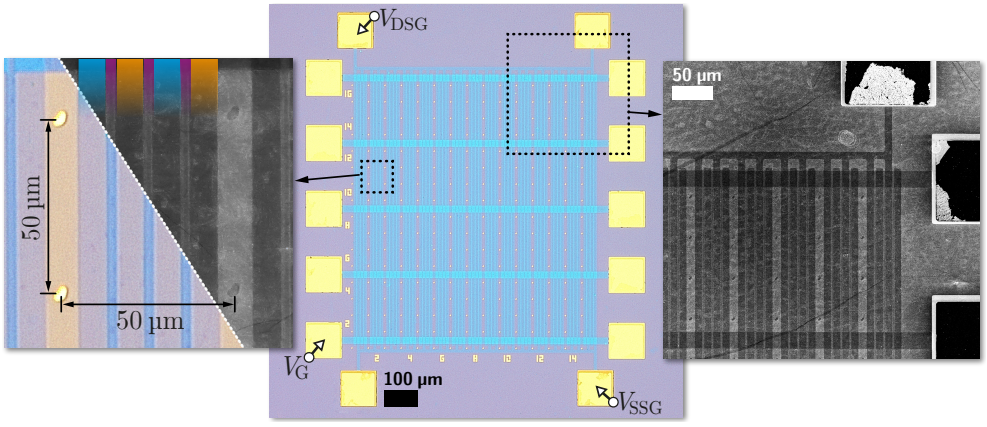

Figure 5.9: Microscopy images of a completed BTG-cell of the triple graphene platform with magnifications (left and right): A substrate contains of 16 single cells each containing 255 writing fields with $50\,\mu\text{m}^2$ in size (cf. figure 5.7). The two graphene layers of side and center gates are clearly visible both in SEM and OM images.

mentioned methods and discusses why a PECVD process was chosen and how it was optimized. On top of the intermediate oxide another sheet of graphene is deposited by applying the same transfer method as before. Structuring is again done by UV-lithography and reactive ion etching (e). This time the lithography has to be extremely precise. Contact terminals for the center gate are deposited the same way as for the side gates (f). The final top oxide is again a SiO_2 layer from PECVD (g). UV-lithography and etching is applied to open both SiO_2 layers above the metal pads for contact access (h). Etching is done by hydrofluoric acid (HF). Since the metal is buried on different levels, etching on the center gate terminals is done quicker. Erosion of the metal is not an issue due to the high etch resistivity of TiN. However, the unmasked area for the contacts inside the photoresist are designed ∼20 % smaller than the actual metal pads considering for lateral etching. The final TG platform is shown in figure 5.9 with SEM and OM images.

5.1.3 Fabrication of Graphene/Metal Heterostructures

Replacing the first graphene layer for the side gates by embedded metal electrodes is a huge saving of time and resources. Fabrication at the start can be processed on wafer-scale for several more steps. Furthermore, the transfer of the graphene layer has to be done only once for the center gate. Unfortunately, planarity of the surface is deteriorated by the substitution of metal, since chemical mechanical polishing was not available. Implications of that specific issue are investigated in section 5.1.7. The upcoming process description refers to figure 5.11, which comprises the complete process flow of the heterostructure. The specific parameters used in every process are documented in appendix 9.1.

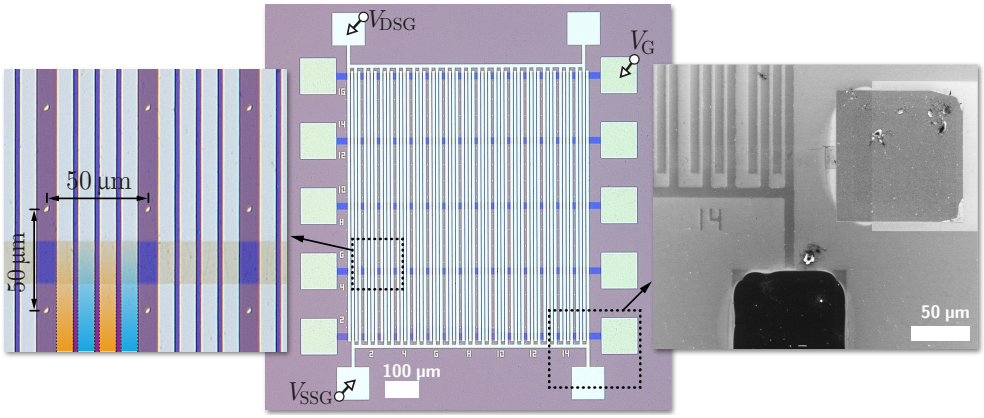

Figure 5.10: Microscopy images of a completed BTG-cell of the heterostructure platform with magnifications (left and right): A substrate contains of 16 single cells each containing 255 writing fields with 50 μm^2 in size (cf. figure 5.7).

As previously discussed, both designs share the same 4-inch wafer with the same oxidation at the beginning (a). However, the heterostructure uses titanium side gates instead of graphene side gates. In terms of UV-lithography, this means that the layer for the initial alignment marks (like for the TG structure) is merged with the layer for the side gates. To achieve high planarity even without CMP the metal marks and side gates are fully embedded, thus level with the thermal SiO_2. Photoresist patterning is done by UV-lithography and RIE is used to etch the trenches precisely 30 nm inside the SiO_2 (b). The subsequent deposition process must yield precisely 30 nm as well (c). Processes on the machines had to be investigated and configured accordingly. For the same reason as described earlier in the TG fabrication process, titanium is used to fill the trenches. This minimizes the risk of damaging the substrate at high temperatures, which is even more important for the HS platform. After the

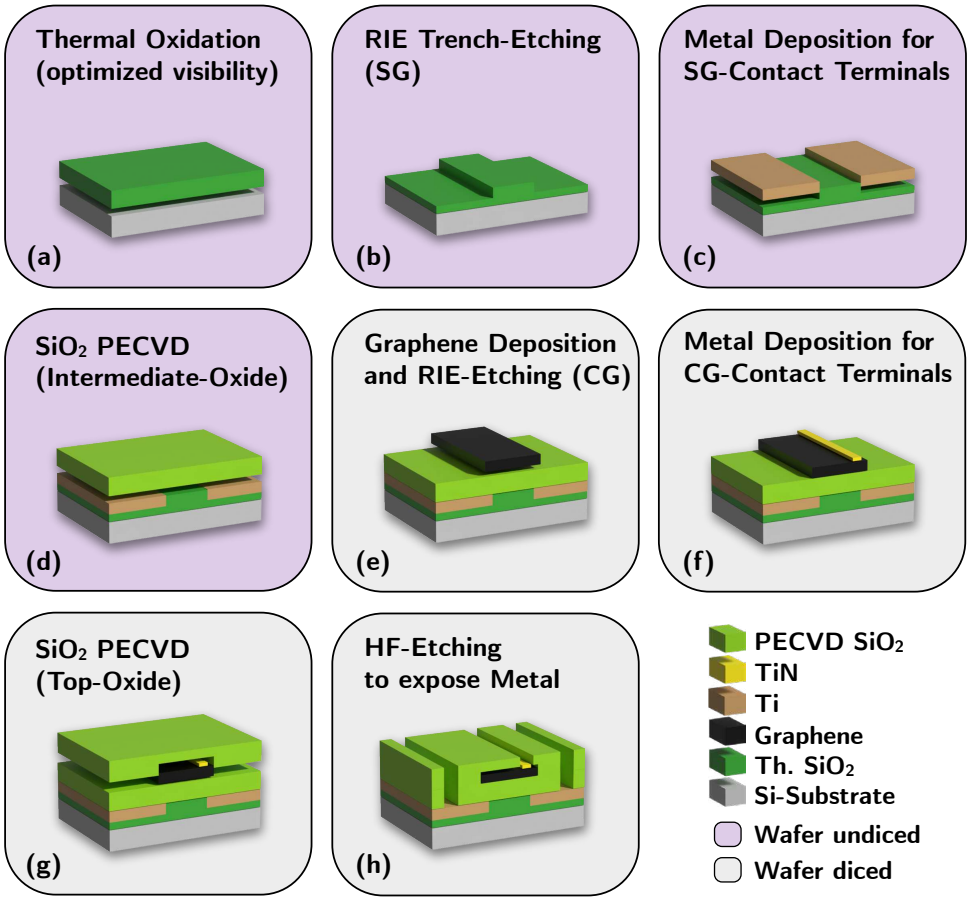

Figure 5.11: Process Flow of the graphene/metal heterostructure (HS) design. In contrast to the triple graphene design, there are more process steps executed on the undiced wafer. Detailed explanations are given within the text of this section.

titanium lift-off, PECVD-SiO_2 (intermediate oxide) is deposited (d). So far, every process had been deployed on the 4-inch wafer from the early start. After deposition of the top oxide the wafer was diced into 1.2 cm x 1.2 cm sample substrates. From then, the remaining fabrication process was exactly the same as for TG fabrication (e-h). The final HS platform is shown in figure 5.10 with SEM and OM images.

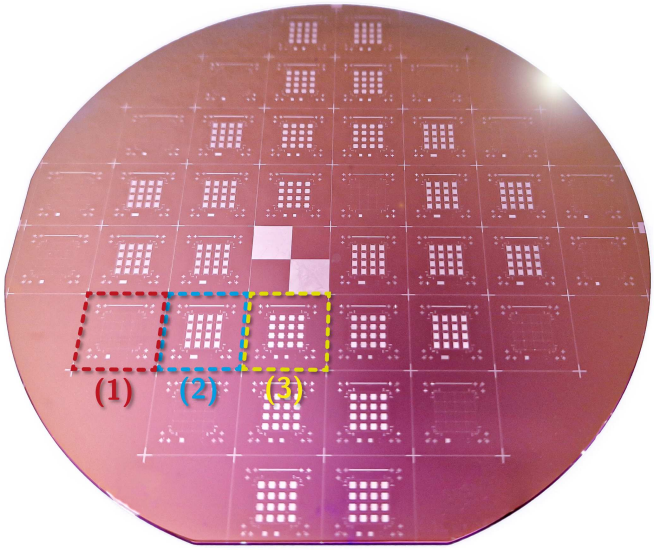

Figure 5.12: Processed 4-inch wafer before dicing. Dashed lines mark a single 1.2 cm^2-substrate with (1), the triple graphene design and (2), the heterostructure. Note that the wafer includes an additional design (3) with swapped side and center gates, which eventually had been dismissed. Yet, it was still part of the latest full wafer-scale mask.

5.1.4 Graphene Transfer from Copper

In principle, the presented platforms do not rely on a transfer of graphene. For example, Pang et al. [147] reported on a direct growth of graphene on SiO_2, which would allow to continue the fabrication on wafer-scale. Unfortunately, this process requires temperatures above 1000 °C, exceeding the limits of thermal expansion with metalization, even for titanium. Toh et al. [148] reported on low temperature laser enhanced CVD processes which is a sort of complex setup, but could be considered in the future. However, the scope of this thesis neither includes optimization nor development of graphene growing methods since the graphene is only used as a plain electrode. The alternative at hand is a transfer process which can be carried out without sophisticated techniques. Eventually, a wet-transfer proposed by Li et al. and Deokar et al. [145, 146] is deployed utilizing CVD-pre-grown

graphene on copper foil coated with PMMA. The density of defects and hence the carrier mobility strongly depends on the type of the transfer and on its execution [149]. A meta study of Ullah et al. [150] showed that a wet-transfer is actually the best option if the focus does not lie on quality but on simple, fast and reliable production. Alternative wet-transfers are the so-called bubble transfers from CVD-grown graphene on germanium [151] or epitaxial-grown graphene on ruthenium [152]. The transfer in general requires a lot of attention and needs to be executed carefully. The wafer is diced into 1.2 cm x 1.2 cm sized samples to allow transfer of 1 cm x 1 cm sized sheets with PMMA on graphene on copper. The slightly larger substrates provide an easier way to handle the transfer. Figure 5.13 depicts the detailed procedure: To remove the copper from the PMMA/graphene sheet, the foil is dipped into an aqueous copper etchant based on ferric chloride ($FeCl_3$) (1). Due to the strong hygroscopic nature of the PMMA, the sheet keeps floating on the surface. After the full removal of the copper layer beneath the PMMA/graphene sheet, a quartz slide is used to scoop the sheet and to subsequently drop it on DI-water (2). Ferric chloride is a strong dye and must be handled with caution. Therefore, a water-bath washes and cleans the sheet, which can be repeated multiple times if necessary. Thereafter, the substrate can be placed underwater below the sheet, hold by tweezers and slowly elevated. With careful attention, the sheet eventually attaches to the substrate's surface (3). A five minutes bake on a hotplate at 70 °C dried the

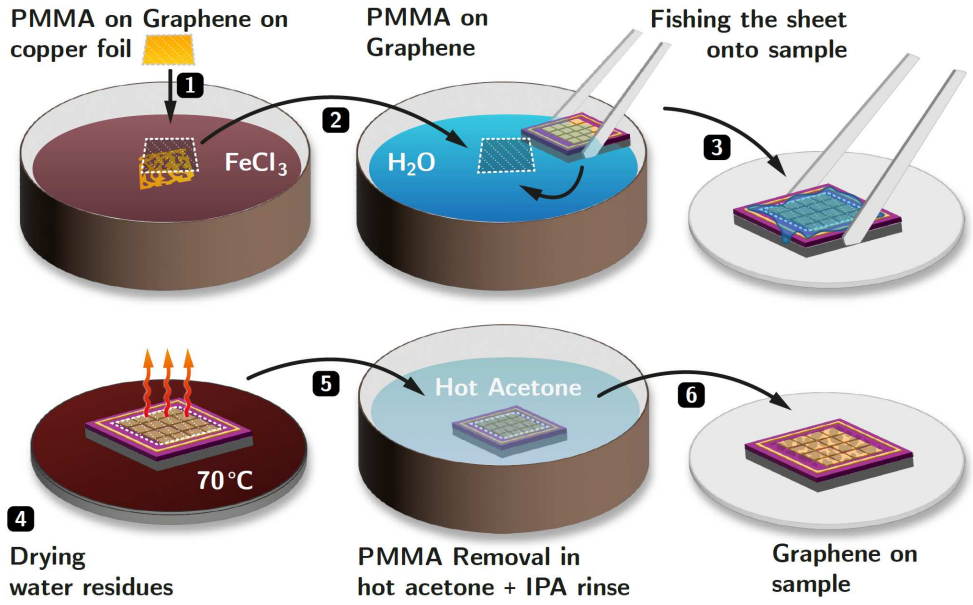

Figure 5.13: A complete transfer of graphene from copper foil. Detailed explanations are given within the text of this section.

residual water on the substrate (4). The PMMA/graphene sheet now permanently adheres to the surface of the substrate. A bath in hot acetone at roughly 42 °C removes the PMMA layer leaving just the graphene (5). Note that resist residuals are a general issue in PMMA based transfers [150]. In fact, persistent residuals may significantly increase the contact resistance at the metal interface [153]. Cleaning with oxygen plasma would fully remove the PMMA, however, the graphene would be fully removed as well. Therefore, the substrate stays at least three hours in the hot acetone to remove as much residues as possible. A high temperature PMMA removal around 400 °C was also investigated. However, the results did not differ from bathing the substrate in hot acetone, which eventually was preferred since high temperature is always a risk of damaging the substrate from thermal expansion of the metal. The acetone remaining on the substrate is then dissolved by an isopropyl alcohol (IPA) rinse followed by blow-drying (6).

5.1.5 Optimizing the Visibility of Graphene

For atomically thin materials, such as graphene, the visibility on various substrates is essential. Without the ability to actually recognize the graphene with an optical microscope, subsequent processing is difficult or even impossible. Blake et al. and Abergel et al. [154, 155] were the first to study the visibility of graphene, based on the mere contrast or on CIE (Commission Internationale de l'Eclairage) color spaces. In 2012, Kontis et al. [156] supplemented the work of Blake by adding an evaluation method for RGB color spaces (many optical microscopes are just using a digital camera projecting the image onto a display, hence the need for RGB). However, a rating of perceived visibility from a huge variety of materials in RGB-based applications is missing in this study. A comprehensive investigation on the visibility of 2D materials had been published in 2015 by Müller et al. [157]. An improved index had been developed to evaluate the visibility for several color spaces for any material stack with known refraction and absorption. Based on this work, simulations had been executed to find the best substrate-/intermediate oxide combination in order to maximize the visibility of the transferred graphene.[23]

Optical visibility is defined as the perceived difference from color values of the material stack with and without the material of interest in the respected color space. The wave distribution and its scattering are calculated using the Fresnel equations in matrix formulation as proposed by Yeh et al. [158]. The resulting spectral density function $S(\lambda)$ can be transformed to the RGB color

[23]The visibility simulation software (VS.Lab) is available for download at *www.iht.rwth-aachen.de/cms/iht/Forschung/~mwki/Simulationsprogramm/* (as of December 2022).

space by applying the CIE color matching functions and a matrix transformation. The color matching functions (or tristimulus) are developed to link the real wave spectrum to the trichromatic characteristic of the human eye [159]. The equations below briefly explain the Fresnel formalism from a perpendicular observer (angle of incident $\phi = 0°$):

$$\boldsymbol{A} = \prod_{j=1}^{N} \boldsymbol{T}_{i,j} \cdot \boldsymbol{P}_j \; . \tag{5.1}$$

Matrix $\boldsymbol{A}$ is a product of all interface wave transitions $\boldsymbol{T}_{i,j}$ and the wave propagation $\boldsymbol{P}_i$ with $i = j - 1$ over N layers. The matrices are assembled as

$$\boldsymbol{T}_{i,j} = \frac{1}{\frac{2\tilde{n}_i}{\tilde{n}_i+\tilde{n}_j}} \begin{pmatrix} 1 & \frac{\tilde{n}_j-\tilde{n}_i}{\tilde{n}_j+\tilde{n}_i} \\ \frac{\tilde{n}_j-\tilde{n}_i}{\tilde{n}_j+\tilde{n}_i} & 1 \end{pmatrix}, \; \boldsymbol{P}_i = \begin{pmatrix} e^{\mathrm{i}\frac{2\pi}{\lambda}\tilde{n}_i\tau_i} & 1 \\ 1 & e^{-\mathrm{i}\frac{2\pi}{\lambda}\tilde{n}_i\tau_i} \end{pmatrix}. \tag{5.2}$$

At layer i the thickness is given by τ_i and the complex refraction index is given by $\tilde{n}_i = n_i + \mathrm{i}k_i$. λ is the current wavelength. The formulation is valid for transversal electrical polarization (TE). For transversal magnetic polarization (TM) the sign of the complex refraction index $\tilde{n}$ swaps. The simulation software takes both polarization methods into account and merges the two spectra. Considering that the last layer, i.e. the substrate does not propagate the wave any more the resulting spectral density function can be interpreted as[24]

$$S(\lambda) = \left(\frac{\boldsymbol{A}_{21}}{\boldsymbol{A}_{11}} \right)^2 \; . \tag{5.3}$$

Integrating over $S(\lambda)$, a light source $I_{\mathrm{LS}}(\lambda)$ and the CIE color matching functions $\bar{x}, \bar{y}, \bar{z}$ within the limits of visible light yields:

$$\begin{pmatrix} X \\ Y \\ Z \end{pmatrix} = \int_{380\,\mathrm{nm}}^{780\,\mathrm{nm}} S(\lambda)\, I_{\mathrm{LS}}(\lambda) \begin{pmatrix} \bar{x}(\lambda) \\ \bar{y}(\lambda) \\ \bar{z}(\lambda) \end{pmatrix} \mathrm{d}\lambda \; . \tag{5.4}$$

The resulting vector consists of the CIE XYZ color space values. They are the basis for any conversion to any color space by definition [160]. In case of RGB the conversion is done by the matrix multiplication

$$\begin{pmatrix} R \\ G \\ B \end{pmatrix} = 255 \cdot \Gamma_{\mathrm{C}} \cdot \begin{pmatrix} 3.24 & -1.54 & -0.50 \\ -0.97 & 1.88 & 0.04 \\ 0.06 & -0.20 & 1.06 \end{pmatrix} \cdot \begin{pmatrix} X \\ Y \\ Z \end{pmatrix} \; . \; [161] \tag{5.5}$$

[24] Note that the explanations given are extremely simplified and do reflect only a fraction of the actual simulation algorithm. See [157] for a detailed description.

The XYZ colors are defined within the range from 0 to 1. Multiplication with 255 and rounding to the nearest integer expands the linear space to the scope of RGB. The Γ_C-function is a necessary adjustment (gamma correction) to match the RGB gamut. The entire procedure has to be executed for the background and for the foreground stack in order to evaluate the perceived difference. This is done by the so-called weighted color difference index (WCD+)[25]:

$$\text{WCD+} = f_{\text{w}}(\beta_R, \omega_R)|\Delta R| + f_{\text{w}}(255, \omega_G)|\Delta G| + f_{\text{w}}(255, \omega_B)|\Delta B| \; . \tag{5.6}$$

The difference of the color value is given by ΔC (whereas C stands for R, G or B, respectively). The weighting function f_{w} is defined as

$$f_{\text{w}}(\beta_C, \omega_C) = \omega_C \cdot {}^{\beta_C}/_{255} \; . \tag{5.7}$$

The variable ω_C represents the direct weight of the respected color for the human eye specified by [159] ($\omega_R = 0.21, \omega_G = 0.72, \omega_B = 0.07$). β_C is the arithmetic mean of the foreground RGB color value and the background RGB color value. The C again represents one of the channels R, G or B, respectively. As shown with equation 5.6, β_C is only relevant for the red channel. This is in fact a very important adaptation since the human eye is most sensitive for differences in green colors. This means that the remaining red and blue channel have to be weighted with the absolute influence (arithmetic mean). However, the blue channel has a very low impact anyway so that it can be neglected in that part and β_B is also set to 255. Without this adaptation the index does not reflect a perfect criteria for visibility [157].

Applying the simulation to the new BTG fabrication yields process windows for the substrate SiO_2 in which the graphene still exhibits very good visibility. The WCD+ index is designed to provide a comparable criteria for the visibility. However, the absolute value depends on the human perception and varies of course amongst any observer. Typical values for the index are zero for no visibility and up to 20 and above for excellent visibility. For this thesis, a WCD+ value >3 is set to be the limit for accepted visibility for graphene. The curve in figure 5.14 shows the WCD+ index for a graphene monolayer on a silicon/silicon dioxide substrate. The thickness of the silicon dioxide runs from 10 to 310 nm. The background of the figure actually shows the difference of the perceived colors. The curve is an excerpt from figure 9.3 (appendix 9.3), which shows that high visibility can only be achieved for thicknesses below 400 nm. The accepted visibility for this selection ranges from 44 to 120 nm and from 240 to 310 nm. This basic evaluation is only

[25] To avoid confusion with the deprecated WCD index by Kontis et al., the '+' is added. Unlike the WCD, the WCD+ includes an adaption to the non-linear nature of the RGB space.

relevant for the TG structure, since it includes graphene deposition directly onto the thermally grown SiO_2. Fabrication, however, is done on wafer-level, accommodating samples of the TG design and the heterostructure on the same substrate. Therefore, all plans for optimized visibility must consider both designs.

In section 5.1.2 it was briefly mentioned that several options are available for the intermediate and top oxide. As a consequence, the visibility of graphene had been investigated for all of those options. To avoid making the simulation unnecessarily complicated, a base simulation had been chosen in which only the materials of intermediate oxide and top oxide alter. The variable for all simulations is still the thickness of the substrate SiO_2. This is the only parameter not affecting the characteristic of the final CNT device, yet having a major impact on the optical visibility of graphene. Besides that, the ideal oxide thickness for side and center gates is rather based on electrical properties than on optical considerations. With that in mind, the simulation is set to use always 20 nm for both side and center gate. The curves in figure 5.15 extend the mere visibility on SiO_2 by aluminum oxide for both the side and the center gate. The visibility changes for every investigated position of

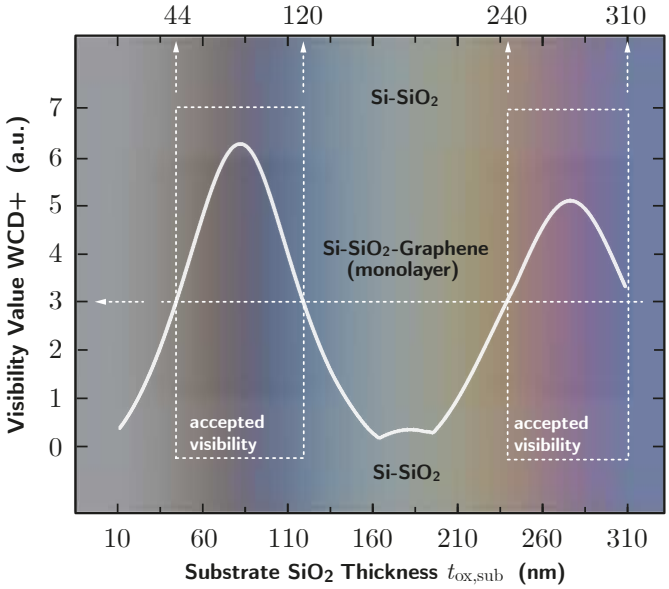

Figure 5.14: WCD+ index for a graphene monolayer on Si/SiO_2. The background shows the difference of the perceived colors (middle: w/ graphene, top and bottom: w/o graphene). Best visibility is achieved with a SiO_2 oxidation within a process window from 44 to 120 nm and from 240 to 310 nm. A full range of the WCD+ index from 10 to 1000 nm is given in appendix 9.3. (Note that WCD+ values for the colors shown in the figure might not be valid for the CMYK color space of the printed version of this thesis.)

the graphene inside the BTG stack. The dashed rectangles represent the accepted visibility window for each curve based upon a WCD+ index >3. The overall process window coincides with their smallest intersect.

- The best visibility for graphene in combination with aluminum oxide appears at 72 nm of thermally grown SiO_2. The accepted process windows extend from 44 to 112 nm and from 240 to 308 nm.

As observed and calculated for many transition metal oxides, the dielectric properties are rarely comparable to oxides stemming from semiconductors or metals [162]. This also is reflected in the curves in figure 5.16. The plot extends the visibility on SiO_2 by tungsten oxide for both the side and the center gate. Accepted visibility windows are obviously limited. This adds up to a few reasons why a WO_3 deposition was not acceptable (cf. section 5.1.6).

- The best visibility for graphene in combination with tungsten oxide appears at 52 nm of thermally grown SiO_2. The accepted process windows extend from 44 to 77 nm and from 239 to 263 nm.

Figure 5.17 finally shows the visibility for an exclusive SiO_2 process.

- The best visibility for graphene in combination with PECVD silicon dioxide appears at 67 nm of thermally grown SiO_2. The accepted process windows extend from 44 to 98 nm and from 240 to 296 nm.

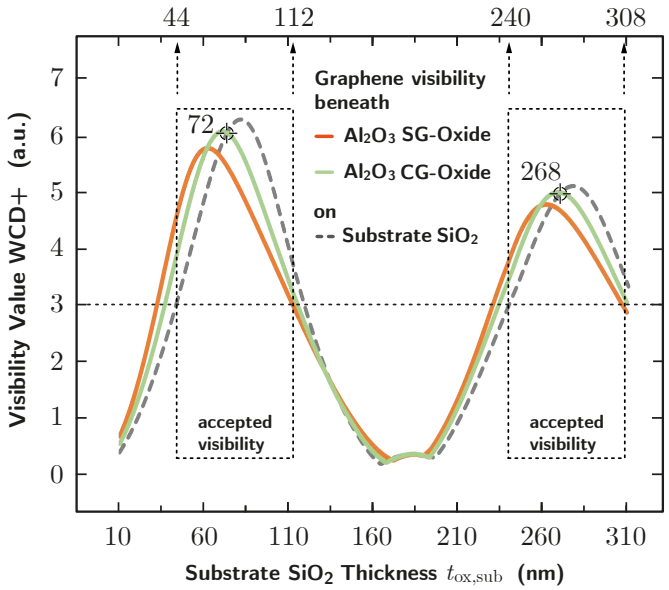

Figure 5.15: WCD+ index for a graphene monolayer on or beneath $Si/SiO_2/Al_2O_3$. Intermediate and top oxide thicknesses are set to 20 nm, SiO_2 is variable though. Color bars indicate the accepted visibility for each curve. Best process window coincide with their smallest intersect.

As already described in section 5.1.2, for the intermediate and top oxide deposition PECVD SiO_2 was chosen. However, all three oxides exhibit very similar visibility process windows. Even for oxides not mentioned in this thesis, such as hafnium oxide or molybdenum oxide, the dominant factor is always the substrate oxide. The second visibility window in figure 5.17 with a peak at 272 nm is the targeted choice for wafer production for the new BTG. Although WCD+ values are slightly lower at this point, it is important to preserve enough insulation to the silicon substrate. 30 nm of SiO_2 are used for buried side gates for the heterostructure. The remaining oxide should be thicker than 100 nm in order to provide a buffer and sufficient insulation. The purple colored marks within the second accepted visibility window indicate the actual SiO_2 thickness of the wafer which contains most of the samples used in this thesis. Although 272 nm had been targeted, oxidation yielded 250 nm due to fluctuating furnace conditions. However, a deviation of 22 nm is still tolerable, and even favorable in case of the heterostructure since visibility optimization is only relevant for the center gate here (green curve).

A key feature of the BTG platform is its universal application which includes 2D material deposition. To support this idea, table 5.1 lists WCD+ values for common materials for the latest configuration of 250 nm thermally grown SiO_2 plus a total of 40 nm PECVD SiO_2.

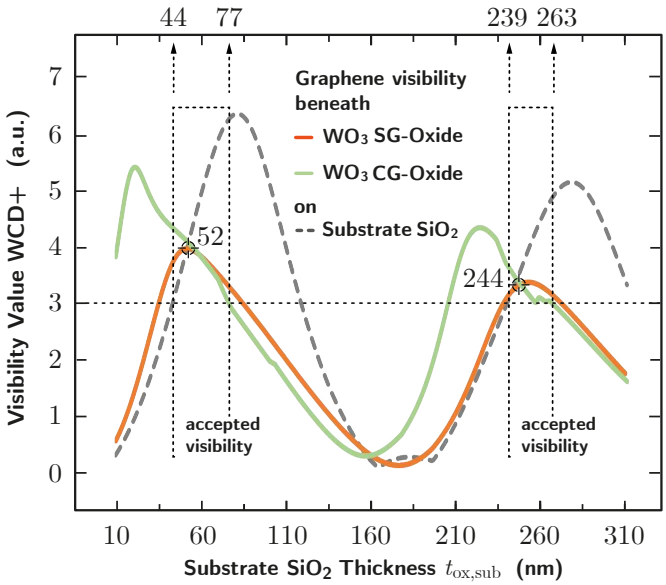

Figure 5.16: WCD+ index for a graphene monolayer on or beneath $Si/SiO_2/WO_3$. Intermediate and top oxide thicknesses are set to 20 nm, SiO_2 is variable though. Color bars indicate the accepted visibility for each curve. Best process window coincides with their smallest intersect.

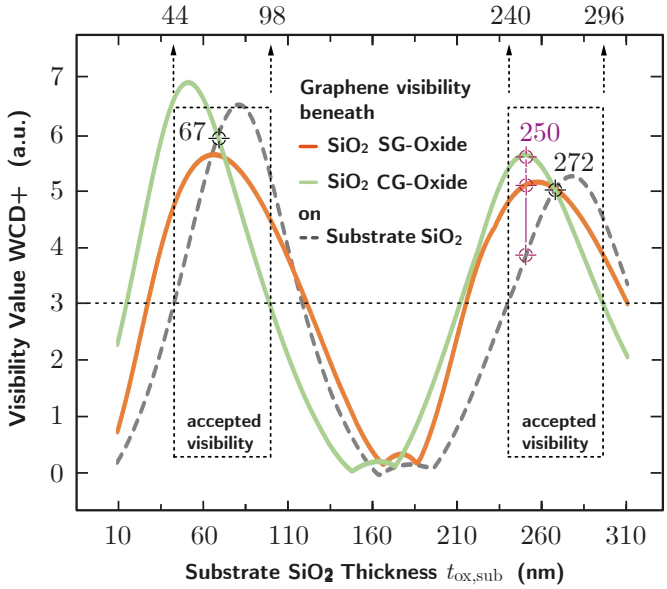

Figure 5.17: WCD+ index for a graphene monolayer on or beneath Si/SiO_2/PECVD-SiO_2. Intermediate and top oxide thicknesses are set to 20 nm, SiO_2 is variable. Color bars indicate the accepted visibility for each curve. Best process window coincide with their smallest intersect. The purple colored marks within the second accepted visibility window at 250 nm indicate the actual SiO_2 thickness used for the processed wafers.

	WCD+	Monolayer thickness	Simulation (FG|BG)
Tungsten diselenide (WSe_2)	4.90	6.70 Å [163]	
Tungsten disulfide (WS_2)	15.57	6.20 Å [164]	
Molybdenum diselenide ($MoSe_2$)	11.76	6.47 Å [165]	
Molybdenum disulfide (MoS_2)	8.11	6.15 Å [165]	
Hexagonal boron nitride (h-BN)	0.99	3.33 Å [166]	
Graphene	2.62	3.35 Å [167]	

Table 5.1: WCD+ values for different 2D materials on the new BTG. The simulated color impressions consist of the background (BG) which is Si/250 nm SiO_2/40 nm PECVD SiO_2. The foreground contains the background stack including the monolayer of the respected 2D material. Except boron nitride, almost all of the materials exhibit acceptable visibility on the platform. (Note that the WCD+ values for the colors depicted in that table might not be valid for the CMYK color space of the printed version of this thesis.)

5.1.6 Optimizing the Oxide Deposition

To keep interface states and parasitic capacitances effectively low, every gate dielectric should exhibit the highest quality possible. The new BTG architecture is no exception here. The most dense and stable dielectrics are usually metal or semi-metal oxides obtained by oxygen diffusion. This oxidation process requires very high temperatures in the range of 1000 °C (in case of silicon) [139]. Since the platform always contains at least one metal layer, extreme temperatures would immediately damage the metal and/or the substrate. Therefore, PVD and CVD methods with lower temperatures had to be applied, hence lower quality oxides.[26]

In the early phase of this work, tungsten oxide (WO_3) made from thermal evaporation was a candidate to be used as the top gate dielectric because it is expected that the process does not damage graphene layers. Figure 5.18 shows a completed cell of the heterostructure with PECVD SiO_2 intermediate oxide and WO_3 top oxide. However, as it turned out later in the process, the electrical integrity of evaporated WO_3 is simply not good enough to serve as gate dielectric (cf. figure 5.19). As reported by Vemuri et al. [168] the electrical properties of WO_3 heavily depend on structural factors such as grain size, grain boundary, specific phase, dopants and stoichiometry. Without further investigation, the assumption is that the stoichiometry is not perfect when made by thermal evaporation. This theory is supported by Zheng et al. [169], who reported on equally low electrical resistance for likewise deposited films. Additionally, the material showed a highly amorphous structure, which obviously lowers the film quality as well. Eventually, all plans of using WO_3 had been dismissed. In the making of this thesis, no studies had been found so far reporting on high quality WO_3-films successfully made from thermal evaporation.

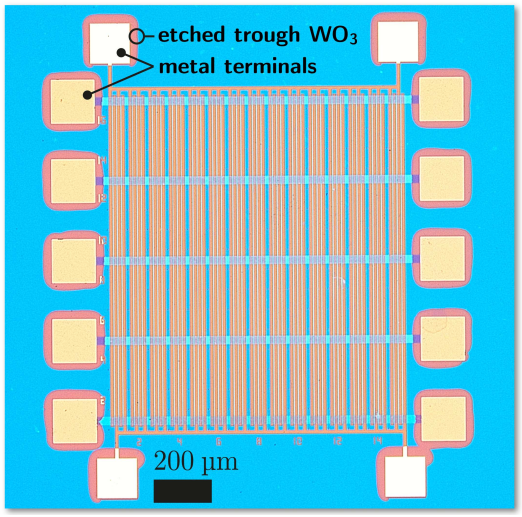

Figure 5.18: Optical microscopy image of a single cell of the new BTG (heterostructure) with tungsten oxide (WO_3) used as center gate dielectric. After deposition, the contact terminals had been exposed by wet-etching through the WO_3 with BOE. The characteristic blue color even matches with simulation results extracted from VS.Lab (cf. 5.1.5).

[26] The basic working principle of the used deposition methods are discussed in chapter 4.1.

Aluminum oxide (Al_2O_3) is considered to be one of the best dielectrics for gate insulation due to its high resistivity and relative high permittivity [170]. The most common method to manufacture thin films of Al_2O_3 without oxidizing the aluminum is atomic layer deposition (ALD). Unfortunately, ALD was unavailable at TU Dortmund University at the time. Nonetheless, access to ALD was granted by cooperation with the Hofmann Group at Cambridge University who successfully worked on ozone-enhanced ALD on graphene in the past [171, 172]. However, the inclusion of a remote process made manufacturing very inconvenient and pushed SiO_2 into the spotlight since it can easily be deposited using a PECVD machine accessible at the lab.

Usually, the oxide quality of PECVD cannot compete with ALD. Therefore, the default PECVD process had to be optimized as much as possible. Within a comprehensive study, parameters such as power, stoichiometry, temperature and gas flow had been investigated. Additionally, the process had been enhanced by a helium feed, which was first proposed by Batey et al. [173]. In summary, best performance in electrical integrity could be found for low power deposition at $30\,^{mW}/_{cm^2}$, a SiH_4:N_2O flow ratio of 40:100 sccm plus 2000 sccm of helium.[27] Deposition temperature and pressure had been set to 350 °C and 1000 mTorr, respectively. Figure 5.19 shows that this adjustment reduced leakage current by almost two orders of magnitude (compared to the machine's default process, cf. appendix 9.3).

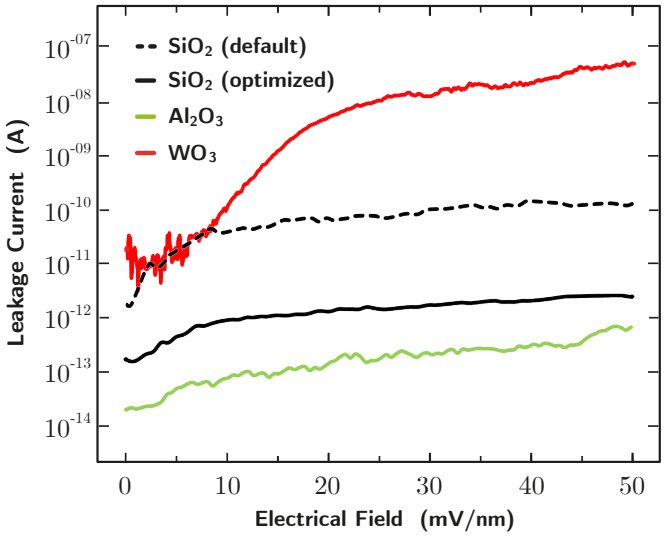

Figure 5.19: Comparison of electrical integrity of WO_3 by thermal evaporation, Al_2O_3 by ALD and SiO_2 by PECVD (w/ and w/o optimization). Measurements had been executed for different thicknesses, therefore the voltage is normalized to the electrical field.

[27] SiH_4 is blended by 98 % helium. That is, 40 sccm corresponds to 0.8 sccm of pure SiH_4.

5.1.7 Substrate Analysis

In this section, topological and electrical properties of the finished substrate are investigated. This includes scanning electron microscope (SEM) analysis of the cross-section, atomic force microscope (AFM) measurements of the surface, Raman measurements of the graphene and electrical measurements to evaluate the connection and continuity of all gate electrodes. Note that from now on the term *BTG* always refers to the new BTG substrates for simplification.

An ideal topological feature would be total flatness of the BTG substrate surface. Any gap between the CNT and the surface will eventually weaken the sharp transitions of the electrical potential (cf. section 5.1.1). As it was previously mentioned, this characteristic can hardly be achieved without chemical and mechanical polishing (CMP). Thus, fabrication process had to consider a plane gate geometry. For the heterostructure, the side gate electrodes had been buried within the substrate oxide by initially etching the masked oxide and subsequently depositing the metal layer with a subsequent lift-off. A RIE process using argon and trifluoromethane etched the oxide at a constant rate of $25\,^{\mathrm{nm}}/_{\mathrm{min}}$. The targeted depth was 30 nm which had been measured by ellipsometry before and after the etching to record the actual depth. This value was then the targeted metal thickness for the sputter deposition to achieve some kind of pseudo-planarity. The deposition rate had been extracted by SEM analysis beforehand. Figure 5.20 shows SEM

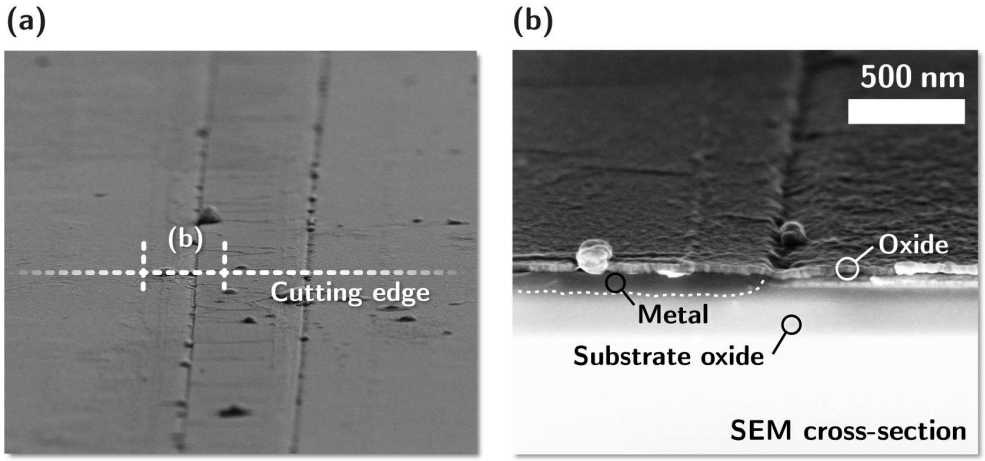

Figure 5.20: SEM micrograph from an 80°-angle of the path between two side gates before the breach indicated by the dashed red line (a). SEM cross-section of the edge from (a), magnified transition to the side gate. The metal is not fully buried inside the substrate oxide (b).

micrographs of the surface (a) and the cross-section (b) of an embedded side gate after the first oxide deposition. A small metal hillock is clearly visible in (b), indicating that the sputtering deposition rate had either been extracted incorrectly or that the process is not as reproducible as assumed for a 30 nm sputtering deposition. For any further investigation of the topology, AFM measurements had been conducted. Figure 5.21a confirms the metal elevation and identifies it to be around 7 nm. The deposition rate could then be adjusted accordingly by linear interpolation from the AFM results. Figure 5.21b shows the AFM results after the first recalibration of the process. This time, however, deposition time was too short and the titanium is actually below the SiO_2-level creating a 2 nm valley. In the final recalibration of the deposition process the unevenness could eventually be eliminated. (cf. figure 5.21c). The extreme spiking at the metal edges (peaking at 15 nm) seemed to be an unavoidable artifact after lift-off. However, after oxide deposition the edges fully collapsed.

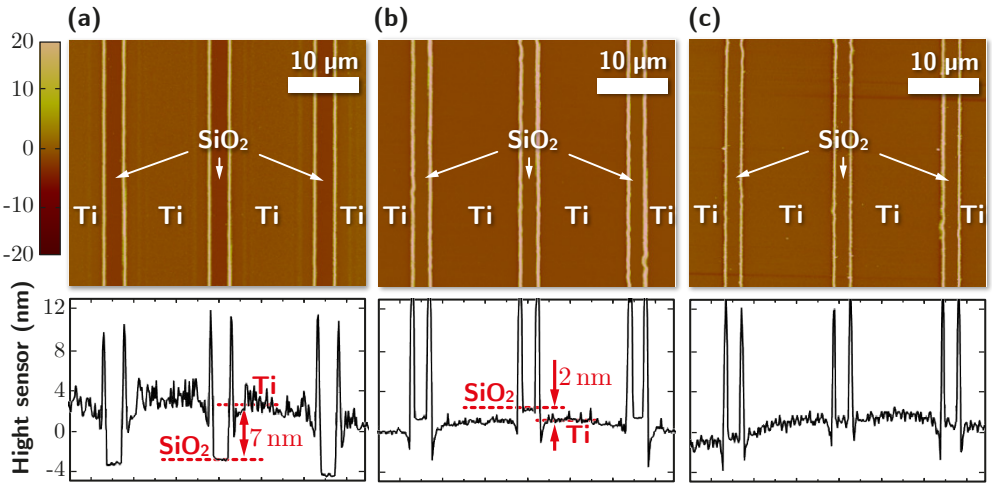

Figure 5.21: 2D AFM (top) and 1D AFM line-scan measurements (bottom) of the heterostructure after the titanium side gate integration. The RIE-etched depth of the trenches was measured to be exactly 30 nm. (a) The surplus of 7 nm titanium relative to the SiO_2-substrate came from imprecise sputtering deposition. (b) First recalibration turned out to be a failed deposition, too. The target had been missed at roughly 2 nm. (c) Final recalibration eventually yields a planar surface.

The AFM surface analysis of the triple graphene substrates revealed some roughness as well. Figure 5.22 shows the 2D AFM measurement and the AFM line-scan. The data contains a lot of noise from irregularities and defects in the graphene layer. Filtered and reduced to its average the relative height is restricted to ∼8 nm. In theory one or even a few layers of graphene buried beneath the oxide should not impact the surface topology to this

extent. It is assumed that during RIE pattering the oxide right beneath the graphene is also being etched. The actual etching time is 30 seconds, which experiments showed to be necessary to fully remove the graphene. However, due to inhomogeneities in the entire transferred graphene film some areas might be etched faster than others. This leaves the oxide exposed to the RIE etching plasma roughening the surface. Some PMMA residuals after graphene transfer might also contribute to this issue. It is assumed that the effort to minimize surface roughness, that is changing the graphene transfer method, would unproportionally exceed its benefits. Therefore, an overall surface roughness of about 8 nm as measured by AFM was tolerated.

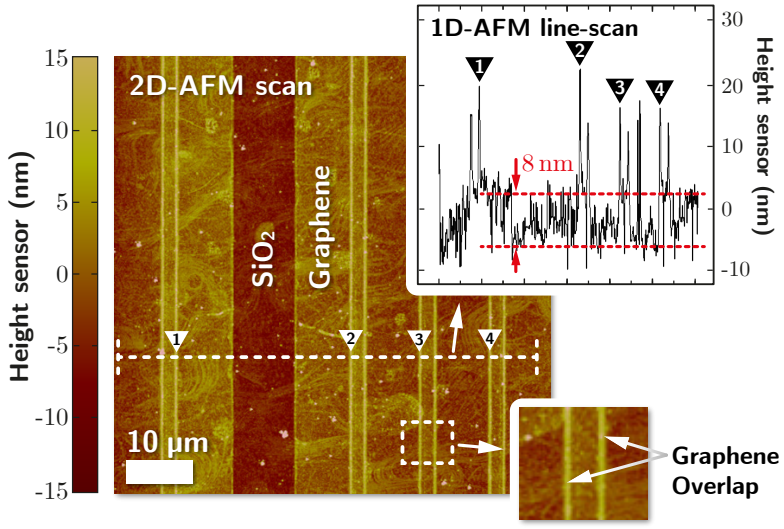

Figure 5.22: 2D AFM and 1D AFM line-scan measurements of the triple graphene platform. The overlaps of the graphene side gate layer and the center gate layer are clearly visible and appear as peaks in the line-scan.

Due to the restrictions in alignment of the available UV-lithography machine a perfect overlap of all three gates is not guaranteed. The examples in figure 5.23 show SEM micrographs of the triple gate overlap and reflect typical outcomes after fabrication. The heterostructure sample in (a) exhibits no overlap at all. The center gate (CG) is shifted to the right relative to the side gates (SG) causing a gap of approximately 200 nm in between. The triple graphene substrate depicted in (b) exhibits only a small misalignment, whereas the gates in the heterostructure in (c) are almost perfectly aligned. The investigation also reveals that the structures made by UV-lithography end up to be 0.3 µm to 0.7 µm wider than originally designed. This is directly linked to the lithography process of both side gates and center gates, which uses a shadow mask in combination with a positive photoresist. After

development the solved pattern in the resist remains as valley-shaped pits with positively inclined edges narrowing down the pattern, thus widening the unexposed areas, i.e. the relevant features. This effect has been known for decades and the solution at hand is of course the use of a negative photoresist leading to an undercut of the pattern for structural fidelity and an improved lift-off [174]. However, the used positive photoresist AR-P3120 showed much better results than several tested negative photoresists, such as AR-N4340 and AR-N2020 (all manufactured by Allresist GmbH), which could not preserve structural integrity over the full expanse of the gates. Considering the extent of this issue, the gained width of the gates for the positive photoresist is acceptable.

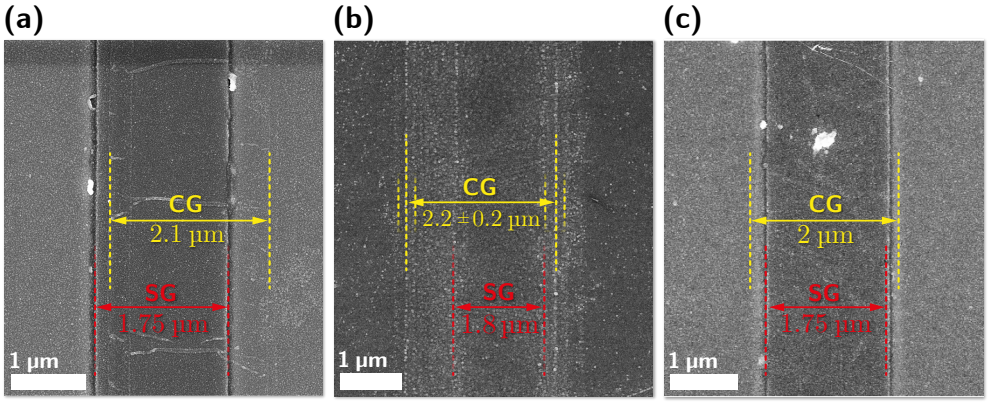

Figure 5.23: Valuation of the alignment precision after UV-lithography: (a) Center gate shifted to the right, failed alignment (heterostructure). (b) Center gate shifted to the left but is still overlapping (triple graphene substrate, no sharp graphene edges visible, hence the tolerances). (c) Perfect alignment of all gates (heterostructure). All examples were fabricated under the same conditions with the same methods.

To evaluate the impact of plasma enhanced oxide deposition on the graphene layer, Raman measurements were conducted [175]. Figure 5.24 shows the Raman spectra before (black curve) and after (green curve) the SiO_2 had been deposited, respectively. For comparison, measurements for Al_2O_3 are also included (orange curve). The marked peaks reveal information about the morphology of the graphene layer: The D-peak reflects the probability of any scattering event happened with a lattice defect. Therefore, the smaller the D-peak, the smaller the defect concentration of the graphene [176, 177]. Even for plain graphene without oxide deposition a D-peak appears, suggesting that the transferred graphene already exhibits some defects. However, an increase of defects after a wet-transfer of graphene is quite common, but could be reduced by time consuming methods [150, 178]. The concentration of defects can be used to determine the quality of the graphene. Usually the

ratio of D- to G-peak is a good indicator for the evaluation. The D/G-ratio is 0.14 for the graphene before and 0.5 after the SiO_2 deposition. According to Cançado et al. [179] this translates to approximated defect distances of $l_D > 24\,nm$ and $l_D > 15\,nm$, respectively. For the Al_2O_3, that is made from ALD, the Raman spectrum nearly stays the same, suggesting that ALD is the most gentle process for the graphene. However, when analyzing the spectrum for SiO_2, it can be assumed that the graphene is still intact since the 2D-peak has only shifted by $\sim 10\,cm^{-1}$ from the graphene's characteristic signature 2D-peak at $2674\,cm^{-1}$ [176]. Thus, PECVD is still an option, despite its light damaging effects on the graphene.

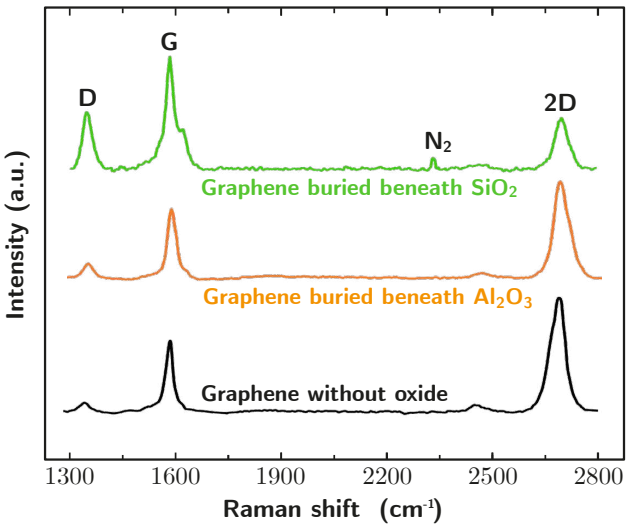

Figure 5.24: Raman spectra of the transferred graphene sheet before (black curve) and after the plasma enhanced deposition of SiO_2 (green curve) and atomic layer deposition of Al_2O_3 [175]. Note that spectra are not equally scaled in intensity. The peak at $2328\,cm^{-1}$ is attributed to atmospheric nitrogen (N_2) and can be neglected.

Further investigation of the transferred graphene layer was done by crossway electrical measurements throughout the structured graphene before and after SiO_2 deposition. Along the shortest path (measuring of two working opposite contact pads) the impedance of the center gate graphene averaged at $21\,k\Omega$. After deposition, the impedance was measured at $24.5\,k\Omega$ on average, an increase by 17 %. Thus, the structural and electrical integrity of the layer seems partially impaired but mostly intact. However, not every terminal provided electrical contact neither after the oxide deposition nor before that. The resistance at the metal/graphene interface is reportedly a bottleneck for any graphene application [180–182]. Many of the metal contacts connecting to the graphene at the edges of a BTG cell did exhibit very high resistances and often no conductivity at all. To encounter this issue, Franklin et al. [183]

reported on double metal pads creating a metal/graphene/metal stack. They observed strong improvement in the contact resistance and attributed it to an enhancement of the effective graphene/metal coupling and to higher graphene doping from the presence of a second metal layer. Figure 5.25 shows an application example of double contact pads for the BTG heterostructure. Six out of ten pads had been equipped with gold bottom layers. A noticeable improvement of the contact resistance could not be detected for this setup. However, none of those double contacts failed connectivity, whereas two of the remaining single pads did not provide any contact at all.

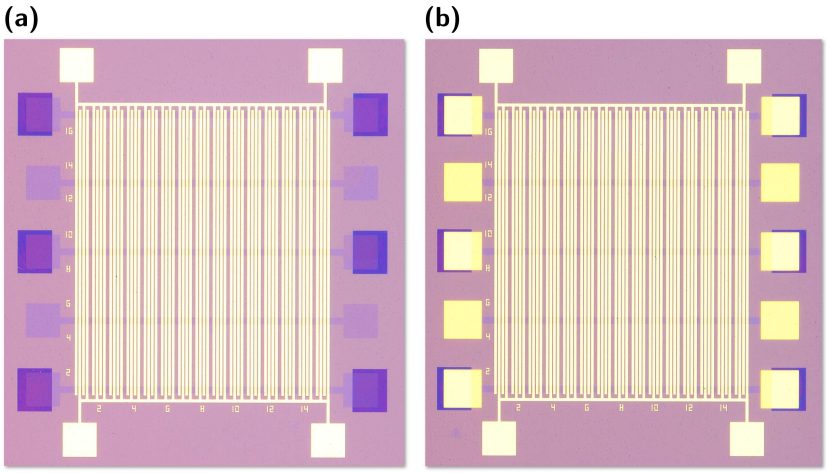

Figure 5.25: Double contact pads for the BTG heterostructure. Six out of ten pads had been equipped with gold bottom layers. (a) Graphene on top, gold bottom layers appear blueish since their thickness is only 8 nm. (b) Same cell after oxide deposition, contact etching and top metal deposition for all pads.

Note that unintentional electrostatic doping of the graphene by the side gate potentials should be of no concern here. A decline of the density of states within the graphene layer would appear by moving the Fermi-level to the very vicinity of the Dirac-point. However, a static potential configuration from the side gates coincides with that event is highly unlikely and would be detectable in the transfer characteristics. Fluctuation of the graphene's conductivity by unintentional doping would also not affect the functionality. After all, the graphene is only used for electrostatic biasing and does not need to drive any significant electrical current. Furthermore, permanent contact to the oxide from below and above results in chemical doping of the graphene, which always provides available states at the interface. In conclusion, it can be assumed that the buried graphene layers are suitable enough to serve as gate electrodes for the BTGs.

5.2 The Buried Multi Gate Substrates

The buried multi gate (BMG) architecture was designed and manufactured by Grap et al. [16, 48] at the Institute for Semiconductor Technology, RWTH Aachen University. Due to the close cooperation, BMG substrates were available for this thesis. Chapter II, section 2.2.2 describes the benefits of having an entire set of individually addressable gates i.e. multiple gates. For example, an EF-FET configuration can only be achieved by implementing alternating potential barriers within a multi gate landscape. This section explains the design of the BMG architecture and how it is fabricated.

Figure 5.26 shows the schematics in a cross-section. In the latest version of the platform the CNT is exposed to 17 gates buried beneath 20 nm of aluminum oxide from an ALD process. A single BMG cell has an annular shape with a 50 µm diameter. The mutually insulated gates are the result of a damascene process with subsequent chemical mechanical polishing. Titanium nitride and silicon dioxide were deposited in an ALD/remote-PECVD cluster-tool in alternating sequence.

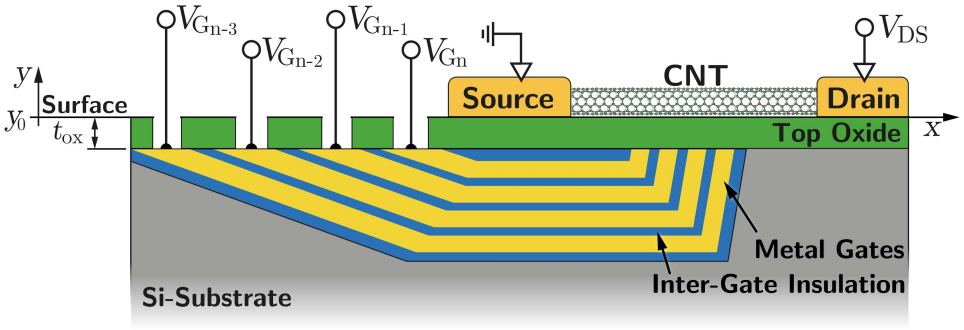

Figure 5.26: Schematics of the BMG platform by Grap et al. (showing four exemplary gates). The latest version consists of n = 17 individually addressable TiN-gates insulated by SiO_2 (inter-gate insulation) and buried beneath $t_{ox} = 20$ nm of Al_2O_3.

5.2.1 Substrate Fabrication

Figure 5.27 depicts the fabrication process and unravels the fundamental idea behind the BMG architecture. Fabrication begins with the deposition of a SiO_2 hard mask on a silicon substrate using remote plasma-enhanced chemical vapor deposition (rPECVD). Afterwards, the hard mask is patterned with UV-lithography and wet etched in buffered oxide etch (BOE) that yields annular shaped SiO_2-mesas. A thin layer of photoresist then masks the surrounding SiO_2-mesas (a). A hard bake at 300 °C for five minutes rounds the edges of the resist. Therefore, the subsequent SF_6/O_2-plasma etching erodes the resist

while, at the same time, the SiO_2 hard mask stays intact. This results in a torus-shaped groove with very shallow flanks at the outer edge and steep flanks at the inner edge (b). The next step as shown in (c) involves alternating in-situ deposition of 5 nm of TiN and 14 nm of SiO_2 (ALD/rPECVD cluster-tool). The groove in the Si-substrate is conformally covered by the ALD-deposited TiN. Note that the SiO_2 from rPECVD has a lower deposition rate on the steep flank than on the shallow flank (ratio ~0.5). This way 14 nm of SiO_2 deposition reduces to 7 nm SiO_2 inter-gate insulation in the multi gate area. The length of the gates is directly given by the TiN deposition i.e. 5 nm. To uncover and flatten the gate and contact areas, the samples are polished using CMP (d). Finally, ALD deposition of 20 nm Al_2O_3 serves as gate oxide on top (e). To regain access to the outer ring for electrically contacting the gates, a small window has to be etched in the top oxide (f). Due to low selectivity for almost any ionized gases in a RIE process, the windows are wet-etched by a 1:1 H_2O:H_3PO_4-mixture with a rate of 5.25 $^{nm}/_{min}$ at 50 °C (cf. appendix 9.3). (f) also shows the contact configuration for a CNT device.

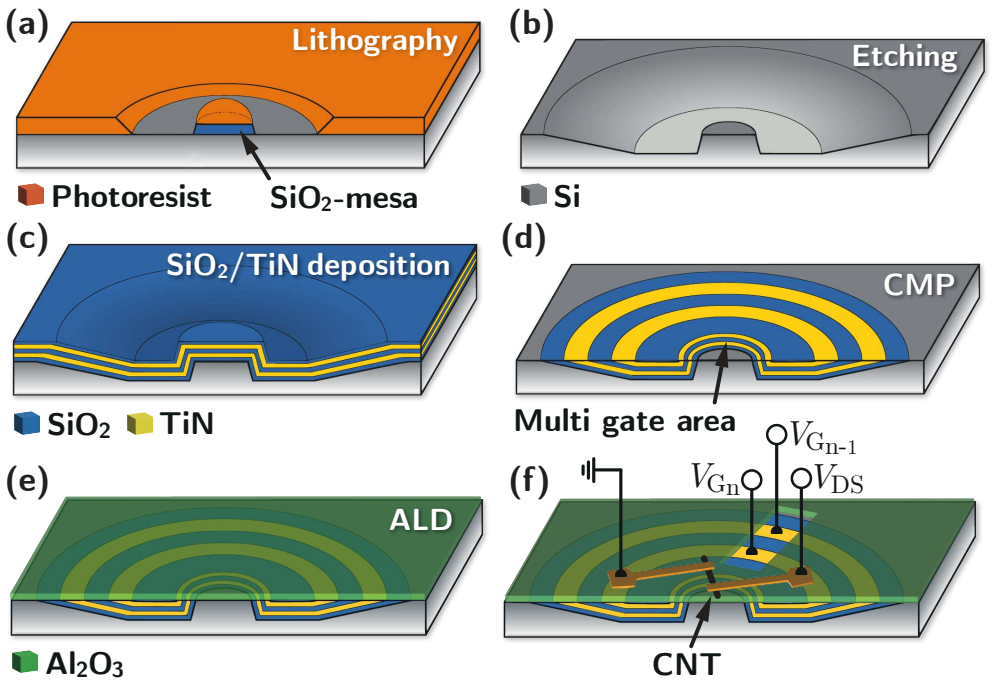

Figure 5.27: Process flow of the BMG substrate **(a-e)** and completed CNT device with access window through the top oxide for gate contacts **(f)**. Detailed explanations are given in the text of this section. (The figure is modeled after [16] with permission from T. Grap.)

5.2.2 Substrate Analysis

Thoroughly assessment of the BMG architecture had been done by Grap [48]. One of the main concern was the integrity of the inter-gate insulation and the conductivity of the metal gates. Not only diffusion of oxygen during the SiO_2 deposition could occur, but also oxidation of the TiN layers. However, measurements ensured that the SiO_2 between the TiN is stable up to 10 V and exhibits only small leakage currents of $\sim 10^{-13}$ A. A rapid thermal annealing process at 500 °C was carried out after deposition to improve the conductivity of the TiN layers.[28]. The unavoidable parallel annealing of the SiO_2 layers had basically no effect on the leakage current. The SEM micrograph displayed in figure 5.28.d shows the cross-section of a BMG test substrate with only five gates. Mutual insulation is in fact very thin but visibly maintained throughout the emergence at the surface. The other SEM micrographs show a bird's eye view of a full BMG cell (a) and a magnification to the multi gate area (b,c).

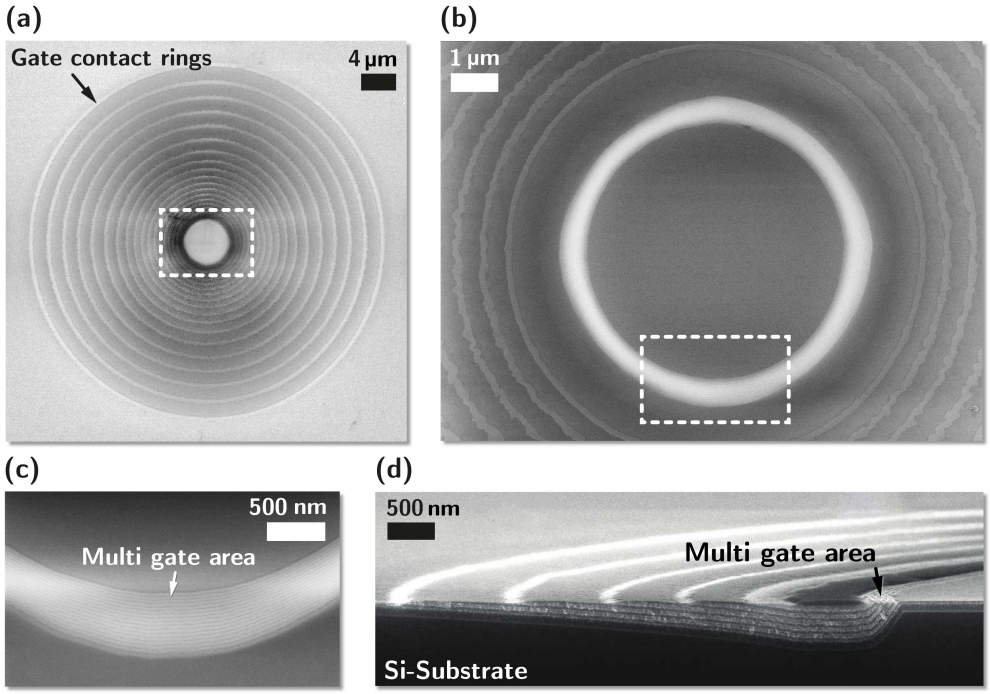

Figure 5.28: SEM micrograph analysis: (a) Bird's eye view of the full extent of a BMG cell with the outer contact-area and (b) magnification of the same cell. **(c)** Much greater magnification reveals the multi gate area in detail at the inner ring of the cell (magnified from (b)). **(d)** Cross-section of a BMG test substrate with only five gates. The alternating layer deposition is clearly visible (image reused with permission from Thomas Grap [48]).

[28] Rapid thermal annealing after thin film deposition of TiN to improve the electrical properties was originally proposed by Ponon et al. [184] and van Bui et al. [185]

The BTG and the BMG architectures are obviously not only different in structure, they also derived from a very different fabrication process. The major difference and also advantage of the BMG substrates is the use of CMP, which is available at RWTH Aachen University. The AFM image in figure 5.29 exemplifies how surface roughness could be reduced to the minimum after polishing. The subsequently deposited aluminum oxide layer (by ALD) had no effect on surface roughness. Within the multi gate area, measurable elevations are restricted to about 1 nm, which can be assumed superb surface topology.

The latest version of the BMG features seventeen 5 nm TiN gates insulated by 7 nm SiO_2. Other demonstrations of multi gate platforms exhibit gates with lateral dimensions on the order of 50 nm and larger, which do not comply with the quantum conditions of an energy filtering device [186–189].

Because of its dimensions, surface smoothness is far more important for the BMGs than it is for the BTGs: A difference in height of two neighboring gates should not exceed the distance between those gates. Otherwise the potential distribution will fluctuate on a greater scale lowering the control over the gate landscape.

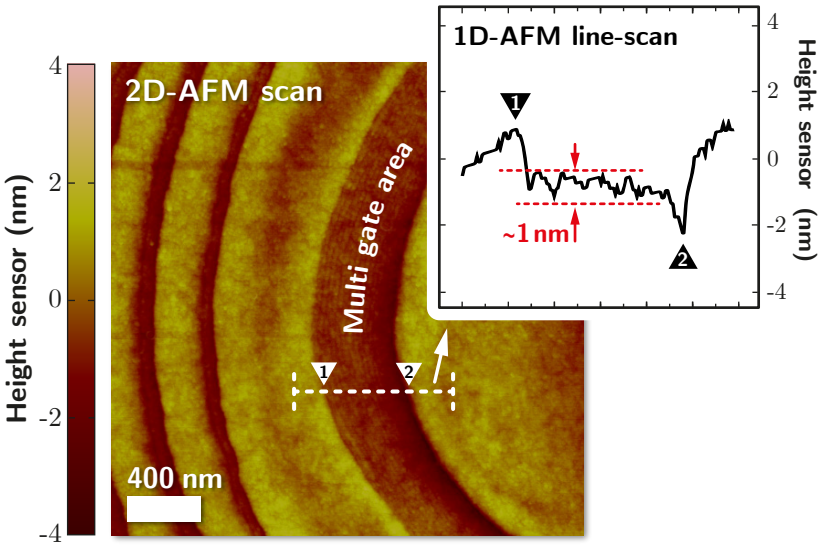

Figure 5.29: 2D AFM and 1D AFM line-scan measurements of a single cell of the buried multi gates. Surface roughness does not exceed 1 nm in the relevant multi-gate area.

Chapter VI

Fabrication of Carbon Nanotube Transistors

Once the triple and multi gate substrates are introduced, this chapter is concerned with the fabrication of the actual CNTFET devices on those platforms. Both BTG and BMG platforms demand a similar approach in nano-fabrication techniques, yet, the BMGs need two extra steps in the process. The entire fabrication is almost exclusively based on electron beam lithography and physical vapor deposition methods. This chapter includes the deposition of carbon nanotubes, the necessary post-production for the BMGs and the fabrication of metal contact terminals.

6.1 CNT Surface Application

CNTs synthesized via VSS or VLS were purchased from IoLiTec Ionic Liquids Technologies GmbH with diameters ranging from 1 nm to 2 nm and with average lengths of 2 µm. The CNTs came untreated and were stored as a deep black-colored powder. Any surface application requires some sort of a liquid agent. Since CNTs are extremely hydrophobic, a dispersion in water needs chemical alteration with several strong acids. The next section 6.1.1 takes a closer look on this subject. The fastest and simplest method to liquefy the CNTs is to disperse the powder in isopropyl alcohol (IPA). For 100 ml IPA a tiny pinch of CNT powder (estimated 10 µg) should be sufficient. Meaningful studies do not exist on that matter, cautiously mixing at its own discretion is recommended though.[29] Before application to any surface, the IPA-CNT colloid needs ultrasonic treatment in order to dilute and disentangle the CNTs and avoid the formation of clusters. Note that at this point in the fabrication process, steps for BTG and BMG substrates are still identical. It will be specifically mentioned below when this is no longer the case.

Experiments suggest that spin-on deposition achieves the best results in having the right amount of CNTs distributed on the substrate. The CNT density on the surface must be high enough so that there is a high probability of finding a single CNT across the triple or multi gate area. However, the CNT density must not become too high for too many CNT clusters to deposit (clumping). Further experiments showed that lowest rate of clumping is obtained at a spin-on velocity of 3000 rpm for 60 s. Going slower or even faster measurably increases chances of clumping. Using no spin-on but sole dry-heating of the substrate led to the worst occurrence of clumping.

After spin-on, the substrate is dried on a hotplate. Although the BTG and BMG substrates are designed to accommodate as many cells as possible, the probability for one CNT to align perfectly across a gate area is low. This means that searching for suited CNT candidates is an integral part of the fabrication process. Since dimensions of a CNT are simply too small for most optical microscopes, searching is done by SEM. To gain sufficiently high contrast, a beam energy of 10 keV was most practical. The search included random scans, but also meander-like patterns within stepwise stage moving. The exact coordinates relative to orientation marks must be saved once an gate-aligned CNT is found. Figure 6.1 shows one CNT example for each platform right after spotting. As a reminder: Only the BTG substrates are manufactured within the scope of this thesis. The BMG samples have been

[29] Note that even an extremely small amount of the powder results in very high concentration of CNTs in the liquid.

obtained from colleagues at RWTH Aachen University. However, the available BMG substrates lack all kinds of alignment marks in the vicinity of each cell. They still have to be integrated to the substrate. Optical lithography is way too inaccurate to be used at this point in the process. Thus, for every cell hosting a suitable CNT, an additional electron beam lithography step for the alignment marks is carried out.

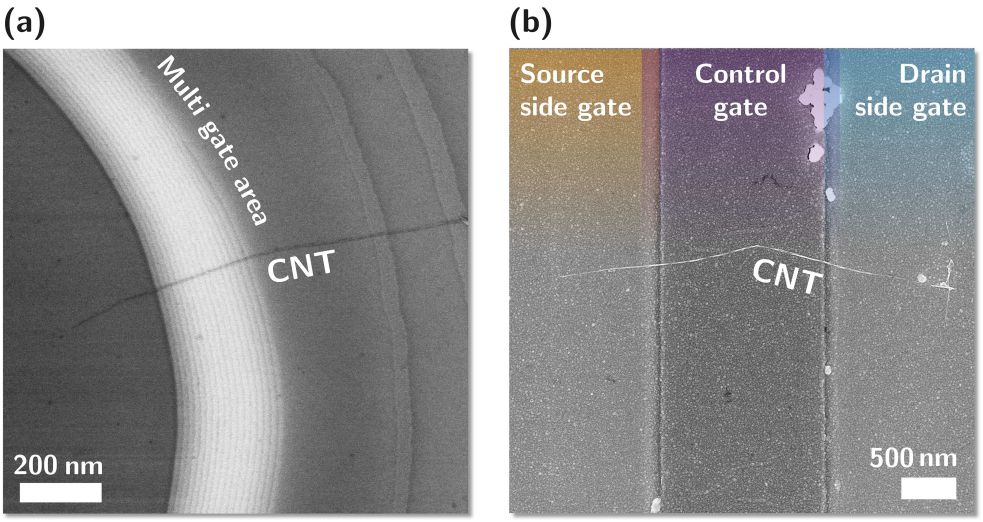

Figure 6.1: (a) SEM micrograph of a CNT perfectly aligned perpendicular to the multi gate area of a BMG cell. (b) SEM micrograph of a CNT aligned across the triple gate section within a BTG cell (b).

6.1.1 Dielectrophoretic Alignment

Deposition of CNTs is a random process. As of today it is not feasible to just choose a single CNT, seizing and placing it anywhere at will. However, there is the option of so-called dielectrophoretic (DEP) alignment, which will be discussed in this section.

DEP alignment is based on an induced dipole moment forcing particles to interact with a non-uniform electrical field emitted by an electrode pair. Having those particles dispersed in a dielectric liquid, the particles are moved by the so called dielectrophoretic force. Considering cylindrical objects, the DEP-force can be split into one part interacting with the short axis (lateral force) and another part interacting with the long axis (vertical force) [190]. As a component of the DEP-force, the permittivity is treated as a complex function depending on the specific conductance and the applied frequency. However, the vertical force is more distinct for low frequencies but will decrease with higher frequencies and is eventually inferior to the lateral force

after reaching a certain frequency f_0. This means that it is possible to almost freely maneuver nano-objects towards their final position only by shifting the frequency above or below f_0. Since the permittivity is directly related to the material, f_0 will alter with different objects and dispersions [191]. Apart from the fact that CNTs can only roughly considered to be cylindrical objects, the CNT dispersion also must maintain a droplet shape after dripping it onto the surface of the substrate. Due to its lack of surface tension IPA will immediately flatten out and quickly evaporate. In this case the CNTs do not move as easily and do not have sufficient time to align properly. To disperse the CNTs in water instead, is a labor intense task. To test the dielectrophoretic application beforehand, nanowires (NWs) are used instead since they disperse much better in water than CNTs. Indium arsenide (InAs) nanowires with 2 µm average length and deionized water ($f_0 \approx 10\,\mathrm{MHz}$) were used. Test samples were composed of large electrode arrays with hundreds of electrode pairs to obtain meaningful and statistically relevant results. Figure 6.2 shows one electrode pair used in the experiments along with an unaligned InAs-nanowire and an overall aligned InAs-nanowire, respectively. Nanowires, which only have been exposed to frequencies below f_0 did indeed get attracted but could not fully align along the electrodes due to insufficient lateral force (a). Having the frequency operating at a low level and then increased above f_0 (therefore also increasing the relative influence of the lateral force) the nanowire aligned entirely (b).

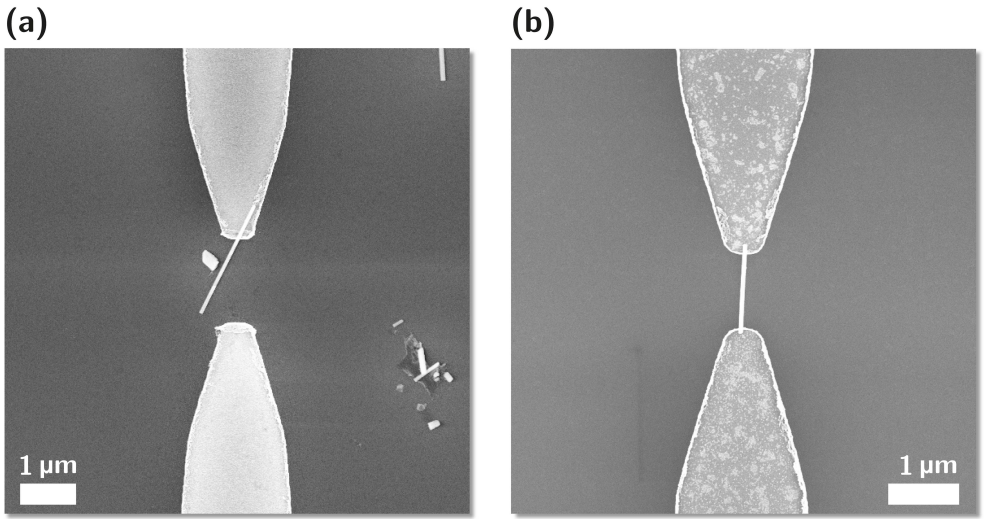

Figure 6.2: SEM micrographs of InAs-nanowires attached to electrodes on test samples after DEP: (a) The example shows an unaligned nanowire with no prior frequency variation. Nanowires were indeed attracted, but only by their long axis, failing to connect both electrodes. (b) Nanowires being exposed to a frequency shift above f_0 fully aligned themselves across both electrodes.

To exchange the nanowires for CNTs in water, chemical alternation i.e. functionalization has to be accomplished. This process inserts functional carboxyl groups (–COOH) on the sidewall of a CNT eliminating its hydrophobic characteristic [192, 193]. Osorio et al. [194] published a meta study to find the best approach. They recommend to immerse the pristine CNTs in a 3:1 mixture of H_2SO_4:HNO_3 at room temperature with a subsequent ultrasonic bath for at least two hours. Extraction can be enforced by vacuum filtering through a cellulose acetate membrane with sub-300 nm pores and repeated water rinsing. The experimental setup of Osorio et al. could be successfully recreated (cf. figure 6.3a). However, after filtering the CNT density was extremely low, even after excessively increasing the initial amount of CNT powder. A specific benefit over the spinning-on method as described in the previous section, could not be observed. On the contrary, the effort put into the dielectrophoretic setup with the necessary chemical CNT treatment does not support the idea of having a universal platform for easy transistor characterization. Figures 6.3b,c show SEM micrographs of a functionalized and dielectrophoretically aligned CNT (b) as well as attracted non-functionalized CNT clusters (c), both from water dispersions. The huge reduction of CNT clusters in (b) clearly points out how water solubility was enabled by the acid treatment.

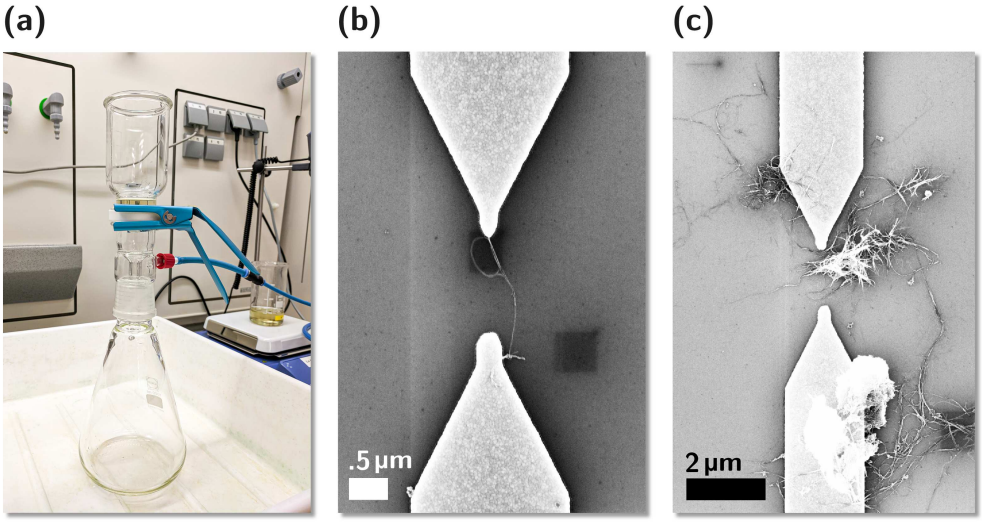

Figure 6.3: (a) Experimental setup for CNT functionalization. Membrane vacuum filtration setup in the foreground, CNTs dispersed in acids in the background. (b) SEM micrograph of an DEP-aligned CNT with prior functionalization treatment. (c) SEM micrograph of a cluster of non-functionalized CNTs.

6.2 E-beam Fabrication

The resolution of UV-lithography mask aligners used in research do not cope with the size of suitable CNTs and its individual position. Sophisticated projection lithography and ultra deep UV-lithography are mostly reserved to industrial development. Instead, the fabrication of transistors with deposited CNTs is done via e-beam lithography (EBL) as introduced in chapter 4.2.2.

6.2.1 Overlay Patterning

The ability to align a pattern on a mask with an existing structure on a wafer/sample is called overlay lithography or in case of EBL overlay patterning. Since CNTs are randomly deposited onto the BTGs and BMGs, their position relative to the positioning marks are crucial for designing the CAD-masks for contact fabrication (or any other purpose). A previously taken SEM-image of the CNT is placed in the CAD software in order to have a real location reference. The coordinates in the CAD-mask can (but do not have to)[30] concur with the coordinate system already being implemented on the sample. The coordinates in the software are labeled as U and V, whereas X and Y are usually reserved for the absolute position of the stage. Figure 6.4a illustrates a CAD-example for contact terminals on a BTG substrate.

Depending on the minimum feature size of the targeted structures, the effort to put in focusing the electron beam can be variable. As "a rule of thumb", for 200 nm wide structures the single spot beam-imprint inside the resist should not exceed 20 nm in diameter. The space between two scanned lines in U,V-coordinates is called area step size A_{uv} (in case horizontal distance equals vertical distance) and should be set according to the beam-imprint size. For a beam-imprint size of 20 nm, an A_{uv} of 10 nm means that exposed areas are just about to adjoin each other. However, this does not take scattering into account. An additional distance of approximately 2 nm to either side should be considered here.[31] The reproducibility of EBL is based on the exposure dose D_0, which is composed of the scan dwelling time τ_{d}, i.e. the inverse beam speed, the beam current I_{b}, and the area step size A_{uv}:

$$D_0\,[\mu\mathrm{C}/\mathrm{cm}^2] = I_{\mathrm{b}} \cdot \tau_{\mathrm{d}} \cdot A_{\mathrm{uv}}^{-2}\ . \tag{6.1}$$

[30] In case the EBL's U,V-coordinates do not match with the CAD tool's U,V-coordinates, the EBL software provides a built-in third coordinate system, the local u,v-coordinates. It allows for more flexibility when it comes to writing multiple masks in a series. However, introducing a third coordinate system makes the entire procedure unnecessarily complex. To design the CAD-mask always within the same coordinates is faster and easier.

[31] Based on experimental experience. The impact of scattering i.e. the proximity effect is a major research subject on its own and exceeds the scope of this thesis.

The beam current I_b has to be measured before every run. It depends on the filament electron extraction voltage, the beam aperture and the acceleration voltage. After tuning the beam - including lens correction procedures - the software's internal U,V-coordinates have to be aligned to the imposed coordinate system on the sample. At least three position marks on the sample need to be assigned to the relating U,V-values (so-called 3-point alignment, cf. figure 6.4b). From this point, navigation within the CAD-mask equals the actual movement of the stage holding the sample. To maintain a focused beam over the entire pattern, the CAD-mask is automatically divided into so-called square writefields of 50, 100, or even 1000 µm in size. Within one writefield the beam scan is controlled by the deflector lenses. To write a neighboring writefield, the stage has to move accordingly. Choosing a small

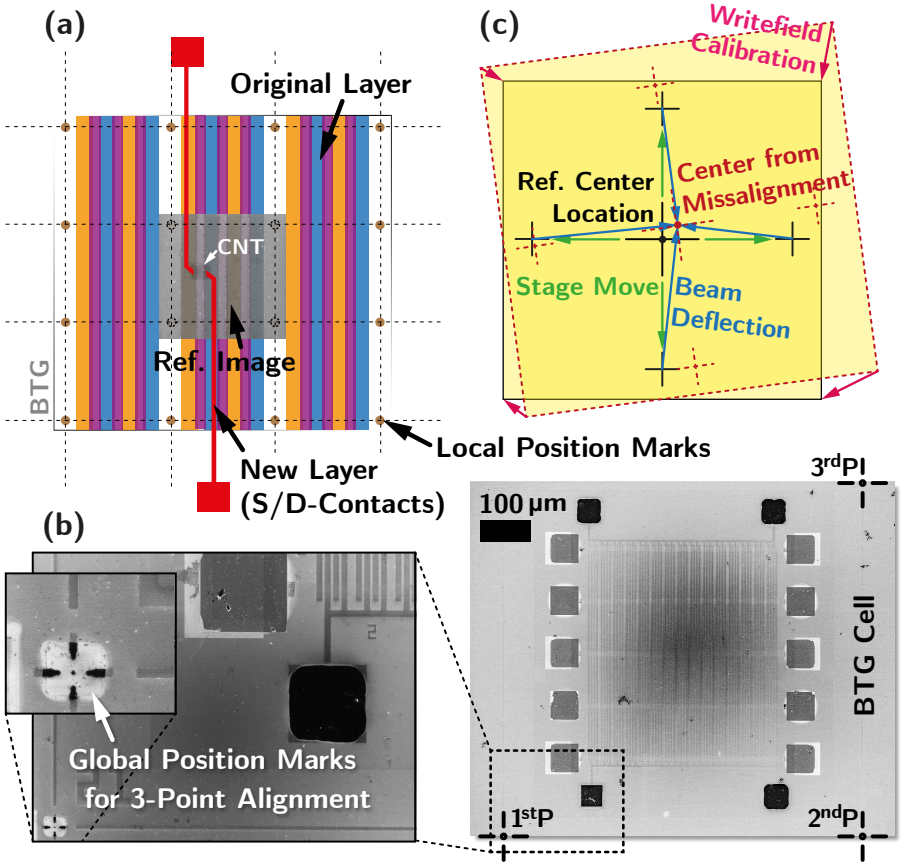

Figure 6.4: EBL workflow for the BTGs: (a) Based on a SEM micrograph the new layer is drawn in reference to existing structures. Local position marks are not only used as reference, but also for high accuracy mark scans. (b) Global position marks are located in every corner of each cell indicating the sample's own U,V-coordinates for 3-point alignment. (c) The writefield alignment corrects any tilting of the fields for perfect stitching.

writefield means higher resolution capability, since the beam does not have to be deflected far away from its central point with maximum focus. The formation of writefields requires coordination in its line-up to prevent tilted stitching. To handle the stitching, a procedure called writefield alignment is executed (cf. figure 6.4c).[32] It begins by taking a reference image at the current stage location. Then, the stage moves a definite distance away from the reference to repeat the image recording. Since the stage has moved, the deflector lenses have to consider the distance in order to reproduce the reference image. The new image can then be compared with the reference - either manually or automatically. After repeating this for three further positions, the deviation from the reference can be used to adjust the lenses so that all writefields will perfectly stitch together. The generation of writefields can be influenced by the CAD-mask design. The first writefield always begins at the lower left corner where the first polygon is placed. The most critical structure in the design should therefore not be located on or near the edge of a writefield, but instead at its very center.

To increase the alignment accuracy even further, an additional mark scan has to be conducted. The marks to be scanned have to lie inside the limits of a single writefield, which has to be considered early in the design of the substrate. The EBL software recognizes the alignment marks in the CAD-mask (there are certain layers reserved in the GDS format to indicate special purposes) and starts the procedure automatically. Similar to the writefield alignment, four positions are scanned whereas for every mark its center must be selected in the image taken. The software calculates any remaining shift to eventually accomplish perfect overlay of the mask and the structures on the sample. The mark scan had been used for all EBL steps within the CNTFET fabrication process. However, unlike the writefield alignment the mark scan is an optional procedure just to increase alignment accuracy down to at least 50 nm at the specific writefield containing those marks. Without the mark scan estimated accuracy is around 300 nm to 1 µm.

6.2.2 CSAR62 for Improved Lift-Off Conditions

After exposed areas of the resist are dissolved by a developer, post processing includes either etching or metal deposition. The latter is denoted as lift-off and is discussed in this section. Directly after the metal has been deposited, the substrate receives a bath in a solvent to remove the remaining resist entirely and to lift the surplus metal, hence the term lift-off process. But, there are a few conditions deciding over the success of a lift-off. A very simple

[32] Note that modern EBL systems support stitching-free patterning with moving-stage motor control units. However, the available system only supports stitched patterning.

rule to follow is having a resist-to-metal thickness ratio of at least 3:1. For example, a 100 nm metal layer requires at least 300 nm of resist [195]. At the same time, the resist itself plays an important role for the lift-off. In order to actually lift the metal, the developed area in the resist must exhibit slightly negatively inclined flanks, the so-called undercut (cf. figure 6.5a). As an alternative, a two-layer resist can be used, where the bottom layer has a higher sensitivity for the exposure dose than the top layer. This way, the bottom resist will experience a much wider opening after developing (cf. figure 6.5b). There is a number of excellent e-beam resists, however, PMMA is the most common one. The sensitivity of PMMA is easily adjustable by the use of different molecular weights. PMMA 50 K translates to a molecular weight of 50 $^{kg}/_{mol}$ and has a 20 % higher sensitivity for the exposure dose than PMMA 950 K [196]. Unfortunately, the sensitivity of PMMA in general is relatively low. Therefore, a necessary higher dwell time amplifies scattering effects in PMMA and limits the resolution. Especially areas in close proximity are very much affected of mutual overexposure through scattering that decrease contrast after developing. This makes lithography fabrication with PMMA in which metal contacts are supposed to be only 50 to 100 nm apart very difficult. A two-layer resist application adds to this problem since the bottom resist becomes wider than the actual design. A high resolution PMMA lithography is still possible though. Using an ultra thin layer thickness (<50 nm) and a high accelerating voltage (∼30 kV) for deeper penetration prevents the beam from scattering inside the resist [197]. However, applying an ultra thin resist drastically limits a follow-up metal deposition in its thickness. Another method to gain high contrast is to develop at low temperatures. Cord et al. [198] found that developing at -15 °C will result in the highest contrast possible for PMMA lithography.

An advanced alternative to PMMA is the chemically enhanced and high resolution resist named CSAR62[33]. This extremely sensitive EBL resist has almost no problems with scattering. Instead of a two-layer resist to improve lift-off, CSAR62 can exhibit the undercut as depicted in figure 6.5a just by

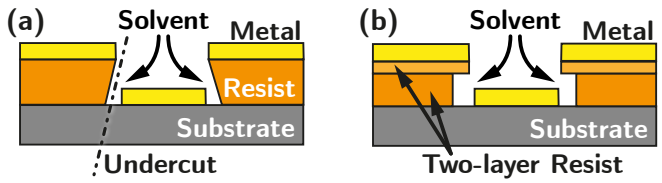

Figure 6.5: (a) Lift-off for one-layer resist with undercut. (b) Lift-off for two-layer resist with different openings.

[33] Poly α-methyl styrene-co-α-chloroacrylate methylester by Allresist GmbH [199].

adjusting the exposure dose. According to the manufacturer the usual dose to clear for CSAR62 is 55 $\mu C/cm^2$ for 240 nm layer thickness. Experiments within the scope of this thesis showed that increasing the dose to 90 $\mu C/cm^2$ inclines the flanks just enough for very good lift-off results with almost no scattering effects. The optimal dose for PMMA is 170 $\mu C/cm^2$ for a 200 nm bottom layer and a 100 nm top layer. Figure 6.6 compares both PMMA and CSAR62 right after developing and deposition in terms of scattering and lift-off results, respectively. In all cases, the beam was working at 15 kV. Obviously, the proximity effect is much more pronounced with PMMA. Even for exposure doses between 170 and 140 $\mu C/cm^2$ there was either overexposure for higher doses or immediate underexposure for smaller doses. Usually this effect can be avoided by changes in contrast throughout the development process. However, below 100 nm it was unacceptably difficult to adjust the contrast any further. As a consequence CSAR62 has become the choice for all EBL process steps since it provides a higher resolution and inhibits scattering to a much greater degree than PMMA. Furthermore, patterning is done faster with CSAR62 due to its higher sensitivity.

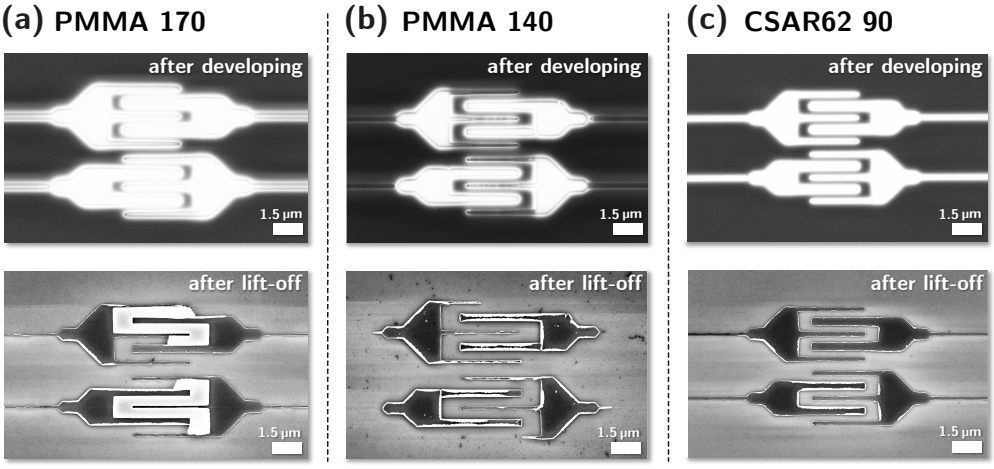

Figure 6.6: PMMA and CSAR62 comparison (same pattern amongst all images, smallest feature size is 100 nm): (a) PMMA exposed at 170 $\mu C/cm^2$ exhibits large scattering issues. Subsequent metal lift-off did not succeed flawlessly. (b) PMMA exposed at a reduced dose of 140 $\mu C/cm^2$ exhibits signs of underexposure leading to metal peeling. (c) CSAR62 exposed to 90 $\mu C/cm^2$ yields the best results. Developed contours are clear and distinct.

Besides improving the resists, the type of metal deposition after developing plays an important role, too. Lift-off works best if the metal deposition exhibits a strong anisotropy (low conformity). This will work in favor of any resist undercuts or two-layer systems. Otherwise, any metal adhering to the sides of the developed areas prevents the resist from being removed by the

solvent. A very high anisotropy during the deposition process is achieved by thermal evaporation. During the experiments sputtering also proved to be a good choice, although its conformity is considerably higher [139]. However, the number of failed lift-off procedures after sputtering was slightly higher than with thermal evaporation. Thus, any critical structures in terms of small sizes were fabricated by thermal evaporation.

6.2.3 Fabrication of Alignment Marks and Contact Windows

As previously mentioned, the BMG platform needs additional process steps before any CNT can be contacted. This includes the fabrication of alignment marks and etched contact windows through the oxide. Since only a few CNTs are eventually selected (usually around five to eight per sample), the alignment marks are individually fabricated only at the locations with suited CNTs present. The alignment marks are placed inside a 50 µm writefield with 25 µm distance to each other. They provide the necessary alignment accuracy when it comes to the local writefield alignment during contact fabrication. Note that it actually does not matter where the marks are physically located inside the writefield. It is only important that every overlay mask is based on the reference image including the visible marks. However, for automatic calculation of the exact mismatch during writefield alignment a symmetrical and even distribution of marks keeps errors at a minimum. The shape of the marks should also be symmetrical, in order to be able to recognize the exact center. The highest accuracy is achieved when designing the marks as small as possible, leaving only a small margin to deviate from the center. Fabrication of metal marks has the advantage of high material contrast when the marks are being scanned for the writefield alignment. For larger marks, this should always be the first choice. However, metal marks require a lift-off process, which can be critical for stand-alone and dot-like structures of ∼200 nm in terms of unwanted peel off. To simply minimize any risk at this point, the alternative at hand is etching the marks since etching is necessary anyway later in the process.

EBL has been carried out with 240 nm of CSAR62 at 15 kV and a dose of 55 $\mu C/cm^2$ since no undercut is needed for etching. Then the resist was developed by amyl-acetate for 60 seconds and rinsed in IPA. Phosphoric acid mixed 1:1 in DI-water at 50 °C is used as etchant for the aluminum oxide on top. The etching rate here is 5.25 nm/min, which has been experimentally determined (appendix 9.3). A complete penetration of the oxide has to be avoided at all costs. Otherwise, the marks might uncover parts of the outer contact area. Any writefield alignment is always a compulsory exposure at the mark's location and approximately five times greater in size than the

marks. After development, the area around the marks will be uncovered and the metal layer from the deposition would inevitably short-circuit some gate contacts. For this reason, the etching goal is to leave a recognizable mark of only about 10 nm depth, which is nearly half the thickness of the oxide. After etching is complete, the resist is removed by dioxolane. Rinsing is done with acetone first and IPA second (dioxolane has a better solubility in acetone). Figure 6.7 shows the SEM-image of a BMG cell after finishing the alignment mark fabrication. The visibility of all four marks is not particularly distinctive, but good enough to locate the center of each mark. The diameter of each mark is set at 500 nm in the CAD-mask. This already takes into account the highly isotropic etching profile of phosphoric acid. Eventually, the diameter of each mark on the sample measured about 1.5 µm, thus being three times larger than originally designed.

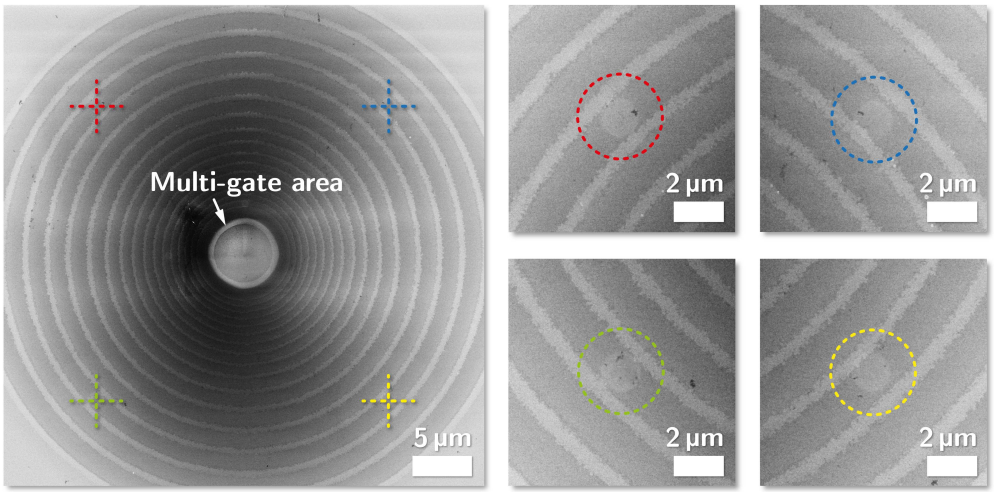

Figure 6.7: BMG cell after alignment mark fabrication: All four marks are placed 25 µm apart from each other whilst centered exactly inside a 50 µm writefield. Marks are circularly shaped featuring a ∼1.5 µm diameter.

After implementing the alignment marks, the sample is ready for any subsequent high accuracy EBL. Before the contact terminals can be fabricated though, appropriate access to the outer contact rings has to be established. One option is to etch small individual windows into the oxide right at the relevant ring. This has the advantage of not risking any unwanted short-circuits since the metal does only contact the area within the designed window. However, this requires an extremely precise alignment in the making, which is possible, yet often prone to failure. Moreover, the following contact lithography has to be as precise as the previous window lithography in order to coincide with the windows, thus multiplying the chance for failure. The other option is to etch thin but long stripes across the contact area. This

method increases the chance of accidentally short-circuiting some of the unprotected gate contact rings, but this is statistically less likely than miss-alignments when fabricating individual windows.[34] Etching is again executed with phosphoric acid mixed 1:1 with DI-Water at 50 °C. This time, the goal is indeed the complete removal of the oxide at the dedicated location, which corresponds to an etching time of 3:50 min.

Once more, the isotropic etching profile must be considered in the design of the windows. The resulting openings are roughly six times wider than in the CAD-mask. The selectivity of materials for the etching process had been tested in a series of experiments beforehand. It turned out that after being exposed to 30 s of phosphoric acid the buried inter-gate insulation, that is SiO_2, showed no noticeable change. This observation is congruent with the results of van Gelder et al. [200]. According to their work the high selectivity comes from the high water content in the etchant. The titanium nitride showed also no visible signs of any etch susceptibility. However, electrical measurements detected a small, yet acceptable increase in contact resistance from 38.2 Ω to 42.5 Ω on average for three test samples. Removing the resist after etching is done the same way as for the alignment marks. An example of the resulting contact windows are shown in the SEM-image in figure 6.8.

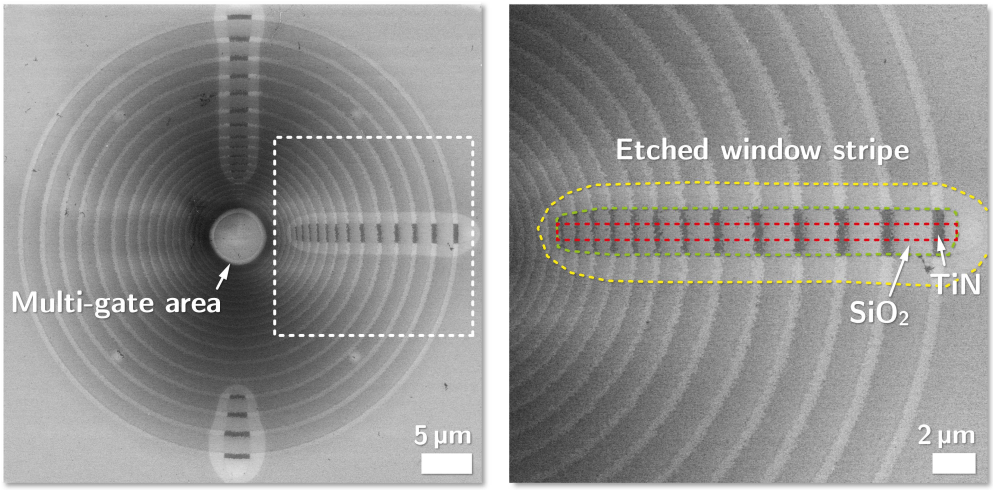

Figure 6.8: BMG cell after contact window fabrication: Within the stripes the dark shade of the metal is a good indicator for a successful etching process since the used SEM detector works in favor of high material contrast. The red dashed line indicates where the CAD-mask was placed, the green dashed line shows the actual etched-through boundary and the yellow dashed line shows the maximal reach of the etchant under the resist during the process. In this area, the aluminum oxide had been etched but not to its full extend.

[34] Based on observations amongst 15 fabricated samples.

6.2.4 Fabrication of Contact Terminals

The random positions of the CNTs on either platform requires EBL in order to contact them precisely. The necessary alignment marks for the BTG substrates were added right at the beginning of the fabrication cycle. Global marks are placed in every corner of a cell on a 1.4 mm grid. Local writefield alignment marks (precision marks) are placed inside the gate structure with 50 µm in distance to each other. The basic principle of the electron beam lithography is the same for both BTG and BMG platforms. Since four precision marks must be located inside a writefield to exploit full accuracy, the writefield size must be chosen accordingly. That is, 100 µm for a BTG field and 50 µm for a BMG field. After a suited CNT was found, an SEM micrograph is taken of the corresponding field including all four precision marks and the CNT placed in this field. The image is then used as reference in the CAD software to design the contact terminals accordingly.

Figure 6.9 shows the CAD-mask for an exemplary BTG heterostructure S/D-contact EBL. Exposure dose was 90 $\mu C/cm^2$ at 15 kV accelerating voltage. The thickness of the CSAR62 resist was 240 nm. Development and stopping was done by amyl-acetate for 60 seconds and DI-water, respectively. A layer of 60 nm gold was deposited by thermal evaporation at $1.2 \cdot 10^{-5}$ mbar. The lift-off procedure for removing the resist and the metal excess was done by dioxolane, then acetone to solve the dioxolane, which then in turn was solved in a bath of isopropyl alcohol. The finished BTG-cell with the fabricated contact terminals and a SEM magnification of the contacted CNT are shown in figure 6.10. The same EBL, developer and deposition parameters are chosen for contact fabrication on a triple graphene BTG. The completed cell and a corresponding

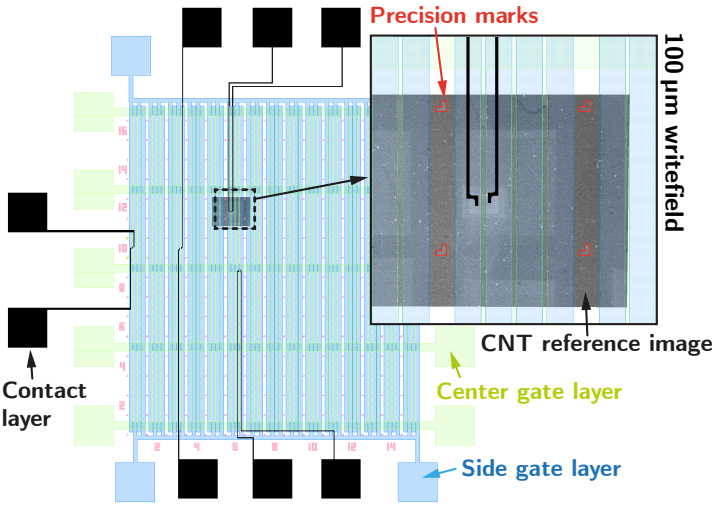

Figure 6.9: CAD mask for CNT contact fabrication. This particular example belongs to the fabrication of CNT contacts on a heterostructure platform. The finished cell is shown by figure 6.10. The relevant layer for the contact terminals is colored in black.

SEM magnification are shown in figure 6.11. As discussed in section 5.1.7 gate-alignment within UV-lithography had manifold outcomes. The gate alignment of the example fabrications is very different. The lithography of the center gate layer of the TG platform resulted in a misalignment with an approximately 150 nm shift to the left. However, a small overlap of the center gate and side gates is still present. On the other hand, the heterostructure example exhibits almost perfect overlap in both directions.

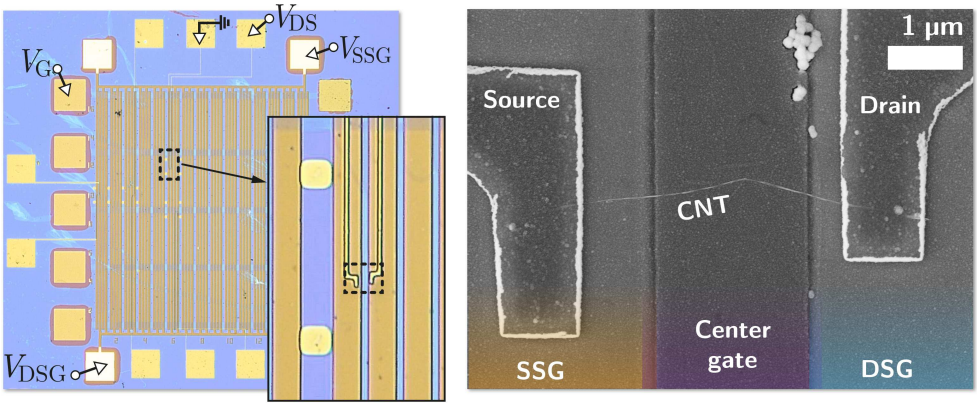

Figure 6.10: BTG heterostructure with CNT contact terminals: OM image of the entire BTG cell with the S/D contact paths (left) and further zoom-in of the CNTFET device in a SEM micrograph (right).

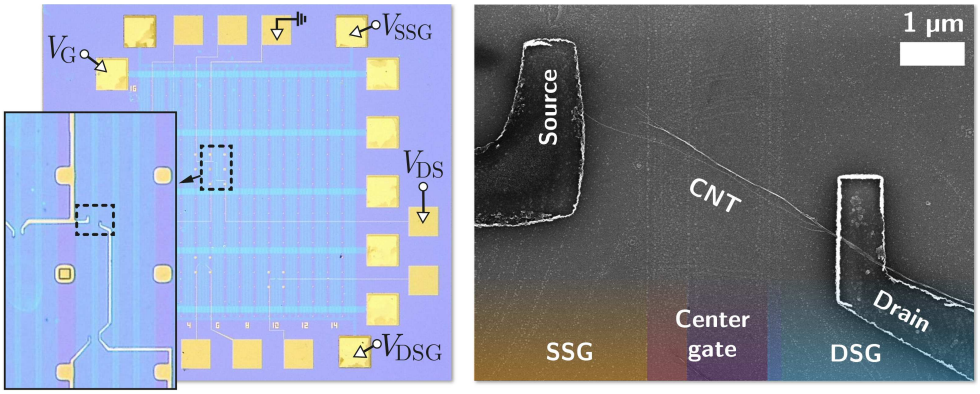

Figure 6.11: BTG triple graphene substrate with CNT contact terminals: OM image of the entire BTG cell with the S/D contact paths (left) and further zoom-in of the CNTFET device in a SEM micrograph (right). Note that the CNT of relevance is the less visible branch connecting the contacts.

After the fabrication of alignment marks and contact windows for the BMGs, as discussed in section 6.2.3, fabrication of contact terminals must be carried out the same way as for the BTGs. However, the patterning design is much more sophisticated than for the BTG substrates. For the realization of energy

filtering devices, all gates must either be individually addressable or clustered into three electrode sets for high/low potentials and a control gate. Figure 6.12 shows an SEM micrograph of the metal leads connecting to gate contact rings. This application examples includes source and drain contacts (S,D), 12 reconfigurable gates (G_{1-12}) and one control gate terminal (G_C) (and its duplicate on the other side of the ring to measure the contact resistance). A zoom-in of the dashed lines is displayed in figure 6.13, which shows how the metal bridges connect through the etched window with the contact rings. The smallest gate contact bridge near the center has 300 nm in width and is positioned just four further connections away from the very last ring. A connection to the last ring, however, requires a width of the contact of only 50 nm. Although fabrication of contacts that small would be feasible in terms of EBL, it would also lead to a dramatic increase of failed lift-off procedures. Considering the effort, which goes into every device, taking this risk seems unjustified and unnecessary since having 12 gates implemented is sufficient enough for basic energy filtering devices. The image also shows the magnified view of the corresponding CNT laying perfectly across the multi gate area. The alignment of all metal contacts was executed very precisely, despite the obvious damage by over-etching of the precision marks in this example. By using previous images, every position of the marks had been restored from comparing

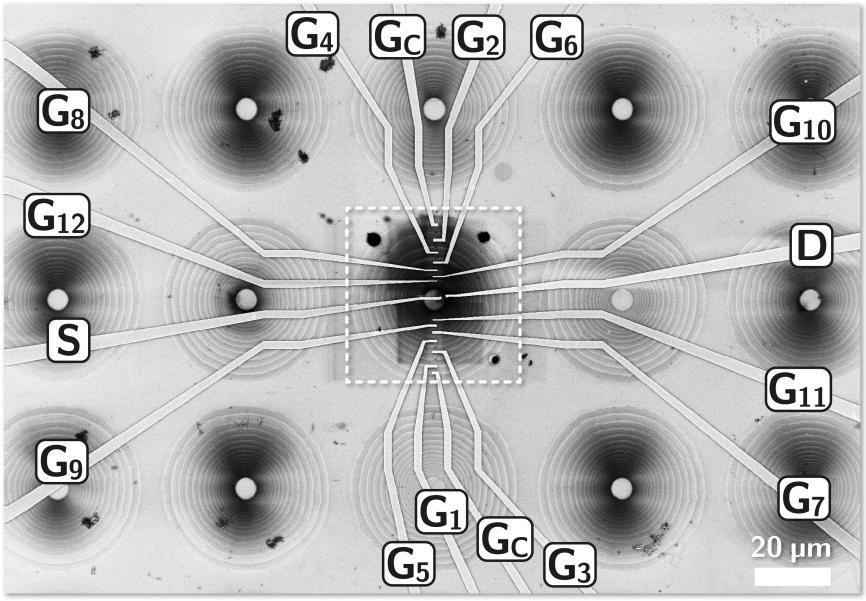

Figure 6.12: SEM micrograph of a BMG substrate with finished contact terminals. In this example 13 of 17 available gates are individually connected, including the control gate for EF-FET configurations (cf. section 2.2.2). Source and drain contacts lead directly to the CNT across the multi gate area in the center.

the surroundings in the reference, such as particles or the contact rings. The SEM micrographs in figure 6.14 show another example of a completed device. Here, the contact metal is made from PVD sputtering of titanium and titanium nitride. The CNT is again perfectly located across the multi gate area as depicted by the left image. The image on the right shows the same device but from an angle of 45°. All fabrication parameters can be found in appendix 9.3.

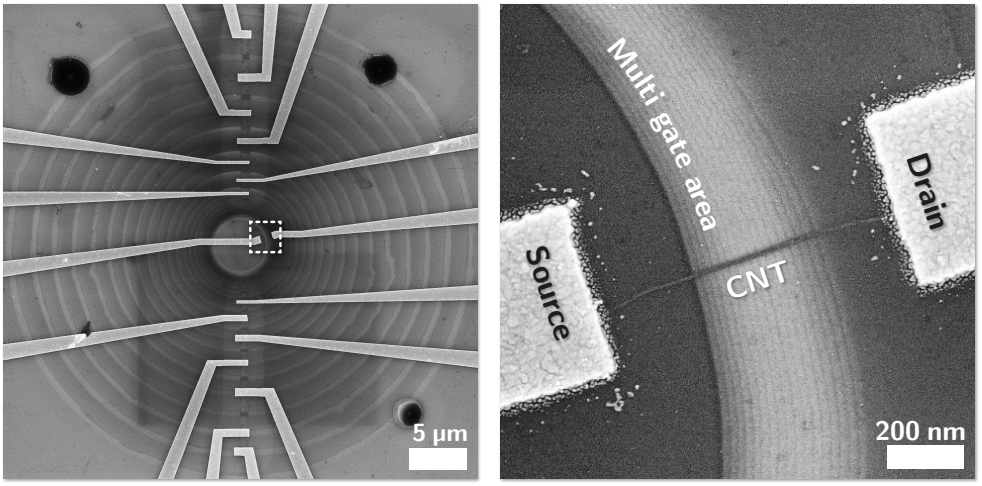

Figure 6.13: SEM micrographs of the BMG substrate with 12 gate contacts, two control gate contacts and one contact for each source and drain. The CNT inside the dashed area is magnified on the right image.

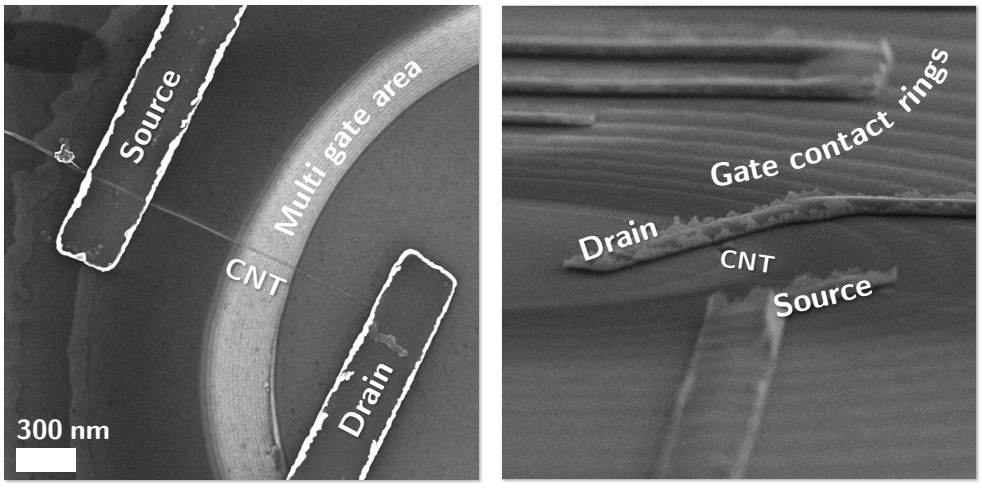

Figure 6.14: SEM micrographs of an additional application example for a CNT device on the BMG platform. Here, the contact metal is made from PVD sputtering of titanium and titanium nitride.

Chapter VII
Electrical Measurements

ELECTRICAL measurements for static transistor characterization are subdivided into three different sections. Within the first sections CNT devices were characterized as Schottky-Barrier-CNTFETs. The second section includes measurements of TFET configurations on the BTG platform and the third section deals with the characterization of energy filtering CNTFET devices on the BMG platform.

A comprehensive transistor characterization consists of transfer and output characteristics ($I_{\mathrm{D}}(V_{\mathrm{G}})$ and $I_{\mathrm{D}}(V_{\mathrm{DS}})$, respectively) as discussed earlier in chapter 2.1.1. However, the output characteristics are of less importance when focusing on investigations regarding subthreshold slope and on on-/off-ratio. Therefore, the output characteristics are included for only a few examples.

7.1 Measurement Setup

As described in chapter 4.3, the used measurement setup accessible at the lab consists of an Everbeing probe station with an Agilent 4156C parameter analyzer equipped with four source measuring units (SMUs) and two voltage source units (VSUs). Since the majority of samples had gold contact pads, the used probing needles were also made of gold to minimize the risk of scratching or damaging the pads.[35] In order to be able to address more than five contacts at the same time, an additional setup at RWTH Aachen University was used involving a chip carrier and ultrasonic bonding. The carrier distributes every bonded wire to outgoing triaxial BNC plugs split over two parameter analyzers for a sufficient amount of SMUs (Keysight B1500A with 8 SMUs and Agilent 4156C with 4 SMUs).

7.2 Characterization of Schottky-Barrier-CNTFETs

Preliminary investigations of typical CNTFET behaviour were conducted on simple back-gate substrates with a 230 nm SiO_2 gate dielectric. Figure 7.1a and b show a SEM micrograph of an exemplary CNTFET and its transfer characteristic, respectively. As expected, the CNT does exhibit ambipolar behavior, which is typical of Schottky-Barrier-FETs. The source and drain interfaces can be interpreted as metal-semiconductor contacts as discussed in

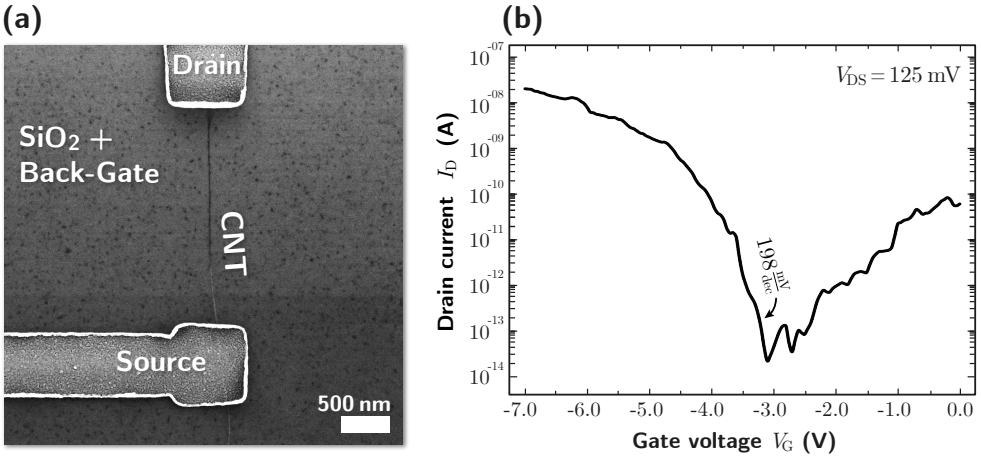

Figure 7.1: (a) SEM micrograph of an exemplary back-gated CNTFET. The wet-thermally oxidized silicon (230 nm SiO_2) serves as gate dielectric and the the silicon substrate as gate electrode. (b) Transfer characteristic of the CNTFET showing Schottky-Barrier MOSFET behavior with asymmetric ambipolarity and *p*-type behavior.

[35] Usually probing needles are made from very hard tungsten or tungsten alloys to protect the tip from damages and wear. However, gold probing needles are relatively soft being more suited to touch the likewise soft gold contact pads.

chapter 3.2. The ambipolarity is obtained due to hole injection for negative gate voltages and electron injection for positive gate voltages. Additionally, a chemical p-doping effect can occur, which is caused by oxygen molecules adsorbed on the CNT-surface when exposed to ambient air or oxidizing chemicals [201, 202]. This behavior is rather unpredictable and manifests itself in a shift of the threshold voltage, i.e. a shift of the minimum drain current. However, this can easily be compensated by an adjustment in the applied voltage. Some of the CNTs used in the measurements showed a very pronounced shift, like the device in figure 7.1b. Others, however, showed only a very small or no shift at all.

The inverse subthreshold slope S in the transfer characteristic of figure 7.1b within the range of $V_\mathrm{G} = -3\,\mathrm{V} \ldots -4\,\mathrm{V}$ reads $\sim 198\,\mathrm{mV/dec}$. Since determination of a CNT's permittivity ϵ_CNT and its diameter d_CNT is rather difficult, the gate geometry factor λ_ch can only be estimated for the present device. According to the supplier of the CNTs, the diameter is in-between 2 and 4 nm with unknown permittivity. However, Uchida et al. experimentally identified ϵ_CNT to be 1.88 for a (17,0)-CNT with $d_\mathrm{CNT} = 1.33\,\mathrm{nm}$ [203].[36] Assuming that CNTs with slightly larger diameters still have a similar permittivity and that the present setup can be considered a simple single-gate planar FET-device, allows to use $\lambda_\mathrm{ch} = \sqrt{\frac{\epsilon_\mathrm{CNT}}{\epsilon_\mathrm{ox}} t_\mathrm{ox} d_\mathrm{CNT}}$ [87]. For reference, a (17,0)-CNT and a 230 nm silicon dioxide gate dielectric ($\epsilon_\mathrm{ox} = 3.8$) results in $\lambda_\mathrm{ch} = \sim 12.3\,\mathrm{nm}$. Inserting this value for λ_ch into equation 3.13 yields an inverse subthreshold slope $S = 174\,\mathrm{mV/dec}$ at room temperature, which comes relatively close to the characteristic of the present CNT. According to [31], the tunneling distance d_t scales $\propto (m^*)^{-1/2}$ being $\sim 5\,\mathrm{nm}$ for CNTs. Note that equation 3.13 is an approximation and is only true for $\lambda_\mathrm{ch} > d_\mathrm{t}$.

The BTG platform can also be used to setup a Schottky-Barrier-CNTFET. To do so, all three gates were temporarily connected acting as one extensive single gate. Figure 7.2 shows the transfer characteristic for that case (red curve) supplemented by an additional measurement with deactivated - i.e. floating side gates (black curve) for comparison. The maximum on-current driven by the selected device is $\sim 100\,\mathrm{nA}$ with an on-/off-ratio in the range of six orders of magnitude. With deactivated side gates the current reduces to $\sim 5\,\mathrm{nA}$. With only $\sim 80\,\mathrm{fA}$ at $V_\mathrm{G} = 0\,\mathrm{V}$ the off-current is relatively small, which coincides with the previous investigation of semiconducting CNTs with plain back-gate platforms. The inverse subthreshold slope S is similar for

[36] This is still an approximation. Uchida et al. calculated the dielectric properties from a cylindrical capacitor setup in, which the measured (17,0)-CNT contains a smaller (8,0)-CNT and is wrapped by a larger (23,0)-CNT.

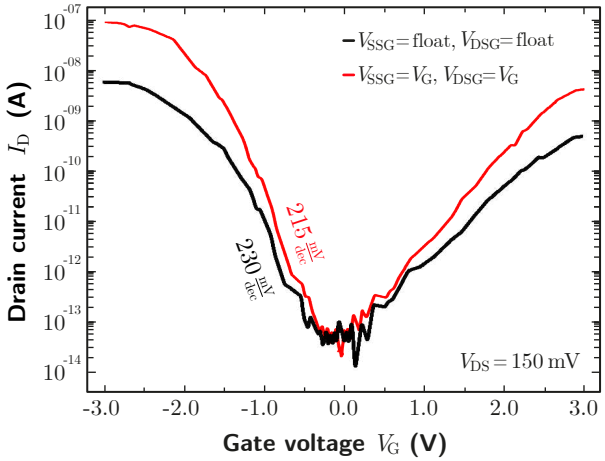

Figure 7.2: Transfer characteristic for floating side gates (black curve) and for a gate union $V_{SSG} = V_{DSG} = V_G$ (red curve) showing typical SB-FET behavior.

both curves with 230 mV/dec for floating side gates and 215 mV/dec for the gate union. The characteristic is similar to typical SB-CNTFETs found in literature [12, 204, 205]. Unlike the back-gate device, this CNTFET has its minimum in drain current near $V_G = 0$ V.

7.3 Characterization of Tunnel-CNTFETs

To achieve steeper inverse subthreshold slopes, TFET configurations were implemented with the BTG platform. Figure 7.3 shows the transfer characteristic of a Tunnel-CNTFET (T-CNTFET) device with applied side gate voltages from 1 V to 3 V for the SSG and -1 V to -3 V for the DSG.[37] Unfortunately, measurements could not be carried out on a device with

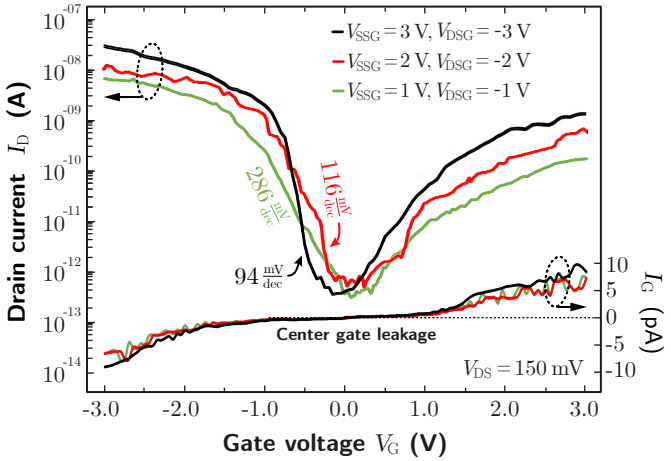

Figure 7.3: T-CNTFET transfer characteristic on the BTGs for three different side gate configurations including center gate leakage current.

[37] Note that for all measurements carried out on the BTGs, the notation used for gate voltage V_G is synonymous to center gate voltage.

perfectly aligned gates as introduced in the previous chapter due to contact issues. Instead, the selected device exhibits a slight misalignment gap, which is limits the inverse subthreshold slope. The best result could be achieved for side gate voltages $V_{SSG} = 3\,V$ and $V_{DSG} = -3\,V$ at room temperature yielding $S = 94\,^{mV}/_{dec}$. The maximum on-current peaks at $\sim$35 nA while the off-current is well below $\sim$1 pA accomplishing an on-/off-ratio of $\sim$5 decades. The figure also includes the overall center gate leakage current I_G being slightly larger than for typical top gate architectures [206]. This is because the electrodes of source and drain cover a relatively large area on the surface all across the buried gate architecture, which eventually increases the possibility for leakage adding to the drain current at $V_G = 0\,V$. This also contributes to the larger inverse subthreshold slope. However, the gate current here is still low enough and has presumably no significant impact on the drain current characteristic.

Measurements at different temperatures can help to verify the characteristic of the fabricated device even further. Figure 7.4 shows the transfer characteristics at room temperature (295 K, from fig. 7.3 as reference), at 373 K and at 423 K.[38] Source side gate and drain side gate are set again to 3 V and -3 V, respectively, implementing the same doping profile as for the previous measurement. A change in the inverse subthreshold slope could not be observed, which is a very strong indication that the device does indeed behave like a TFET. Since its functionality is mainly shaped by the band-pass characteristic filtering the Boltzmann-tail, a higher temperature has only a weak influence on the subthreshold slope. With temperature rising to 423 K the off-state current increases by almost two orders of magnitude

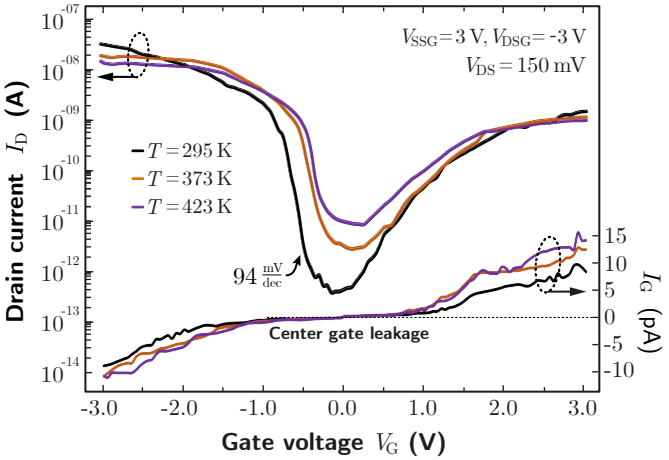

Figure 7.4: T-CNTFET transfer characteristic on the BTGs for three different side gate configurations including center gate leakage current. Measurements are carried out at room temperature (295 K), 373 K and 423 K.

[38] 295 K ≈ 22 °C, 373 K ≈ 100 °C, 423 K ≈ 150 °C.

reducing the on-/off-ratio to ∼4.2 decades at 373 K and ∼3.3 decades at 473 K, respectively. This is probably due to thermal activation of the carriers across the potential barrier of the channel conduction band depending exponentially on the temperature. In contrast, the decrease of the maximum on-current results mainly from the increased phonon scattering at higher temperatures [207–209]. As shown by the figure, the gate leakage current I_G also slightly increases for higher temperatures with a maximum of 16 pA at 423 K. This could in fact be attributed to the electron Frenkel–Poole emission through the intermediate gate dielectric [45]. As some research reported in the past, the influence of temperature on the transfer characteristic is less pronounced for CNTFETs than for MOSFET devices especially in terms of shifting the threshold voltage [210–212].

Figure 7.5 depicts the output characteristics for different gate voltages V_G ranging from -3 V to -1.5 V (a) and at different temperatures (b). As expected, with rising temperature, the drain current I_D decreases as mentioned earlier. The range for the maximum drain-source voltage V_{DS} is very hard to estimate with CNTs. The device can consist of a single CNT sensitive to high currents or more than one CNTs entangled in a string, which increases the capability of driving higher currents.[39] Since there is always an uncertainty about the amount of CNTs, the maximum drain-source voltage V_{DS} was generally limited to 150 mV in order to protect the devices from any damage. The characteristic of the curves depicted in the figure are

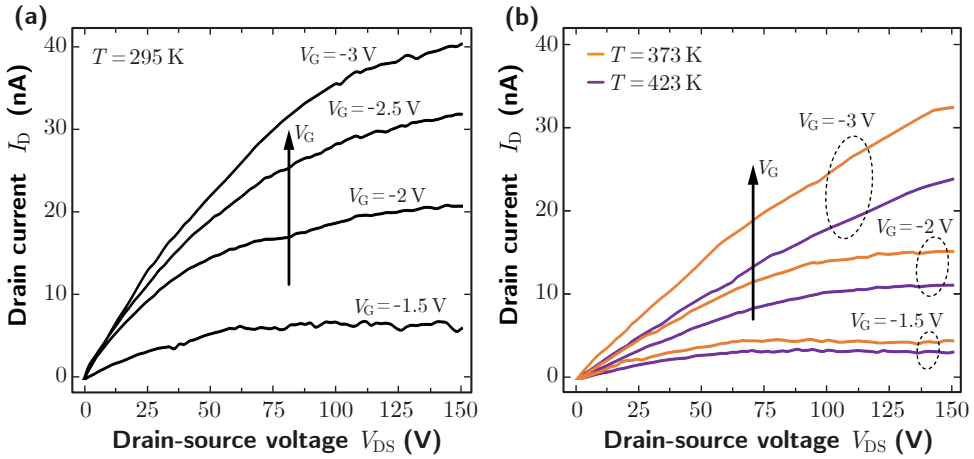

Figure 7.5: Output characteristics for the same CNTFET device used in figure 7.4. (a) Measurements at room temperature. (b) Measurements at high temperature.

[39] Of course there is always the possibility of having metallic CNTs join the string. If all of them are in fact metallic, the device is quickly identified as such and rejected. A combination of metallic and semiconducting CNTs will reveal itself by showing very poor characteristics.

particularly interesting, because they actually reflect typical transistor behavior showing the saturation of I_D for an increase of V_{DS}. Furthermore, having measured the output characteristic for negative gate voltages (p-type) allows estimating the hole mobility μ_h. It can be extracted from the transconductance ${}^{dI_D}/_{dV_G} = \mu_h({}^{C}/_{L^2})V_{DS}$ at $V_{DS} = 25\,\text{mV}$, where ${}^{C}/_{L} = {}^{(2\pi\epsilon_0\epsilon_{ox})}/_{\ln(2t_{ox}r^{-1})}$ for a cylindrical capacitance. As mentioned earlier, the diameter $d = 2r$ is in-between 2 and 4 nm, according to the CNT-supplier. Since the energetic alignment of the intrinsic region is controlled by the center gate, d_{ox} is set to be 20 nm, the thickness of the top oxide. The relative permittivity for SiO_2 is $\epsilon_{ox} = 3.9$ and the channel length is $L = 1.8\,\mu\text{m}$. From figure 7.5a, ${}^{dI_D}/_{dV_G}$ can be estimated to be $5\,{}^{nA}/_{V}$ in the saturation regime. Therefore, the calculated hole mobility is between $\mu_h = 49.6\,{}^{cm^2}/_{Vs}$ (for $r = 2\,\text{nm}$) and $\mu_h = 61.1\,{}^{cm^2}/_{Vs}$ (for $r = 1\,\text{nm}$). Such a hole mobility seems rather low, but is in fact well comparable to that of other CNTFET devices found in literature [60, 61].

7.4 Characterization of Energy Filtering CNTFETs

As discussed in chapter 2.2.2, the implementation of an energy filtering FET requires alternating potential barriers. This method will generate a so-called superlattice acting as a miniband enabling a band-pass filter for the high energetic Boltzmann tail. The application example shown by figure 7.6 is fabricated using the BMG platform and provides 14 mutually insulated gates. Gate 14 is used as the control gate V_{CG}, the remaining even gate numbers are connected (V_G^{even}) and the remaining odd gate numbers are connected (V_G^{odd})

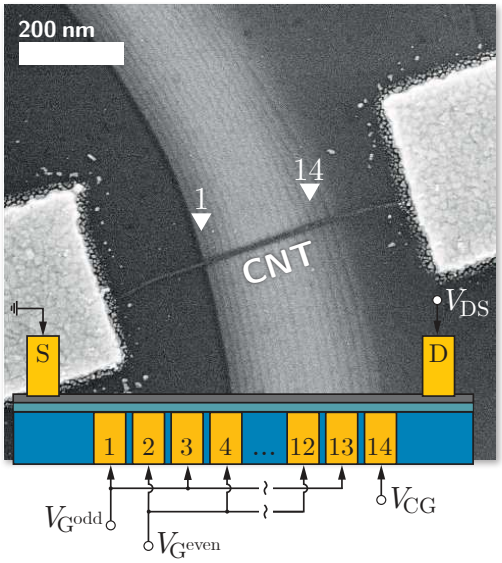

Figure 7.6: The completed EF-CNTFET device on the BMG platform. All odd gates from 1 to 13 and all even gates from 2 to 12 are connected. Gate 14 severs as the control gate.

for the periodic potential generation. The measured transfer characteristic as shown in figure 7.7a is recorded for $V_{DS} = 150\,mV$ (black curve) and $V_{DS} = 100\,mV$ (red curve). The applied control gate voltage V_{CG} ranged from -3 V to 3 V. However, the graph is cropped at $V_{CG} = 0\,V$ since the device did not exhibit any ambipolarity and no further increase of I_D for positive V_{CG} were recorded. An increase of the current might have been observable for much greater gate voltages. However, the CNT or the oxide can be damaged at higher voltages. Several alternating potentials were tested beforehand and the on-/off ratio peaked with four orders of magnitude at a setup of $V_G^{odd} = -3\,V$ and $V_G^{even} = 3\,V$. For $V_{DS} = 150\,mV$ the inverse subthreshold slope reads $56\,^{mV}/_{dec}$, which is just below the thermionic limit of $60\,^{mV}/_{dec}$ suggesting that the device does in fact function as a steep slope transistor. The drain current I_D stays relatively constant for $V_{CG} < -1.5\,V$ at an average of 900 pA. It can be assumed that the restriction is due to the fact that the carrier density increases for higher channel potentials but at the same time carrier velocity decreases according to the continuity equation (cf. 2.2.2). The gate leakage current was measured for the control gate and between the remaining connection of odd and even gates (figure 7.7b). Although the leakage current across the gates seems very high, the actual impact on the drain current I_D is negligible. A high current across the gates only lowers the effective gate potential, which is not enough to ruin the functionality of the device. However, the leakage current through the control gate I_{CG} is relatively high as well, but stays low enough for $V_{CG} > -1\,V$ and unchanged when I_D rapidly increases.

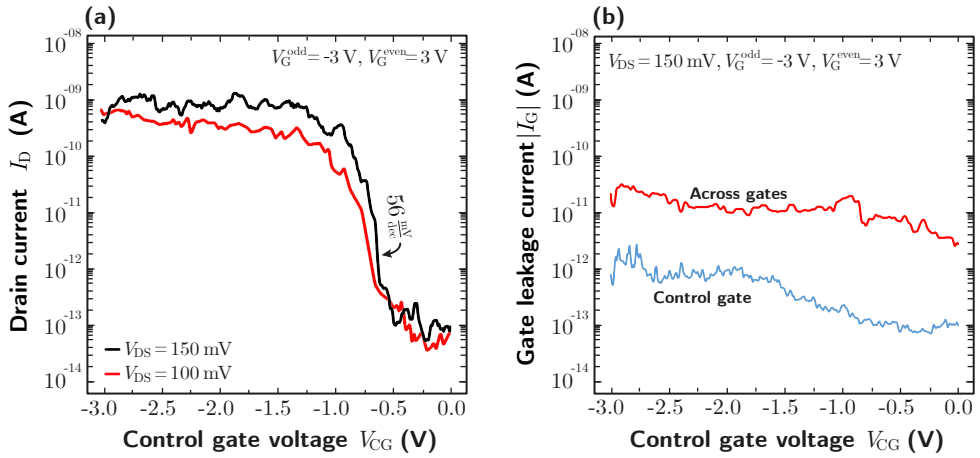

Figure 7.7: EF-CNTFET characteristics on the BMG platform: (a) Transfer characteristic for $V_{DS} = 100\,mV$ (red curve) and $V_{DS} = 150\,mV$ (black curve). Periodic potentials are set to -3 V and 3 V, respectively. (b) Gate leakage current for the control gate (blue curve) and across all even and all odd gates (red curve).

Further characterization examples are given by figure 7.8. Each of the device used in (a) and (b), respectively, had a damaged control gate contact and could only be controlled by the two remaining gate terminals V_G^{even} and V_G^{odd}. The transfer characteristics shown in (a) are recorded for $V_{DS} = 150\,mV$ (black curve), $V_{DS} = 100\,mV$ (red curve) and for $V_G^{even} = V_G^{odd}$, which means that the entire multi gate area functions as one single gate. In this example, the device does not behave like a Schottky-barrier FET, but rather like a conventional MOSFET. There are neither signs of Schottky-barrier tunneling nor ambipolarity. The on-/off-ratio even exceeds 5 orders of magnitude and the inverse subthreshold slope is at $S = 85\,^{mV}/_{dec}$. For different voltages V_G^{even} and V_G^{odd} the characteristic becomes very different as shown by (b). Having V_G^{even} set to positive 5 V has obviously no effect since there is no ambipolarity present with this device. By negatively increasing V_G^{odd} and approaching an alternating potential pattern, the drain current stays almost unchanged (green curve). This is actually the same case as for the EF-FET configuration for $V_{CG} = 0\,V$ in figure 7.7a. Only an additional control gate can switch the device. The situation changes, however, for negative V_G^{even} (yellow curve). Now, the transistor is controlled by V_G^{odd} and turns into the same state as seen in (a) but much faster, since V_G^{even} is set to constant -5 V. The maximum inverse subthreshold slope measured for this configuration was $67\,^{mV}/_{dec}$. If only one of the two gate branches is used, the transistor exhibits a negative shift for the threshold voltage but also with an overall lower drain current I_D (purple curve).

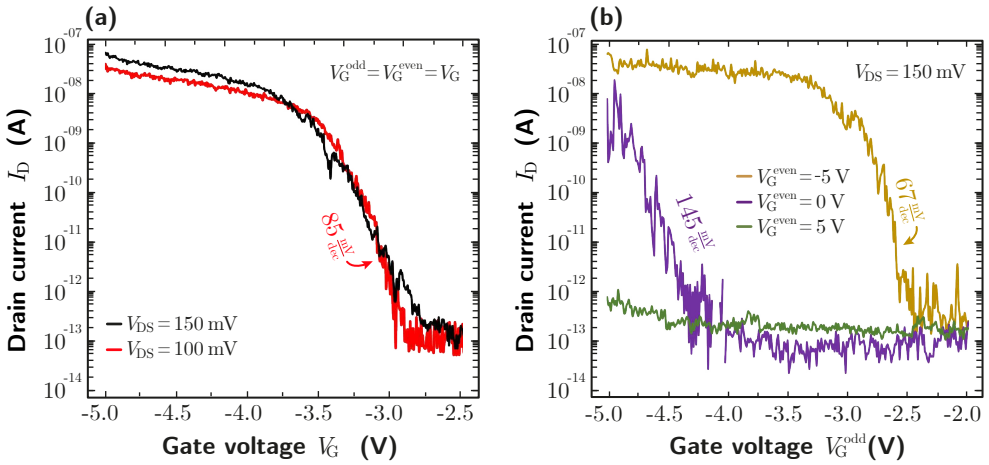

Figure 7.8: Transfer characteristics of two CNTFETs on the BMG platform: (a) All gates acting as one single gate for $V_{DS} = 100\,mV$ (red curve) and $V_{DS} = 150\,mV$ (black curve). (b) All even gates are setup with a constant voltage of $V_G^{even} = -5\,V$ (yellow curve), $V_G^{even} = 0\,V$ (purple curve) and $V_G^{even} = 5\,V$ (green curve). No control gate was used. Note that some measurements origin from different runs with different integration times, which reflects in relatively noisy signals here.

Chapter VIII

Conclusions

8.1 Summary

In the present thesis, steep slope transistors (SSTs) have been discussed as a low-power alternative for conventional MOSFET devices. The thesis focused on two prominent examples of SSTs; the band-pass filtering Tunnel-FET and the superlattice FET. Such devices do not rely on injecting carriers from the high-energetic Boltzmann-tail of the Fermi distribution. Therefore, they are not bound to the thermionic limit for the inverse subthreshold slope of $60\,^{\mathrm{mV}}/_{\mathrm{dec}}$. This allows the transition from the off-state to the on-state to be much faster, which in turn allows to reduce the supply voltage accordingly.

For the manufacturing of Tunnel-FETs, graphene-based substrates have been designed and fabricated to accommodate 1D or 2D materials. Since a Tunnel-FET needs three individually adjustable gate potentials (electrostatic doping), the architecture is called buried triple gate (BTG) platform. It is a vertical stacked design featuring graphene/metal electrodes to implement the electrostatic doping profile needed to setup Tunnel-FET devices. The fabrication of the BTG platform has been carried out in the cleanroom facilities of the Chair of Micro- and Nanoelectronics at TU Dortmund University. The platform has been produced on wafer-scale level with several optical lithography steps, PVD and CVD techniques, reactive ion etching and wet etching structuring procedures. From bottom to top, the final design consists of a Si/SiO_2-substrate with embedded metal side gates (or graphene as an alternative) buried by an intermediate dielectric. On top of that comes the graphene main gate layer which is then buried by the final top dielectric. All electrodes are equipped with metal pads to provide contact areas for electrical measurement needles. The layout of the structured electrode layers has been simulated with Comsol Multiphysics to calculate the margin of possible overlaps and to investigate the steepness of the potential distribution along the electrode landscape. Moreover, several analytical methods have been used to assess the substrates. Surface roughness could be minimized to an almost planar surface due to AFM measurements. The graphene layers were investigated regarding their quality and integrity as electrode by Raman measurements. Despite the “rough” wet-transfer of the graphene, the results showed that the thin films were still intact and capable of potential biasing. Although the platform is designed for any 1D or 2D material, carbon nanotubes (CNTs) have been chosen as channel material since they exhibit excellent properties. Due to their unique structure, an almost ballistic carrier transport is observed at long distances. Because of the vigorous covalent carbon bonding in the sp^2 configuration, carbon nanotubes are able to transport vast electric currents. The subsequent fabrication of the CNT-Tunnel-FET has been carried out with electron beam lithography since

the CNTs had been randomly distributed onto the BTG surface requiring individual contact terminals for source and drain. Static electrical measurements of the fabricated devices demonstrated the field-effect transistor characteristic with an inverse subthreshold slope down to 94 $^{\mathrm{mV}}/_{\mathrm{dec}}$ and a current on-/off-ratio of ∼5 orders of magnitude. Increasing the temperature up to 150 °C during measurements triggered a decrease in performance, however, less pronounced than for conventional MOSFET devices. Furthermore, the inverse subthreshold slope stayed constant at those high temperatures, a strong indicator that the device does in fact behave like a Tunnel-FET.

The mentioned superlattice FET or simply energy filtering FET (EF-FET) has been fabricated on a different architecture, called the buried multi gate (BMG) platform. In contrast to the BTGs, the BMGs were designed and fabricated in cooperation with RWTH Aachen University. The BMG substrates provide 17 mutually insulated and individually addressable gates in close distance (7 nm). This more elaborated gate electrode landscape is required for the implementation of an alternating potential sequence which generates a so-called superlattice in the channel, hence the term superlattice FET. This enables quantum tunneling between the periodic potential barriers which eventually causes a miniband to appear acting as band-pass filter for the high-energetic Boltzmann-tail. Before the channel material could be deposited, i.e. the CNTs, alignment marks and contact windows had to be fabricated on the BMG surface, which was carried electron beam lithography and wet-chemical etching. Finally, source and drain contacts were added to the deposited CNTs the same way as for the Tunnel-FET devices on the BTG substrates. The electrical characterization of the devices showed very steep subthreshold slopes down to 56 $^{\mathrm{mV}}/_{\mathrm{dec}}$ in the EF-FET configuration which is just below the thermionic limit. Despite an expected restriction in the maximum on-current due to the involved quantum tunneling, the on-/off-ratio still read ∼4 orders of magnitude after all.

The CNTFET measurements demonstrated the working principle of the BTG and the BMG architectures for electrostatic doping of low-dimensional materials. Both platforms are universal and can be used for application and analysis of electrostatic doping of various 1D and 2D materials. Moreover, the achieved results in this work can be considered to be a successful validation of the concept for steep slope transistor devices with the potential to obtain a central role in future low-power applications.

8.2 Outlook

The design, development and execution of a comprehensive technology process in micro- and nanoelectronics consumes a lot of time and resources. Thus, the fabricated BTG platform could only be as sophisticated as the scope of this thesis allowed it to be. Consequently, there is yet plenty of room for optimizations, alternative materials, fixing flaws and establishing new processes. For instance, downscaling below the 100 nm lateral dimensions could be obtained using further mask optimization or high-resolution pattering technologies, including electron-beam lithography. In addition, the steepness of the doping gradient strongly depends on the oxide thicknesses. For simplification of the fabrication process, relatively thick (20 nm) SiO_2 layers have been used, prepared by an established PECVD process, to ensure low leakage currents from the buried gate electrodes to the source and drain terminals. The optimization of the SiO_2 deposition may allow for much thinner oxide layers. Instead of PECVD, ozone-enhanced atomic layer deposition of ultra-thin and highly insulating oxides (below 10 nm) on graphene could also be used providing even sharper potential gradients. Furthermore, the simple graphene transfer process could be replaced by a high-quality wafer-scale transfer or direct growth of graphene on oxides for complete wafer-scale fabrication. In addition, recently established techniques using computer vision to find isolated CNTs, followed by automated electrode routing, could replace time consuming manual searching and thus increase the manufacturing throughput.

To further investigate the characteristics of the fabricated devices, electrical measurements for high frequencies should be investigated as well as very low temperature setups below 10 K in order to increase the ratio of the bandgap to the thermal broadening of the Fermi distribution E_g/k_BT. Beyond extended investigation of the existing carbon nanotube devices, the application of promising 2D materials, such as tungsten diselenide (WSe_2) or molybdenum disulfide (MoS_2) should be considered to reinforce the universal character of both BTG and BMG architectures.

Appendix

9.1 Process Specifications for the new BTG Substrates

BTG UV-Lithography Masks

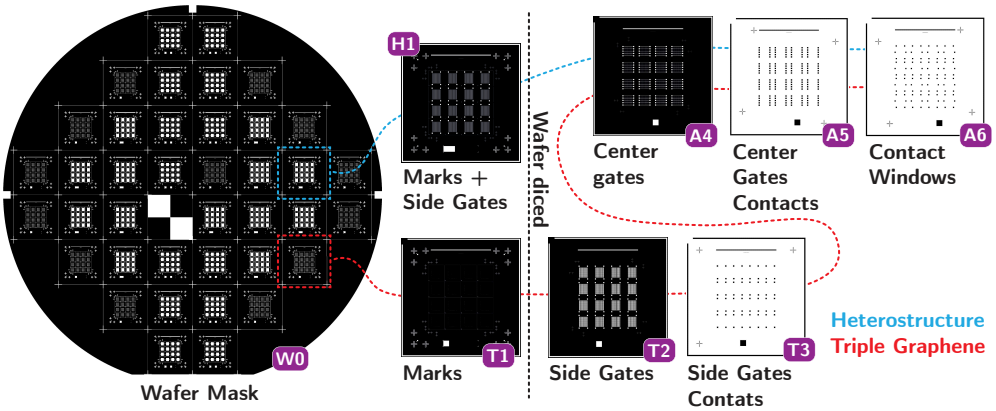

Figure 9.1: All used mask layouts for UV-Lithography. The masks are referenced in the process flow descriptions.

Heterostructure (HS) Process Flow

PR-1.1	Wafer Clean
PR-2.1	Wafer Wet-Thermal Oxidation for 250 nm SiO_2
PR-3.1	UV-Lithography, positive, Mask: W0/H1
PR-4.1	Dry-Etching (RIE) of 30 nm SiO_2
PR-5.1	PVD Sputtering for 30 nm Ti
PR-1.3	Lift-Off
PR-1.2	Soft Cleaning C
PR-6.1	PECVD for 20 nm SiO_2
PR-7.-	Wafer Dicing for 1.2 cm x 1.2 cm substrates
PR-1.2	Soft Cleaning B
PR-8.-	Graphene Wet-Transfer
PR-3.1	UV-Lithography, positive, Mask: A4
PR-4.2	Dry-Etching (RIE) of Graphene
PR-1.2	Soft Cleaning B
PR-3.2	UV-Lithography, negative, Mask: A5
PR-5.2	PVD Sputtering for 60 nm TiN
PR-1.3	Lift-Off
PR-1.2	Soft Cleaning C
PR-6.1	PECVD for 20 nm SiO_2
PR-3.2	UV-Lithography, negative, Mask: A6
PR-4.3	Wet-Etching (HF) of ~40 nm SiO_2
PR-1.2	Soft Cleaning B

Triple Graphene (TG) Process Flow

PR-1.1	Wafer Clean
PR-2.1	Wafer Wet-Thermal Oxidation for 250 nm SiO_2
PR-3.1	UV-Lithography, positive, Mask: W0/T1
PR-4.1	Dry-Etching (RIE) of 30 nm SiO_2
PR-5.1	PVD Sputtering for 30 nm Ti
PR-1.3	Lift-Off
PR-1.2	Soft Cleaning C
PR-7.-	Wafer Dicing for 1.2 cm x 1.2 cm substrates
PR-1.2	Soft Cleaning B
PR-8.-	Graphene Wet-Transfer
PR-3.1	UV-Lithography, positive, Mask: T2
PR-4.2	Dry-Etching (RIE) of Graphene
PR-1.2	Soft Cleaning B
PR-3.2	UV-Lithography, negative, Mask: T3
PR-5.2	PVD Sputtering for 60 nm TiN
PR-1.3	Lift-Off
PR-1.2	Soft Cleaning C
PR-6.1	PECVD for 20 nm SiO_2
PR-8.-	Graphene Wet-Transfer
PR-3.1	UV-Lithography, positive, Mask: A4
PR-4.2	Dry-Etching (RIE) of Graphene
PR-1.2	Soft Cleaning B
PR-3.2	UV-Lithography, negative, Mask: A5
PR-5.2	PVD Sputtering for 60 nm TiN
PR-1.3	Lift-Off
PR-1.2	Soft Cleaning C
PR-6.1	PECVD for 20 nm SiO_2
PR-3.2	UV-Lithography, negative, Mask: A6
PR-4.3	Wet-Etching (HF) of $\sim$40 nm SiO_2
PR-1.2	Soft Cleaning B

CNT Device Process Flow

PR-9.-	CNT deposition and searching
PR-3.3	E-beam Lithography for Lift-Off, Mask: Individual Contact Terminals
PR-5.3	PVD Thermal Evaporation for 60 nm Au
PR-1.4	Lift-Off
PR-1.2	Soft Cleaning C

9.2 Process Specifications for the BMG Substrates

Process Flow (starting after Al_2O_3 ALD executed by IHT/Aachen)

PR-1.2	Soft Cleaning B
PR-9.-	CNT deposition and searching
PR-3.3	E-beam Lithography for Etching, Mask: Individual Alignment Marks
PR-4.4	Wet-Etching (H_3PO_4/H_2O) of 10 nmAl_2O_3
PR-1.2	Soft Cleaning A
PR-3.3	E-beam Lithography for Etching, Mask: Individual Contact Windows
PR-4.4	Wet-Etching (H_3PO_4/H_2O) of 20 nmAl_2O_3
PR-1.2	Soft Cleaning A
PR-3.3	E-beam Lithography for Lift-Off, Mask: Individual Contact Terminals
PR-5.3	PVD Thermal Evaporation for 60 nm Au
PR-1.4	Lift-Off
PR-1.2	Soft Cleaning C

9.3 Process Recipes

PR-1 Cleaning and Lift-Off

PR-1.1 Wafer Clean

- NCW-601A[a] ultrasonic bath 50 °C
- DI-water rinse
- Piranha 10 min, 80 °C
- DI-water rinse
- Spin rinse dryer (DI-water, N_2)

PR-1.2 Soft Cleaning [X]

- Dioxolane bath (AR 600-71[b]) 5 min [A]
- Acetone bath 5 min [A/B]
- Isopropyl alcohol bath 5 min [A/B/C]
- DI-water rinse [A/B/C]
- N_2 blow-drying [A/B/C]

PR-1.3 Lift-Off for AR-P 3120[b] and AR-N 4340[b]

- Acetone bath 42 °C, stirred
- Isopropyl alcohol bath

PR-1.4 Lift-Off for AR-P 6200[b] (CSAR62)

- Dioxolane bath (AR 600-71[b]) 40 °C, stirred
- Acetone bath
- Isopropyl alcohol bath

PR-2 Thermal Oxidation of Silicon

PR-2.1 Wet-Thermal Oxidation (H_2O)

- Temperature: 1024 °C
- Rate of growth: 8.96 $^{nm}/_{min}$

PR-3 Lithography

PR-3.1 Positive UV-Lithography

- Hotplate 10 min, 100 °C
- HMDS adherence agent CVD
- Hotplate 1 min, 100 °C
- AR-P 3120[b] photoresist spin-on 4000 rpm, 60 s yielding 550 nm
- Hotplate 2 min, 100 °C
- UV exposure i-line, 19 s yielding 65 $^{mJ}/_{cm^2}$
- AR 300-35[b]/DI-water 3:2 puddle development 90 s
- DI-water rinse / N_2 blow-drying

PR-3.2 Negative UV-Lithography

- Hotplate 10 min, 100 °C
- HMDS adherence agent CVD
- Hotplate 1 min, 100 °C
- AR-N 4340[b] photoresist spin-on 4000 rpm, 60 s yielding 1.4 µm
- Hotplate 1 min, 90 °C
- UV exposure i-line, 40 s yielding 140 $^{mJ}/_{cm^2}$
- Hotplate reversal bake 2 min, 95 °C
- AR 300-35[b] puddle development 65 s
- DI-water rinse / N_2 blow-drying

PR-3.3 E-Beam Lithography

- Hotplate 10 min, 100 °C
- AR-P 6200[b] 9 % (CSAR62) spin-on 3000 rpm, 60 s yielding 240 nm
- Hotplate 1 min, 150 °C
- EBL: 15 keV, 10 µm aperture, exposure dose ($^{\mu C}/_{cm^2}$): 55 (Etching), 90 (Lift-Off)
- AR 600-546[b] puddle development 60 s
- Isopropyl alcohol rinse
- DI-water rinse / N_2 blow-drying

[a]Manufactured by Wako Pure Chemical Industries Ltd., [b]manufactured by Allresist GmbH.

PR-4 Etching

PR-4.1 Dry-Etching (RIE) of SiO_2

- Gas blend: 24 sccm Ar + 25 sccm CHF_3
- Parameters: 225 W RF with 380 V bias at 30 mTorr
- Rate of etching: 25 $^{nm}/_{min}$

PR-4.2 Dry-Etching (RIE) of Graphene

- Gas blend: 14 sccm Ar + 10 sccm O_2
- Parameters: 130 W RF with 320 V bias at 40 mTorr
- Time for complete removal: 30 s

PR-4.3 Wet-Etching (HF)

- Hydrofluoric acid bath
- DI-water rinse / N_2 blow-drying
- Rate of etching: 1.3 $^{nm}/_{s}$

PR-4.4 Wet-Etching (H_3PO_4)

- Phosphoric acid / DI-water bath (2:1), 50 °C
- DI-water rinse / N_2 blow-drying
- Rate of etching: 5.2 $^{nm}/_{min}$ (cf. figure 9.2)

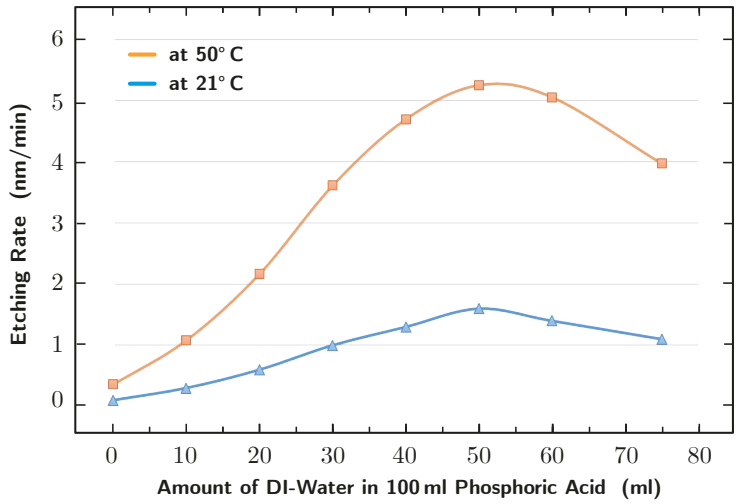

Figure 9.2: Etching rates of aluminum oxide with phosphoric acid and DI-water for different mixture ratios at 21 °C and 50 °C.

PR-5 PVD

PR-5.1 Magnetron Sputtering of Ti

- Gas blend: 20 sccm Ar
- Parameters: 2500 W with 375 V bias at 2 mTorr
- Rate of deposition: 12.6 $^{nm}/_{min}$

PR-5.2 Magnetron Sputtering of TiN

- Gas blend: 43 sccm Ar + 7 sccm N_2
- Parameters: 2000 W with 305 V bias at 4 mTorr
- Rate of deposition: 12 $^{nm}/_{min}$

PR-5.3 Thermal Evaporation of Au

- Pressure at $2.2{\cdot}10^{-5}$ mBar
- Rate of deposition: 0.2 $^{nm}/_{s}$

PR-6 PECVD

PR-6.1 PECVD for SiO_2 (default)

- Gas blend: 192 sccm SiH4 in 98 %He + 355 sccm N_2O
- Parameters: 50 W HF for 240 mm table, 1000 mTorr, 350 °C
- Rate of deposition: 40 $^{nm}/_{min}$

9.4 Extended WCD+ Simulations

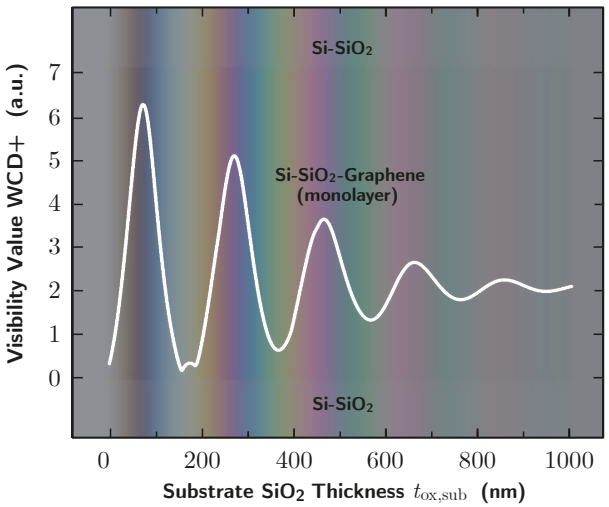

Figure 9.3: Simulation of the visibility of monolayer graphene on a Si-SiO_2-Substrate for up to 1000 nm SiO_2 thickness (cf. chapter 5.1.5). A repeating pattern emerges every 180 nm with decreasing values for the visibility index WCD+.

9.5 Miscellaneous

Images of additional CNTFET devices on BTG Substrates

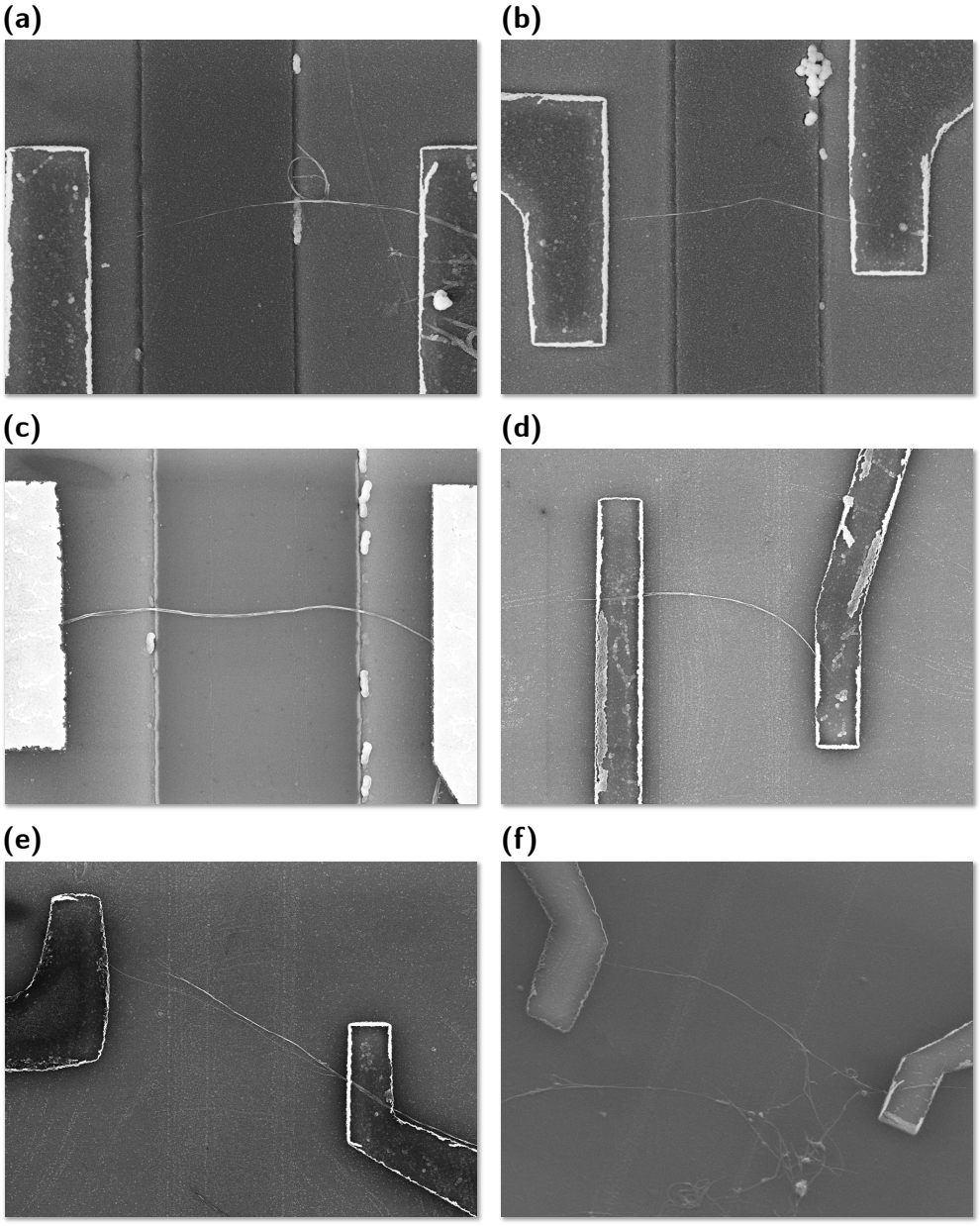

Figure 9.4: (a,b) Examples of CNTFET devices on the BTG heterostructure with titanium nitride contacts from sputtering. (c) CNTFET device on the BTG heterostructure with gold contacts from thermal evaporation. (d-f) Examples of CNTFET devices on the BTG triple graphene platform with titanium nitride contacts from sputtering.

Images of additional CNTFET devices on BMG Substrates

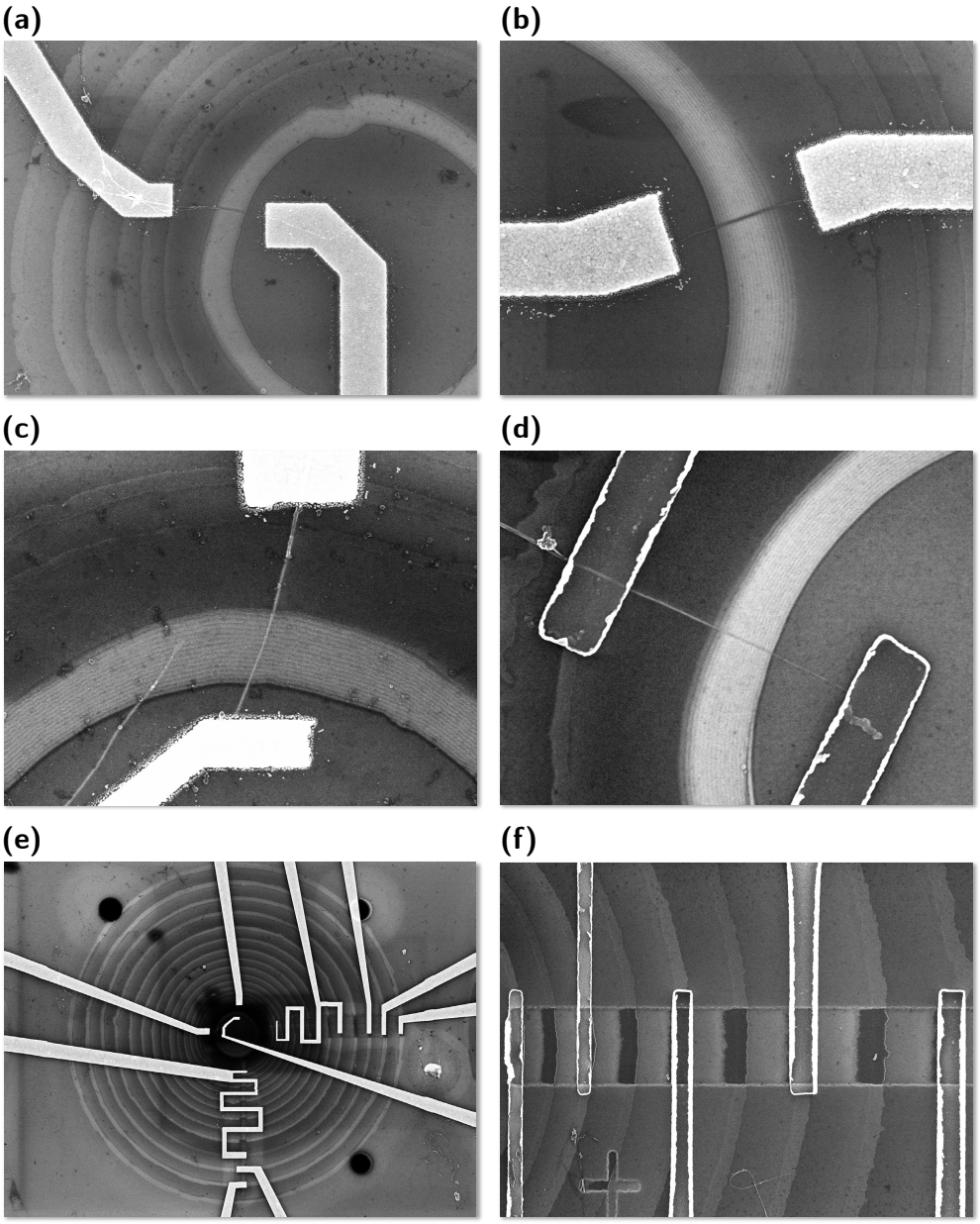

Figure 9.5: (a-c) Examples of CNTFET devices on the BMG platform with gold contacts from thermal evaporation. (d) CNTFET devices on the BMG platform with titanium nitride contacts from sputtering. (e) A full BMG cell with gold terminals connecting the partially exposed gate rings. (f) Metal fingers in contact with the exposed contact rings in alternating sequence.

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