Research

Programmable mixed-signal circuits

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Abstract

A novel concept for programmable mixed-signal circuits is presented based on programmable transmission gates. For implementation, memristively switching devices are suggested as the most promising candidates for realization of fast and small-footprint signal routing switches with small resistance and capacity. As a proof-of-concept, LT Spice simulations of digital and analogue example circuits implemented by the new concept are demonstrated. It is discussed how important design parameters can be tuned in the circuity. Compared to competing technologies such as Field Programmable Analogue Arrays or Application-Specific Integrated Circuits, the presented concept allows for development of ultra-flexible, reconfigurable, and cheap embedded mixed-signal circuits for applications where only limited space is available or high bandwidth is required.

Article highlights

- New concept for programmable analog and digital signal circuits.
- Memristive signal switches providing low ON resistance and parasitic capacity.

- Small footprint and high bandwidth reconfigurable adaptive circuits.

1 Introduction

State-of-the-art programmable logic devices (PLD) allow for customized hardware-based implementation of logic functions in integrated circuits [1, 2]. On the one hand side they are cost-effective alternatives to digital application-specific integrated circuits (ASICs) especially for prototyping or relatively low device quantities. On the other hand, their operation performance is generally superior (speed, delay times and power consumption) compared to software-based implementation of complex logic functions. PLD-concepts include programmable logic arrays (PLAs), programmable array logic (PAL), generic array logic (GAL), complex programmable logic devices (CPLDs), as well as field-programmable gate arrays (FPGAs) [3, 4]. Today, FGPAs are the dominating technology for customized hardware-based implementation of complex logic functions. FPGAs are based on programmable SRAM- (static

random access memory) or Flash-based look-up tables, in which the binary function can be programmed.

The analog counterpart of programmable logic is the field programmable analog array (FPAA) [5–8]. FPAAs are based on reconfigurable analog blocks (CAB), which are composed of operational amplifiers, filters, transistors, and/or various passive components [6, 9]. These CABs can be connected using floating-gate transistors or similar signal routing switches to enable customized analog functionality by programming an interconnection network [6]. Routing between CABs is generally flexible. The combination of mixed logic and analogue signals is motivated by their remarkable potential of energy-efficient computing compared to software-based solutions. For example, P. Hasler estimated that vector–matrix multiplication (VMM) implemented using FPAAs have the potential of being 1000 times more power-efficient than software-based implementations [10]. In the context of energy-efficient computing and VMM-based artificial neuronal data processing, combination of programmable mixed logic and analog platforms have attracted high attention. For example, Mar et al. and later Wunderlich et al. demonstrated solutions for mixed-signal processing by combination of configurable logic and analogue blocks [11, 12]. A design methodology for a high-performance analogue vector–matrix multiplier with the potential of sub-micro-watt power consumption has been demonstrated by Schlottmann et al. [13]. Recently, a mixed analogue and digital FPAA-based System-on-Chip implementation integrated with the open-source MSP 430 microcontroller has been shown by George et al. [14]. With their approach, the authors confirmed the power-efficiency projection by P. Hasler. However, FPAA approaches are generally based on a relatively small amount of CABs (typically less than 100) with only a few input nodes that, for example, limit the VMM-array size to 27×27 [6, 13, 14]. The number of CABs may thus limit the complexity of signal processing due to the reduced set of monolithically integrated functionality. While the integrated functionalities in a CAB (such as transductions amplifiers) offer optimization of each component integrated in a CAB in respect to the bandwidth, this advantage comes with significant circuitry-overhead. The CABs used by S. George et al. require a chip-area of approximately 470×470 µm^2 [14], which is almost 1.8×10^6 F^2 (with F the minimum feature size, in their study the authors used $F = 350$ nm). Since only parts of the circuitry in a CAB are used depending on the configuration, monolithically integrated CABs have considerable poor area-efficiency. This circuitry-overhead results in large signal path distances across the FPAA on average, which can counteract the previously mentioned bandwidth advantage. This becomes more important the more CABs and hence signal processing complexity are used.

The bandwidth limitation remains a major challenge for multi-CAB based reconfigurable analogue circuits [15, 16].

Another drawback of current FPAA technology is due to the use of conventional MOSFETs [17], floating gate transistors [18, 19] or CMOS transmission gates [20] for implementation of the signal switches. These devices act as ON/OFF switches for signal routing. Ideally, the ON resistance and parasitic capacity is as small as possible to increase the signal bandwidth [21]. However, transistor-based switches with small-footprint (i.e. small channel width and length), including CMOS transmission gates [20], transconductors [22] and current conveyors [23], show typically a relatively high ON resistance of some tens of kΩ [10] to hundrets of kΩ and/or require a relatively large chip area to increase the channel width [18]. For example, Z. Chen et al. report on small ON resistances of only 150 Ω [15]. But this is achieved using considerably large transistor channel widths of 80 – 100 µm (technology node 65 nm). Another common method to lower the ON resistance is to program multiple switches in parallel [20], which also requires a significant chip area overhead.

As an alternative for FPAA-based vector–matrix multiplication and analogue signal processing, memristors and memristive switches [24–26] attracted high attention in the last decade. Memristive switches have been suggested for energy-efficient computing [27], neuromorphics [28], in-memory computing [29, 30], and artificial neuronal data processing [31–33]. Memristive switches are two-terminal devices with a small footprint of $4F^2$ [34–37] and allow to encode at least two different logic levels by a high resistive OFF state and a low resistive ON state (HRS and LRS, respectively). They are usually based on the valance change mechanism (VCM) [38] or electrochemical metallization (ECM) effect [39]. These devices have been successfully scaled down to sub 10 nm dimensions [40], offer high switching speeds down to some nanoseconds and below [41, 42], and have been fabricated using established and industry-relevant CMOS- or back-end-of-line processes (BEOL) [43–46]. Very recently, Li et al. suggested a novel memristive FPAA for analog computing [47], which was experimentally implemented with 2 µm feature size technology. Here, the memristive switches were integrated in CABs in addition to active and passive components. Moreover, thanks to the large resistance window between the OFF state (100 MΩ) and ON state (tunable between 500 Ω and 20 kΩ) the authors also suggested to use memristive devices for signal routing. However, the CABs and the interconnection network both of conventional or memristor-based FPAAs still require a significant area overhead of 60% to 90% of the integrated circuit [19, 48, 49].

Here, a new routing and circuitry layout, so-called programmable mixed-signal circuits (PMSCs), for field programmable digital and analogue circuits and combination

thereof are suggested. A PMSC is an array of very simple configurable unit cells (CUC), that are only made of three programmable signal routing gates and a *p*- or *n*-type MOS transistor (*p*MOS/*n*MOS). An advantage of using memristive devices for signal routing is that the ON resistance is typically independent on the device size. Thus, a very small footprint can be achieved when programmable signal routing is provided by memristive devices. This routing and circuitry layout is completely different to conventional FPAA approaches, that are based on monolithically integrated CABs, which are connected by floating-gate switches.

The most important features of the proposed new concept for programmable mixed-signal circuits are:

- High signal bandwidth by using memristive switches with low ON resistance and small parasitic capacity,
- Small foot-print circuit design due to small circuit overhead,
- And cost-effective solution for design of integrated analogue circuits.

This study demonstrates the basic applicability of PMSCs using LT Spice simulations of selected digital and analogue circuits based on an industry-relevant 130 nm technology node. In the next section, the methods are described (that is, the simulation setup and model). The actual concept of PMSCs is introduced in Sect. 3. In Sect. 4, digital and analogue example applications are presented and discussed in detail. A short conclusion is given in Sect. 5.
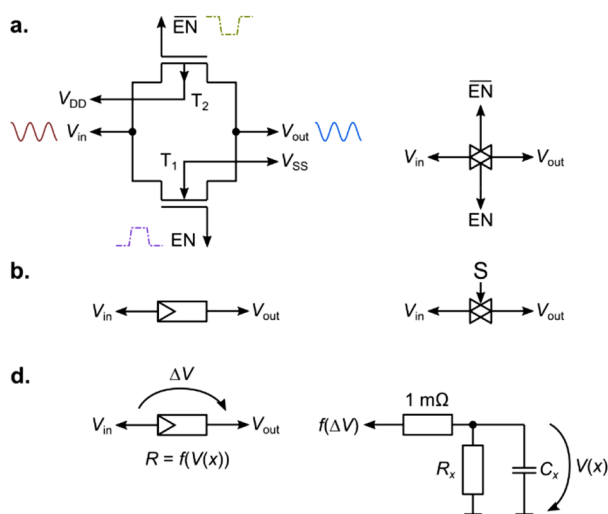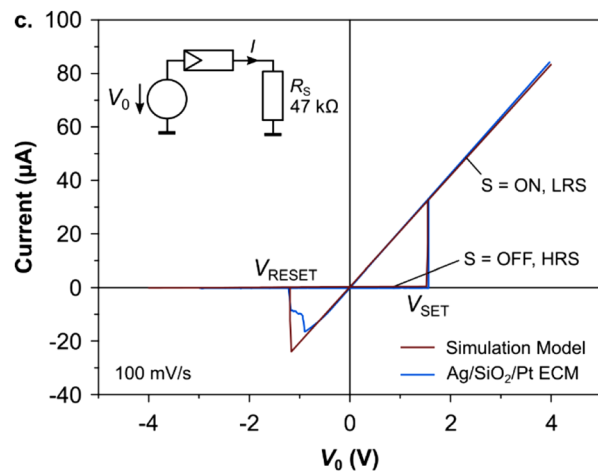
2 Methods

LT Spice XVII (x64) v. 17.0.36.0 has been used for circuit simulation, which is common and widely used for circuit simulation including simulation of the dynamic behavior of memristive devices [50–52]. All transistors are based on the Berkeley Predictive Technology Model (*n*MOS and *p*MOS level 54, 130 nm node V1.0) [53]. Examples of the simulated DC- and AC- performance of the transistors compared to experimental data reported in literature are given in Fig. S1 and S2 in the supplementary material. Wire resistances and parasitic stray capacities based on 130 nm technology nodes have been included in the modelling [54]. A detailed discussion on the parasitic capacity and resistance, which is taken into account in the LT Spice model, is given in section S2 in the supplementary material. If not otherwise specified, the transient simulation method (normal solver) has been used.

Instead of transistor-based signal routing such as CMOS transmission gates (Fig. 1a), the interconnection is based on memristive devices (Fig. 1b). The memristive device will be essentially used as a transistor-less transmission gate with programmable state variable S. S can be ON or OFF, thus allowing or suppressing signal propagation. An experimental current/voltage characteristic of a Ag/SiO$_2$/Pt based ECM crossbar-cell in series to a 47 kΩ resistor and a sweep-rate of 100 mV/s is shown in Fig. 1c (blue curve) [55]. Details on the fabrication process of the crossbar-cell are given in Refs. [55–57]. The OFF state resistance is ≫ 10 MΩ and the

Fig. 1 Signal routing by using memristive switches. **a** Circuit of a CMOS transmission gate (left) and corresponding circuit symbol (right). With the EN (=enable) signal, the transmission gate can be switched ON or OFF. **b** Conventional circuit symbol of a memristive device (left) and circuit symbol of a memristive device used as transmission gate with programmable state S (right). **c** Current/voltage characteristics of a Ag/SiO$_2$/Pt ECM cell in series to R_S (blue curve) and the empirical ECM model (red curve). The experimental data has been redrawn with permission from Ref. [55]. **d** Simplified schematic of the empirical ECM model

ON state resistance is $\approx 1\ \text{k}\Omega$. Due to multilevel switching capability of SiO_2-based ECM cells [58–60], the ON resistance can be typically tuned between $100\ \Omega$ to $1\ \text{M}\Omega$ and is almost independent of the device size [61–64]. These resistance values and the switching voltages are comparable to the performance reported for a number of VCM- and ECM-type devices [46, 65–67] fabricated by CMOS- and/or BEOL-compatible 27 nm to 90 nm technology nodes.

For circuit simulation an empirical ECM model was made based on the experimental switching performance, which consists of a capacitor and a dynamic resistor in parallel (Fig. 1d). A capacity of $C = \varepsilon_0\varepsilon_r A/d \approx 10^{-17}\ \text{F}$ (where ε_0 is the vacuum permittivity) for the memristive switch given for SiO_2 (relative permittivity $\varepsilon_r = 3.9$), a scaled-down electrode diameter of $A = 0.13\ \mu\text{m} \times 0.13\ \mu\text{m}$ and a SiO_2 thickness of $d = 30\ \text{nm}$ are chosen. Note, the effective footprint of the BEOL-integrated memristive switch can be smaller than the pitch of the metal 6 level. The resistance window is given by $R = 1\ \text{k}\Omega$ in the LRS (state $S = \text{ON} \mathrel{\hat{=}} 1$) and a parasitic $R = 10\ \text{M}\Omega$ (state $S = \text{OFF} \mathrel{\hat{=}} 0$) in the HRS, respectively. Due to the BEOL-integration, the stray capacity of the memristive switch to the CMOS-circuit level is in the order of $10^{-20}\ \text{F}$ to $10^{-18}\ \text{F}$ depending on the metal 1–metal 6 wiring. Thus, it is expected that the parasitic capacity of a signal routing switch is mainly dominated by the geometric capacity of memristive switch. The dynamic resistance hysteresis is calculated by the voltage drop $V(x)$ across a capacitor C_x, which is used to model the internal state variable. When the voltage across the in- and out-terminal of the memristive device is above the quasi-static SET voltage, C_x is charged up to $V(x) = 1$, which eventually switches the memristive device to the ON state. When the voltage across both terminals is below the quasi-static RESET voltage, C_x is discharged to $V(x) = 0$ and the memristive device switches back to the OFF state. A dynamic time constant can be tuned by adjusting R_x, and C_x. The quasi-static SET (1.55 V) and RESET (-20 mV) voltage as well as the circuit element values were chosen so that the electrical characteristics of the simulation model (red curve

in Fig. 1c) fits to the experimental results (blue curve in Fig. 1c). Note, the voltage at which a RESET is observed ($\approx -1.6\ \text{V}$) both experimentally and based on the simulation is larger than the intrinsic RESET voltage 20 mV of the ECM cell due to the voltage drop across R_S. This model has been optimized to reduce the required simulation computing power. The initial state (i.e. ON or OFF) of the switching device can be selected by the LT Spice param S. Note, this dynamic model can only be simulated using the transient simulation mode. For simulation of the small signal bandwidth and phase the dynamic resistance of the model is replaced by a static resistance with identical ON and OFF resistance values compared to the dynamic model.

3 Implementation

A PMSC is made of at least a single array of configurable unit cells. There are three types of CUCs: nMOS- (Fig. 2a) and pMOS- (Fig. 2b) CUCs, and cross-CUCs (Fig. 2c). Signal propagation within and across CUCs is provided by three transmission gates S1, S2 and S3 implemented by memristive devices. The channel lengths L_n and L_p, and channel widths W_n and W_p of nMOs- and pMOS-transistors are identical, respectively, i.e. here $L_n = L_p = 130\ \text{nm}$, and $W_n = W_p = 130\ \text{nm}$ for simplification. Note, these are the smallest dimensions possible for the given technology node (130 nm). Thus, for a practical implementation, transistors with larger L_n, L_p, and W_n and W_p may be designed to reduce the impact of device-to-device variations. This is of particular importance for analogue circuits. Alternatively, $L_n = L_p = W_n = W_p = 130\ \text{nm}$ may be used when the PMSC is fabricated by utilizing a smaller technology node such as 90 nm. L_1, L_2 are horizontal and R_{11}, R_{21}, R_{12} and R_{22} are vertical bidirectional ports of an individual unit cell. To evaluate the PMSC performance on chip-level, the parasitic resistance and capacity of the wiring within a unit cell have been also taken into account (with a sheet resistance of $70\ \text{m}\Omega/\square$ and line capacity of 230 fF/mm [54]). It is important to note that – from an application-level
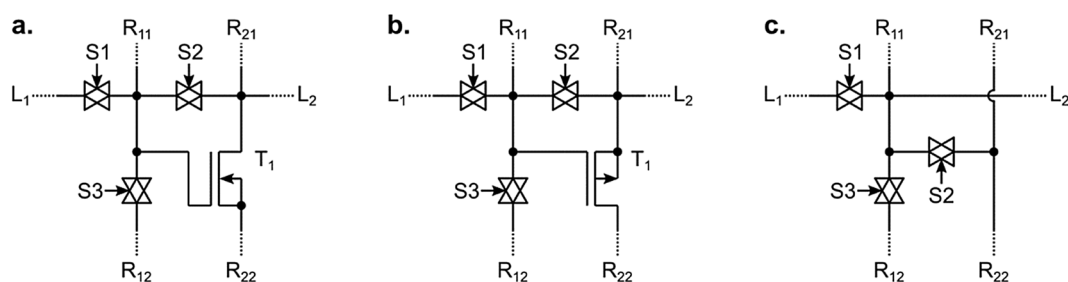

Fig. 2 Circuitry of configurable unit cells for **a** nMOS- and **b** pMOS-transistors, and **c** a cross-junction. The dotted-lines indicate the connections to neighboring CUCs

perspective – not only the properties of the PMSC but also of the external components (such as the printed circuit board or discrete elements) will determine the overall performance. For example, the line capacity of the wiring of the printed circuit board may be significantly larger than 230 fF/mm. However, this will be also true if a conventional ASIC would be used. Therefore, we only focus on the chip-level performance in this work.

Figure 3 depicts a PMSC made of a CUC array. For simplicity and readability, the PMSCs is rather small and made of an array of (7×4) CUCs. Here, $L_{11} \ldots L_{42}$ and $R_{11} \ldots R_{142}$ are horizontal and vertical bidirectional in- and output-ports, respectively. For practical applications, larger arrays may be designed to allow for implementation of complex circuits. It is also possible to interconnect multiple CUC arrays by memristor-based transmission gates to allow for higher circuit complexity. In this proof-of-concept study the array size is kept as small as possible to make the basic working principle of PMSCs clearer. In a practical PMSC the programming circuit for the memristive elements will require additional space on the chip. The memristive switches S_1–S_3 may be arranged in a matrix above the top-most metal layer. For the 130 nm node the top-most metal 6 layer pitch is 1204 nm. Thus, there will be significant space on the CMOS-level available for area-efficient implementation of the programming circuitry. The programming circuit may be based on concepts reported in literature [68, 69]. Note, the programming circuit is not shown in this study for simplification.

Any PMSC may be composed of two or more rows of pMOS-CUCs and nMOS-CUCs, respectively. Since a CUC does not internally allow isolated vertical and horizontal

signal transmission, additional cross-junction CUCs are separating the array into a left and right plane, respectively. The combination of pMOS- and nMOS-CUCs allows for implementation of circuits with a combination of pMOS and nMOS transistors, such as differential amplifiers or CMOS-like logic circuits. In principle, input and output signals as well as the positive and negative supply voltages V_{DD} and V_{SS} and references voltages may be connected to any port L_x or R_x.

Instead of using memristively switching devices as programmable transmission gates conventional CMOS transmissions gates, which are programmable by connecting the enable-terminals to either SRAM-cells or embedded floating-gate-transistors, could also be used. In this case, the proposed PMSC platform can be fully fabricated using state-of-the-art CMOS technology. However, the circuity overhead and bandwidth limitations would be significant drawbacks, which are comparable to conventional FPAAs. For example, a single SRAM-cell is made of four to eight transistors. In addition, a nMOS and a pMOS transistor are used for implementation of the transmission gate (Fig. 1a). Assuming an effective area consumption of at least $6F^2$ for each transistor results in a total area consumption of at least $36F^2$ to $60F^2$ per SRAM-controlled transmission gate (without decoder and read-out periphery). Compared to SRAM-based implementations, floating-gate-transistor programmable transmission gates may require less chip area. The area consumption of a floating gate transistor is $6F^2$. In addition to the two transmission gate transistors an inverter circuit is needed to generate the EN and $\overline{\text{EN}}$ signal, which requires an additional area consumption of at least $12F^2$ (this is the minimum area consumption of the
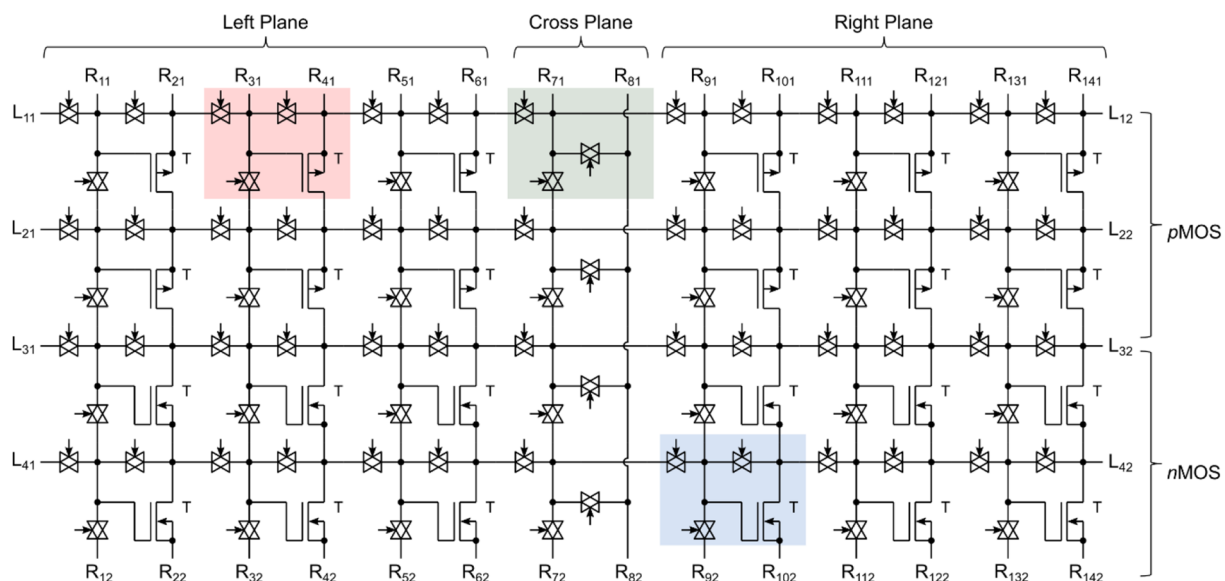

Fig. 3 Example of a PMSC composed of a (7×4)-CUC array, here with 2x (3×2) pMOS- and 2x (3×2) nMOS-transistors and (1×4) cross-junctions. A pMOS-, nMOS- and cross-junction CUC are exemplarily highlighted in light red, blue and green, respectively

nMOS and pMOS transistors of a CMOS NOT gate). In total, the floating-gate-transistor implementation requires an area consumption of minimum $18F^2$. For comparison, the minimum area consumption of a memristive device without the programming interface is only $4F^2$. In case of BEOL-integrated memristive devices there is another important advantage compared to transistor-based switches: due to the BEOL-integration the distance between the memristive devices and the substrate is increased. One or more of the buried metal layers may be designed to effectively shield the top-most memristive devices from the CMOS circuity, which decreases the parasitic capacities. However, it should be noted that the pitch between the memristive devices will be given by the top-most metal pitch [54] in case of BEOL-integration [46, 70, 71], which may be larger than the size of the memristive devices.

A smaller footprint for CUCs could be achieved by directly replacing the nMOS and pMOS transistors of the transmission gate by two programmable floating-gate nMOS and pMOS transistors in parallel [72, 73] or memristively programmable transistors [74]. However, as previously discussed, a drawback of transistor based transmission gates in general is the relatively high transistor ON-state resistance (typ. some tens of kΩ for < 0.35 μm technology nodes) [20]. This can be compensated by using relatively large transistor channel widths, which however result in a larger area consumption, larger parasitic capacity and thus a lower bandwidth.

Note, the memristive devices are only switched during programming but not during operation of the PMSC. This is ensured by limiting the voltage amplitudes $V_\sim$ during PMSC operation well below the effective SET and RESET voltages. Due to the voltage drop across memristive elements in the ON state which are connected in series, the absolute value of the effective RESET voltage is larger than the intrinsic RESET voltage of the memristive device. In this case, the maximum absolute signal and supply voltages for low frequencies ($f \to 0$) may not exceed 1 V for practical applications. At higher frequencies, the absolute SET and RESET voltage shift to higher voltages due to the non-linear switching kinetics of memristive devices [75]. This may allow for higher signal and supply voltage amplitudes for $f > 100$ Hz.

Another important design aspect is a large ON/OFF resistance ratio of the memristive devices and a linear current/voltage behavior within the voltage amplitude $V_\sim$. For practical applications, the resistance ratio may be at least 10^3. These conditions are not fulfilled by all memristive devices. For example, the device in [46] was BEOL fabricated using a 28 nm node and has relatively high SET and RESET voltages of ±2 V. However, the ON/OFF resistance ratio is only 10^2. In general, ECM cells usually have larger ON/OFF ratios than VCM-type devices [79]. But this advantage comes with typically smaller absolute SET and RESET voltages of ECM cells compared to VCM-devices. A disadvantage of some VCM-type devices is that their current/voltage behavior is considerably non-linear in the ON state. On contrast, the design requirements are exemplarily fulfilled for the ECM cell shown in Fig. 1c, the nanoscale Cu-TaO$_x$ memristor reported by Chin et al. [65] as well as the Ta/HfO$_x$/Pd memristor reported by Li et al. [47]. Table 1 gives an overview of some selected ECM- and VCM-type devices and their applicability for PMSCs.

4 Example applications

In the following section, three example applications implemented in PMSC are shown. For readability, the active signal lines are highlighted in red. Passive signal lines and connections that essentially do not contribute to the circuit operation are drawn in black by dotted lines. The examples are kept relatively simple to make the basic working principle clearer. However, larger PMSCs or connection of multiple PMSC arrays may also allow for more complex circuities. It may be possible to split larger PMSCs arrays in several small to medium sized CUC arrays, to provide circuits with higher signal bandwidth. Multiple PMSC arrays may then be interconnected using memristor-based

Table 1 Comparison of some selected ECM- and VCM-type devices and evaluation of their applicability for PMSCs

Device	Technology/size	Applicability	Refs.
HfO$_2$	65 nm	(−) Low SET voltage	[45]
HfO$_2$	50 nm pillars	(−) Low SET voltage	[76]
HfO$_2$	90 nm	(?)SET voltage not specified	[44]
Cu-based devices	27 nm	(+) High SET voltage, high ON/OFF ratio	[77]
TaO$_x$	5 nm × 40 nm	(+) High SET voltage, high ON/OFF ratio	[65]
TaON	28 nm	(+) High SET voltage, high ON/OFF ratio	[66]
Al$_2$O$_3$	90 nm	(+) High SET voltage, high ON/OFF ratio	[78]
HfO$_x$	2 μm	(+) High SET voltage, high ON/OFF ratio	[47]
SiO$_2$	3 μm	(+) High SET voltage, high ON/OFF ratio	This study

transmission gates similar to those which are used within a CUC.

4.1 NOT gate

Figure 4a depicts the conventional implementation of a CMOS NOT gate with a single input V_{in} and output V_{out}. The CMOS NOT gate is made of pMOS and nMOS transistors, T_1 and T_2, in series, which reduce the static power to a minimum. Since the electron mobility is about 3 times larger than the hole mobility, circuit symmetry is achieved by using a channel width W_p of the pMOS that is 3 times larger than the channel width W_n of the nMOS. The PMSC implementation of the NOT gate is shown in Fig. 4b. The memristor-based transmission gates are programmed and provide the red highlighted signal path. This is achieved by programming all red-colored transmission gates to the ON state (active). All other transmission gates are programmed to the OFF state.

In conventional circuitry design the channel length and width can be chosen within the specifications of the technology node for balancing the CMOS NOT gate. However, this is not directly possible for PMSCs, where all transistors have a fixed channel length and width (i.e. here for each pMOS and nMOS transistor $L = W = 130$ nm). An alternative for design of an effective channel length or width is a series or parallel connection of multiple CUCs. In Fig. 4b, the topmost CUC line contains three pMOS transistors that are connected in parallel. This ensures that the effective combined channel width of the pMOS transistors $T_{1,1}$–$T_{1,3}$

is three times larger than the channel width of the nMOS transistor T_2.

All other transistors that are not highlighted in red are effectively floating, and the leakage current is almost insignificant, i.e. the leakage current is at least three orders of magnitude smaller than the current of active paths. Cross-junctions are not required for a NOT gate. Thus, the NOT gate could be implemented by only using the left plane in Fig. 3. The simulated transfer characteristic (output vs. input volage, V_{out} vs. V_{in}) of the PMSC NOT gate for different signal frequencies $f = 10$ kHz to 100 MHz is shown in Fig. 4c. The transfer characteristic for $f \rightarrow$ DC (not shown) does not differ from the characteristic for $f = 10$ kHz. Here for the simulation, the supply voltages are $V_{DD} = 0.5$ V and $V_{SS} = 0$ V, respectively. The curves for $f < 10$ MHz are almost identical. For high frequencies ($f > 10$ MHz), the transfer curve shifts towards lower V_{in}, which lowers the noise margin of the logic 0 level. This may be compensated by intentionally making the effective combined W_p even larger than $3 \times W_n$ by routing additional pMOS transistors in parallel to the upmost pMOS transistors. When a lower noise margin of the logic 0 level is tolerable, switching frequencies above 10 MHz can be used. Figure 4d exemplarily shows the transfer characteristic of a 2-stage PMSC NOT gate for a logic pulse length of 10 ns. The 2-stage PMSC NOT gate is implemented by a series connection of two PMSC NOT gates, that are connected by a programmable transmission gate. Note, it is assumed that the interconnect between the two PMSC NOT gates is at least three times larger compared to the parasitic wiring resistance within a CUC. Thus, for simplification an interconnect
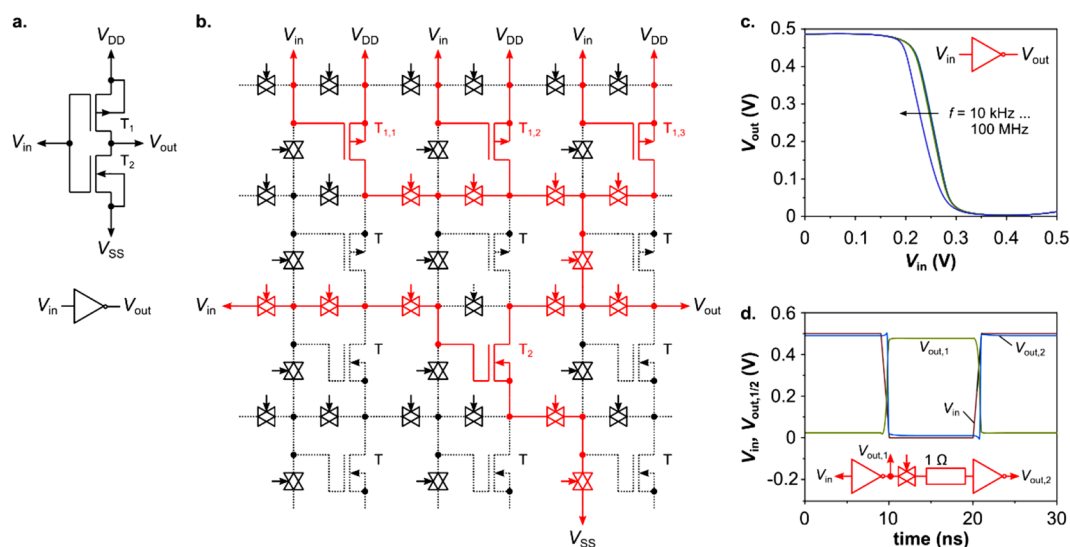

Fig. 4 Conventional (**a**) and (**b**) PMSC implementation of a NOT gate. (**c**) Corresponding input/output characteristic V_{out}/V_{in} of the PMSC NOT gate. (**d**) Transient input and output voltages a 2-stage PMSC NOT gate (i.e. series connection of two NOT gates) with a input signal rise/fall time of 0.9 ns and a pulse length of 10 ns

resistance of 1 Ω is assumed. Evidently, the output of the second NOT gate $V_{out,2}$ is almost identical to the input signal V_{in}.

4.2 Current mirror

Current mirrors are important circuits blocks for a variety of applications such as providing bias currents for active loads or differential amplifiers (Sect. 4.3). A simple conventional current mirror is shown in Fig. 5a. Here, I_1 is externally supplied. Ideally, $I_2 = I_1$ and I_2 is insignificant of the load resistor R_L. In practice, this is only fulfilled

in a certain impedance range of R_2 due to the limited output resistance of T_2, which is caused by the channel length modulation effect. A PMSC implementation of a current mirror is depicted in Fig. 5b. The active signal path and active memristor based transmission gates are highlighted in red. Similar to the NOT gate (Sect. 4.1) a cross plane is not required for implementation of a current mirror. For simplicity, R_L is considered to be an external circuit element. The current characteristic I_2 vs. I_1 of the PMSC implemented current mirror is shown in Fig. 5c. For the simulation, the supply voltages were
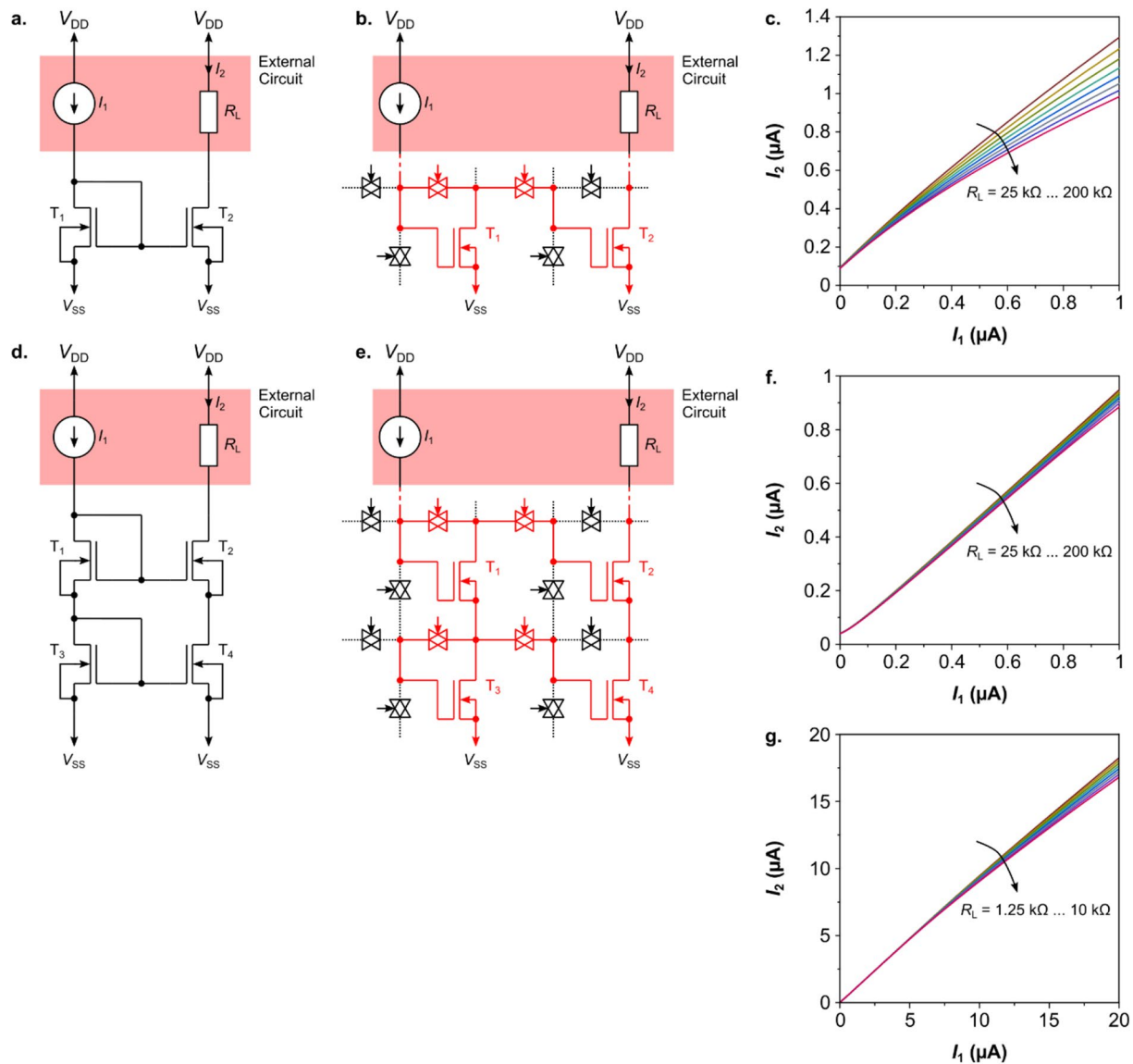

Fig. 5 Implementation of a current mirror. **a** Conventional current-mirror, **b** PMSC implemented current mirror, and **c** I_2 vs. I_1 characteristic of the current-mirror from **b** for different load resistance R_L. **d** Optimized cascode current-mirror. **e** PMSC implementation and corresponding I_2 vs. I_1 characteristic of the cascode current-mirror. I_2 vs. I_1 characteristic of the cascode current-mirror from **e** for **f** $0 \leq I_1 \leq 1$ μA, and **g** $0 \leq I_1 \leq 20$ μA, respectively

set to $V_{DD} = 0.5$ V and $V_{SS} = 0$ V. The load R_L was changed between 25 and 200 kΩ.

Due to the limited OFF resistance of the transmission gates, a current of $I_2 \approx 100$ nA is driven even when $I_1 = 0$, because there will be a small gate-source-voltage drop for T_2. For $I_1 > 400$ nA, I_2 differs significantly from I_1 and is affected by the load resistance R_L. This is not only due to the resistance of the transmission gates but also

Fig. 6 Schematic of a simple differential amplifier with a single output voltage V_{out}. The individual sub-circuits are highlighted in light red ((1), current-mirror), blue ((2), differential amplifier), and orange ((3), current source), respectively

due to the limited output resistance of T_2. This can be significantly improved by using a cascode current-mirror as shown in Fig. 5d, e. Figure 5f, g show the corresponding I_2 vs. I_1 characteristic of the cascode current-mirror from Fig. 5e for $0 \leq I_1 \leq 1$ μA, and $0 \leq I_1 \leq 20$ μA, respectively. In Fig. 5f, the current offset $I_2 \approx 45$ nA for $I_1 = 0$ for the PMSC implementation of the cascode current-mirror (Fig. 5e) is about 50 % smaller compared to the simple current-mirror (Fig. 5b). The impact of the load resistance R_L on I_2 is also much smaller compared to the higher output resistance of the cascode stage formed by T_2 and T_4. Figure 5g shows the I_2 vs. I_1 characteristic for larger currents using the same PMSC implementation as shown in Fig. 5e. In this case the load resistance R_L needs to be smaller compared to Fig. 5f to ensure that $I_2 \cdot R_L < V_{DD}$.

4.3 Differential amplifier

Compared to a CMOS NOT gate and a current mirror, a differential amplifier is a more complex circuit. Figure 6 depicts a simplified differential amplifier. $T_1 - T_2$ make a current-mirror based on *p*MOS transistors. The actual differential stage with input voltages $V_{in,1}$ and $V_{in,2}$ is implemented by T_3 and T_4. T_5 is used as current source, which may be controlled by an external or on-chip generated reference voltage V_{ref}.

A PMSC implementation of the differential amplifier depicted in Fig. 6 is shown in Fig. 7. In contrast to the PMSC NOT gate and current mirror, a cross plane is now required, which crosses the gate-source-voltage node for
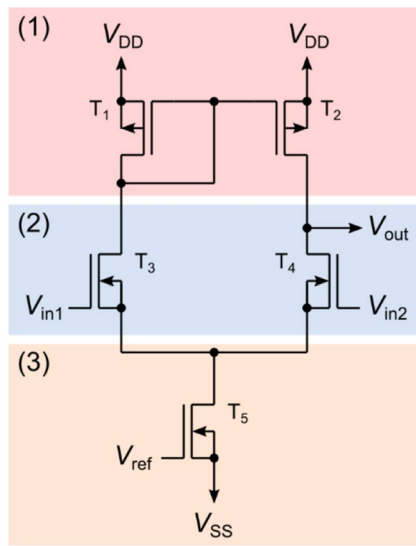

Fig. 7 PMSC implementation of a differential amplifier as shown in Fig. 6 by using a (7×4) CUC array. The individual sub-circuits are highlighted in light red ((1), current mirror), blue ((2), differential amplifier), and ora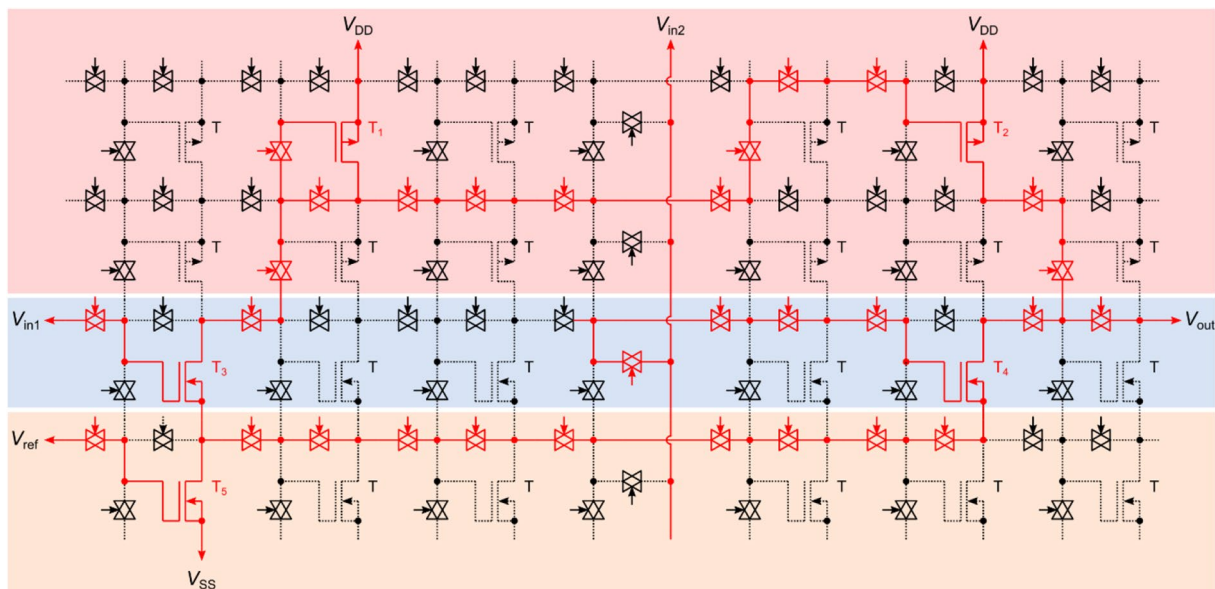nge ((3), current source), respectively. The actual signal routing is shown by red straight lines. Dotted lines indicate lines which do not contribute to signal propagation

both active pMOS transistors of the current mirror. The cross plane also provides the signal $V_{in,2}$ for the differential stage. $V_{in,2}$ is connected to a vertical port R_{81}. Note, the horizontal and vertical ports are bidirectional and can be used for any arbitrary signal, including supply voltages as well as logic or analog input and output signals.

In Fig. 8a the input/output ($V_{in,1}$ vs. V_{out}) voltage characteristic of a differential amplifier implemented by PMSC is shown for different frequencies $f = 10$ kHz … 100 MHz, with $V_{in,2} = 0$. Note, the input/output voltage characteristic for $f \rightarrow$ DC (not shown) does not differ from the curve for $f = 10$ kHz. For high frequencies (i.e. $f > 10$ MHz), the offset voltage is increased from < 1 mV (for $f = 10$ kHz … 1 MHz) to 20 mV for $f = 100$ MHz. The reference voltage V_{ref} was chosen by try-and-error and for $V_{ref} = 0.395$ V the lowest offset voltage was found. Note, in practice, these ideal references voltages may not be provided. Figure 8b depicts the impact of a ± 10 % tolerance of V_{ref} on the offset voltage and open circuit gain. In this case, we found a maximum absolute offset voltage of 14 mV and a gain of 5.1–5.3 V/V for $V_{ref} = 0.395$ V ± 10 % (i.e. 0.3555 V $\leq V_{ref} \leq 0.4345$ V).

4.4 4-Stage Operational Amplifier

An operational amplifier (OPA) is typically composed of a differential stage, an output stage and additional feedback and reference stages. An ideal OPA has an infinite high input impedance, a zero output impedance and an infinitive high open circuit voltage gain $A \rightarrow \infty$. Non-ideal monolithic commercial operation amplifiers usually have high open circuit voltage gains of some $10–10^4$ V/mV or even higher. As an example, the LM 741 has a gain of up to $A = 200$ V/mV. The open circuit voltage gain of the differential stage in shown in Fig. 7 is only $A = 5.1$ V/V. In general,

for non-ideal OPAs, the open circuit voltage gain needs to be considered when designed an analog circuit. A straightforward method to take the non-ideal gain into account is based on a linear equivalent circuit of the amplifier, which is discussed in section S3 in the supplementary material. The total gain G for the non-ideal inverting amplifier is (see Eq. S1–S6):

$$G = \frac{V_{out}}{V_{in}} = -\frac{A}{1 + \frac{R_1}{R_2}(1 + A)} = -\frac{R_2}{R_1}\frac{1}{1 + \frac{1}{A}\left(1 + \frac{R_2}{R_1}\right)} \quad (1)$$

In similar manner as described in section S3 in the supplementary material, the total gain for a non-ideal non-inverting amplifier is (see Eq. S8):

$$G = \frac{V_{out}}{V_{in}} = \frac{1 + \frac{R_2}{R_1}}{1 + \frac{1 + \frac{R_2}{R_1}}{A}} \quad (2)$$

As an example, for an inverting amplifier using only the differential stage (Fig. 7) with $A = 5.1$ V/V, $R_1 = 100$ kΩ and $R_2 = 100$ kΩ the total gain is $G \approx -0.72$, which is an error of 28 % compared to an inverting amplifier using an ideal OPA. Another problem of the differential stage is that it can only drive small output currents without affecting the differential gain.

As an improvement, the differential stage can be included in a 4-stage operational amplifier fully implemented in PMSC technology as shown in Fig. 9. Here, this prototypical amplifier demonstrates that much higher open gain amplifications can be achieved by combination of multiple stages. The actual implementation (LT Spice circuitry) can be found in the Supplementary Data. Note, for simplicity each stage is implemented in a separate PMSC
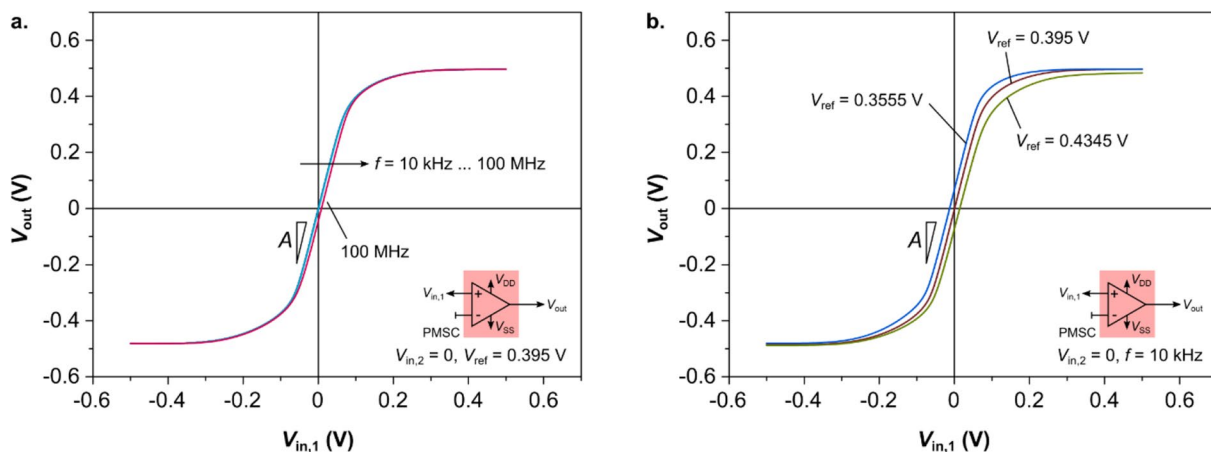
Fig. 8 **a** Input/output ($V_{in,1}$ vs. V_{out}) voltage characteristic of the differential amplifier for different frequencies f. The open circuit voltage gain of the differential stage is $A = 5.1$ V/V. The inset depicts the circuity. **b** Impact of a ± 10 % tolerance of V_{ref} on the offset voltage and open circuit gain
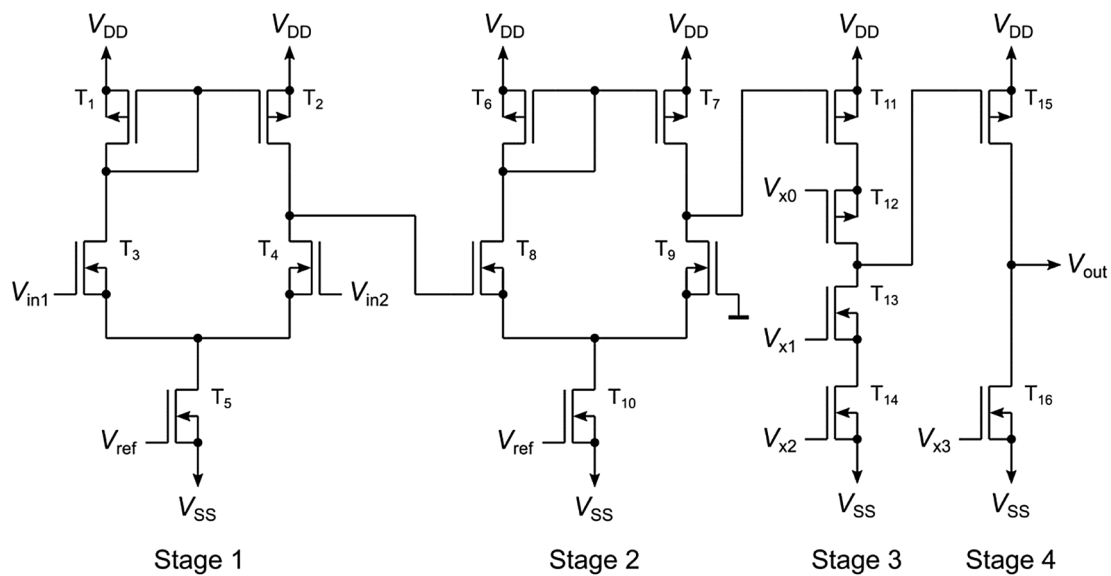
Fig. 9 Circuitry of the proposed 4-stage operational amplifier

block, which are combined by programmable transmission gates and a series resistance of 1 Ω, respectively. The first stage of the operational amplifier is identical to the differential amplifier as shown in Fig. 7. The output voltage of this stage is fed into a second cascode current-mirror differential amplifier (second stage). Stage 1 and 2 are acting as a 2-stage direct coupled differential amplifier, which is similar to circuit layouts reported in Refs. [80–82]. Here, this circuit layout has been chosen for simplicity because the LT Spice layout for stage 1 and 2 are almost identical. The third stage is used to decouple the output stage (fourth stage) from the differential stages. The output stage is a pMOS amplifier with nMOS current source as load. It acts as an inverter. Thus, the purpose of the third stage is also to ensure pin-compatibility of the 4-stage operational amplifier to the single differential amplifier (Fig. 7). It is also important that the fourth stage can provide a relatively large output current and maximum output voltage swing, that is, the output voltage range driven rail to rail (V_{DD} vs. V_{SS}). This is achieved by designing the effective pMOS channel width $W_p = x \cdot W_n$ (where W_n is the channel width of the nMOS transistor) using parallel connection of $x = 6$ pMOS-based CUCs. When $x < 6$ the output swing towards V_{DD} is decreased. For $x \gg 6$ the bandwidth is decreased due to the increase of the effective input impedance of the pMOS transistors. Thus, $x = 6$ is a fair tradeoff between output voltage swing, bandwidth and circuit complexity (i.e. number of CUCs used for implementation).

The input/output characteristic of the 4-stage operational amplifier is shown in Fig. 10 for different small and large signal input signal frequencies f_s and f. From the small signal input/output characteristic (using a
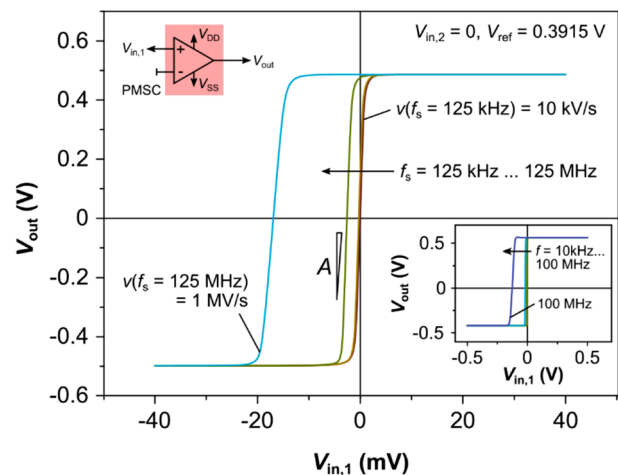

Fig. 10 Small signal (input peak-to-peak voltage $V_{in,1\text{-p-p}}' = 80$ mV) input/output ($V_{in,1}$ vs. V_{out}) voltage of the 4-stage operational amplifier. The inset shows the large signal (input peak-to-peak voltage $V_{in,1\text{-p-p}} = 1$ V) input/output voltage. The small signal input signal frequencies f_s have been chosen so that the sweep rates v for each curve are identical to the large signal sweep rates, respectively

peak-to-peak input voltage of $V_{in,1\text{-p-p}}' = 80$ mV) a differential gain of up to $A = 517$ V/V (for $f_s = 125$ kHz) is found, which is two orders of magnitude larger than of a single differential stage (Fig. 8). However, the steeper differential gain comes with a significant drift of the input/output characteristic for higher frequencies as can be seen in the inset (large signal response with $V_{in,1\text{-p-p}} = 1$ V).

The differential gain and the offset voltage for low frequencies can only be seen in the small signal input/output characteristic, which is essentially a zoom into the large

signal input/output characteristic. To be able to compare the dynamic small and large signal behavior of the 4-stage OPA one has to ensure that the sweep rates v for each large signal and corresponding small signal input voltage are identical. The sweep rate is calculated by:

$$v = f \times V_{in,1-p-p}\big|_{\text{large signal}} \equiv f_s \times V'_{in,1-p-p}\big|_{\text{small signal}} \quad (3)$$

For example, the sweep rate for the large signal frequency of $f = 10$ kHz is $v = 10$ kHz $\times$ 1V $= 10$ kV/s. Consequently, the small signal frequency $f_s = 125$ kHz needs to be 12.5-times larger than f to ensure a sweep rate of $v = 10$ kV/s in both cases. The offset voltage of the 4-stage OPA can be adjusted by the reference voltages. V_{ref}, V_{x0}, V_{x1}, V_{x2}, and V_{x3}, are reference voltages for the differential amplifier (stage 1 and 2) and the stage 3 and 4 drive transistors, respectively. All reference voltages were chosen by try-and-error to yield the best performance of the operational amplifier. In practice, these ideal references voltages may not be provided, and the impact of the reference voltage tolerance has been discussed above (see also Fig. 8b). With $V_{ref} = 0.3915$ V, $V_{x0} = -0.5$ V, $V_{x1} = 0$, $V_{x2} = -0.09$ V, and $V_{x3} = -0.05$ V the absolute offset voltage is < 2.75 mV for low frequencies ($f_s \leq 12.5$ MHz, which corresponds to $f \leq 1$ MHz), which is increased up to 17 mV for $f_s = 125$ MHz ($f = 10$ MHz) and 120 mV for $f = 100$ MHz. The gain is decreased from $A = 517$ V/V for $f = 10$ kHz to $A = 25$ V/V for $f = 100$ MHz. At $f = 1$ MHz the gain $A = 495$ V/V is still reasonably high. With a gain of $A = 495$ V/V, $R_1 = 100$

kΩ and $R_2 = 100$ kΩ the total gain of a 4-stage OPA based inverting amplifier is $G \approx -0.996$. This is an error of only 0.4 % in respect to the gain of an ideal amplifier, and it is much smaller compared to the error of 28 % of the differential stage alone.

The dynamic behavior of the 4-stage OPA used for implementation of an inverting amplifier with different total gains is shown in Fig. 11. The inverting amplifier circuity is depicted in Fig. 12a. By changing R_2 the gain is set between $G = -1$ ($R_2 = 100$ kΩ), $G = -2$ ($R_2 = 200$ kΩ), $G = -5$ ($R_2 = 500$ kΩ) and $G = -10$ ($R_2 = 1$ MΩ), respectively. $R_1 = 100$ kΩ is kept constant. Figure 12b and c depict the normalized gain and phase of the amplifier circuit. Note, the simulated phase of $\approx 180°$ agrees to that of an ideal inverting amplifier. The bandwidth can be defined by the 3 dB cut-off frequency, which is 4.9 GHz for $G = -1$, 4.5 GHz for $G = -2$, 3.8 GHz for $G = -5$ and 3.3 GHz for $G = -10$, respectively. For comparison, the 3 dB cut-off frequency is reduced to 2.17 GHz for $G = -1$ and assuming a ten times higher parasitic capacity of the memristive switch ($C = 10 \cdot 10^{-17}$ F $= 10^{-16}$ F). It should be noted that the amplifier could become instable due to a significant change of the phase at these frequencies. A relatively constant phase of $180° \pm 3.5°$ for all total gains from $G = -1$ to -10 is ensured up to a frequency of 1.4 GHz.

The input/output voltage characteristic of an inverting amplifier with total gain $G = -0.5, -1, -2, -5$ and -10 is depicted in Fig. 12a. Depending on the gain, the amplifier output voltage is driven into saturation at a certain
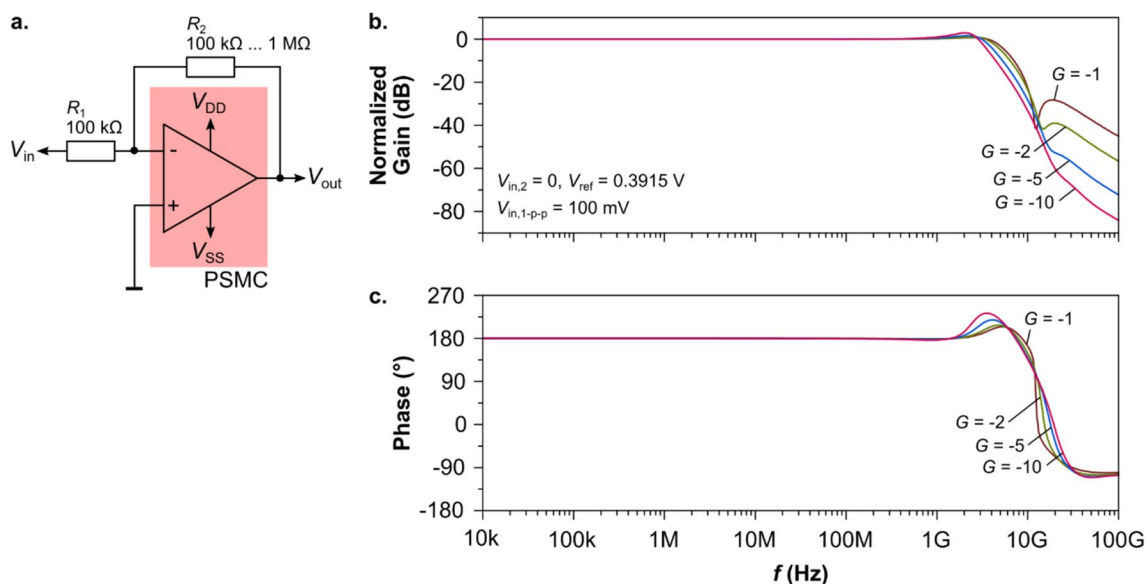

Fig. 11 Small signal bandwidth of a PMSC-based inverting amplifier. **a** Corresponding circuitry. R_1 and R_2 are external components. **b** Normalized gain and **c** corresponding phase of the PMSC-based inverting amplifier. The small signal input voltage amplitude was set to 50 mV, which corresponds to a peak-to-peak voltage of

$V_{in,1-p-p} = 100$ mV. Note, these characteristics are valid for the conditions shown in **a** inside an integrated circuit, i.e. without any external load and without taking ESD precautions and bonding into account

input voltage. The output saturation voltage is limited by the amplifier rail voltages ($V_{DD} = 0.5$ V and $V_{SS} = -0.5$ V). Exemplarily for $G = -10$ the simulated positive saturation output voltage is $V_+ = 0.484$ V, which is quite close to V_{DD}. However, the simulated negative saturation output voltage is between $V_- = -0.474$ V and $V_- = -0.48$ V, and is slightly affected by the input voltage. This is due to an asymmetry of the 4-stage amplifier, which may be improved by additional compensation stages, parallelization of the nMOS output stage transistor(s), and/or tuning of the internal reference voltages. For a smaller gain such as $G = -1$ the saturation asymmetry is even more visible and the negative saturation voltage is only -0.4 V.

In contrast to an inverting or non-inverting amplifier, where the output voltage is fed back into the negative input terminal, a Schmitt trigger has a positive feedback loop (Fig. 12b). The input/output voltage characteristic is that of a differential amplifier with voltage hysteresis. The switching voltages V_{ON}, V_{OFF} to turn the output on ($V_{out} \rightarrow V_+$) or off ($V_{out} \rightarrow V_-$) can be tuned by R_1 and R_2:

$$V_{ON} = -\frac{R_1}{R_2} V_+ \tag{4}$$

$$V_{OFF} = -\frac{R_1}{R_2} V_- \tag{5}$$

Note, V_+ and V_- are the positive and negative output saturation voltages. The hysteresis window is:

$$\Delta V = V_{ON} - V_{OFF} \tag{6}$$

Exemplarily, for $R_1 = 200$ kΩ and $R_2 = 400$ kΩ $\Delta V = 0.46$V is found in Fig. 12b. For an ideal operational amplifier, one would expect $\Delta V = 0.5$V. The difference between the PMSC-based OPA and the ideal OPA is that the PMSC-based OPA cannot drive the output voltages fully to the rails, so that here $V_+ < V_{DD}$, $|V_-| < |V_{SS}|$ and $V_+ \neq |V_-|$. However, the deviation from the ideal case can be compensated by choosing slightly larger resistances for R_2.

Fig. 12 a Circuitry and input/output voltage characteristic of a PMSC-based inverting amplifier with different total gains $G = -0.5$ to -10, respectively. **b** Circuitry and input/output voltage characteristic of a PMSC-based non-inverting Schmitt trigger with different hysteresis windows. The input voltage signal rise time is $t_r = 10$ μs and the reference voltage is $V_{ref} = 0.3915$ V in **a** and **b**, respectively
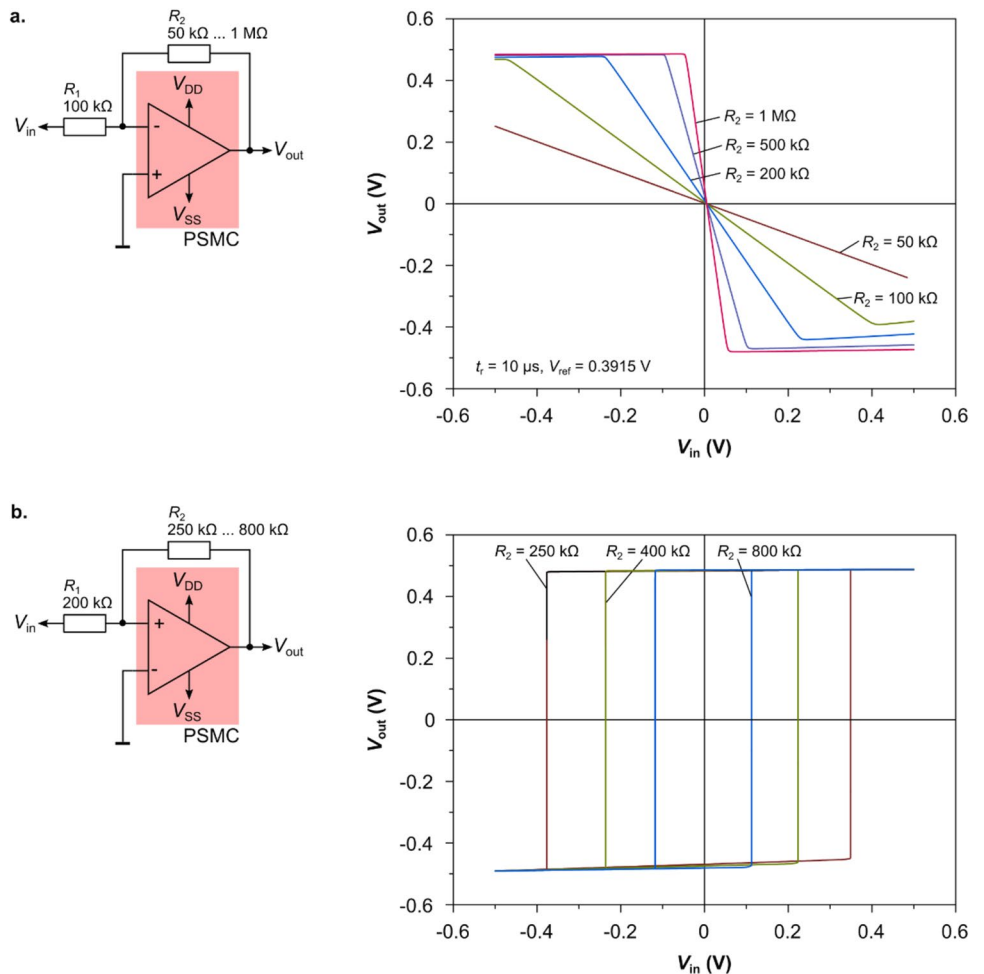
5 Conclusions

In this study a new concept for a programmable mixed-signal circuit based on a hybrid structure of conventional CMOS components (*n*MOS and *p*MOS) and programmable transmission gates is demonstrated. It is discussed that memristive switches are promising candidates for implementation of programmable transmission gates. However, as an alternative, programmable transmission gates may be also realized by SRAM-controlled CMOS transmission gates, or floating gate or memristively programmable transistor based transmission gates. The study further shows LT Spice simulations of several digital and analogue example circuits that can be implemented by PMSC, namely a logic inverter gate, current mirrors, differential amplifier, and a 4-stage operational amplifier. It is discussed how to tune design parameters such as effective channel width in PMSCs by routing multiple transistors in parallel and/or series. This concept may allow for development of novel cheap, high bandwidth and small-footprint embedded reconfigurable mixed-signal circuits such as filters or amplifiers.

Author contributions ST had the idea, performed the simulation and data analysis and wrote the manuscript.

Data availability The datasets generated during and/or analyzed during the current study are available in the TU Dortmund University repository, http://dx.doi.org/10.17877/DE290R-23222.

Declarations

Conflict of interest The authors declare no competing interests.

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