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Characterization and Modeling of the Threshold Voltage Instability in p-Gate GaN HEMTs

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Abstract

The p-gate GaN HEMT is a modern power semiconductor transistor capable of overcoming the switching speed limitation of conventional Silicon-based technologies. However, the GaN HEMT is a fairly new technology that still suffers undesired effects that affect its operation. Nowadays, the most prominent effects are the shift and instability of the threshold voltage V_{th}, caused by capacitive coupling into the gate stack as well as trapping, accumulation, and depletion of carriers.

In this study, an experimental characterization of the V_{th} behavior is executed and subsequently used to develop a physically-based compact model. For this purpose, a custom setup is developed capable of high-resolution transient measurements for pulse lengths ranging from 100 ns up to 100 s. Utilizing the setup, commercially available state-of-the-art p-gate GaN HEMTs are investigated, showing a V_{th} shift and instability that appears relevant up to the nominal operation.

The experimental results show that the drain-source voltage V_{DS} yields a V_{th} shift, which, when applied for long durations (e.g., during off-state), leads to an additional V_{th} instability. The gate-source voltage V_{GS} also yields significant V_{th} instabilities, which correlate with the V_{DS}-induced effects. Furthermore, the driving conditions causing an impact on V_{th} appear to also correlate with the devices' short-circuit capability and degradation. However, no available models cover the V_{th} behavior, which is necessary to predict their impact and reliability concerns. Consequently, a compact model is developed based on the surface potential for the drain path, extended by the conduction mechanisms covering the gate path. Finally, the V_{th} shift is modeled based on capacitive coupling into the gate, while for the V_{th} instabilities, a possible implementation is exemplified for the impact of V_{DS}.

by Thorsten Sezgin-Oeder

Technische Universität Dortmund
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Charakterisierung und Modellbildung der Schwellenspannungs-Instabilität von p-Gate GaN HEMTs

Kurzfassung

Der p-Gate GaN-HEMT ist ein moderner Leistungshalbleitertransistor, der die Beschränkung Schaltgeschwindigkeit herkömmlicher siliziumbasierte Technologien überwinden kann. Dieser ist jedoch eine relativ neue Technologie, die noch immer unter unerwünschten Effekten leidet, welche den Betrieb beeinträchtigen. Heutzutage sind die auffälligsten Effekte die Verschiebung und Instabilität der Schwellenspannung V_{th}, die durch kapazitive Kopplung in das Gate sowie durch Trapping, Akkumulation und Verarmung von Ladungsträgern verursacht werden.

In dieser Studie wird eine experimentelle Charakterisierung des V_{th}-Verhaltens durchgeführt und anschließend zur Entwicklung eines physikalisch basierten Kompaktmodells verwendet. Zu diesem Zweck wird ein spezifischer Pulsaufbau entwickelt, der hochauflösende transiente Messungen für Pulslängen von 100 ns bis zu 100 s ermöglicht. Unter Verwendung des Aufbaus werden neusete kommerziell erhältliche p-Gate GaN-HEMTs untersucht, welche eine Verschiebung und Instabilität von V_{th} zeigen, die bis zum Nennbetrieb relevant erscheint.

Die experimentellen Ergebnisse zeigen, dass die Drain-Source-Spannung V_{DS} zu einer V_{th}-Verschiebung führt, die bei längerem Anlegen zu einer zusätzlichen V_{th}-Instabilität führt. Die Gate-Source-Spannung V_{GS} führt ebenfalls zu erheblichen V_{th}-Instabilitäten, die mit den V_{DS}-induzierten Effekten korrelieren. Außerdem scheinen die Betriebsbedingung, die sich auf V_{th} auswirken, auch mit der Kurzschlussfähigkeit und der Alterung der Bauelemente zu korrelieren. Es gibt jedoch keine verfügbaren Modelle, die das V_{th}-Verhalten abdecken, das für die Vorhersage der Auswir-kungen und der Zuverlässigkeit erforderlich ist. Daher wird ein kompaktes Modell entwickelt, das den Drain-Pfad über das Oberflächenpotenzial berücksichtigt und um die Leitmechanismen des Gate-Pfads erweitert. Schließlich wird die V_{th}-Verschiebung

als kapazitive Kopplung in das Gate modelliert, während für die V_{th}-Instabilitäten eine mögliche Implementierung bzgl. der V_{DS}-Auswirkungen gezeigt ist.

von Thorsten Sezgin-Oeder

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First of all, I want to thank my supervisor Prof. Dr.-Ing. Martin Pfost for giving me the opportunity to work as a research assistant and for guidance through the way of my doctorate. A large part of this happened because you once asked me: "How to measure holes in a GaN HEMT?". Although I never counted a single hole, I prepared about 100+ pages of information that are helpful for a better understanding of modern GaN HEMTs while pushing the boundaries of research. If you ask me today, I would answer: "Applying a nominal gate voltage results in the injection of holes which accumulate at the AlGaN barrier, causing an increase in the effective gate charge and thus a threshold voltage instability."

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Contents

Chapter 1

Introduction

A transition towards globally sustainable energy production is mandatory to preserve our home planet and contain the ongoing climate change. To achieve the energy transition goals, a change in the generation, transmission, conversion, and a reduction in energy consumption must take place. In 2020, renewable energy provided nearly 30% of the global electricity supply [1], which within Germany even reached around 40% in 2021 [2]. Although a continuous growth of renewable energy production has been recorded over the last decades, the global demand for energy consumption continued to rise simultaneously. Consequently, huge improvements must be realized regarding the efficiency of production, transmission, conversion, and electrical energy usage.

An indispensable key feature of renewable energy production is the power electronic (PE) system, which is mandatory for frequency and voltage adjustment at the transmission grid feed-in process. Typically, the PEs convert direct current (DC) into alternating current (AC), thus, they are called DC/AC converter or simply power inverter. A common application would be the output stages of e.g., photovoltaic and wind turbine converters. On the other end, withdrawing the produced energy provided by the transmission grid, a re-conversion is necessary, which is done using AC/DC converter, also known as a rectifier. Furthermore, considering the vast majority of electrical applications, a subsequent voltage adjustment is needed, which is why so-called DC/DC converters are necessary. The only conversion remaining is AC to AC, which can either be done with matrix converters or alternatively two consecutive AC/DC and DC/AC converters with an intermediate stage.

Apart from the PE-based converters that are necessary to feed in as well as to withdraw energy from the transmission grid, PEs can also be utilized to overcome physical limitations of the AC grid itself. Transmitting energy in the AC grid typically revolves around distances of not more than 300 km due to parasitic losses and increasing field emission. However, providing energy over much larger distances of 1000 km or more, a DC grid can be used as typically done to e.g., to supply the

industry located in South Germany with energy generated by off-shore parks in the North Sea [3]. Although DC grids appear to be a promising solution, implementing safety measures is much more complicated. A turn-off process in an AC grid typically revolves around an electrical arc that occurs at mechanical dislocation and only expires at the zero crossing of the alternating current. Since there is no zero crossing in a DC grid, the turn-off needs to be done in a different approach which is achieved using multilevel PE-based stages. In the end, PEs are a central feature of modern power production, transmission, and usage.

For efficient energy transmission and usage, PE-based converters and applications need to operate as low on losses as possible. The design and functionality of every PE is based on passive components such as capacitors, inductivities, and sometimes transformers, as well as passive and active semiconductor switching devices such as diodes and transistors. The losses of passive components typically scale with their size, which correlates to the switching speed and frequency of the transistors used in PE systems. Consequently, the efficiency of PEs strictly depends on the semiconductor devices' efficiency.

"*The key for the next essential step towards an energy-efficient world lies in the use of new materials, like wide-bandgap semiconductors which are allowing for greater power efficiency, smaller size, lighter weight, lower cost. together*" - Infineon [4]

Conventional semiconductor devices used in PE systems are primarily based on silicon (Si) or at least utilize Si as a substrate material. A steady trend of these devices is the increase in integration density, which ultimately raises demands on the capability to withstand higher voltages and temperatures. Nowadays, the physical limitation of Si-based devices has been reached, which is confined by the material-dependent bandgap energy of 1.1 eV. To overcome this limitation, wide-bandgap (WBG) materials started to become more relevant, whereby silicon carbide (SiC) and gallium nitride (GaN) offering bandgap energies of around 3.3 eV appear to be the most promising candidates for the development of future PE systems.

Utilizing WBG materials, conventional Si-based transistor technologies such as the metal oxide semiconductor field effect transistor (MOSFET) and insulated gate bipolar transistor (IGBT) can be build-up on SiC and directly replace their pre-

decessor to improve the systems voltage and temperature capability instantly. On the other hand, GaN appears unsuitable for building conventional devices but, in turn, offers a distinctive feature that allows for the development of a new technology, the so-called high electron mobility transistor (HEMT). The HEMT is based on the existence of a two-dimensional electron gas (2DEG) that forms in-between a aluminum gallium nitride (AlGaN)/GaN heterojunction due to spontaneous and piezoelectric polarization [5]. Compared to a MOSFET, the HEMT is not dependent on a timely enhancement and depletion of a channel region, resulting in a much faster turn-on and -off of the device. As a consequence, HEMTs allow for the development of PE systems with increased frequencies while at the same time remaining relatively low on losses. Furthermore, higher frequencies allow for size reduction of subsequent components, thus reducing the system size, which increases the overall power density. However, the usage of WBG materials allows for the development of high-power and high-frequency PEs [6].

1.1 State-of-the-art

The intrinsic 2DEG formation in a GaN-based HEMT leads to a normally-on device, which is not desirable for fail-safe PEs. To obtain a normally-off device, several gate structures have been introduced over the years [7]. Currently, a p-doped cap layer in the gate stack (p-gate) [8, 9] is the most promising solution and already commercialized [10]. In the early stages of development, the GaN HEMT suffered from a phenomenon of drain current collapse [11], which caused a temporarily increased (dynamic) $R_{\mathrm{DS,on}}$. This resulted from electrons that occupy trap states in the surface passivization [12] and the buffer [13] at high drain-source voltages V_{DS}. Besides many measures, with the introduction of the p-gate that injects holes into the 2DEG, the dynamic $R_{\mathrm{DS,on}}$ can nowadays mostly be neglected [14].

Despite these improvements, the p-gate GaN HEMT is still affected by the drain voltage [15, 16] and the gate voltage [17, 18] that was previously applied to the device, similarly to the hysteresis known from many magnetics. This undesired behavior can also be interpreted as an instability (a transient change) of the threshold voltage V_{th} and is attributed to carrier accumulation, depletion, and trapping

phenomena. In addition, the drain voltage is found to impact the gate barrier by capacitive coupling [19], which appears to be an additional static phenomenon causing a V_{th} shift. However, the shift and instability of V_{th} can be problematic considering advanced PE systems since the change in V_{th} can be large, leading to device damage under error conditions (e.g., overload or short-circuit). Investigating state-of-the-art commercial p-gate GaN HEMTs, their reliability and robustness correlate to the behavior of V_{th}. At the same time, degradation mechanisms show to be accompanied by a change in V_{th} [20, 21].

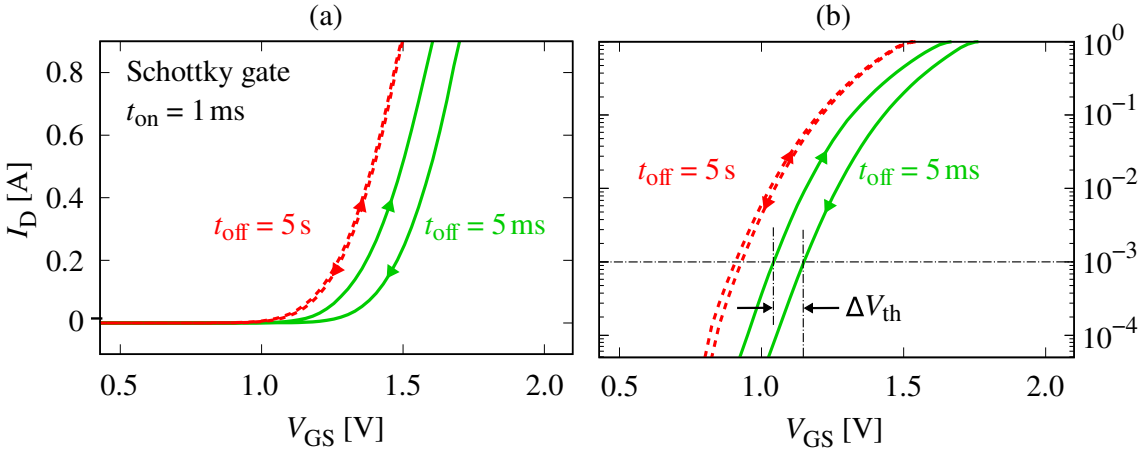

Figure 1.1: Transfer characteristics in (a) linear and (b) semi-logarithmic scale of a p-gate GaN HEMT at $V_{\mathrm{DS}} = 10\,\mathrm{V}$ acquired with a Keysight B1505 semiconductor device analyzer. Here, pulsed measurements with different off-state duration (t_{off}) are carried out in a consecutive up- and down-sweep.

A common practice to demonstrate the behavior of V_{th} is to extract a reference value and a stress-induced shift from the DC transfer characteristics. Typically, these measurements are acquired using a semiconductor device analyzer [15, 21, 22]. In Fig. 1.1(a), the transfer characteristics of a commercially available p-gate (Schottky-type) GaN HEMT are shown, measured with a Keysight B1505 device analyzer. Here, a constant drain-source voltage of $V_{\mathrm{DS}} = 10\,\mathrm{V}$ is applied while pulsing the gate-source voltage V_{GS} with constant on- and off-state duration (t_{on}, t_{off}). The gate-source voltage V_{GS} pulses are applied as a pulse train function in a double mode operation, where V_{GS} is incrementally increased and then decreased (a consecutive up- and down-sweep). The drain current I_{D} is measured and extracted

as the average value during the on-state duration. As a result, a I_D hysteresis can be observed depending on the pulse timing (t_{on} and t_{off}), which is shown to be a common phenomenon [23].

In order to extract V_{th}, it is assumed to be defined as a V_{GS} required for $I_D = 1\,mA$ at operation in saturation ($V_{DS} = 10\,V$), as depicted in Fig. 1.1(b). Here, the measurements from Fig. 1.1(a) are plotted in a semi-logarithmic scale, whereby the I_D hysteresis can be translated into a V_{th} shift. For $t_{off} = 5\,ms$ a positive V_{th} shift is observed between up- and down-sweep, whereas for $t_{off} = 5\,s$ the shift disappears almost completely. Since the V_{th} shift tends to vanish for long off-state durations, the impact on V_{th} appears to be time-dependent and ultimately decreases over time. Consequently, the impact of V_{GS} results in a V_{th} instability rather than a static shift. This is reported for p-gate (ohmic-type) GaN HEMTs [24], insulating-gate GaN HEMTs [25] and semi-vertical GaN-on-Si trench-FETs [26].

1.2 Motivation and Approach

The threshold voltage V_{th} of modern p-gate GaN HEMTs is typically investigated in the DC transfer characteristics, which can be acquired using pulsed measurements. Thereby, a shift of V_{th} can be observed that can be shown to correlate with the pulse timing (on- and off-duration), which is commonly referred to as a V_{th} instability. However, since the V_{th} instability appears to be a transient phenomenon, the investigation should be based on transient rather than DC measurements to better understand the actual behavior. Concerning this matter, the commonly used semiconductor device analyzers are too slow to measure the V_{th} instability accurately. Typically, their minimum measurement duration is about 1 ms with turn-on slopes oftentimes larger then 100 µs. For this purpose, a custom pulse setup is required to offer high-resolution measurements capable of fast-switching transients with relatively short pulse durations.

Utilizing transient measurements can help to acquire the time constants of the V_{th} instabilities and separate the impact that various driving conditions have on them. Furthermore, investigating the time domain can help distinguish effects that cause a dynamic instability or a static shift. These effects are usually ascribed to

the applied bias voltages V_{GS} and V_{DS}, which are typically investigated separately in most studies. However, the occurrence of a V_{th} shift and a V_{th} instability might not be independent or correlate with each other. Consequently, the respective impact of each bias voltage, V_{GS} and V_{DS}, on the behavior of V_{th} should be investigated separately and subsequently confirmed whether they correlate. This massively helps to understand the origin of the effects and, in the long-term, to either prevent or predict a bias-induced impact on the V_{th} behavior. The V_{th} behavior can eventually affect the reliability, which must still be sufficiently shown and understood. A better understanding of the V_{th} behavior could even be used to predict alterations of the short-circuit capability or be used for device health monitoring.

In order to predict the behavior of modern p-gate GaN HEMTs, it is mandatory to own an accurate model, which can subsequently be used for the development of PE systems. However, to the best of knowledge, there are no GaN HEMTs models that cover the V_{th} behavior, which is necessary to predict the impact of the applied bias and reliability concerns. Many of the available models are significantly different, making it considerably difficult to find an adequate extension. For this purpose, a unified physically-based compact model is developed that aims for scaleability towards different devices in various current and voltage classes. Furthermore, for an easy accessibility, a parameter extraction strategy is required that allows to create fitting device models solely from datasheet information.

1.3 Thesis organization

The thesis is structured in five main chapters covering the theoretical foundations of power semiconductor devices, the undesired effects associated with GaN HEMTs, the construction of the measurement setup, the acquired results of the experimental characterization, and finally the development of the compact model.

In Sec. 2, the limitation of Silicon as a material are discussed, which ultimately led to the need to find WBG materials such as GaN to improve modern power transistors. The technology does also implies limitations, which can partially be overcome utilizing new structures such as the HEMT, which compared to the conventional MOSFET yields an increase in switching speed.

In Sec. 3, several undesired effects are discussed that have been revealed during the development of the GaN HEMT. In the early stages, the devices were affected by a current collapse that led to a dynamic on-state resistance $R_{\mathrm{DS,on}}$, which, in turn, has mostly been resolved. Nowadays, the most prominent effects are the shift and instability of the threshold voltage V_{th}, caused by capacitive coupling and carrier trapping mechanisms in the gate stack.

In Sec. 4, the experimental setup is presented to investigate the V_{th} shift and instability through transient measurements. These undesired effects are shown to still be visible in commercially available state-of-the-art p-gate GaN HEMTs, which are the center part of the investigation. The developed setup is aimed at fast transient measurements that offer a high-resolution and accurate evaluation. Subsequently, the transient results are translated into DC characteristics that allow for determination of the V_{th} value, whose variation appears to be observable for operation up to the nominal driving conditions.

In Sec. 5, the experimental results of the investigation are presented. Here, it is shown that applying V_{DS} during the on-state results in a shift of V_{th} while the V_{DS} during the off-state results in an additional time-dependent V_{th} instability. Furthermore, the applied V_{GS} is proven to significantly impact V_{th}, which is also shown to be an instability. Finally, the bias conditions causing the V_{th} shift and instabilities are proven to correlate with the short-circuit capability and degradation of the devices.

Finally, in Sec. 6, a physically-based compact model is developed that includes the effect of the V_{th} shift and an approach to model V_{th} instabilities. The core model is developed based on surface potential, which is used to acquire the drain current. Since many undesired effects occur in the gate stack, this region is modeled as an extension by including its physical conduction mechanisms. Then, the V_{th} shift model is developed based on the capacitive coupling through the usage of the capacitance model. In the end, a possible implementation of V_{th} instabilities is showcased exemplarily for the impact of V_{DS}.

Chapter 2

Power Semiconductor Devices

Silicon (Si) is the most explored and evolved material used for the development of semiconductor devices and a foundation of modern PE-based applications. An ongoing trend of modern PEs is an efficiency and power density increase accompanied by a size reduction of the system. This, however, is strongly related to the used semiconductor devices, whereby primarily material properties determine the limitations of improvement, as discussed in Sec. 2.1. Technological aspects like the device structure and its operating functionality can also be a significant limitation factor, as outlined in Sec. 2.2.

In order to overcome these limitations, more advanced materials need to be utilized to develop modern PE applications. Nowadays, a trend is to use wide bandgap (WBG) semiconductor materials such as silicon carbide (SiC) or gallium nitride (GaN) that offer many benefits, as explained in Sec. 2.3. However, the material properties are not only beneficial because GaN offers a unique operating principle capable of overcoming conventional technologies by far, see Sec. 2.4.

2.1 Material Limitation

An increase in power density and a size reduction of the PEs increases the inherent system temperature during operation and, thus, the semiconductor devices. Furthermore, a size reduction of the device structure is critical regarding increasing demands of higher off-state voltages. The energy bandgap E_{G} of the semiconductor materials physically limits operational temperature and voltage. Although the manufacturing of Si devices is the most advanced process in all semiconductor industry, increased requirements led to hitting the physical material limitations [27, 28].

Common Si-based devices such as the MOSFET are based on unipolar carrier transport mechanisms. These unipolar devices are restricted by the correlation of the on-state resistance $R_{\mathrm{DS,on}}$ and the maximum off-state voltage V_{DS}. This relation is called silicon limit and is shown in Fig. 2.1. Here, the $R_{\mathrm{DS,on}}$ of monolithically

grown semiconductor structures decreases with the amount of implanted dopants, which simultaneously reduces the maximum applicable voltage V_{DS}. An increased amount of dopants leads to an increase in the carrier density and, consequently, a steeper electrical field slope. If the internal electrical field reaches the material-specific critical limit, impact ionization with subsequent avalanche carrier generation occurs, leading to a loss of control and possibly the destruction of the structure. However, a material-specific physical limitation is defined based on the relation of the doping concentration between $R_{\mathrm{DS,on}}$ and V_{DS}. Furthermore, the semiconductor material's critical electrical field E_{crit} is related to its energy bandgap E_{G}. Due to this, the need for materials with higher E_{G} arose, resulting in WBG compound materials such as SiC and GaN to appear as the most promising candidates [29].

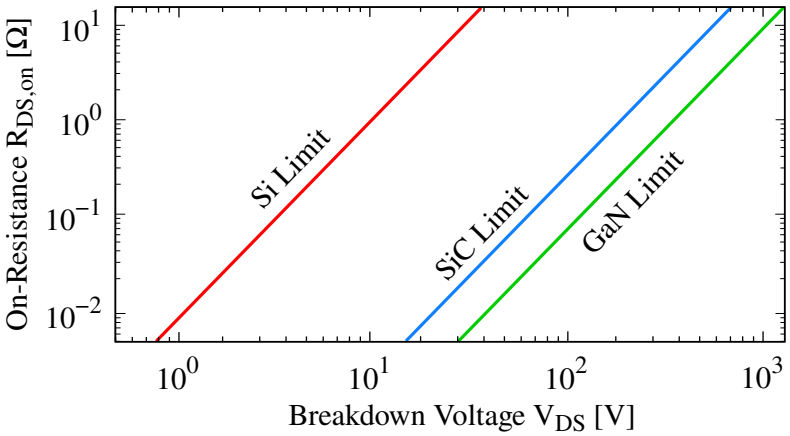

Figure 2.1: Theoretical on-state resistance $R_{\mathrm{DS,on}}$ and breakdwon voltage V_{DS} limit, comparing the materials silicon (Si), silicon carbide (SiC) and gallium nitride (GaN) [30]. Here, the lines indicate the correlation of $R_{\mathrm{DS,on}}$ and the maximum applicable V_{DS} at unipolar operation. For SiC and GaN the limitation is much higher, due to wider bandgaps and possibly higher doping concentrations.

Apart from the bandgap E_{G} and critical field E_{crit}, other material properties need to be considered when developing power semiconductor devices, as listed in Tab. 2.1. While the applicable voltage is mainly limited by E_{G} and E_{crit}, the $R_{\mathrm{DS,on}}$ is, besides the doping concentration, also affected by the electron mobility μ_0 and saturation velocity v_{sat}. Considering the development of conventional technologies such as the MOSFET, the bulk materials SiC and GaN initially seem to be unsuitable because

of their reduced electron mobility. On the other hand, due to the higher E_G of SiC, the doping concentration can be increased, which subsequently lowers $R_{DS,on}$ while simultaneously maintaining an operation below E_{crit}. Apart from that, utilizing GaN in a heterostructure, a two-dimensional electron gas (2DEG) can be formed, offering much higher mobility. Based on this, the technology of a HEMT is created, which can overcome existing limitations of conventional devices, as discussed in Sec. 2.3.

Table 2.1: Physical properties of the materials silicon (Si), silicon carbide (SiC) and gallium nitride (GaN) at room temperature and light doping [31].

Property	Symbol	Unit	Si	SiC	GaN
Bandgap energy	E_G	eV	1.17	3.26	3.47
Critical field	E_{crit}	MV/cm	0.3	3.0	3.5
Saturation velocity	v_{sat}	cm/s	$1.05 \cdot 10^7$	$2 \cdot 10^7$	$2.5 \cdot 10^7$
Electron mobility	μ_0	cm^2/Vs	1420	1000	990 (bulk)
					2000 (2DEG)

2.2 Technological Limitation

Semiconductor devices are the core element of PE applications and define the specifications of circuit development. In order to achieve higher power densities in the scope of an application, the output power and switching frequency have to be increased [29]. Here, instead of simply increasing the output power in developing new applications, the efficiency can also be increased by using modern semiconductor materials and technologies. Furthermore, developing fast-switching applications results in a drastic downsizing of passive components such as capacitances and inductivities (e.g., LC filters) and, thus, much-increased power densities.

In recent years, the physical limitations of unipolar Si-based semiconductor devices have been reached, leaving them unsuitable for developing future PE applications. In order to reach areas of operation with increased output power and switching frequencies, more advanced technologies utilizing WBG materials need to be considered. Prominent key technologies such as the SiC MOSFET [32] and

the GaN HEMT became competitive to push existing limitations of conventional Si-based devices [6, 32], as illustrated in Fig. 2.2.

The MOSFET is the most used transistor technology in analog and digital circuits and a fundamental part of modern PE systems. The functional principle is based on the accumulation and depletion of carriers in a channel region resulting from the charging and discharging of the gate-oxide capacitance. For example, applying a positive voltage yields a charge to build up in the gate capacitance, attracting carriers into the channel region and forming a conductive layer for the on-state. However, based on the sizing, the capacitance can be large, resulting in enhanced charging and discharging durations and, thus, in the turn-on and -off speed, limiting its potential switching frequency. The formation of an electron-hole plasma in the parasitic body diode can eventually reduce the switching speed, too. Furthermore, the MOSFET is a unipolar device that is restricted by the material properties (cf. Sec. 2.1). While the technological limitation of switching speed is inevitable, the output power and rated voltage can be increased by using SiC instead of Si as a bulk material for developing more advanced MOSFETs [32].

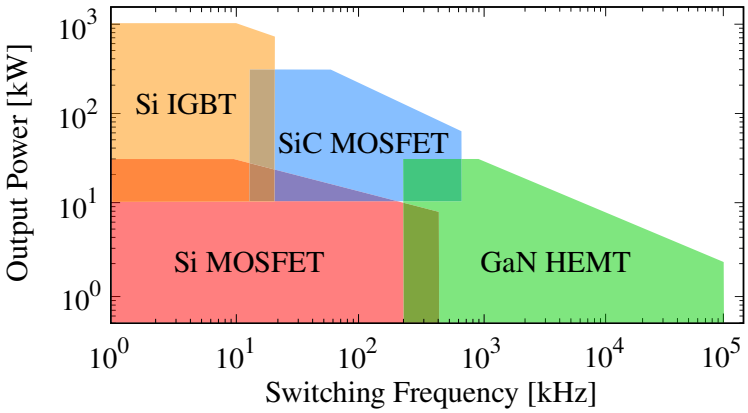

Figure 2.2: Output power over switching frequency of different semiconductor technologies, showing their area of operation in an power electronic application. [33]

The IGBT is a modification of the conventional MOSFET to overcome the silicon limit set by the unipolar carrier transport. The function principle can be described as a MOSFET controlled bipolar junction transistor. By adding a hole-emitting layer to the drift region, the generation of an electron-hole plasma occurs during the

on-state. Consequently, the doping concentration of the drift region can be small, ensuring high applicable voltages in the off-state. At the same time the plasma offers a very low resistance in the on-state. On the other hand, the IGBT suffers similar switching restrictions as the MOSFET, while the additional formation and removal of the electron-hole plasma reduces the speed even further. However, Si-based IGBTs became mainstream in the area of low-frequency, high-voltage, and high-power PE applications that remain relevant in the future [34].

Finally, the introduction of the GaN-based HEMT has significantly improved the potential switching frequency of modern PE systems. Here, the function principle is based on a lateral AlGaN/GaN heterojunction forming a 2DEG resulting in a unipolar device. However, compared to a MOSFET or IGBT, the gate capacitance is significantly lower with a factor of 1/10 to 1/100 for comparable devices, resulting in much faster switching possibilities. Nowadays, the GaN HEMT is highly desirable for next-generation high-efficient PEs [6].

2.3 Gallium Nitride

Gallium nitride (GaN) is a group III-V semiconductor wide bandgap (WBG) material that is commonly used in heterojunction structures. One of the first relevant heterojunction structure was gallium arsenid (GaAs), which is up until today used in high-frequency applications. Firstly, in 1978 the phenomena of a mobility enhancement behavior were reported for the $Al_xGa_{1-x}As$/GaAs heterojunction [35]. In the early stages, this has been described by spatially separated mobile carriers forming a pseudo-two-dimensional electron gas (2DEG) in the heterojunction interface. Later in 1999, a similar phenomenon was observed for the $Al_xGa_{1-x}N$/GaN heterojunction. The appearance of the 2DEG has been described by the mechanisms of spontaneous and piezoelectric polarization that occur in Ga-faced crystalline structures [5].

2.3.1 Crystal Structure

Many III-V semiconductor materials such as GaAs, GaN or aluminium nitride (AlN) are polar materials because they can have net polarization based on the shift of their sublattices [36]. The GaAs lattice forms a zinc-blende structure similar to the Si

diamond lattice, whereas they have two different basis atoms. While GaN can be found in zinc-blende structures, typically group III nitrides crystallize at room temperature in the thermodynamically stable wurtzite structure [37].

The crystal lattice of a wurtzite Ga-face GaN structure is illustrated in Fig. 2.3. Here, the crystal is heteroepitaxially grown in the [0001] direction, resulting in a hexagonal basal plane of gallium (Ga) atoms on top of the unit cell (Ga-face), as shown in Fig. 2.3(a). The lattice consists of two hexagonally close-packed layers of anions and cations, which are displaced by 5/8 unit cell size (c) in the [0001] direction. Here, the anions are Ga atoms, and the cations are nitrogen (N) atoms.

In between the layers, two tetrahedron cells of anions and cations can be found, see Fig. 2.3(b). Here, these cells are inverse to each other and tip into the center of the hexagonal basal planes of the respective atoms. At room temperature, the distance between two atoms in each layer is $a = 0.3189\,\text{nm}$, while the distance between two identical layers in [0001] direction is $c = 0.5185\,\text{nm}$ [38]. This arrangement results in a ratio of c/a = 1.6259, which differs from the ideal ratio of 1.633 leading to a lack of inversion symmetry of the GaN wurtzite structure [39].

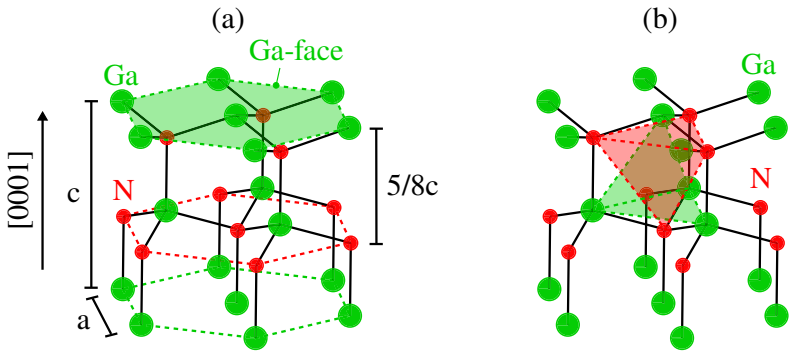

Figure 2.3: Ball-stick model of the crystal structure of wurtzite GaN, grown in [0001] direction. In (a) the formation of the hexagonal basal planes and the Ga-face are highlighted, while in (b) the two tetrahedron cells are indicated. [40]

2.3.2 Polarization

The atoms, their bonding mechanisms, and the lattice shape determine the polarization of a crystalline structure. In crystals of III-V compound materials, covalent

bonds attach each basis atom to four atoms of the other type. The spatial distribution of the bonding electrons heavily depends on their electronegativity. In group III-nitride materials, N atoms have the highest electronegativity, strongly attracting bonding electrons. This behavior leads to an ionic contribution in the covalent bond which can turn from a microscopic into a macroscopic polarization if the crystal lattice lacks inversion symmetry [36]. Since this effect occurs in the equilibrium lattice without strain, it is called spontaneous polarization. This effect exists in zinc-blende structures such as GaAs but is much more pronounced and relevant in wurtzite structures. In the crystal lattice of the wurtzite Ga-face GaN structure (cf. Fig. 2.3), the polarity points against the growth in [0001] direction. In N-face crystals, the polarity points in the growth direction.

The polarization of wurtzite structures is affected by the ionic contribution in the covalent bond but also by the non-ideality of the crystal lattice [36]. The correlation of spontaneous polarization strength P_{SP} and the lattice constant a for typical group III nitrides is shown in Fig. 2.4. Here, the polarization in AlN is up to three times higher than in GaN, which is affected by the change in the lattice constants a and c (cf. Fig. 2.3). These constants are set for binary compound materials such as AlN and GaN but can be adjusted in between by the creation of a ternary compound such as $Al_xGa_{1-x}N$ [41]. Apart from that, a change in lattice constants also results in a change in the bandgap energy.

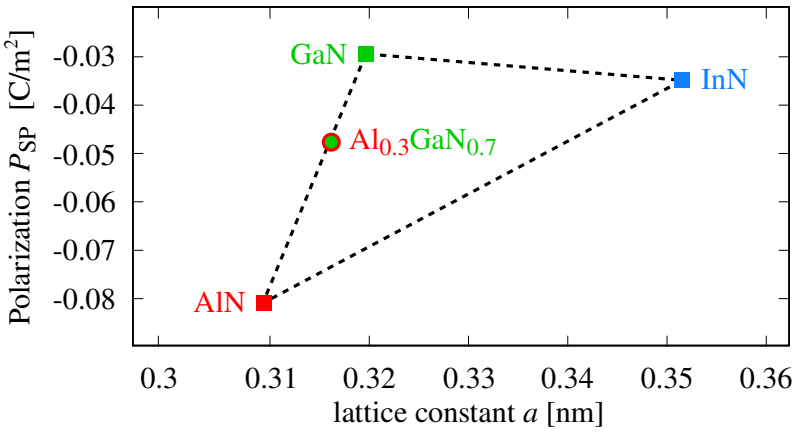

Figure 2.4: Strength of the spontaneous polarization P_{SP} versus the lattice constant a, for the most relevant group III-nitride compound materials. [41]

In an equilibrium lattice, the polarity is defined by spontaneous polarization, which can be considered the basic state. Applying strain to the crystal lattice leads to deformation and, consequently, superposed piezoelectric polarization. In Fig. 2.5(a), an example of unstrained equilibrium lattice is shown, whereby the lattice constants a_0 and c_0 refer to the initial state. Applying compression strain to the lattice leads to an increase in height and a decrease in width of the unit cell, as illustrated in Fig. 2.5(b). Then, the lattice ratio $c_{\text{comp}}/a_{\text{comp}}$ increases compared to c_0/a_0. Since the ratio of the unstrained lattice is smaller than the ideal ratio, the compression strain tends to yield the lattice towards ideality. This means that the piezoelectric polarization points against the spontaneous polarization, consequently reducing the overall polarity. Contrary, tensile strain leads to a decrease in lattice ratio and an increase of polarity, see Fig. 2.5(c). However, the combination of spontaneous and piezoelectric polarization in wurtzite GaN and AlN structures can be up to ten times larger compared to conventional III–V compound materials [5].

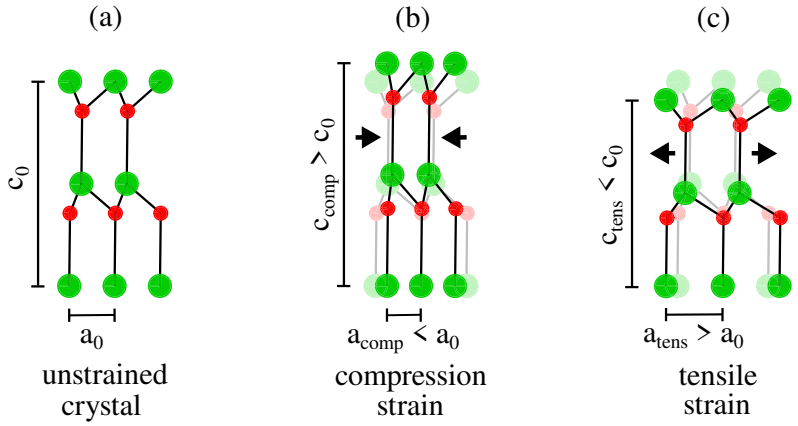

Figure 2.5: Two-dimensional cross-section of the GaN crystal unit cell in [0001] direction (cf. Fig. 2.3), illustrating the impact of strain on the lattice constants [40].

2.3.3 Two-Dimensional Electron Gas

The spontaneous and piezoelectric polarization can be beneficially exploited to develop semiconductor devices based on III-V materials. The spontaneous polarization of GaN (cf. Fig. 2.5) can be increased by adding aluminum (Al) into the compound, thus creating AlGaN. Here, the Al content does not only increase the spontaneous

polarization but also results in a smaller lattice constant of AlGaN in comparison to GaN, as illustrated in Fig. 2.6(a). Now, epitaxially growing AlGaN on top of a GaN results in the AlGaN initially adopting the larger lattice constant of the GaN layer, as showcased in Fig. 2.6(b). Due to this, tensile strained AlGaN starts to form in the initial growing area, which causes an additional piezoelectric polarization within the AlGaN layer itself.

Epitaxially growing AlGaN on Ga-faced GaN, both spontaneous as well as piezoelectric polarization align in direction [5] leading to a constructive superimposition, as illustrated in Fig. 2.6(c). Based on the differences in spontaneous polarization strength of AlGaN and GaN as well as due to the additional piezoelectric polarization, a net polarization remains in the AlGaN layer. Here, the positive part of the polarized charge is located at the AlGaN/GaN interface. Eventually, the positive charge attracts electrons from the GaN region that accumulate at the interface maintaining charge neutrality. However, these electrons are highly mobile (cf. Tab. 2.1) and gather in a very thin layer (sheet charge) close to the interface, which is why they are called two-dimensional electron gas (2DEG). Since the AlGaN layer forms an energy barrier, the 2DEG electrons tend to remain within the GaN region close to the AlGaN/GaN interface.

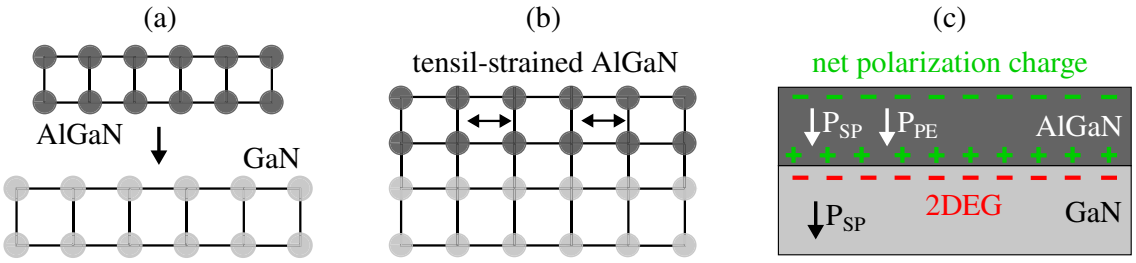

Figure 2.6: Crystal lattice (a) before and (b) after AlGaN is epitaxially grown on GaN. (c) Resulting spontaneous (P_{SP}) and piezoelectric (P_{PE}) polarization, which lead to a net polarization charge that attracts electrons at the AlGaN/GaN, thus creating a two-dimensional electron gas (2DEG) [5].

The formation of the 2DEG can also be explained based on the energy band diagram of the AlGaN/GaN heterojunction. Looking at the two materials prior to their contact as shown in Fig. 2.7(a), a difference in the bandgap energy E_{G} can be observed. This is due to the Al content in the AlGaN compound, which regarding

GaN does not only reduces the lattice constant but also leads to an increase of E_G. As a result, the distance from the conduction band energy E_C to the Fermi energy level E_F of AlGaN is higher than in the case of GaN.

Putting AlGaN and GaN into contact results in an equalization of E_F and thus to step in E_C, as illustrated in Fig. 2.7(b). This step in E_C is a typical property of heterojunction interfaces but does not remain persistent for tensile strained AlGaN growing on GaN. Simultaneously to the step formation, a net polarization charge occurs in AlGaN [cf. Fig. 2.6(c)], which consequently attracts electrons. Here, the electrons can not easily pass over or through the AlGaN barrier, resulting in an accumulation close to the interface. This negative sheet charge results in a localized increase of E_F, typically illustrated as a downward bending of E_C.

As a result, E_C forms a triangular-shaped potential well close to the AlGaN/GaN interface that can persist below E_F [5], as depicted in Fig. 2.7(c). Here, an excerpt and zoom of Fig. 2.7(b) is depicted. However, electrons accumulating below E_F are free carriers with high mobility that contribute to the conductivity of the sheet charge. Consequently, all electrons accumulating in the potential well below E_F are considered as the 2DEG.

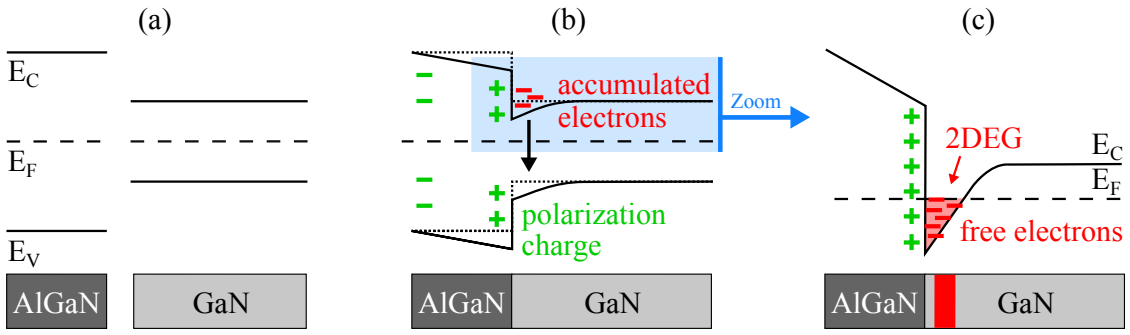

Figure 2.7: Band diagram of the AlGaN/GaN heterojunction (a) prior and (b) in-contact. Here, the polarization charge induces electron accumulation, leading to conduction band E_C bending. (c) The E_C bending can persist below the fermi energy level E_F, resulting in free electrons contributing to the 2DEG.

Although the AlGaN/GaN heterojunction forms a potential well, the density of states in the 2DEG is found to be related to the Al content and the thickness of the AlGaN layer [42]. As already mentioned, the Al content impacts the AlGaN lattice

constant and consequently the spontaneous polarization (cf. Fig. 2.5). Additionally, the lattice mismatch of the two layers (cf. Fig. 2.6) changes the tensile-strain-induced piezoelectric polarization that occurs in the AlGaN barrier.

Beyond that, despite the epitaxial growth of AlGaN which initially adapts the lattice constant of GaN (leading to tensile strain), strain relaxation occurs in the ascending layers of the AlGaN lattice. This results in a saturation of the possible piezoelectric polarization. In conclusion, the Al content and AlGaN thickness impact the net polarization charge, which in turn attracts carriers forming the 2DEG. Typically, the Al content is set to about 20 % to 35 % resulting in a necessary AlGaN thickness between 10 nm and 30 nm [43].

2.4 High Electron Mobility Transistor

The first functional GaN-based high electron mobility transistor (HEMT) has been reported in 1999 as an alternative to conventional field effect transistors such as MOSFETs and IGBTs [44]. The operating principle of HEMTs is based on the formation of a 2DEG in an AlGaN/GaN heterojunction (cf. Sec. 2.3.3), which is why they are typically realized as a laterally structured devices. The 2DEG does show a significant increase in electron mobility as well as the capability of a possible up to 10 times higher switching speed, which results in GaN HEMTs being promising candidates for the development of future PE-based applications [6, 45, 46].

2.4.1 Structure

The vast amount of state-of-the art GaN-based devices are 650 V-class GaN-on-Si HEMTs, whose cross-section illustrating their main structure is depicted in Fig. 2.8. In order to grow GaN on a Si substrate, an interlayer (buffer) is needed to balance several material properties, as discussed in more detail in Sec. 2.4.2. On top of the buffer, the AlGaN/GaN heterojunction is epitaxially grown, which ultimately forms the lateral structured 2DEG and thus conducts between drain and source contact (normally-on) without applying an external voltage.

For the development of fail-save PE systems a normally-on device is not desirable, leading to an introduction of different gate structures over the recent years,

as discussed in Sec. 2.4.3. Currently, a p-doped GaN (p-GaN) layer in the gate stack is the most promising solution to achieve a normally-off device. Furthermore, depending on the doping concentration of the p-GaN the gate stack either acts as an ohmic or a Schottky contact (cf. Fig. 2.12), as explained in Sec. 2.4.3. However, the behavior of the threshold voltage (V_{th}) is shown to be significantly different for HEMTs with ohmic of Schottky contact.

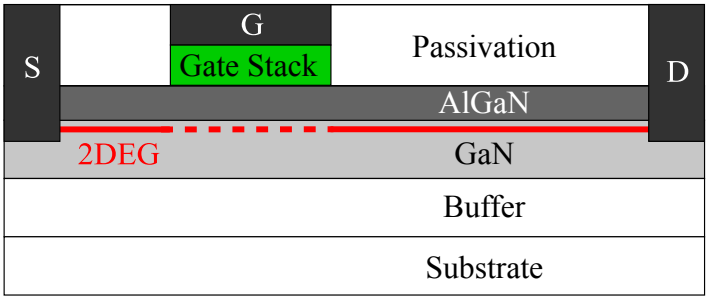

Figure 2.8: Simplified cross-section of the lateral GaN HEMT. The 2DEG forms in the AlGaN/GaN heterojunction which is typically grown on a buffer layer connecting it to the substrate. Nowadays, most gate stacks consist of a p-GaN layer.

2.4.2 Substrate

An obvious choice for the production of GaN-based devices is the usage of GaN as a substrate material. Although Si is among the most common materials on our planet, the availability of Gallium (Ga) is pretty decent as it is given as a by-waste of large-scale industrial aluminum (Al) production [47]. About 95 % of all mined bauxite is used for Al production and later converted using the Bayer process [48]. Here, Ga is an inherent by-product that is extracted during the Al refinement.

On the other hand, several issues prevent current commercial GaN devices from being produced on GaN substrates. First, the production of monocrystalline GaN substrates is relatively new and fairly complex compared to well-established Si crystals. Second, up until 2023 the diameter of producible GaN substrates are significantly lower with only 150 mm (6 inch) [49] compared to the up to 300 mm (12 inch) for Si substrates. Both of these issues lead to high production costs, hindering large-scale commercialization. Finally, as shown in Fig. 2.8, the HEMT is a later-

ally structured GaN device, meaning that most of its substrate does not participate in the main operation of current flow nor voltage blocking.

In lateral HEMTs, the thickness of the AlGaN/GaN heterojunction forming the 2DEG can be lower than 1 µm while still maintaining sufficient operation. On the other hand, in order to be able to handle the substrate during the manufacturing process, a minimum thickness of about 700 µm (for 6 inch diameter) is needed providing enough stiffness while simultaneously preventing it from breaking into pieces [50]. As illustrated in Fig. 2.9(a) (extract from Fig. 2.8), the HEMT structure only accounts for about one per mil of the overall thickness. Because of this, more cost-efficient substrate materials are often chosen for commercialization.

In order to utilize non-GaN substrate materials, the GaN layers need to be epitaxially grown on top of them, yielding the necessity of an interlayer (buffer) to function as a transition for the mostly different material properties. Here, several geometrical and physical properties must be considered, which may have to be compensated in the buffer layer. For example, a mismatch of the crystal lattice constants can cause tensions that eventually lead to microscopic dislocations and the emergence of traps, as discussed in Sec. 3.1.

In addition to that, a mismatch in the thermal expansion can lead to macroscopic crack formation and possible destruction. Furthermore, to benefit from the possible downsizing of HEMT structures, the thermal conductivity of the substrate should be sufficient to dissipate emerging heat during operation. The substrate is also required to insulate the occurring electrical field and the flow of disruptive leakage currents in the vertical direction. Finally, the substrate material must be cost-

Table 2.2: Physical properties of materials that could possibly be used as substrate for the production of GaN-based semiconductor devices such as the HEMT. [37]

Property	Unit	GaN	AlN	SiC	Al_2O_3	Si
Lattice constant	nm	0.3189	0.3112	0.308	0.2747	0.54301
Lattice mismatch	%	0	1	3.4	13	70
Thermal expension	10^{-6}/K	5.59	4.2	4.2	7.5	3.59
Thermal conductivity	W/mK	130	150	490	50	150
Isolation	$\Omega \cdot$ cm	10^9	10^{11}	10^{11}	10^{14}	10^4

efficient in production and processing to be competitive. Materials that possess a similar lattice constant and thermal expansion as GaN are AlN and SiC. These two also offer sufficient thermal conductivity and electrical isolation, see Tab. 2.2 [37]. On the other hand, up until 2023, AlN substrates are also only available up until 100 mm (4 inch) [51], while SiC substrates are still very expensive [52].

A much cheaper material capable of large diameter substrates is aluminum oxide (Al_2O_3), also known as sapphire, which is the most important substrate for mass production of optical diodes [53]. In turn, its lattice mismatch and thermal expansion are much higher, while it only offers low thermal conductivity. Finally, Si is the industry's most common substrate material due to its low cost, excellent availability, and large diameter capability. Despite having large lattice and thermal expansion mismatches as well as having low isolation capabilities, it quickly became the primary focus for commercialization of GaN HEMTs [53, 54].

In order to utilize Si as a substrate for GaN HEMTs, a buffer layer (cf. Fig. 2.8) is needed to compensate for dissimilar material properties. Over the years, two transition structures have prevailed, one being the step-graded AlGaN shown in Fig. 2.9(b) and the other a AlGaN superlattice that is depicted in Fig. 2.9(c). As a first step of building the buffer, a thin AlN base layer is grown on top of the Si substrate. Here, the AlN layer is needed to improve the low isolation capability of the Si substrate [53] as well as to align the mismatch in thermal expansion.

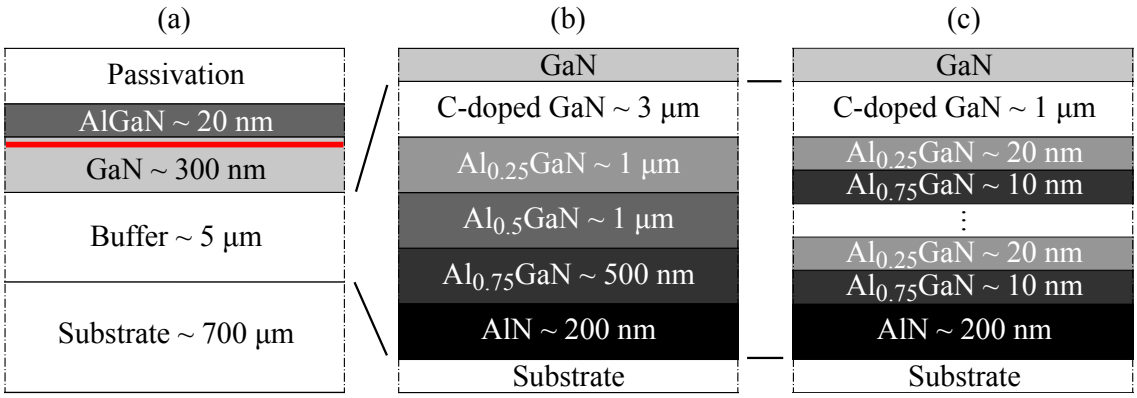

Figure 2.9: Cross-section of the GaN-on-Si technology, showing (a) the lateral HEMT structure (cf. Fig. 2.8) and the buffer layer produced by (b) step-graded AlGaN or (c) AlGaN superlattice structures [55] with roughly estimated thicknesses.

Afterward, AlGaN can be epitaxially grown on top of the AlN isolation. Then, the actual transition layer can be produced by, for example, gradually decreasing the Al content in step-graded AlGaN, leading to a relaxation of the lattice mismatch and thermal expansion, see Fig. 2.9(b). On the other hand, for the AlGaN superlattice in Fig. 2.9(c), very thin layers with alternating Al contents are stacked, leading to a multitude of heterojunctions. Here, a similar relaxation occurs while the heterojunctions beneficially improve the isolation capability [55].

Finally, independent of the transition structure, the buffer is topped by a GaN layer that is needed to form the AlGaN/GaN heterojunction (cf. Fig. 2.8). However, for further improvement of the buffer isolation, the initial GaN layer can be treated by e.g., carbon (C)-doping which has been shown to enhance the breakdown voltage capability of the GaN HEMTs by hundreds of volts [56]. Furthermore, the C-doped GaN layer has proven to reduce disruptive effects such as knee walkout and current collapse [57], as discussed in Sec. 3.1.

2.4.3 Gate Stack

In the early stages of development, the GaN HEMT has been a normally-on device due to the intrinsic formation of the 2DEG in the AlGaN/GaN heterojunction. However, normally-on devices are typically unsuitable for developing fail-safe PE systems, which led to the desire for normally-off devices. To obtain a normally-off HEMT, its 2DEG formation needs to be partially prevented or removed. Based on the physics of the formation (cf. Sec. 2.3.3), this can be achieved by either modifying the polarization charge at the AlGaN/GaN junction or by elevating the energy level in the potential well. However, any 2DEG modification must be reversible by applying a voltage (V_{GS}) to ensure a reliable turn-on of the normally-off HEMT.

Over the years, several gate structures have been introduced [7] that either modify or remove the 2DEG formation in the area below the gate contact. Thereby, many early approaches used metal-insulator-semiconductor (MIS) gate structures [58]. Although the additional insulator does not modify the 2DEG formation itself, it can prevent the flow of a significant gate current and lead to carrier accumulation during on-state, similar to a MOSFET.

In order to modify the 2DEG, a negative charge can be induced in the AlGaN layer, which subsequently neutralizes the positive polarization charge and thus prevents the formation of the 2DEG. This has been realized using a fluoride-based plasma treatment [59] and shown to be reliable for voltages up to 1200 V [60]. Another option is to recess the AlGaN layer and thereby reducing the tensile-strain induced piezoelectric polarization (cf. Fig. 2.5) leading to the development of the recessed MIS gate [61, 62]. On the other hand, the MIS-based gate-stack structures suffer from a trapping-induced collapse of the drain current resulting in a dynamic $R_{\mathrm{DS,on}}$ behavior, as further discussed in Sec. 3.1. Due to this, the recessed MIS gate appears to be unreliable for future development.

A significant reduction of the current collapse has been achieved with the introduction of a p-doped cap layer (p-gate) in the gate-stack [8, 9], as illustrated in Fig. 2.10. The p-gate reduces the current collapse by elevating the energy level in the potential well that initially forms the 2DEG and leads to a normally-off operation. While the energy band diagram of the AlGaN/GaN junction (cf. Fig. 2.7) is still applicable for most of the device, the additional doping of the p-GaN layer in the gate-stack (cf. Fig. 2.8) tends to impact the energy bands of the adjoining layers and thus the 2DEG formation itself.

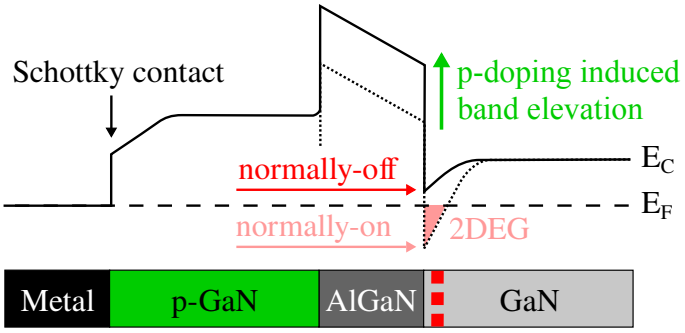

Figure 2.10: Energy band diagramm of the gate-stack cross-section (cf. Fig. 2.8) showing the creation of normally-off operation by adding a p-doped GaN layer.

The additional holes in the p-GaN increase the distance from the conduction band energy E_{C} from the fermi energy level E_{F} within the layer, which can also be interpreted as an E_{C} elevation. Then, due to a carrier imbalance, holes from the p-GaN layer diffuse into the thin AlGaN, which results in a band elevation too and

thus lifting E_C of the 2DEG potential-well above the E_F. Hence, no free electrons forming the 2DEG exist in the area below the gate stack, yielding a normally-off operation. However, for the on-state, a positive voltage can be applied, lifting the E_F and subsequently allowing free electrons to form the 2DEG. This approach of a normally-off HEMT became known as the gate injection transistor (GIT) or p-gate GaN HEMT and the subject of further commercialization [10, 54].

In Fig. 2.11, the cross-section of a p-gate GaN HEMT is shown. Applying a positive gate voltage on the HEMT leads to the formation of a current path from the gate metal through the p-doped GaN and the intrinsic AlGaN into the 2DEG and finally towards the source contact. Thereby, based on the distribution of carriers in this p-GaN/i-AlGaN/2DEG structure, it is commonly referred to as a p-i-n heterojunction or rather a forward biased p-i-n diode [63]. However, compared to a common p-i-n diode, the current flow is not based on carrier diffusion but on the effect of thermionic emission (TE) through the AlGaN barrier.

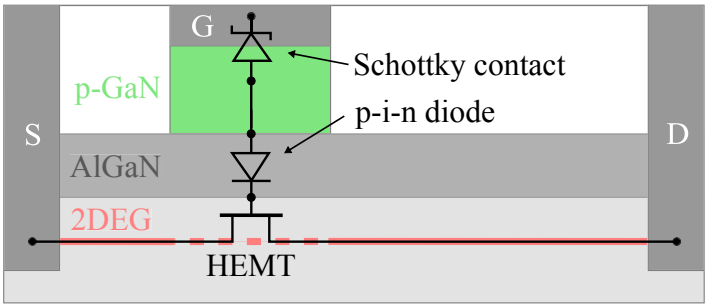

Figure 2.11: Cross-section of a p-gate GaN HEMT, illustrating formation of a Schottky contact and p-i-n diode in the gate-stack attached to the intrinsic HEMT.

Apart from that, the gate metal/p-GaN junction forms a Schottky contact resulting in a reverse-biased Schottky diode. Here, the barrier height of the Schottky contact strongly depends on the material used for metallization and the p-doping concentration in the p-GaN layer. The metallization of the source and drain ohmic-contact is typically realized by alloy stacks of titanium (Ti)/aluminum (Al)/nickel (Ni)/gold (Au) in a metal electron evaporation process [64]. Thereby, Ti/Al serves as contact metal, while Au is needed for low resistive bond pads and Ni as a diffusion barrier which prevents voiding between Al and Au. For reasons of cost reduction

and production efficiency, it is assumed that the Ti/Al/Ni/Au stack is equally used for the fabrication of the p-GaN metallization.

Due to a fixed gate metallization, the Schottky barrier's height and thus the Schottky contact's behavior is solely adjusted by the doping concentration of the p-GaN layer. A low amount of dopants results in a high barrier and the formation of a low current Schottky contact typically referred to as Schottky gate. On the other hand, with high doping, a low barrier occurs that subsequently yields a high current Schottky contact that is often referred to as an ohmic gate.

2.4.4 State-of-the-art Technologies

There is quite a wide variety of available state-of-the-art GaN-based technologies, which are for comparability shown as an overview in Fig. 2.12. The vast amount consists of lateral structured GaN HEMTs, which are available for voltages up to 650 V. Here, the main limiting factors of applicable voltage are the substrate material, its insulation, and the quality of the buffer layer connecting the substrate and the lateral HEMT. For cost and production efficiency, mainly silicon (Si) substrates are used, while only thin layers of GaN are epitaxially grown on top of them (cf.

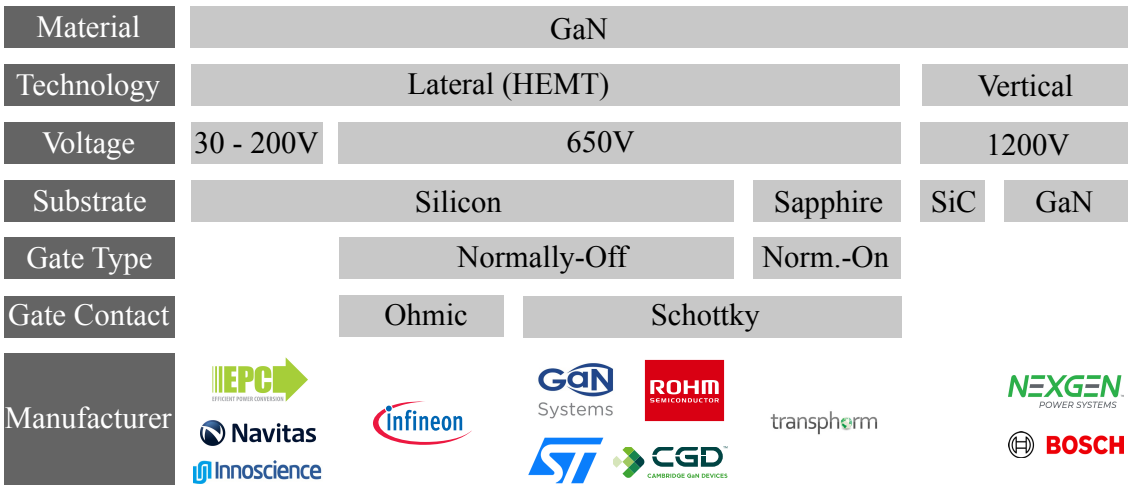

Figure 2.12: State-of-the-art GaN-based technology overview for different voltage classes, substrates, and gate structures. Exemplary manufacturers and their primary area/focus are shown here, although wider line-ups and overlaps may exist.

Sec. 2.4.2). In order to further increase the voltage capability of HEMTs, more advanced substrate materials like SiC or GaN need to be utilized, which are mostly too expensive for the time being. If this is solved, technologies like the vertical GaN MOSFET [65, 66] or the vertical GaN Fin transistor [67, 68] appear to be promising solutions. Apart from that, the most common technological difference in HEMTs are the type and contact of the gate structure (cf. Sec. 2.4.3).

Chapter 3

Undesired Effects

A major goal in developing reliable power semiconductor devices is to reach an ideal operation without interference for all possible operations. However, real devices often suffer structurally-based undesired effects, which must either be tolerated or proactively counteracted. For example, common MOSFETs can suffer from a drain-induced barrier lowering (DIBL) or short-channel effect [69]. This effect reduces the threshold voltage V_{th}, which becomes more crucial for devices with short channel lengths. Now, considering GaN, early HEMTs suffered from an effect called (drain-) current collapse that is discussed in more detail at Sec. 3.1. While the effect has mainly been counteracted during the development of modern devices, the origin might still be relevant for present effects.

Today, the most prominent undesired effect of p-gate GaN HEMTs is the unsteady behavior of V_{th}. The V_{th} behavior depends on the applied gate- and drain-source voltages, which can cause either a V_{th} shift or instability. Here, the V_{th} shift is partially comparable to the DIBL of MOSFETs, as explained in Sec. 3.2. On the other hand, the V_{th} instability is caused by mechanisms of carrier accumulation, depletion, and trapping, which to some extent have similarly been observed for current collapse, as further explained in Sec. 3.3.

3.1 Drain Current Collapse

In the early stages of development, the GaN HEMT suffered from the phenomenon of a collapsing drain current, the so-called current collapse. This effect can be observed in the output characteristics comparing the results of DC and pulsed measurements, as depicted in Fig. 3.1. During the off-state or rather between each on-state of the measurement pulses, the trapping of electrons can occur that can be located at the surface passivization [12] and in the buffer region [13]. The trapped electrons impact the charge in the 2DEG, which then becomes apparent during on-state immediately after a turn-on switching event.

The trapping of electrons is a temporal phenomenon, meaning that the amount of the trap states and thus the impact on the 2DEG fades over time, which becomes more evident for increased on-state durations. Since the 2DEG determines the on-state resistance $R_{\mathrm{DS,on}}$, which appears to vary depending on the on-state duration, this effect is often called dynamic $R_{\mathrm{DS,on}}$. However, this phenomenon can nowadays mostly be neglected, which has been achieved by significant improvements in materials and manufacturing as well as the introduction of advanced structures.

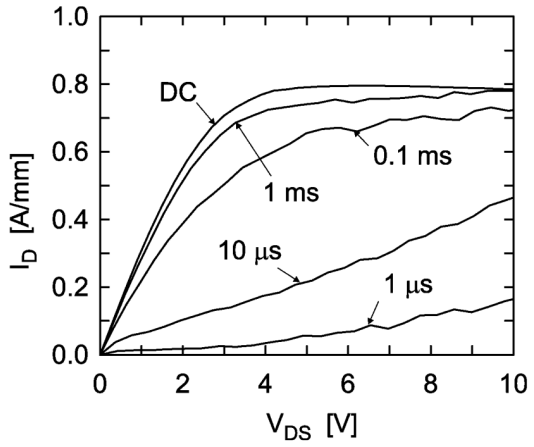

Figure 3.1: *"Experimental $I_{\mathrm{D}} - V_{\mathrm{DS}}$ characteristics obtained in DC and in gate turn-on mode by pulsing. The pulse width is varied from 1 ms to 1 µs with a 100 ms periode. Pulsed I_{D} values are obtained by averaging the $I_{\mathrm{D}}(t)$ samples over the final, stable portion of the pulse width."* - G.Meneghesso, 2004 [70]

3.1.1 Virtual Gate

Initially, the current collapse was observed in MIS-HEMT devices, where it was assumed to be hot electron trapping in the gate insulator at the drain side of the gate [11]. However, devices without a gate insulator were also affected due to the trap states located in the surface passivization [12]. Here, the traps appeared as gate extensions toward the drain side, forming a virtual gate, see Fig. 3.2.

The filling of the trap states results from the acceleration of electrons from the 2DEG, based on the electrical field of the drain voltage V_{DS} and the leakage of electrons from the gate metal due to the gate voltage V_{GS} [71]. The filled surface traps occur as donor-like states, expanding the depletion region and thus diminishing

the carrier density in the 2DEG. Consequently, an overall reduction of the drain current I_D and the transconductance occurs [72].

Apart from the trapping of electrons in surface states, hot electron injection into the buffer region has been observed [73, 74]. Thereby, electrons can be trapped in lattice impurities of the buffer layer as deep-level donor-like states [75], as also shown in Fig. 3.2. As for the surface states, the filled buffer traps diminish the carrier density in the 2DEG and therefore I_D. However, while the filling of traps occurs in the off-state of the device, the electrons stuck in trap states tend to be emitted during the on-state. Consequently, this leads to a transient recovery of the 2DEG [71] and, therefore, the impression of a dynamic $R_{DS,on}$.

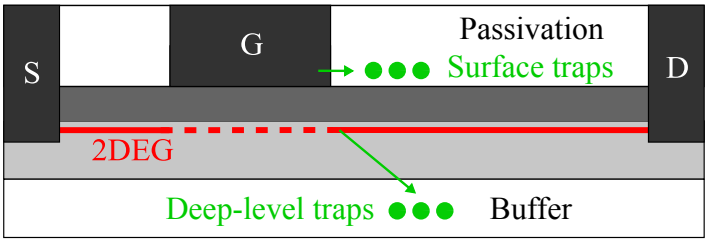

Figure 3.2: Cross-section of the HEMT structure illustrating trapped electrons in the surface passivation and in the buffer. Surface traps mainly occur due to gate-leakage current, while deep-level traps are injected by hot electrons.

3.1.2 Material Quality and Field Plates

In recent years, the materials and the manufacturing processes have been improved to reduce the amount of available trap states. A significant reduction of states in the surface passivization has been accomplished by using silicon nitride (Si_3N_4) [72] or AlN [76] and lately silicon mononitride (SiN) [77] for commercial manufacturing processes. An improvement in the GaN buffer has initially been made by utilizing defined doping of the structure with C, which has further been improved by the usage of iron (Fe) as the dopant [78, 79]. Furthermore, the doping of the GaN buffer has shown to be essential to suppress buffer leakage, short-channel effects such as DIBL as well as a punch-through of the electrical field [80].

Apart from reducing existing trap-states by improving material quality, the introduction of source and gate field plates helped to discharge remaining states during

the turn-on or eventually prevent their occupation in the first place, see Fig. 3.3. Here, the field plates decrease the electrical field peak at the gate-drain edge and thus reduce the energy of hot electrons, which diminishes the amount of electron trapping [81]. However, the improvements of materials used at the surface passivization and as the buffer, along with the introduction of field plates, drastically help to diminish the impact of trapping-induced current collapse [82].

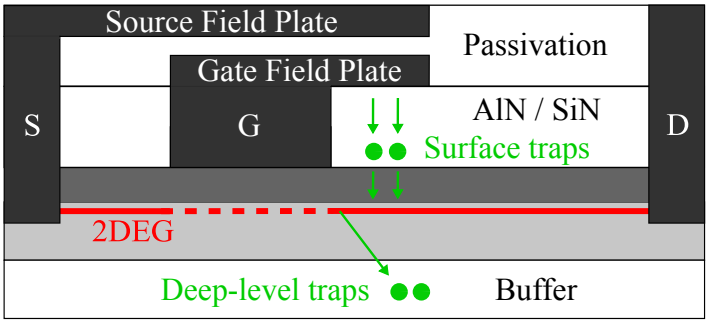

Figure 3.3: Cross-section illustrating source and gate field plates that reduce the amount of trap states due to lower field peaks and discharging them at turn-on.

3.1.3 Hole Injection

In an attempt to finally overcome the current collapse, an improvement in the gate structure was introduced, leading to the invention of the GIT HEMT [9, 83]. The GIT either has a p-doped GaN or AlGaN layer in between the metallization and the AlGaN barrier, as shown in Fig. 3.4. For operation at $V_{\mathrm{GS}} > V_{\mathrm{th}}$, holes from the p-doped GaN layer are injected into the 2DEG. The injected holes neutralize

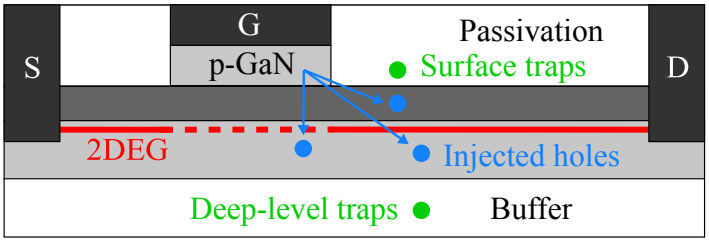

Figure 3.4: Cross-section demonstrating hole injection from p-GaN during on-state, which neutralize trapped electrons and enhance the 2DEG conductivity.

the impact of trapped electrons in the surface and buffer states while attracting additional electrons yielding an enhancement of the 2DEG conductivity.

With the introduction of the conventional GIT, a current collapse-free operation has been shown for moderate voltages of $V_{DS} = 60\,V$ [9]. This is due to the injected holes counteracting the trapped states filled by hot electrons originating from the applied V_{DS}. However, for higher voltages, the impact of deep-level states becomes much more crucial [84], which appears to be problematic for high-voltage applications. As a solution, the hybrid-drain embedded GIT has been developed [85], as shown in Fig. 3.5. Thereby, an additional p-GaN layer is placed near the drain contact. The hybrid drain becomes forward-biased for an operation with high voltages, injecting supplementary holes into the 2DEG. As a result, a current collapse-free operation has been proven for voltages up to $V_{DS} = 800\,V$ [14].

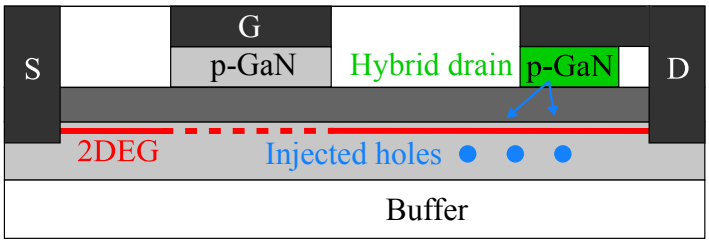

Figure 3.5: Simplified cross-section of the HEMT structure, showing the extension of a hybrid drain that injects holes at high drain-source voltages.

3.2 Threshold Voltage Shift

In MOSFETs, a shift of the threshold voltage V_{th} can be observed that depends on the device structure and the applied drain-source voltage V_{DS}. This V_{th} shift occurs in devices with short channels and is a consequence of the potential distribution and high electric field in the channel region [86]. In such short-channel devices, the energy barrier between the source contact and the channel region can eventually be lowered by the applied V_{DS}. Consequently, the channel current increases corresponding to a negative V_{th} shift. This phenomenon is typically referred to as the short-channel effect or the drain-induced barrier lowering (DIBL) [69].

The DIBL effect is a phenomenon that is specifically related to the structure and thus only relevant for MOSFETs or MOSFET-like devices with sub-micrometer channels. However, there are suggestions that similar behavior could be present in GaN HEMTs [87], although they exhibit a vastly different structure. Nevertheless, the suspected DIBL of HEMTs is only claimed for short-channel devices, which is why it is assumed to be negligible for power devices with a micrometer scale.

Until 2022, the vast majority of studies on the threshold voltage of GaN HEMTs claimed that the applied V_{DS} causes a V_{th} instability [15, 16]. To be more precise, the occurrence of a positive V_{th} instability for off-state V_{DS} stress has been attributed to the effects of hole depletion in the gate stack, as explained in Sec. 3.3.2. As a novelty, in 2022, a correlation of the drain and gate has been discovered that causes a negative V_{th} shift, initially titled as gate/drain coupled barrier lowering (GDCBL) [19]. Compared to the V_{th} instabilities, the GDCBL is a static phenomenon that does not change over time, as demonstrated by transient measurements in Sec. 5.1.1. Furthermore, it is shown that off-state V_{DS} causes a positive V_{th} instability, while on-state V_{DS} yields a negative V_{th} shift.

In Fig. 3.6, the cross-section of a p-gate GaN HEMT is shown, illustrating the equivalent electrical characteristics of the gate-stack area. The formation of the gate-drain capacitance can be described by the series of space charge region (SCR) capacitances that form in the gate stack. Here, the capacitance spreads over the SCR of the reverse-biased Schottky contact C_{SC} and the forward-biased p-i-n diode C_{PN}. Note that the intrinsic HEMT does not further contribute to the gate capacitance, since the impact of the AlGaN barrier is already considered within C_{PN}.

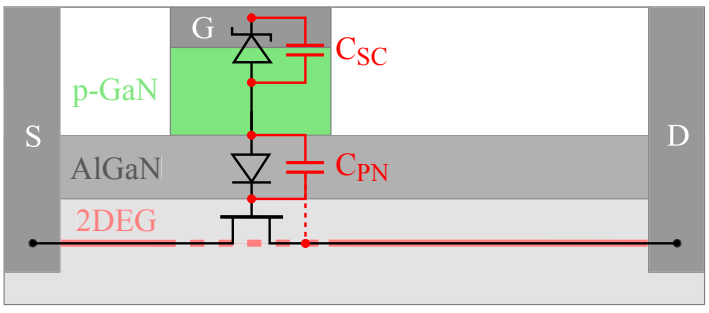

Figure 3.6: Cross-section showing the distribution of the gate-drain capacitance over the Schottky contact, p-i-n diode and intrinsic HEMT (cf. Fig. 2.11).

As explained by [19], applying V_{DS} on the HEMT results in a displacement current that charges or rather redistributes the charge in the SCR capacitances. Consequently, the applied V_{DS} that virtually charges the gate-drain capacitance determines the potential within the floating p-GaN region, which links the two diodes C_{SC} and C_{PN}. As a result, an increase of V_{DS} yields an elevation of the potential in the p-GaN layer that ultimately determines the depth of the potential well forming the 2DEG for the on-state of the device (cf. Sec. 2.4.3).

An increase of the p-GaN potential compares to a lowering of the conduction band energy E_C relative to the fermi energy level E_F, as shown by the gate-stack band diagram in Fig. 3.7. Due to this, more energy states exist in the potential well below E_F, yielding more available electrons and thus enhancing the 2DEG. The potential distribution across the capacitances and thus in the p-GaN layer are fixated by the applied V_{DS}, so the 2DEG enhancement appears as a static phenomenon. Consequently, due to the V_{DS}-induced 2DEG enhancement, a lower V_{GS} is needed for device turn-on, resulting in a negative V_{th} shift.

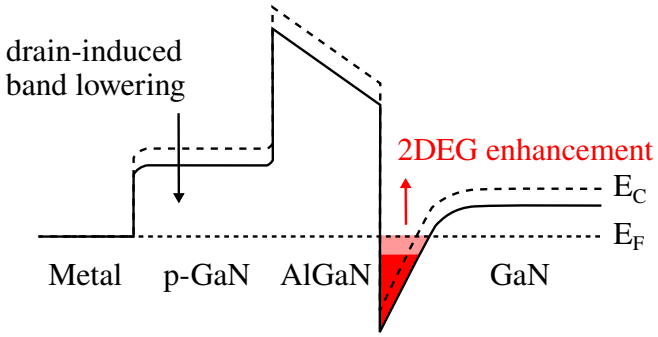

Figure 3.7: Energy band diagram of the gate-stack cross-section (cf. Fig. 2.8) showing the V_{DS}-induced gate barrier lowering, resulting in a 2DEG enhancement.

3.3 Threshold Voltage Instability

The V_{th} instability can be explained by electron depletion and trapping mechanisms, as well as hole accumulation and trapping. These mechanisms cause a temporal change of V_{th} and are proven to be induced by the applied gate voltage V_{GS} during the on- and off-state of a p-gate GaN HEMT. The V_{GS}-induced mechanisms lead

to a change of charge in the 2DEG, which in turn affects the behavior of the drain current I_{D}. All of the mechanisms are believed to occur within the gate stack and the area below, which appear to correlate with the V_{DS}-induced V_{th} shift. The origin and the impact of electron depletion and trapping are discussed in Sec. 3.3.1. The hole accumulation and trapping effects are presented in Sec. 3.3.2.

3.3.1 Electron Depletion and Trapping

The occurrence of electron depletion and trapping and their impact on the 2DEG can be explained using the gate-stack band diagram, as shown in Fig. 3.8. Applying a positive voltage $V_{\mathrm{GS}} \geq 0\,\mathrm{V}$ on the gate-stack results in the p-i-n diode (p-GaN/AlGaN/2DEG cf. Fig. 2.11) to be biased in forward operation. On the other hand, the Schottky diode (metal/p-GaN) is biased in reverse operation.

A positive V_{GS} causes electrons that originate in the 2DEG below the gate to be captured in trap states that are located within the AlGaN barrier [24, 88]. Note that not all possible electron trap states are located in the AlGaN barrier. However, this is only assumed for simplification and will further be denoted as such. Additional trap states are located in the material-transition interfaces of AlGaN/GaN [18] and p-GaN/AlGaN, which exist due to the tension-based lattice defects.

The trapping of electrons in the AlGaN barrier significantly impacts the actual 2DEG below the gate stack. First of all, electron trapping is depends on the electrical field of the applied voltage and can already occurs in nominal V_{GS} operation (cf. Sec. 3.3). The removal of electrons causes a depletion of the 2DEG. Beyond that, the 2DEG is even further depleted due to the negative charge induced by the trapped electrons. However, the depletion of 2DEG electrons ultimately results in a higher V_{GS} needed for the turn-on, translating into a positive V_{th} shift. Since carrier trapping is a mostly temporal phenomenon, this refers to a positive V_{th} instability.

Apart from immediate trapping, the 2DEG electrons can also be injected through the AlGaN barrier into the p-GaN region via thermionic emission (TE) [17]. This similarly causes a depletion of 2DEG electrons but, in turn, no additional charge-based interaction. The electrons injected into the p-GaN region can now either drift to the gate contact through the depleted p-GaN region [17, 89], be captured in other trap states [89] or recombine with holes [17, 89, 90].

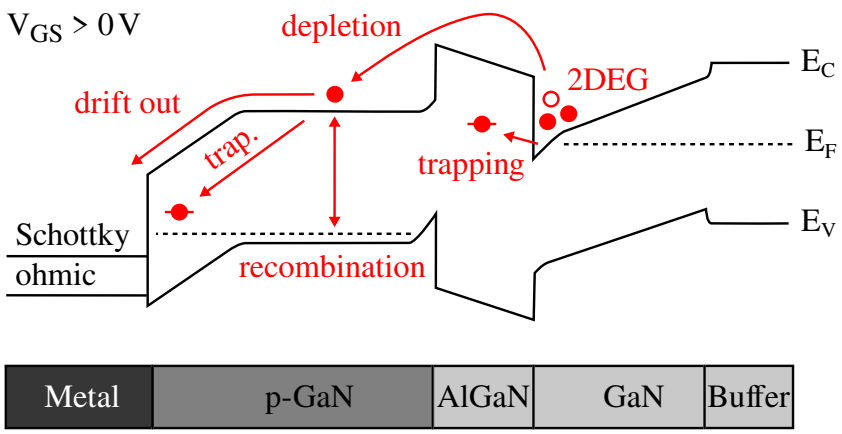

Figure 3.8: Band diagram of the gate-stack (p-gate), illustrating the depletion of the 2DEG electrons due to depletion and trapping at positive voltages $V_{GS} \geq 0\,V$.

While electrons drifting out of the gate contact do not have an additional impact besides the 2DEG depletion, trapping and recombination alter the effective charge in the p-GaN region. Here, trapped electrons remain as a net negative charge, while recombination of electron-hole pairs causes hole deficiency [90]. However, both effects reduce the effective charge of the p-GaN region, which superimposes the impact of the doping concentration that ensures the normally-off operation due to band elevation (cf. Fig. 2.11). Consequently, the charge reduction in the p-GaN region causes a reduction of the 2DEG and, therefore, a positive V_{th} instability.

For a negative voltage $V_{GS} \leq 0\,V$ applied on the gate stack, no free electrons remain below E_F to form the 2DEG. Therefore, an immediate trapping of electrons during the off-state of the device should virtually be negligible. Then again, the electrical field of the negative V_{GS} is still capable of activating trap states in the AlGaN barrier [91]. Consequently, the trap states can be filled by electrons originating in the proximity 2DEG located at the gate-source drift region. On the other hand, the gate-drain drift region's involvement is proven insignificant. However, trapping electrons in the AlGaN barrier causes a positive V_{th} instability.

3.3.2 Hole Accumulation and Trapping

Besides the injection of electrons from the 2DEG, holes can also be injected into the p-GaN by applying positive voltages $V_{GS} \geq 0\,V$ on the gate-stack, as illustrated in

Fig. 3.9. Here, the holes that originate in the gate metal can be injected through the metal/p-GaN interface via TE [18, 92, 93, 94] and field-assisted tunneling [17, 22, 89, 95]. Furthermore, additional holes can appear within the p-GaN region due to the release of acceptor and trap states [18].

The holes that are injected or released into the p-GaN region move along the electrical field towards the p-GaN/AlGaN interface. Here, the additional holes either accumulate at the interface or are captured by trap states in the AlGaN barrier [18, 93]. Consequently, the positive charge of the holes trapped in the AlGaN barrier attracts additional electrons into the 2DEG. Furthermore, the accumulated holes in the p-GaN region increase the effective gate charge resulting in a 2DEG enhancement. As a result, applying a positive V_{GS} can result in the accumulation and trapping of holes, yielding a negative V_{th} instability. Apart from that, the trapping of holes can result in the neutralization of trapped electrons [24, 93, 94, 95], which in turn reduces the trapping-induced positive V_{th} shift (cf. Fig. 3.8).

Besides the accumulation and trapping of holes at the p-GaN/AlGaN interface, excess holes can further be injected through the AlGaN barrier, which in turn limits the preceding effects. Afterward, the injected holes can recombine with electrons from the 2DEG or move through the GaN region towards the source and buffer. At the buffer, holes can accumulate again or get captured in trap states [17, 24]. While recombining electron-hole pairs reduces the 2DEG, the additional charge accumu-

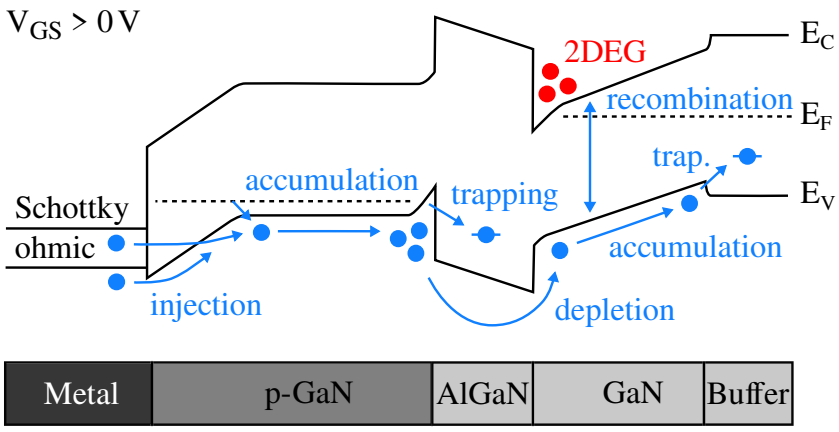

Figure 3.9: Band diagram illustrating the enhancement of the 2DEG that can occurs due to hole accumulation and trapping at positive voltages $V_{GS} \geq 0\,V$.

lated and trapped in the buffer results in a positive charge. Consequently, this charge attracts additional electrons into the 2DEG, causing a negative V_{th} instability.

In contrast to that, applying a negative voltage $V_{\mathrm{GS}} \leq 0\,\mathrm{V}$ on the gate results in the Schottky diode (metal/p-GaN) being forward biased, while the p-i-n diode (p-GaN/AlGaN/2DEG) is reverse biased. However, similarly to the operation with a positive V_{GS}, holes from acceptor or trap states can be released in the p-GaN region [46], see Fig. 3.10. The electrical field forces the released holes to move towards the metal/p-GaN interface, where they can accumulate at the Schottky barrier. A deficiency of holes occurs in the p-GaN region, causing a reduction of the effective gate charge in the area closer to the AlGaN barrier.

Reducing the effective gate charge in the p-GaN region eventually results in fermi energy lowering which lifts the potential well forming the 2DEG and thus reduces the amount of free carriers. Applying a positive voltage for the on-state does not result in an immediate return of holes accumulated at the Schottky barrier. The process of holes moving back to their origin and refilling the states is relatively slow due to the very low gate current [46]. In conclusion, the depletion of holes in the p-GaN, which subsequently accumulate at the Schottky barrier, causes a temporal 2DEG reduction and thus a positive V_{th} instability. This effect appears not only for negative V_{GS} but also for applying V_{DS} during the off-state. Here, the high electric field at the edge of the gate-stack results in ionization and depletion of holes in the

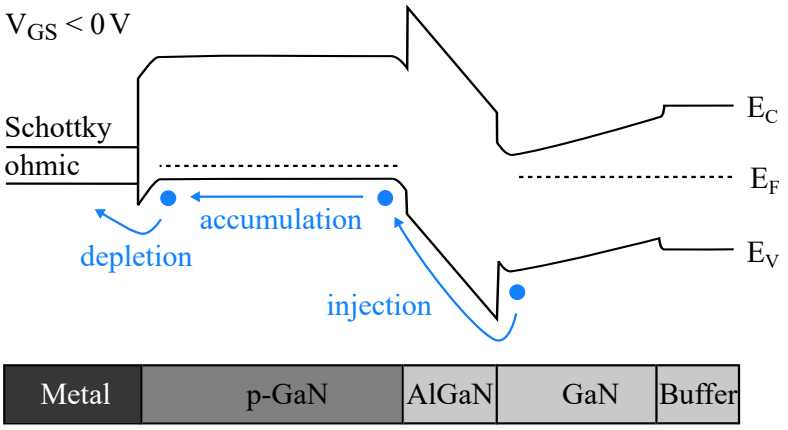

Figure 3.10: Band diagram illustrating the effects of hole injection, depletion, and accumulation, which can occur at negative voltages $V_{\mathrm{GS}} \leq 0\,\mathrm{V}$.

GaN from the acceptor states [15, 16]. Although a different cause, this also results in a positive V_{th} instability.

Apart from the effects within the p-GaN region, an additional injection of holes can occur through the AlGaN barrier, similarly to hole injection at positive V_{GS}. Then, these holes neutralize or refill empty acceptor and trap states, restoring the initial doping-induced gate charge in the p-GaN region. Furthermore, the injected holes can move towards the Schottky barrier, which further increases the accumulated carriers. Beyond that, the excess holes are lifted above the Schottky barrier and drift out the gate stack. Consequently, the additional holes that remain in the p-GaN region after a turn-on, by applying a positive V_{GS}, cause an increase of the effective gate charge and thus a negative V_{th} instability.

Chapter 4

Experimental Investigation

A major part of evaluating the V_{th} behavior of semiconductor devices is the experimental investigation based on measurements. In order to estimate the present relevance of the effects, commercially available GaN HEMTs that are typically used in PE applications are evaluated, as listed in Sec. 4.1. For accurate determination of V_{th} in the time-domain, a custom pulse setup is developed and used, see Sec. 4.2. With this setup, transient single pulse measurements can be acquired that ultimately translate into the V_{th} behavior, as explained in Sec. 4.3. Finally, the self-heating that occurs during measurements is estimated by a thermal model and subsequently used to recalculate the results to neglect temperature-based effects, see Sec. 4.4.

4.1 Devices Under Test

The device under tests (DUTs) are commercially available 600-V class p-gate GaN HEMTs from different manufacturers, listed in Tab. 4.1. In both DUTs, the gate stack contains a p-doped GaN layer (p-gate cf. Sec. 2.4.3), while the metal/p-GaN interfaces are realized as Schottky contacts that differ in leakage current. The device with the high gate-leakage current $I_{\mathrm{G,nom}}$ is the Infineon IGT60R190D1S [96] and labeled *ohmic gate* as suggested by [17]. On the other hand, the low leakage device

Table 4.1: Overview of the devices under test (DUTs).

Property	Symbol	Unit	IGT60R190D1S [96]	GS66504B [97]
Gate-Stack			ohmic gate	Schottky gate
Max. Blocking Voltage	V_{DS}	V	600	650
Nominal Gate Voltage	$V_{\mathrm{GS,nom}}$	V	3.5	6.0
Gate Current at $V_{\mathrm{GS,nom}}$	$I_{\mathrm{G,nom}}$	mA	15	0.08
On-state Resistance	$R_{\mathrm{DS,on}}$	mΩ	140	100
Threshold Voltage	V_{th}	V	1.25	1.1

is the GaN Systems GS66504B [97], which is accordingly labeled as the *Schottky gate*. Besides this, both DUTs have comparable ratings.

4.2 Measurement Setup

In many cases, semiconductor device analyzers such as the Keysight B1505 [98] are used to characterize DUTs. Thereby, DC characteristics are acquired by averaging single pulse measurements with a minimum on-state duration of about 1 ms. However, even much shorter durations can already impact the threshold voltage V_{th} of p-gate GaN HEMTs. Furthermore, the single pulse waveforms done by the device analyzers to acquire the DC characteristics are typically unobtainable for the user, which limits the validity of the results. As shown in Sec. 3.3, already short duration gate pulses with 100 ns duration lead to a severe V_{th} instability, which accordingly can only be obtained using high-resolution transient measurements.

To accurately measure the V_{th} behavior, a custom setup is developed which is capable of time-domain measurements for pulse lengths ranging from a duration of 100 ns up to 100 s. The setup consists of three main parts: the gate driver, the DUT circuit, and the power supply unit. A CMOS-based approach is chosen for fast switching gate driving transients, which is simplified illustrated in Fig. 4.1.

Due to the digital behavior of the CMOS stage, the V_{GS} of the DUT can be switched between two different voltage levels for the on-state (V_{meas}) and off-state

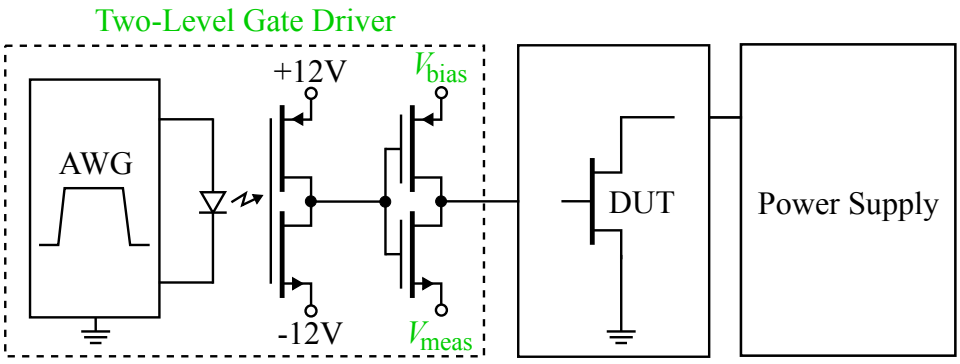

Figure 4.1: Custom setup used for pulsed measurements, emphasizing the two-level gate driver design that is composed of two consecutive CMOS stages.

(V_{bias}). Here, the driving signal is provided using the arbitrary waveform generator (AWG) Keysight 33500B [99], in conjunction with the opto-isolator (optocoupler) Toshiba TLP5771 [100] for galvanic isolation of the driving circuit. Finally, using the CMOS stage Infineon BSD235C [101], switching durations for an on- and off-state of about 12 ns as well as switching transients of 0.33 V/ns can be achieved. Besides this, the driver voltages V_{bias} and V_{meas} are limited to ± 10 V, as recommended by the manufacturers. The voltages are provided by a galvanically isolated auxiliary power supply that can be adjusted with an accuracy of about 50 mV. Finally, ensuring sufficient switching of the CMOS stage, the optocoupler supply is set to ± 12 V.

Utilizing the two-level driver, V_{meas} will already be applied on the DUT during its off-state, which can impact their behavior for voltages above V_{th}, as shown in Sec. 5.1.4. Hence, a off-state duration of 100 s is needed prior to each measurement to avoid an unintentional V_{th} instability. This can reliably be achieved using a third driver voltage. A simple multi-level driver concept could be the usage of an operational amplifier with a dynamic supply-voltage adjustment. The downside is a much slower transition between different voltage levels compared to a CMOS-based design. Another possibility is to add additional CMOS stages as a supply for the main CMOS driver (cf. Fig. 4.1). Thereby, up to four voltages can be implemented, while maintaining fast switching transients. Conversely, supply voltage buffering might be unfavorable, leading to large gate loops and unintentional ringing.

A more robust driver design can be achieved using a common gate bus with switchable voltage sources, as illustrated in Fig. 4.2. Here, the same concept of iso-

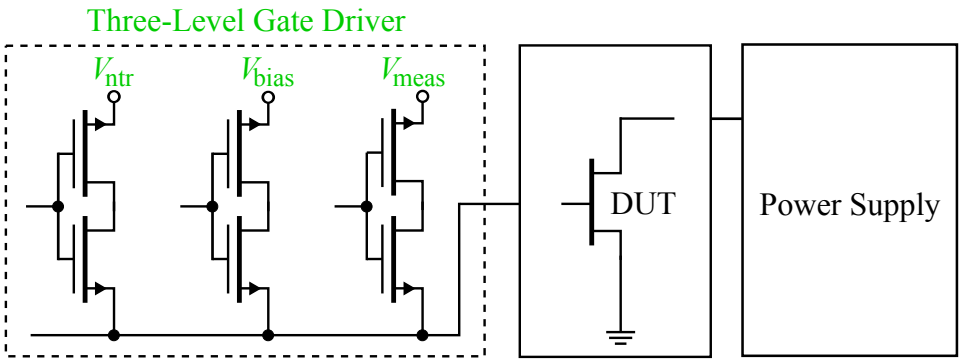

Figure 4.2: Custom setup showing the three-level gate driver design based on opposing n-type MOSFETs. Here, only three levels are shown while more are possible.

lated supply voltage is used, as done for the CMOS design. The supply voltages V_{ntr}, V_{bias}, and V_{meas} are connected to the gate bus by a series of two n-type MOSFETs [102] operated in opposing directions with merged gates. The voltages can be applied to the gate bus for switching the respective MOSFETs to their on-state, while they remain disconnected during their off-state due to the complementary body diodes. However, with the used MOSFETs switching transients with slew-rates comparable to the CMOS driver can be achieved. Apart from that, the control of the three-level gate driver is more complex and prone to error due to the voltage alignment while switching through the different sources.

The V_{th} behavior investigation is based on transient measurements acquired using the oscilloscope Teledyne LeCroy HDO4054A [103], as shown in Fig. 4.3. The low voltage V_{GS} measurements are done using the differential probe Pico TA045 [104]. Furthermore, this probe determines the gate current as voltage drop over the gate resistance ($I_{\mathrm{G}} = V_{\mathrm{R}}/R_{\mathrm{G}}$). The high voltage V_{DS} measurement is done using the differential probe Teledyne LeCroy HVD3106A [105]. Finally, the drain current I_{D} is acquired with the current probe Teledyne LeCroy CP031A [106] offering a maximum current resolution of 1 mA/div.

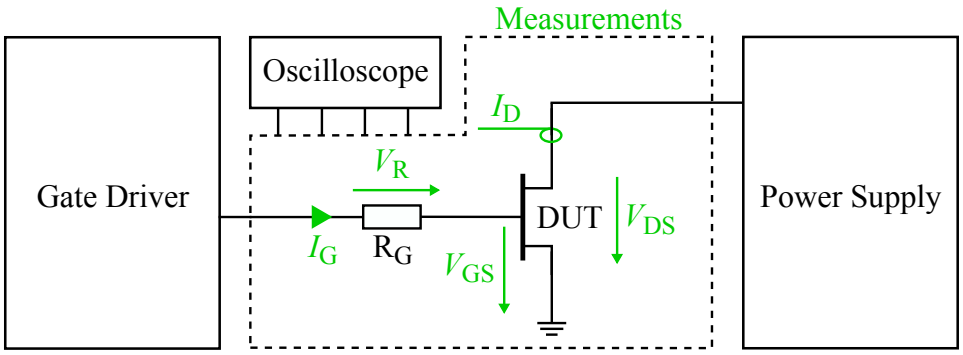

Figure 4.3: Custom setup showing the implementation of the measurements, which are acquired using an oscilloscope for the evaluation of the transient behavior.

4.2.1 High Speed Resolution

The gate driver design allows for fast switching gate transients that result in fast drain transients if a power supply is connected. However, the applied V_{GS} and V_{DS}

appear to have a combined impact on the V_{th} behavior, as showcased in Sec. 5.1.4. To distinguish their respective impact, applying the voltages on the DUT must be independent of each other. Thereby, fast switching V_{DS} transients should be achieved to monitor swift changes of the V_{th} behavior properly.

For this purpose, a half-bridge supply (HBS) power unit is developed, offering high-speed resolution and independent V_{GS}- and V_{DS}-control on the DUT, as shown in Fig. 4.4. Here, the DUT is operated as the low-side (LS) switch of the half-bridge, along with a separately controlled high-side (HS) switching unit. Reducing the HS resistance and its impact on the investigation, four paralleled Rohm SCT3080KL SiC-MOSFETs [107] are used, offering a total $R_{\mathrm{DS,on}}$ of 20 mΩ which is about five times smaller than the $R_{\mathrm{DS,on}}$ of the DUTs. The control of both the HS and LS switches is done by similar high-speed drivers that are interlinked by the AWG.

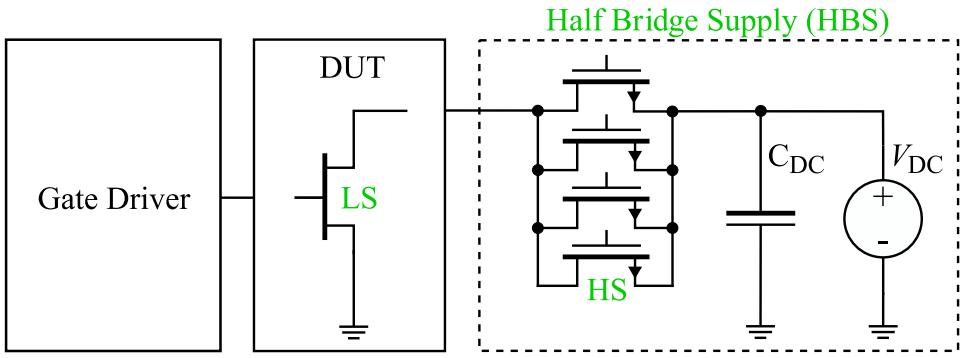

Figure 4.4: Custom setup showing the half-bridge supply (HBS), where the DUT is operated at the low-side (LS) with four SiC-MOSFETs at the high-side (HS).

The DC-link voltage V_{DC} of the HBS setup is provided by the external power supply Keysight N5772A [108] and low inductively connected to the LS switch. To stabilize V_{DC} providing enough energy for transient measurements, a DC-link capacitor C_{DC} is integrated. Here, the capacitance can be adjusted using different units such as 820 µF (max. 1.2 kV) for short durations measurements below 10 µs or even 58 F (max. 16 V) using a super-capacitor for durations up to 100 s.

The impact of a V_{th} instability is observable in the initial I_{D} peak and can persist for up to 100 s in duration. To measure this, long-duration measurements are required, which reduces the time resolution required to observe fast-changing transients. One solution could be a time-exponential acquisition, which would allow

for many measurement points in the early stage after turn-on, which then spreads out for long durations. However, this method is unavailable utilizing the mentioned measurement equipment. As a solution, long-duration measurements are acquired by three consecutive single pulses with increasing durations, as illustrated in Fig. 4.5. The consecutive pulses are set to durations of 100 µs, 100 ms, and 10 s since they overlap, which can be used to verify their conformance.

The resulting I_D, shown for transient measurements in Sec. 5.1.1, is extracted by processing and combining the three pulses. First, each pulse is acquired up to ten times and subsequently averaged to reduce the impact of measurement deviations caused by instrumentation errors, environmental influences and noise. Then, the switching slopes appearing in the overlap regions are cut. Afterward, I_D is extracted in a time-exponential scale, yielding a linear distribution if plotted in a logarithmic timescale. Finally, the curves are combined, resulting in a long-duration I_D waveform offering a high time resolution that can cover fast-switching transients.

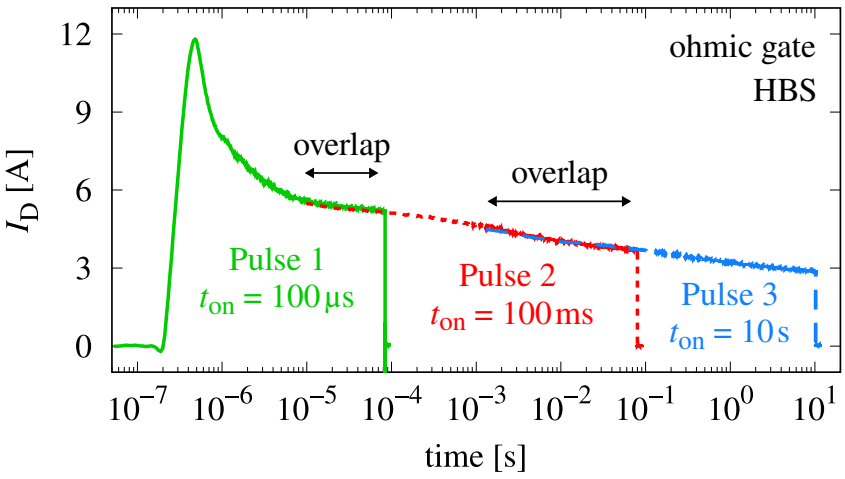

Figure 4.5: Transient I_D constructed from three consecutive pulses with increasing durations, offering a high time resolution for fast-transient measurements with long durations. Note that each pulse is measured up to ten times and then averaged.

4.2.2 High Current Resolution

Although the HBS offers fast switching transients with a resolution of 1 mA, the accuracy might be insufficient, especially investigating the subthreshold region of

the DUTs. In order to increase the resolution, an improved I_D measurement could be implemented utilizing a shunt resistor. However, in the subthreshold region, I_D can range from below 1 nA up to 100 mA, which would require multiple switchable shunts to maintain a reasonable resolution.

Another possibility would be the usage of a source measure unit (SMU), thus replacing the HBS while applying and measuring V_{DS} as well as I_D at the same time. Here, the Keithley 2461 [109] is used because it offers a pulsed measurement acquisition showing reliable results for currents ranging from 100 nA up to 1 A. Furthermore, the SMU automatically change the measurement range internally, allowing for precise results over the wide I_D range. Note that the SMU' current is limited to 1 A and thus only used for subthreshold measurements.

Apart from limited maximum current, the SMU suffers a significant reduction in the applicable switching transients compared to the HBS, as shown in Fig. 4.6. While the HBS reaches transient of about 100 V/µs, the switching duration of the SMU is limited to 150 µs regardless of the voltage. Hence, the initial I_D peak can not be captured using the SMU configuration for high-resolution measurements.

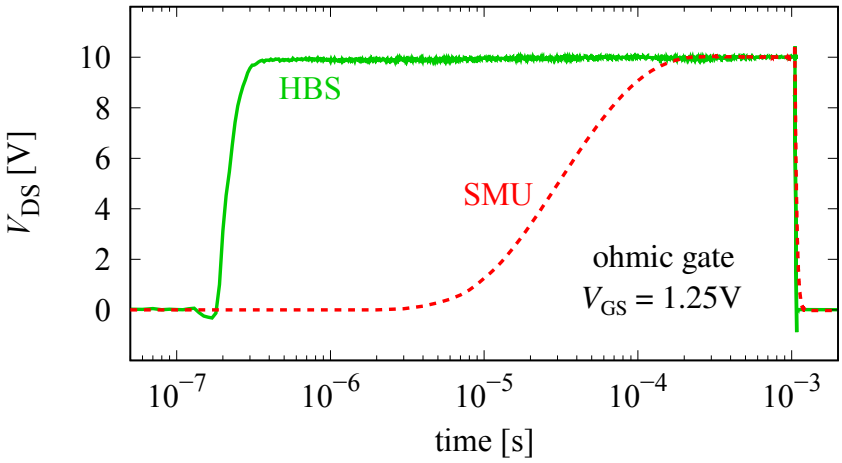

Figure 4.6: Applied V_{DS} pulse from 0 V to 10 V, comparing the switching durations of the half bridge supply (HBS) and the source meassure unit (SMU) for $I_D < 1$ A.

In Fig. 4.7, the transient I_D waveforms of the ohmic-gate DUT are shown, comparing the acquisition of the HBS and the SMU. Here, three different gate-driving conditions are used that demonstrate the occurrence and convergence of a V_{th} in-

stability that appears during the transient I_D measurement. Comparing the I_D waveforms, a drastic reduction in the initial I_D peaks is present for the SMU due to the slower switching transient, which requires 150 µs for turn-on. However, apart from the lower I_D resolution of the HBS, the waveforms of both setups sufficiently match after the 150 µs. Here, the impact of the three conditions appears to persist for up to 100 s before it disappears. This is caused by an V_{th} instability which can possess very long time constants, as further evaluated in Sec. 5.1.1.

In order to obtain reliable results using the SMU, instead of the HBS, the evaluation of I_D is set between the boundaries of 150 µs and 1 ms. Here, the duration is limited to 1 ms to ensure that the impact of self-heating remains negligible for evaluation, as discussed in Sec. 4.4. On the other hand, the lack of fast switching transients using the SMU might significantly reduce the validity of the measurements, especially considering operation conditions at high switching frequencies.

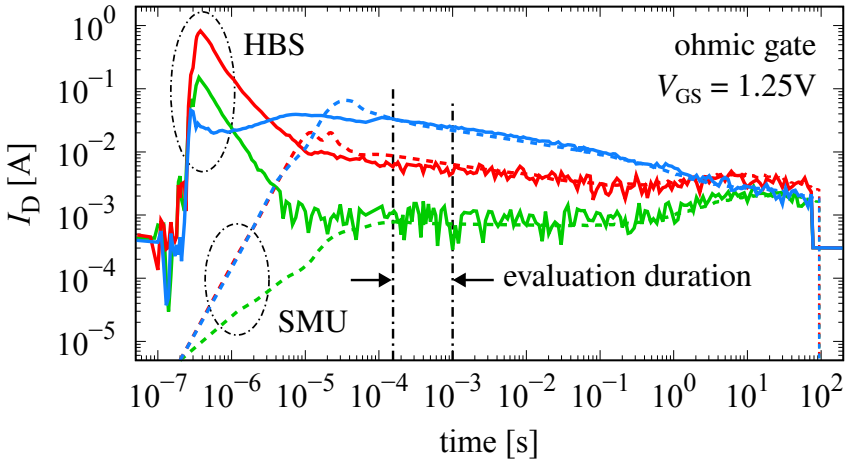

Figure 4.7: Transient I_D waveforms comparing the acquisition accuracy over time for the HBS and the SMU for three different gate-driver conditions.

Now evolving from a transient assessment towards DC characteristics, results of the full subthreshold region can be examined, as depicted in Fig. 4.8. Here, the results acquired by the HBS and SMU are compared to the Keysight B1505 semiconductor device analyzer. The B1505 offers a very high resolution for a DC sweep measuring currents down to 1 nA, while the pulsed operation is limited to 50 µA with a minimum on-state duration of 1 ms. However, looking at the results

comparing the DC and pulsed measurements, a shift of the subthreshold region ΔV_{th} can be observed. This ΔV_{th} is caused by the lack of sufficient off-time during the DC measurements (cf. Fig. 1.1) and further discussed in Sec. 5.1.1. Besides this, both custom setup options agree with the results of the B1505 in pulsed operation, which all prevent a ΔV_{th} due to sufficient off-time duration. Although the HBS offers much faster transients, using the SMU yields a significant improvement in resolution with currents down to 100 nA.

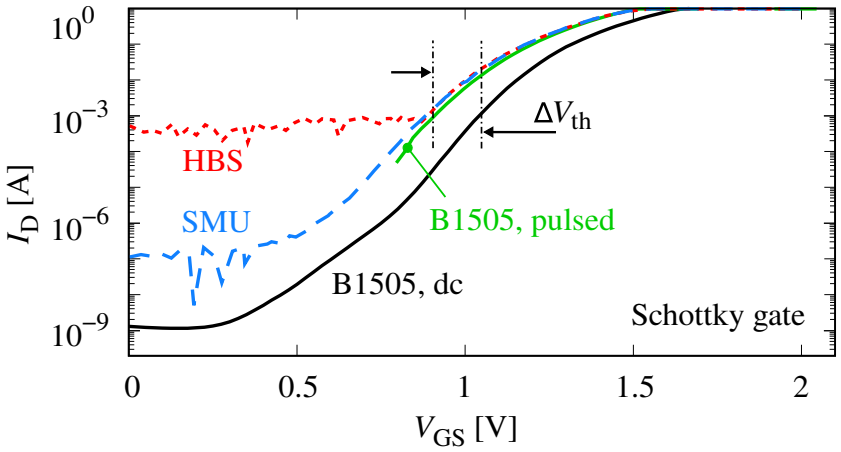

Figure 4.8: Transfer characteristics of the subthreshold region in a semi-logarithmic scale. Here, an acquisition done with the HBS and SMU in pulsed operation is compared to the Keysight B1505 device analyzer in DC and pulsed operation.

4.3 Measurement Procedure

The investigation of the V_{th} behavior is based on single-pulse measurements, whereby the DUT is controlled by the driving conditions of the drain and gate shown in Fig. 4.9. Here, the drain-source voltage V_{DS} is either applied by the HBS (cf. Fig. 4.4) or the SMU. The gate-source voltage V_{GS} is provided by the custom gate driver in either a two-level (2-lvl, cf. Fig. 4.1) or three-level (3-lvl, cf. Fig. 4.2) design, depending on the focus and the requirements of the investigation.

In order to investigate the impact of the V_{DS}-induced V_{th} shift (cf. Sec. 3.2), two different driving conditions are considered, both causing a short-circuit (SC)

operation of the DUT, as depicted in Fig. 4.9 (a). If $V_{DS} > 0\,V$ is already applied during the off-state ($V_{GS} < 0\,V$), a direct turn-on of the DUT results in a SC resembling a hard switching fault (HSF). In turn, the second type represents a SC occurrence during the on-state ($V_{GS} > 0\,V$) or rather a fault under load (FUL). Note that, for a HSF the gate voltage V_{GS} needs to be 0 V or negative prior to the measurement, while for a FUL the V_{GS} is applied about 100 ns prior to V_{DS}.

For the investigation of the V_{GS}-induced V_{th} instability (cf. Sec. 3.3), each V_{GS} pulse provided by the gate driver is split into three phases, as illustrated in Fig. 4.9(b). Initially, the DUT remains in off-state for a duration of $t_{ntr} \geq 100\,s$, which is defined as the *neutralization* phase. The *neutralization* is required to allow the DUT to revert to the same steady-state value of V_{th} prior to each measurement. However, a proper neutralization can only be achieved by using a three-level gate driver that applies a V_{GS} of $V_{ntr} = 0\,V$, while $V_{DS} = 0\,V$ (FUL) is set during this period.

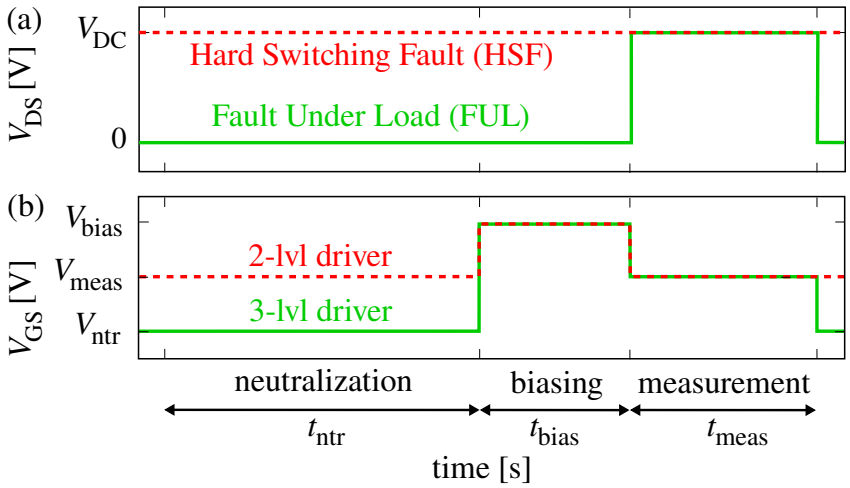

Figure 4.9: Driving conditions of the DUT illustrating the applicable voltage waveforms at the (a) drain and (b) gate. Both drain waveforms can be applied using the HBS or SMU, while the gate waveforms depend on the driver design (2-lvl or 3-lvl).

Afterward, in the *biasing* phase, the preliminary bias voltage V_{bias} is applied for the duration of t_{bias}. Note that a positive V_{bias} can only be applied for a FUL with $V_{DS} = 0\,V$, otherwise a flow of I_D occurs already in the *biasing* phase. Finally, in the *measurement* phase the DUT is turned on with $V_{GS} > 0\,V$ and $V_{DS} > 0\,V$, consequently I_D is measured at the on-state voltage V_{meas} for a duration of t_{meas}.

The preliminary bias conditions V_{bias} and t_{bias} applied during the off-state significantly impact the behavior of V_{th}, as shown in Sec. 5.1. However, their impact is non-linear and highly depends on the structure of the gate stack (cf. Sec. 3.3). For a reasonable comparison of the ohmic-gate and the Schottky-gate DUTs, matching gate-driving conditions are defined and listed in Tab. 4.2. These conditions are chosen to possibly be relevant for an operation in a PE application.

First of all, applying zero bias ($V_{\text{bias}} = 0\,\text{V}$) serves as a *reference* for any comparison. The first significant condition is the gate turn-on *overshoot*, which can be caused intentionally through the gate driver's design and unintentionally by drain-sided feedback. In case of the Schottky-gate DUT, the V_{bias} is set to the maximum voltage the manufacturer recommends. In turn, the ohmic-gate DUT has an inherent self-limitation due to a diode-like increase in gate current for higher voltages. Finally, the excessive *OFF-state* demonstrates the turn-on condition from the maximum negative V_{GS} after a long off-state duration.

Table 4.2: Application-relevant gate-driving conditions. Note that from now on, these will be referred to in their short form: reference, overshoot, and OFF-state.

	ohmic gate		Schottky gate	
driver condition	Vbias	tbias	Vbias	tbias
reference	0 V	0 s	0 V	0 s
turn-on *overshoot*	6 V	100 ns	10 V	100 ns
excessive *OFF-state*	−10 V	10 s	−10 V	10 s

Typically, the evaluation of V_{th} is done by acquiring the DC transfer characteristics and tracking an eventual shift that is induced by the applied *biasing* conditions during the off-state [15, 16, 17]. In this work, all presented DC characteristics are based on single pulse measurements acquired with the custom setup (cf. Sec. 4.2). With this setup, the transient I_{D} waveforms can be measured, converted into DC characteristics, and subsequently used to determine the V_{th} behavior.

In order to illustrate the extraction procedure used to determine the V_{th} behavior of the DUTs, exemplary measurement conditions and their resulting transient I_{D} waveforms are presented in Fig. 4.10. As shown in Fig. 4.10(a), two different gate-driving waveforms are applied, with one serving as a reference and the other as a

biasing condition (cf. Tab. 4.2). Here, both conditions differ in the voltage V_{bias} applied prior to the turn-on, while they utilize the same voltage V_{meas} during on-state. The resulting transient I_{D} waveforms are compared in Fig. 4.10(b), illustrating that their currents appear to be shifted by ΔI_{D} towards each other. To further evaluate this, the transient results are translated into DC characteristics, offering the possibility to compare a wider range of measurements simultaneously. For this purpose, the DC equivalent values of I_{D} are determined by averaging over time starting from the point in time when V_{DS} settles, after turn-on, until the end of the pulse (t_{meas}). Note that the time it takes for V_{DS} settle requires about 150 µs for the SMU, while with the HBS it requires less then 1 µs (cf. Fig. 4.6).

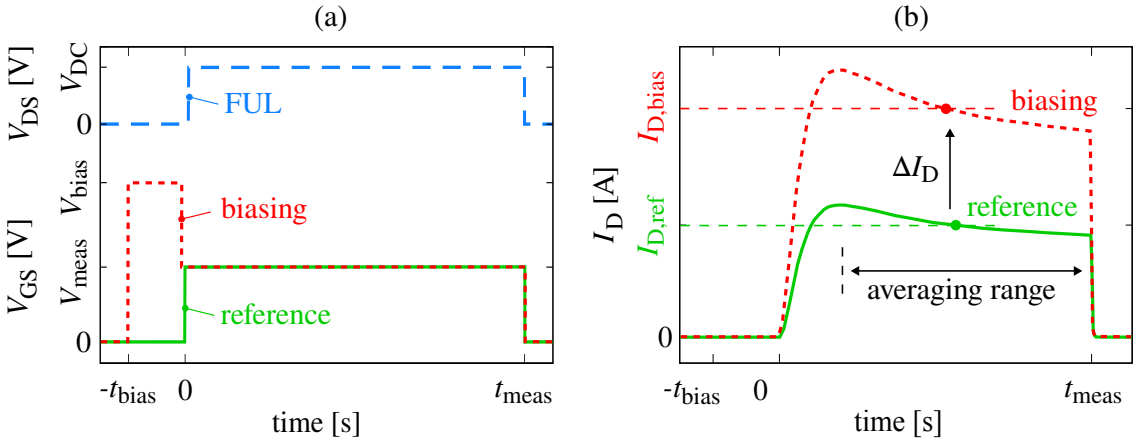

Figure 4.10: Extraction procedure of the threshold voltage V_{th} for exemplary bias conditions, showing (a) the driving conditions and (b) the drain current over time.

As shown by transient measurements in Sec. 5.1.1, the impact of various driving conditions can lead to an instability of V_{th}, which can persist for durations of up to 100 s. The largest part of the deviation can be observed in the initial I_{D} peak between $t_{\mathrm{on}} = 1$ µs to 1 ms, which diminishes over time until it finally converges with the reference behavior. Now considering V_{th} instabilities that occur for operation at high frequencies, investigated with pulse durations below 1 ms, the observed ΔI_{D} from Fig. 4.10(a) appears to be a static phenomenon. However, the ΔI_{D} is a temporal shift (instability), which can merely be translated into a quasi-static behavior. Consequently, the transient I_{D} waveforms are measured, averaged over time, and translated into DC equivalent values. To reduce the impact of self-heating that oc-

curs for operation at increased power, the measurement and averaging duration is limited to 10 µs for the HBS and 1 ms for the SMU, as explained in Sec. 4.4.

Repeating the measurement procedure with subsequent DC extraction of I_D for various gate-source voltages (during on-state $V_{GS} = V_{meas}$), results in the acquisition of the respective transfer characteristics, as shown in Fig. 4.11(a). Here, the resulting transfer characteristics that refer to the two different biasing conditions are compared with each other in the subthreshold region. Although there shape behaves similar, they appear to be shifted towards each other. Thus, assuming V_{th} to refer to a steady value of the drain current I_D, shift of the transfer curves can be translated into a V_{th} shift.

Since there is no unified definition for V_{th}, it is assumed as the V_{GS} required for $I_D = 10\,\text{mA}$. Consequently, comparing the applied biasing condition $V_{bias} \neq 0\,\text{V}$ with the reference condition $V_{bias} = 0\,\text{V}$ [cf. Fig. 4.10(a)], their impact on the transfer curves can be expressed as a threshold voltage shift ΔV_{th}. Finally, repeating the whole procedure for different bias voltages V_{bias}, a full map of the ΔV_{th} is acquired, as depicted in Fig. 4.11(b). As a result, the behavior of a V_{GS}-induced V_{th} instability is acquired, which corresponds to the impact of different V_{bias} at a constant t_{bias}.

Note that V_{th} is chosen to be extracted at 10 mA to remain comparable results for the acquisition with the HBS and the SMU. However, verifying this at 1 mA with the SMU, similar results are acquired, apart from an obvious offset.

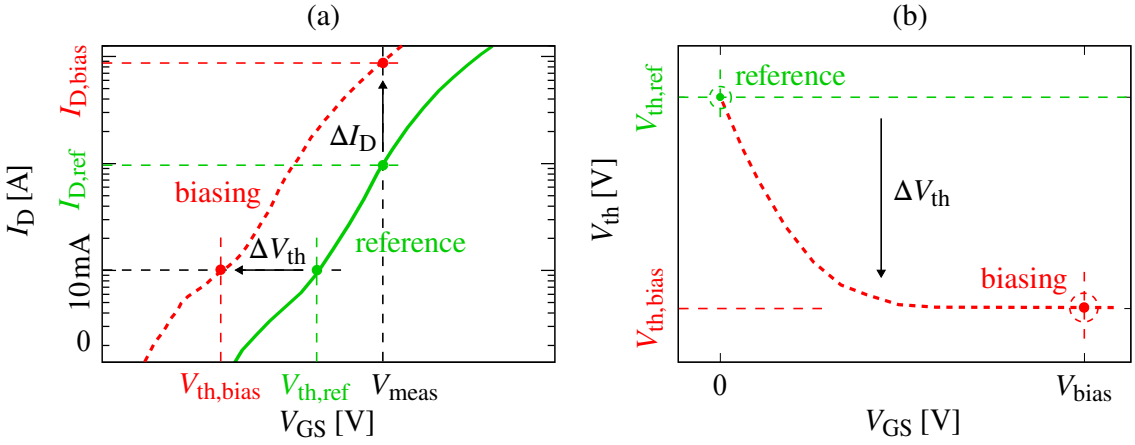

Figure 4.11: Extraction of V_{th} for exemplary bias conditions, showing (a) the DC transfer characteristics in a semi-logarithmic scale and (b) the resulting V_{th} behavior.

4.4 Self-heating

A major concern performing I_D measurements over time is the impact of self-heating that can significantly compromise the resulting waveform and thus the averaging of it. In order to verify this, a one-dimensional analytical temperature model is used to estimate self-heating for a given power dissipation [110]. The model determines the temperature increase of the DUT assuming an equally distributed power dissipation in the active area, considering GaN-specific material parameters.

Since manufacturers of commercially available DUTs do not provide geometrical information, the active areas are determined by opening their packages and measuring them, as shown in Fig. 4.12. For this purpose, a chemical wet-etching procedure is applied on the encapsulated DUTs, utilizing red fuming nitric acid (HNO_3). Afterward, the active area is determined using an optical microscope.

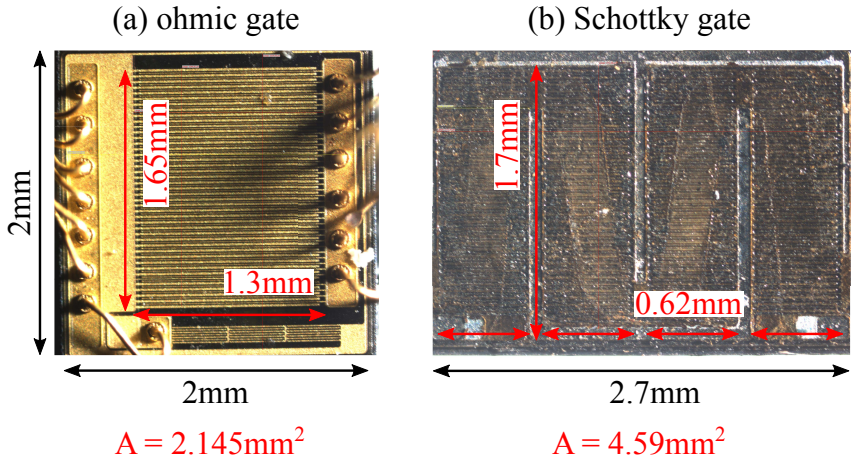

Figure 4.12: Bare die images of the (a) ohmic-gate and (b) Schottky-gate DUT, showing the extraction of their active area A. The dies are revealed by chemical etching of the encapsulation and are measured with an optical microscope.

In order to assess the impact of self-heating that occurs during the transient measurements of the DUTs, the device temperature must be extracted from the I_D pulses, as shown in Fig. 4.13. First, an averaging range is defined, similar to the V_{th} extraction (cf. Fig. 4.10), which is used to determine the DC values, see Fig. 4.13(a). Then, the temperature increase ΔT_{DUT} is calculated over time utilizing an one-

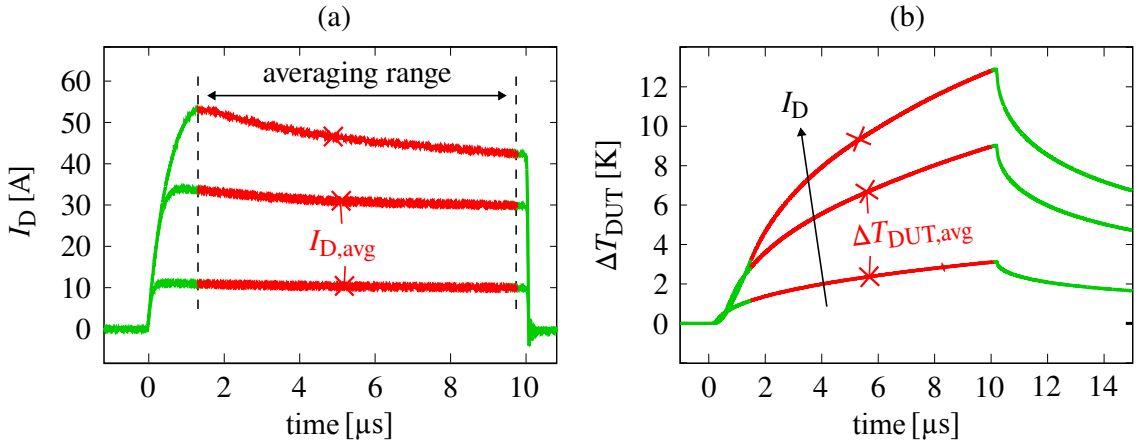

Figure 4.13: Extraction of the device temperature from (a) transient I_D measurements by (b) determination of ΔT_{DUT} using the thermal model.

dimensional analytical temperature model that is derived from an semi-empirical formula [110]. The resulting temperature increase is plotted in Fig. 4.13(b).

The next step is to plot the averaging range of I_D derived from Fig. 4.13(a) over the estimated ΔT_{DUT}, as illustrated in Fig. 4.14(a). By doing so, the temperature gradient can be found, which is then extrapolated to the point of zero temperature increase $\Delta T_{DUT} = 0\,K$. Finally, repeating this procedure for e.g., many V_{GS}, the DC transfer characteristics can be determined excluding the impact of self-heating, see

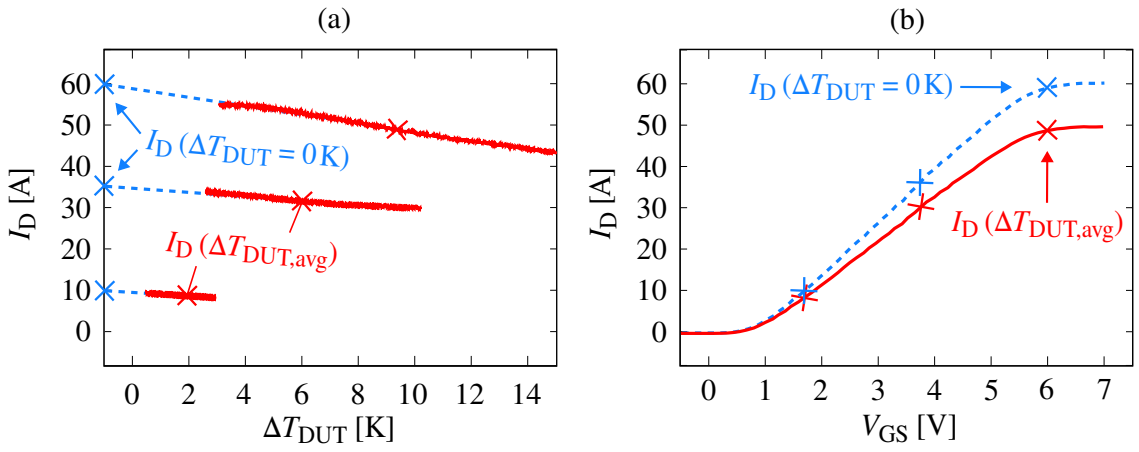

Figure 4.14: Extraction of self-heating, estimated by (a) computation of ΔT_{DUT} over I_D with subsequent extrapolation to $\Delta T_{DUT} = 0\,K$. (b) Transfer characteristics comparing the results with ($\Delta T_{DUT,avg}$) and without ($\Delta T_{DUT} = 0\,K$) self-heating.

Fig. 4.14(b). Here, the results for averaged I_D with $\Delta T_{DUT,avg}$ are compared to the results with extracted self-heating at $\Delta T_{DUT} = 0\,K$. The impact appears negligible for low currents, while at high currents, the increased temperature tends to lower the characteristics significantly. Consequently, this method is used to ensure that the impact of self-heating is excluded while evaluating the behavior of V_{th}.

Although the model estimates the impact of self-heating, the setup, and measurements are optimized to reduce its emergence in the first place. The DUTs are soldered and operated on an insulated metal substrate providing a large thermal capacitance to prevent a rapid temperature increase. The substrate consists of a 30 x 30 x 3 mm core made of Al and 75 µm copper track with an electrical insulation in between, operating as heat sink.

The functionality of the heat sink is given as long as the power dissipation or the measurement duration is kept low. Since the power dissipation is inevitable high for certain measurements, the on-state duration is adjusted respectively. In case of the SMU, the on-state duration is set to a relatively long duration of 1 ms, which is acceptable because it is only used to measure the subthreshold region with currents up to 100 mA. As a result of this, the estimated temperatures of both DUTs are shown in Fig. 4.15(a). Here, the maximum temperature increase reaches up to about 1 K, in case of the ohmic-gate DUT. Hence, the effect of self-heating

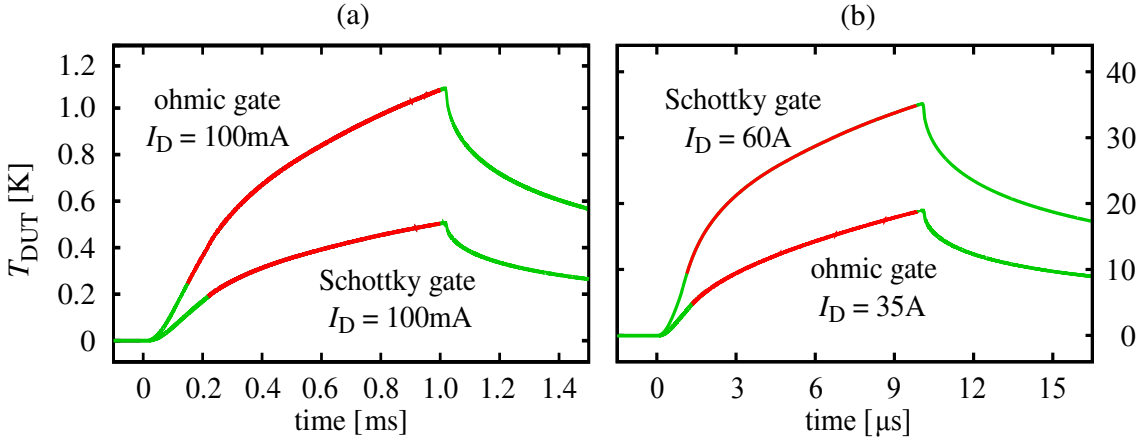

Figure 4.15: Estimated temperature increases, determined with the thermal model. Here, results of both DUTs are compared at maximum operation points acquired with (a) the SMU at low currents and (b) the HBS at high currents.

can be considered negligible performing measurements in the subthreshold region.

Apart from that, looking at measurements with high currents up to 60 A, the effect of self-heating is indispensable, as shown in Fig. 4.15(b). Here, the HBS is used because it provides faster transients and thus the possibility of a much smaller on-state duration that is set to 10 µs. As a result, the temperature increase can indeed be reduced but still reaches up to 40 K in case of the Schottky-gate DUT at maximum current. Consequently, the impact of self-heating needs to be considered while investigating DC characteristics with currents above the subthreshold region.

Chapter 5

Results and Discussion

The behavior of the threshold voltage V_{th} of p-gate GaN HEMTs can be categorized into a static shift and a dynamic instability. In order to evaluate and differentiate between them, a measurement-based investigation is executed, see Sec. 5.1. Here, it is shown that the V_{th} behavior strongly depends on the applied voltages as well as their duration. Starting from transient measurements, the impact of V_{DS} and V_{GS} can be translated into DC characteristics that resemble the V_{th} behavior.

The V_{th} behavior can eventually affect the reliability of DUTs. In order to verify this, the short-circuit (SC) withstand capability is investigated in Sec. 5.2.1, which is found to be affected by the same V_{DS} and V_{GS} conditions that also cause a V_{th} shift or instability. Furthermore, repetitive SC measurements show that the V_{th} shift can be correlated to device degradation and eventually be used as a health monitoring indication, as shown in Sec. 5.2.2.

5.1 Measurement Results

In order to differentiate between a V_{th} shift and a V_{th} instability, transient measurements are carried out showing their impact in the time domain, see Sec. 5.1.1. After this, in Sec. 5.1.2, the DC characteristics are acquired, showcasing the impact of V_{th} for operation up to nominal conditions. Subsequently, using the DC characteristics as well as the findings of the transient measurements, the behavior can be separated into V_{th} shifts shown in Sec. 5.1.3 and V_{th} instabilities in Sec. 5.1.4.

5.1.1 Transient Behavior

Applying either V_{DS} or V_{GS} on the DUTs can result in an unexpected change of the transient behavior. In order to acquire the transient behavior, the devices are investigated in the time domain utilizing single pulse measurements (cf. Sec. 4.3). Thereby, each measurement pulse allows for a specified *neutralization* and *biasing*

during the off-state prior to each *measurement* (cf. Fig. 4.9). This results in transient changes in the on-state state behavior that can persist for very long durations of up to 100 s after a turn-on. Consequently, equally long off-state durations are necessary to investigate the transient behavior. For this purpose, the transient measurements are done utilizing the approach of three consecutive pulses with increasing durations (cf. Fig. 4.5). Note that to acquire matching waveforms during consecutive pulses (pulse train), an off-state duration between each pulse of 100 s is needed.

In Fig. 5.1, the transient drain current I_D waveforms of both DUTs are shown. Here, the impact of different V_{DS} biasing conditions are compared at a fixed V_{GS} close to the threshold (cf. Tab. 4.1). The hard switching fault (HSF) condition resembles a switching condition where V_{DS} is applied prior to V_{GS} or rather during the off-state ($V_{GS} = 0\,V$) of the DUT. On the other hand, the fault under load (FUL) condition corresponds to a turn-on condition where V_{DS} is applied simultaneously to V_{GS} or rather during the on-state ($V_{GS} \geq V_{th}$). Note that the amplitude and duration of I_D ranges over several decades, so both axes are plotted in a logarithmic scale.

Looking at the results of the ohmic-gate DUT in Fig. 5.1(a), a difference in the initial value of I_D can be observed while comparing FUL with HSF. This difference tends to converge over a on-state duration of 100 ms, considering it as an instability (a transient change) of I_D. Compared to FUL, a HSF results in a negative I_D insta-

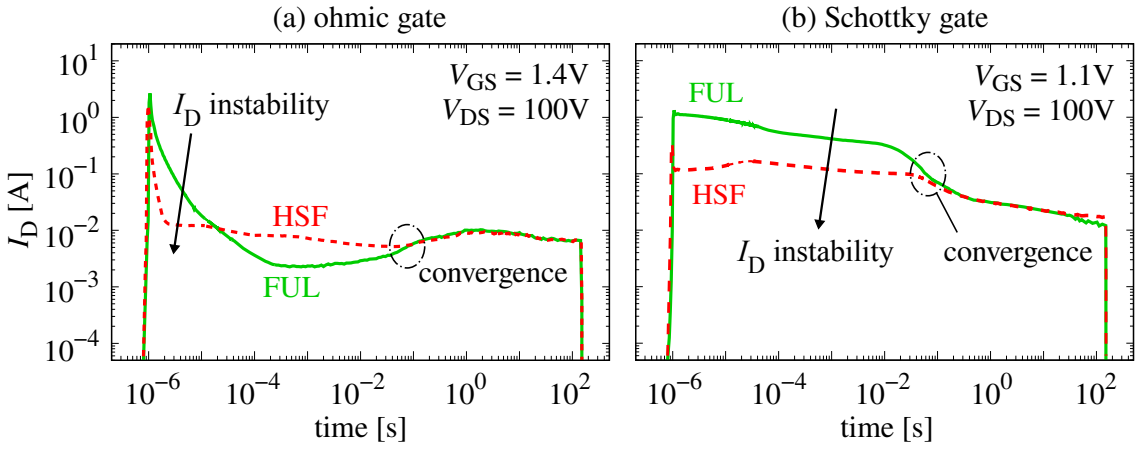

Figure 5.1: Transient drain current of the (a) ohmic-gate and (b) Schottky-gate DUT for high V_{DS} of 100 V and low V_{GS} (close to V_{th}). Here, comparing V_{DS} that is either applied only during on-state (FUL) or already at off-state (HSF).

bility that persists for about 10 µs, which then becomes positive until it converges. On the other hand, looking at the Schottky-gate DUT in Fig. 5.1(b), a negative I_D instability is observable too. However, the initial difference is much higher and persists more notably until the convergence occurs at about 100 ms.

Apart from applying V_{DS} during the on-state (FUL) or already during the off-state (HSF), its actual value does strongly impact the transient I_D waveform, as depicted in Fig. 5.2. Here, different V_{DS} of 10 V, 20 V and 100 V are utilized to measure the transient I_D, while V_{GS} is once again constant. In case of both DUTs, a constant positive I_D shift can be observed without indicating a possible convergence. The results of the ohmic-gate DUT are shown in Fig. 5.2(a), whereby an I_D shift of about one decade can be observed. On the other hand, for the Schottky-gate DUT in Fig. 5.2(b), the I_D shift ranges up to three decades in value. Note that for both DUTs, only the results of off-state V_{DS} (HSF) are shown. However, apart from a difference in the initial value, the results of on-state V_{DS} (FUL) behave similarly. Furthermore, the I_D shifts are found to be a reversible phenomenon.

Summarizing the results, the V_{DS} applied during the on-state results in a static shift of I_D. Additionally, the V_{DS} applied during the off-state yields a superimposed I_D instability. As demonstrated in Sec. 5.1.2, the change of I_D is based on the behavior of V_{th} and consequently to a V_{th} shift and instability. The V_{th} shift (cf. Sec. 3.2) is caused by capacitive coupling of the applied V_{DS} into the gate stack,

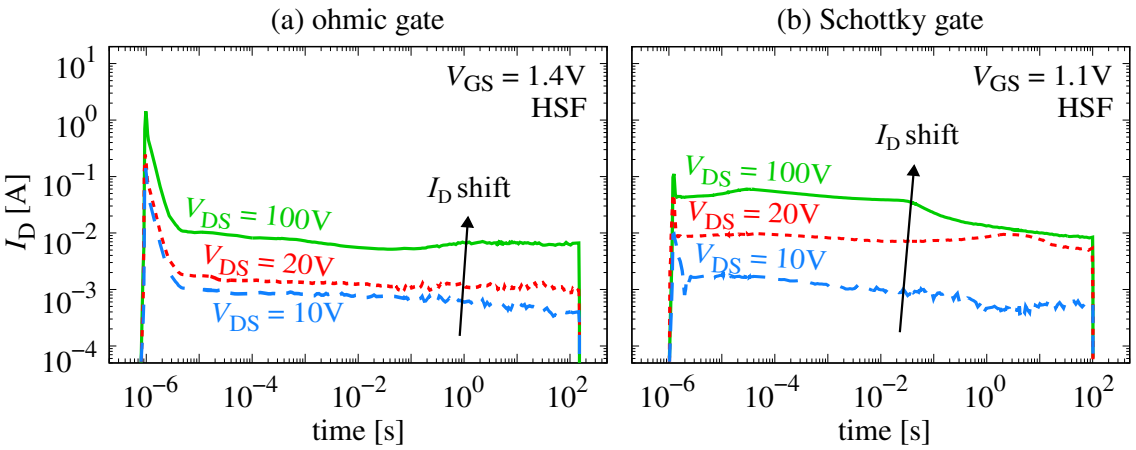

Figure 5.2: Transient drain current of the (a) ohmic-gate and (b) Schottky-gate DUT for low V_{GS} (close to V_{th}), comparing the impact of different V_{DS} values.

resulting in a potential elevation with subsequent gate barrier lowering. Hence an increase of the 2DEG occurs, requiring less V_{GS} for the turn-on. Apart from that, the V_{th} instability is caused by carrier accumulation and trapping mechanisms that can occur in various locations. The essential location is within the gate-stack region (cf. Sec. 3.3) but can also be distributed around the passivization and buffer layer similarly to current collapse (cf. Sec. 3.1).

In addition to V_{DS}, the applied V_{GS} also significantly impacts the transient behavior of p-gate GaN HEMTs. However, compared to V_{DS}, the investigation of V_{GS} can more or less only be done by applying the biasing conditions prior to the measurement or rather during the off-state ($V_{DS} = 0\,V$). For this purpose, distinctive conditions that can be considered relevant for an operation in a PE application are used (cf. Tab. 4.2). Essentially, these conditions are a turn-on *overshoot*, the excessive *OFF-state*, as well as a *reference* without any gate bias for comparison.

The impact of the various gate-driving conditions on the transient I_D is shown in Fig. 5.3. Here, both devices are measured with a low V_{GS} during on-state, while V_{DS} is only applied during on-state (FUL), in order to prevent an unnecessary V_{DS}-induced V_{th} instability. Furthermore, a V_{DS} of 100 V is used to ensure a saturation of the V_{DS}-induced V_{th} shift, as verified in Sec. 5.1.3. A I_D instability related to the applied gate-driving conditions (off-state V_{GS}) can be observed. Here, the V_{GS}-induced instabilities converge within a duration of 1 s.

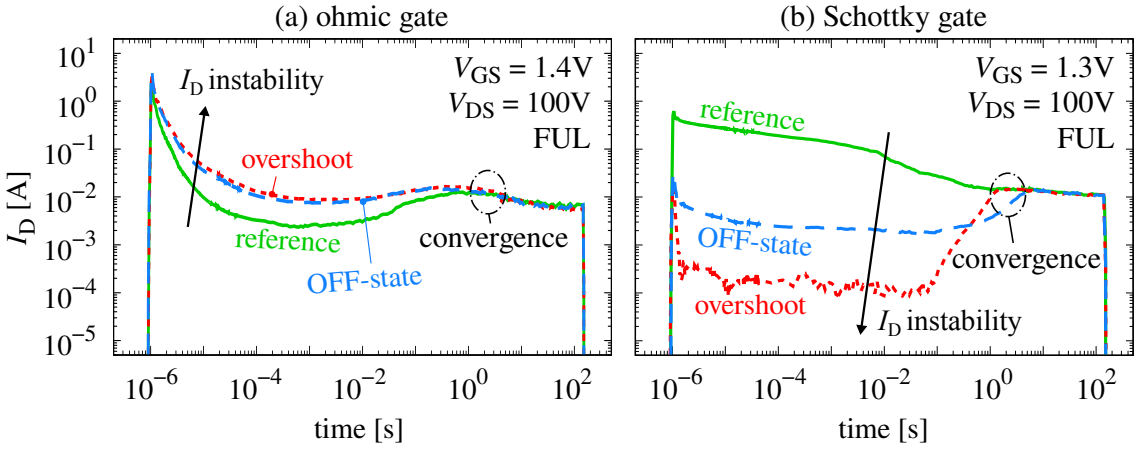

Figure 5.3: Transient I_D for applying $V_{DS} = 100\,V$ only during on-state (FUL) at a low V_{GS}, comparing the impact of different V_{GS} biasing conditions (cf. Tab. 4.2).

For the ohmic-gate DUT, a positive I_D instability is present, whereby the *OFF-state* condition appears to have the biggest impact, as shown in Fig. 5.3(a). On the other hand, a negative I_D instability occurs for the Schottky-gate DUT shown in Fig. 5.3(b), with the *overshoot* resulting in a tremendous I_D reduction. Ultimately, the impact on the Schottky-gate DUT is more prominent compared to the ohmic-gate DUT, which is similarly observed for the V_{DS}-induced behavior.

The impact of the gate-driving conditions on the transient I_D is once more shown in Fig. 5.4, but now for increased on-state values of V_{GS}. Here, for comparison, the nominal V_{GS} recommended by the manufacturer (cf. Tab. 4.1) as well as a lower value leading to roughly the half I_D amplitude are applied on the DUTs. Apart from that, V_{DS} is once again applied only during the on-state (FUL), though with a lower value of 10 V to reduce the impact of self-heating (cf. Sec. 4.4). Note that the emergence of an increased power dissipation is inevitable. Thus, the on-state duration (pulse length) is significantly reduced, preventing a thermal failure while still being long enough to record an eventual convergence.

Both the ohmic-gate DUT in Fig. 5.4(a) as well as the Schottky-gate DUT in Fig. 5.4(b) show that the V_{GS}-induced I_D instabilities appear to be observable and thus relevant up to high (nominal) currents. Although the extent is reduced at high currents, the I_D instabilities remain positive for the ohmic-gate DUT and negative for the Schottky-gate DUT. Besides this, operating the Schottky-gate DUT below

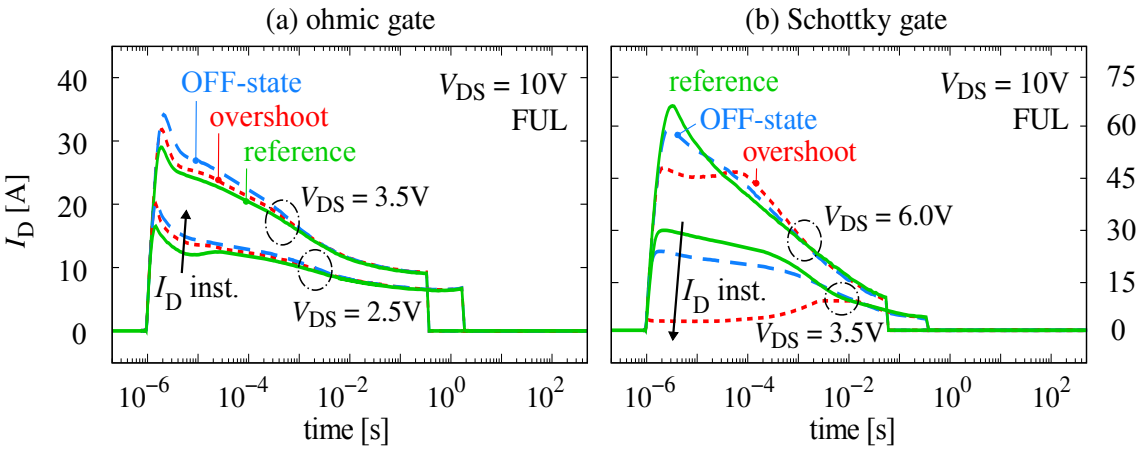

Figure 5.4: Transient I_D for applying $V_{DS} = 100$ V only during on-state (FUL), comparing different gate biasing conditions (cf. Tab. 4.2) at increased V_{GS} values.

the nominal V_{GS} together with a gate *overshoot* can result in the device almost remaining in off-state for a long duration. Furthermore, a remarkable observation is that the duration for convergence tends to reduce for increased V_{GS}. Compared to the low V_{GS} operation (cf. Fig. 5.3) the duration reduces to 1 ms at nominal V_{GS}.

In the end, the applied V_{GS} can eventually lead to an instability of I_D. The instability is based on mechanisms of carrier accumulation and trapping in the gate stack (cf. Sec. 3.3) which subsequently impact the 2DEG below the gate. These mechanisms are functions of the applied voltage and thermal stress, whereby an increase of the carrier density in the 2DEG results in a lifetime reduction of accumulated or trapped charge. Consequently, this shifts the convergence to earlier points in time for increased V_{GS}, which applies to both DUTs. At nominal V_{GS} the convergence occurs after about 1 ms, while for a V_{GS} close to the threshold it can take up to 100 s. Hence, a off-state duration (*neutralization*) of 100 s is mandatory prior to each measurement investigating the V_{th} behavior.

5.1.2 DC Characteristics

For an extended outline of the transient I_D behavior, the time-domain measurements are subsequently translated into DC characteristics. Compared to the transient investigation, only short on-state duration of 10 µs are used. However, this appears to be sufficient capturing the impact of the long-lasting instabilities that can persist between 1 ms to 100 s while also reducing the impact of self-heating (cf. Sec. 4.4).

Nonetheless, even with short on-state durations, self-heating is inevitable for an operation at increased currents and voltages. To circumvent this, a temperature model determines the transient temperature increase and the accompanying current change (cf. Fig. 4.13). Subsequently, this can be deducted from the I_D development over time, hence estimating DC characteristics that can be considered independent of the arising internal heating while measuring the DUTs (cf. Fig. 4.14).

In Fig. 5.5, the DC output characteristics are depicted, comparing the impact of the gate-driving conditions. Here, the same on-state V_{GS} values are used as for the transient behavior (cf. Fig. 5.4). Again, all measurements are acquired using on-state V_{DS} (FUL) preventing possible V_{DS}-induced instabilities. Looking at the results, for operations below V_{DS} saturation, only a minor deviation of the on-resistance $R_{DS,on}$

can be observed. This indicates that the gate bias conditions are not likely to trigger the same trapping mechanisms that cause a dynamic $R_{\mathrm{DS,on}}$ (cf. Sec. 3.1). In contrast, above the V_{DS} saturation, a noticeable shift of I_{D} is present, which resembles a static phenomenon. However, this is identified as an I_{D} instability due to the convergence behavior observed by transient measurements (cf. Fig. 5.4).

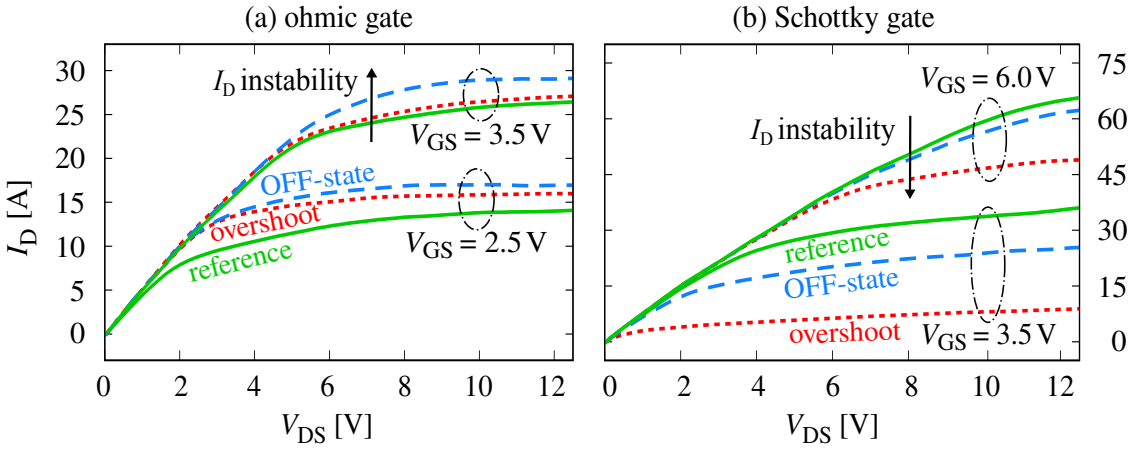

Figure 5.5: Output characteristics acquired by single pulse measurements, comparing the impact of the gate biasing (cf. Tab. 4.2) only using on-state V_{DS} (FUL).

The duration and magnitude of the I_{D} instabilities appear to be strongly related to the applied V_{GS}. Further evaluating this correlation, the DC transfer characteristics are investigated in Fig. 5.6. Since the I_{D} instabilities only appear for operation at V_{DS} saturation, the characteristics are acquired at 10 V. Although the saturation of both DUTs occurs at different voltages (cf. Fig. 5.5), the same V_{DS} is used to maintain comparability. Furthermore, the measurement of the ohmic-gate DUT is limited to $V_{\mathrm{GS}} \leq 6\,\mathrm{V}$. Above that, a very large gate current I_{G} occurs in the gate stack, which can disrupt the measurement and eventually lead to destruction. This is not the case for the Schottky-gate DUT due to its much higher Schottky barrier (cf. Sec. 2.4.3) limiting the emergence of I_{G}.

For operation above the threshold with $V_{\mathrm{GS}} \geq V_{\mathrm{th}}$, a shift of the transfer characteristics is observable related to the different gate bias conditions. Again, this shift can be associated with the transient behavior and therefore determined as a V_{GS}-induced I_{D} instability. For the ohmic-gate DUT shown in Fig. 5.6(a), a positive I_{D} instability occurs that is most pronounced for the *OFF-state* gate bias condition.

Additionally, the impact of the *OFF-state* appears to accelerate for increased V_{GS} but eventually saturates at $V_{GS} \geq 5\,V$. On the other hand, the Schottky-gate DUT in Fig. 5.6(b) does show a much more apparent shift, moving the characteristics towards higher V_{GS} values. This shift results in a decrease of I_D that ultimately can be determined as a negative I_D instability. Thereby, driving the gate with a gate *overshoot* condition appears to have the most significant impact.

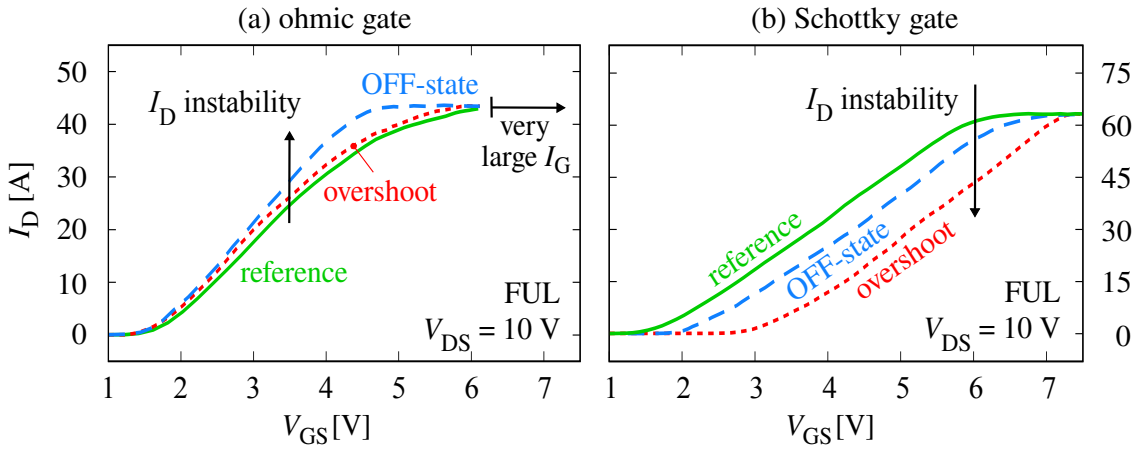

Figure 5.6: Transfer characteristics acquired by single pulse measurements, comparing the impact of the gate biasing conditions (cf. Tab. 4.2). The ohmic-gate DUT measurement is limited to $V_{GS} \leq 6\,V$. Again, only using on-state V_{DS} (FUL).

In summary, applying different gate-driving conditions for operation above V_{DS} saturation can yield a shift of the DC characteristics. This shift results from the transient behavior and is defined as an I_D instability. Furthermore, the observed instabilities appear relevant for voltages up to the nominal V_{GS} operation. Finally, the impact on the ohmic-gate DUT is much lower increasing from 25 A up to 30 A, while for the Schottky-gate DUT it decreases from 60 A down to 40 A.

5.1.3 Threshold Voltage Shift

The findings of the DC characteristics show that the behavior of I_D strongly depends on the voltages applied prior to or during the on-state of the DUTs. Thereby, the I_D instability can be observed for operation above the threshold $V_{GS} \geq V_{th}$ whilst V_{DS} saturation (cf. Fig. 5.6). However, investigating V_{th}, it is mandatory to

examine the region below the threshold (subthreshold) to obtain profound insights. In turn, accurately measuring currents in the subthreshold region is fairly complex due to the exponential behavior of I_D concerning V_{GS}. Typically, this is done using semiconductor device analyzers or a SMUs, which are both capable of accurate measurements ranging from 1 A down to 100 nA (cf. Sec. 4.2.2).

A large part of the initial work of this study is based on measurements using a SMU, although this limits the maximum applicable V_{DS} to 100 V with minimum on-state durations of 1 ms. In order to overcome this, fast high voltage measurements are acquired using the HBS (cf. Sec. 4.2.1), which offers short duration pulses below 10 µs with voltages up to 600 V. On the downside, the current resolution utilizing the HBS is only about 1 mA and thus more inaccurate in comparison to the SMU.

In Fig. 5.7, the transfer characteristics of both DUTs are depicted, illustrating the subthreshold region for applying different V_{DS}. These results are acquired using the HBS and are plotted in a semi-logarithmic scale. Here, a negative shift of the transfer characteristics can be observed for increasing values of V_{DS}, in case of both DUTs. As mentioned in Sec. 4.3, assuming V_{th} to be defined as V_{GS} for $I_D = 10$ mA, the shift of the characteristics can be correlated to a shift of V_{th}. In conclusion, the static I_D shift observed in the transient measurements for different V_{DS} (cf. Fig. 5.2) originates from a static shift of V_{th}. Note that the temperature increase for $I_D \leq 100$ mA, determined by the thermal model, is below 1 K and thus negligible.

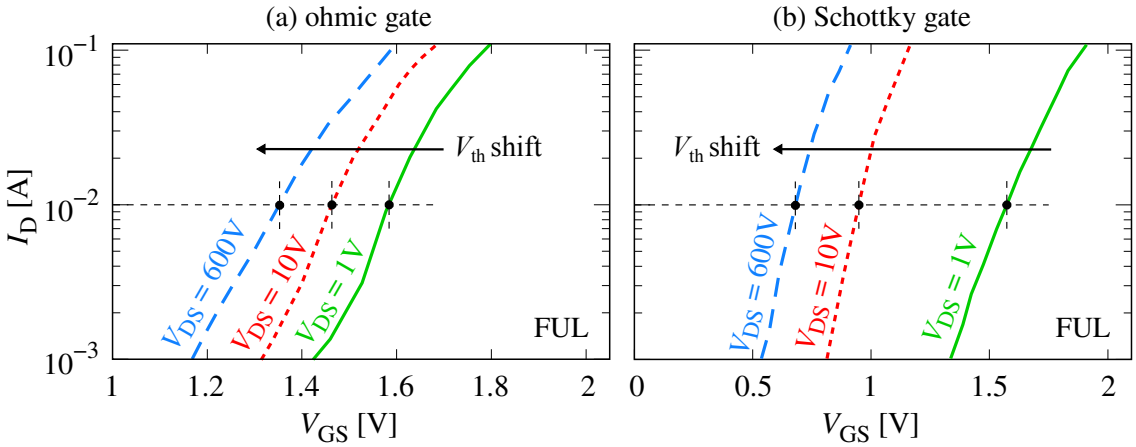

Figure 5.7: Transfer characteristics of the subthreshold region, comparing the impact of different V_{DS} in a semi-logarithmic scale. Here, only on-state V_{DS} (FUL) is used.

The V_{th} shifts of both DUTs for V_{DS} ranging from 1 V up to 600 V are shown in Fig. 5.8. The impact of different on-state durations used for measurement (cf. Fig. 4.9) are compared. For the ohmic-gate DUT a negative V_{th} shift occurs for V_{DS} ranging from 1 V to about 100 V, see Fig. 5.8(a). Above that, the V_{th} shift appears to saturate and only tends to slightly reduce above 500 V. Anyway, the observed negative V_{th} shift can vary between 200 mV and 400 mV depending on the measurement duration. To narrow this down, the DUT might not be fully turned on with on-state durations below 1 µs, whereas above 10 µs no further change is observed investigating the impact of V_{DS}. In case of the Schottky-gate DUT the negative V_{th} shift is about 700 mV and occurs for a V_{DS} between 1 V to 50 V, as shown in Fig. 5.8(b). However, above that, the V_{th} shift saturates too, while the on-state duration appears only to have a minor impact.

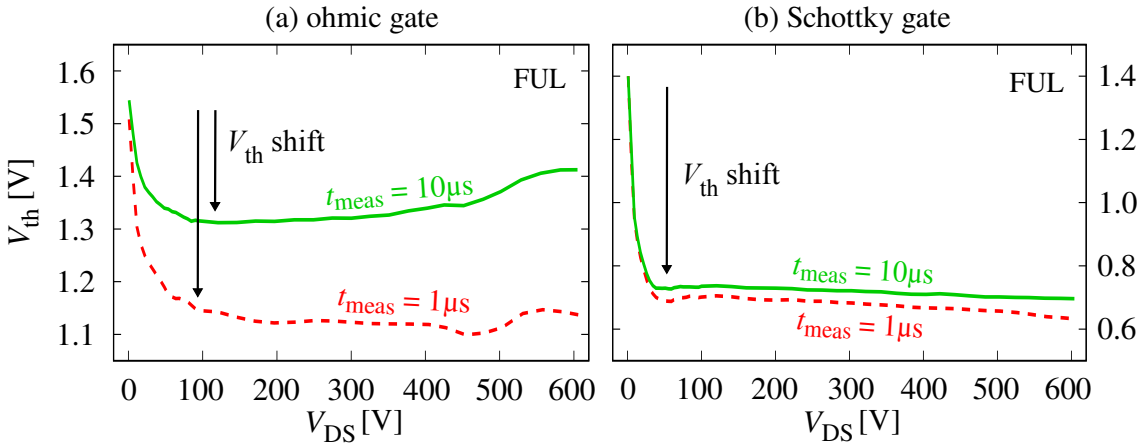

Figure 5.8: Threshold voltage V_{th} of the (a) ohmic-gate and (b) Schottky-gate device, comparing different measurement/on-state durations (cf. t_{meas} in Fig. 4.9).

The slight reduction of the V_{th} shift observed for the ohmic-gate device could be explained by an additional hole injection caused by the hybrid-drain structure (cf. Fig. 3.5), which is only part of the ohmic-gate DUT. The additional holes can appear for voltages above 500 V [14] and move along the 2DEG, where they can be injected through the AlGaN barrier into the floating p-GaN and thus the space-charge region (SCR) capacitances. Here, the additional holes counteract the drift-induced depletion, which shortens the width of the SCR. Since the SCR widening corresponds to the V_{th} shift, the shortening results in a V_{th} shift weakening.

In conclusion, applying increased V_{DS} can result in a static negative V_{th} shift. As explained in Sec. 3.2, this V_{th} shift can be explained by a V_{DS}-induced lowering of the Schottky barrier in the gate stack [19]. A high V_{DS} yields a potential elevation in the p-GaN region and subsequently in the 2DEG. This results in an increase of carriers below the gate stack, whereby less V_{GS} is needed for turn-on, thus, yielding a reduction of V_{th}. The difference between both DUTs can be explained by the more ohmic-like behavior of the ohmic-gate DUT, which tends to alleviate the impact of increased V_{DS}. Furthermore, the observed V_{th} saturation is likely caused by the clamping or weakening of the Schottky barrier. Apart from that, a weakening of the V_{th} shift is identified, which appears to correlate with the injection of holes from a hybrid-drain structure that is only present for the ohmic-gate DUT.

5.1.4 Threshold Voltage Instability

The transient and DC measurements show that V_{DS} applied during on-state can couple into the gate stack capacitances, resulting in a static negative V_{th} shift. However, not only the on-state V_{DS} is relevant. The transient measurements show that the off-state V_{DS} yield an additional I_D instability (cf. Fig. 5.1).

In Fig. 5.9, the V_{th} behaviors of both DUTs are shown, comparing the impact of a V_{DS} that is only during on-state (FUL) with one that is already applied during off-state (HSF). For voltages above $V_{DS} = 50\,\text{V} - 100\,\text{V}$ the V_{th} behavior for HSF appears

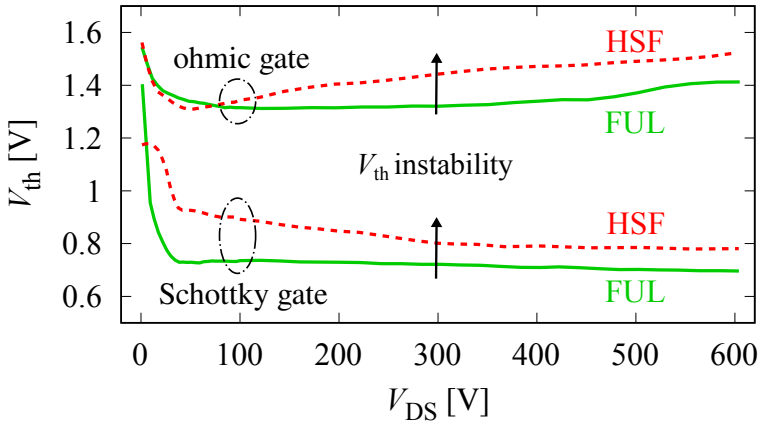

Figure 5.9: Threshold voltage V_{th} of both DUTs, comparing the impact of on-state V_{DS} without (FUL) and with (HSF) additional off-state V_{DS}, for $t_{meas} = 10\,\mu\text{s}$.

to shift above FUL by about 100 mV which remains until 600 V. However, looking at transient measurements (cf. Fig. 5.1), the difference between both conditions is an I_D instability. Consequently, the observed shift of HSF is caused by a V_{th} instability. Hence, applying V_{DS} during the off-state results in a positive V_{th} instability, which superimposes the negative V_{th} shift that occurs for on-state V_{DS}. Note that the measurements are done with on-state durations of 10 µs. Although the Schottky-gate DUT is mainly unaffected, smaller durations result in larger differences between FUL and HSF for the ohmic-gate DUT due to the initial I_D peak.

Correlation of the drain- and gate-driving conditions

Apart from the off-state V_{DS}, investigating the transient behavior with different V_{GS} conditions (cf. Tab. 4.2) does also show an instability of I_D (cf. Fig. 5.3). Furthermore, these V_{GS} conditions remain relevant even up to the nominal operation (cf. Fig. 5.4). In order to distinguish the impact of the V_{GS} conditions from the off-state V_{DS} ones, the following investigation is done solely by applying on-state V_{DS}. Additionally, as for the V_{th} shift (cf. Sec. 5.1.3), the HBS is used for the acquisition offering short-duration and high-voltage measurements

In Fig. 5.10, the transfer characteristics of both DUTs are depicted, comparing the impact of the V_{GS} conditions of the subthreshold region in a semi-logarithmic

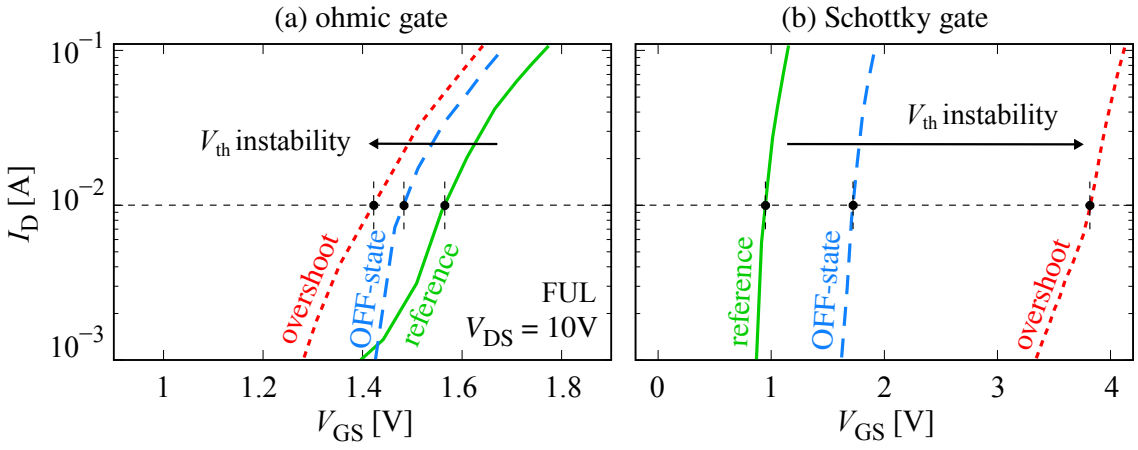

Figure 5.10: Transfer characteristics of the subthreshold region, comparing the impact of different gate-driving conditions (Tab. 4.2) in a semi-logarithmic scale. Here, only on-state V_{DS} (FUL) with a low value of 10 V is used.

scale. Here, a V_{DS} of 10 V is used, resulting in an operation at V_{DS} saturation that is still below the saturation of the V_{th} shift. For the ohmic-gate DUT in Fig. 5.10(a) a shift of the transfer curves is observable, which translates into a negative shift of V_{th}, again assuming it to be defined as V_{GS} for $I_D = 10\,mA$. Considering the convergence over time observed in the transient measurements (cf. Fig. 5.3), the shift of the curves can be assigned to a V_{th} instability. Note that the overlap of the *reference* and *OFF-state* condition is likely to be caused by measurement inaccuracy since it does not appear for the SMU-based acquisition (cf. Sec. 4.2.2).

For the Schottky-gate DUT in Fig. 5.10(b), a similar but positive shift of the transfer curves occur, which accordingly translates into a V_{th} instability. In turn, compared to the *reference* and ohmic-gate DUT, a minor tilt of the *overshoot* condition is observable. However, at $V_{DS} = 10\,V$ the tilt is virtually negligible.

In Fig. 5.11, similar transfer characteristics are shown, but now applying a much higher V_{DS} of 100 V. Both DUTs are investigated for an operation in V_{DS} and V_{th} saturation. For the ohmic-gate DUT in Fig. 5.11(a) all curves remain relatively equal compared to the 10 V measurement, but slightly displaced towards smaller values due to the V_{th} shift induced by the higher V_{DS} (cf. Fig. 5.7). This can similarly be observed for the Schottky-gate DUT, though the tilt of the *overshoot* condition becomes much more significant, see Fig. 5.11(b). Thereby, a crossover of the transfer curves occurs, which ultimately can result in an inconclusive evaluation. For exam-

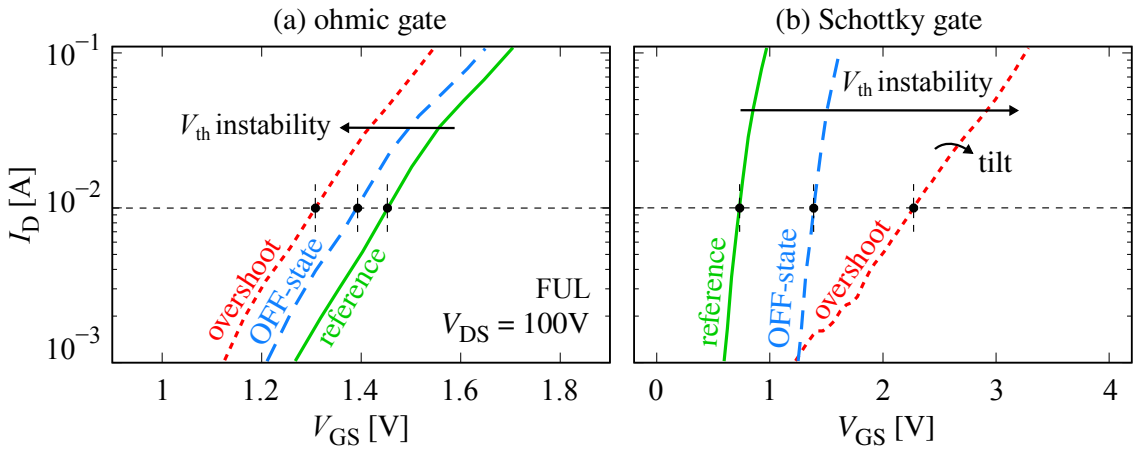

Figure 5.11: Transfer characteristics of the subthreshold region, comparing different gate-driving conditions (Tab. 4.2) for an on-state V_{DS} (FUL) with a value of 100 V.

ple, evaluating V_{th} at $I_D = 1\,mA$ could result in the assumption that the *overshoot* condition doubles V_{th}, while at 30 mA it is almost four times as much.

The behavior of V_{th} depends on the applied V_{DS} and V_{GS}, which at the same time appear to correlate with each other. In order to further investigate this correlation, the V_{th} behavior for the different V_{GS} conditions are shown in Fig. 5.12 varying V_{DS} from 1 V up to 600 V. Note that, the shown *reference* curves are the results of the V_{th} shift investigation (cf. Fig. 5.9) using a on-state duration of 10 µs. However, looking at the impact of the gate conditions on both DUTs, the V_{GS}-induced V_{th} instabilities appears to superimpose the V_{DS}-induced V_{th} shifts.

In case of the ohmic-gate DUT in Fig. 5.12(a) the negative V_{th} instability superimposes the already negative V_{th} shift, which for the *overshoot* condition results in a summarized V_{th} reduction of up to 300 mV. However, the correlation of V_{DS} and V_{GS} appears to be unsteady. For operations above the V_{th} saturation ($V_{DS} \geq 100\,V$), the V_{th} instability tends to follow the shift, whereas below, it is slightly different.

A similar behavior can be observed for the Schottky-gate DUT in Fig. 5.12(b), at which the positive V_{th} instability raises the negative V_{th} shift. Here, the impact of the *overshoot* condition is most significant and results in a summarized V_{th} increase of up to 2.9 V. Furthermore, the impact of the V_{th} instability appears to be much more significant below the V_{th} saturation. This behavior is likely to be caused by the tilt of the *overshoot* condition observable in the transfer characteristics (cf. Fig. 5.11).

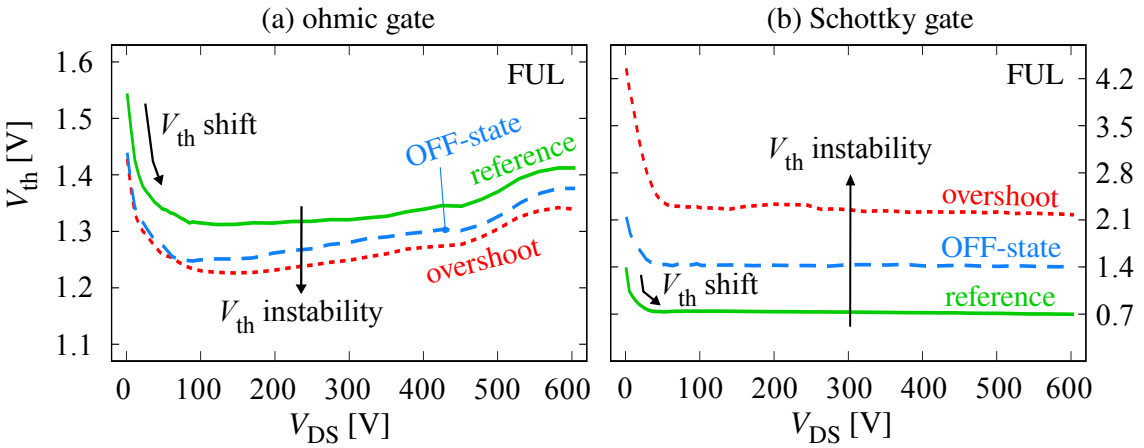

Figure 5.12: Behavior of the threshold voltage V_{th}, correlating the impact of the V_{DS}-induced V_{th} shift with the V_{GS}-induced V_{th} instability.

Consequently, extracting V_{th} at $I_{\mathrm{D}} = 1\,\mathrm{mA}$ would result in a reduction of the V_{th} instability to 2.2 V, while at 30 mA it would further increase to 3.25 V.

Impact of the gate-driving conditions on the ohmic-gate device

The most significant impact of the V_{GS} conditions is observable below the V_{th} saturation, especially for the Schottky-gate DUT. Although the V_{th} instability appears to reach its maximum for low V_{DS}, the DC characteristics show that it is mainly relevant above the V_{DS} saturation. Apart from that, the characteristics' tilt appears negligible at low V_{DS} (cf. Fig. 5.10). As a trade-off, the evaluation of the V_{GS}-induced V_{th} instabilities are done utilizing a V_{DS} of 10 V.

The V_{th} instability behavior of the ohmic-gate DUT is depicted in Fig. 5.13. Here, variations of the applied gate biasing voltage V_{bias} and duration t_{bias} (cf. Fig. 4.9) are used to obtain the behavior of the V_{GS}-induced V_{th} instabilities. The predefined V_{GS} conditions (cf. Tab. 4.2) are indicated for comparability. Note that the results of this investigation are acquired using the SMU (cf. Sec. 4.2.2) to ensure high accuracy. Apart from that, all presented results are acquired on a single DUT since the fabrication spread impacts the initial value of V_{th}. However, the measurements are verified with multiple DUTs, whereby the magnitude of the V_{th} instabilities remain relatively constant in case of both manufacturers.

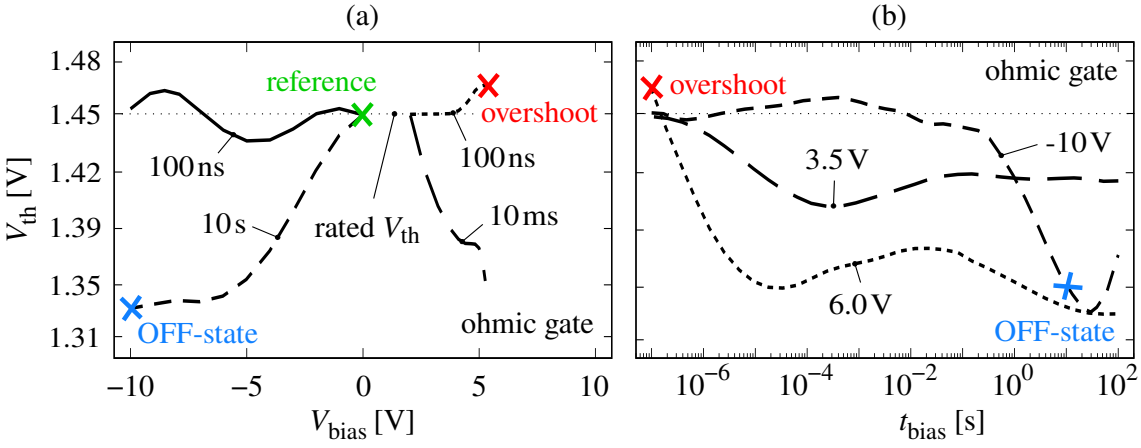

Figure 5.13: The V_{th} instability of the ohmic-gate DUT for (a) a variation of the bias voltage V_{bias} with constant t_{bias} and (b) vice versa, both acquired with $V_{\mathrm{DS}} = 10\,\mathrm{V}$. Note that a linear timescale is used in (a) and a semi-logarithmic timescale in (b).

First of all, applying and varying a negative V_{bias} with a very short duration of 100 ns does not show any significant impact on V_{th}, as shown in Fig. 5.13(a). On the other hand, with a very long duration of 10 s a linear reduction of V_{th} from 1.45 V down to 1.35 V can be observed which tends to saturate for V_{bias} above −5 V. Moreover, looking at the variation of t_{bias} for fixed a V_{bias} of −10 V in Fig. 5.13(b), V_{th} appears to remain constant and unaffected up to about 100 ms. Afterwards, the decrease from 1.45 V down to 1.35 V occurs which peaks at a t_{bias} of around 30 s resulting in a maximum negative V_{th} instability of approximately 100 mV.

This phenomenon could be explained by the injection of holes through the AlGaN barrier into the p-GaN region (cf. Fig. 3.10). Here, the additional holes fill up empty acceptor and trap states and move toward the Schottky barrier, where they accumulate. After the turn-on, the holes can not immediately leave the p-GaN region, temporarily increasing the effective gate charge, thus causing a negative V_{th} instability. On the other hand, increased negative V_{GS} can result in electrons from the p-GaN region to be trapped in the AlGaN barrier. The trapped electrons deplete the 2DEG, resulting in a positive V_{th} instability. Looking at the results in Fig. 5.13(a), the onset of electron trapping occurs for voltages above −5 V, while for the hole accumulation a duration of more than 100 ms is necessary.

Now, looking at the *overshoot* condition in Fig. 5.13(a), applying positive V_{bias} with a short duration of 100 ns can eventually result in a positive V_{th} instability. Since the observed increase is very small for the ohmic-gate DUT, it can be considered negligible. On the other hand, with long durations of 10 ms already low V_{bias} can lead to a noticeable negative V_{th} instability from 1.45 V down to 1.35 V. As can be seen in Fig. 5.13(b) a similar decrease of 100 mV can already be observed applying a high V_{bias} of 6 V with a much lower duration of 10 µs. Here, the negative V_{th} instability is observed to more or less saturate for increasing durations.

The negative V_{th} instability is similar to the reverse operation caused by hole injection through the gate stack (cf. Fig. 3.9). Here, holes flow through the p-GaN and eventually either accumulate at the AlGaN barrier or are trapped inside. Afterward, accumulated holes increase the effective gate charge in the p-GaN region, while the positive charge of the trapped holes attracts additional electrons into the 2DEG. Ultimately, both mechanisms cause a negative V_{th} instability that already appears for very short durations and increases until 10 µs.

Finally, in Fig. 5.13(b) the V_{th} behavior applying the nominal V_{GS} of 3.5 V for various durations is shown. Here, no impact can be observed for durations below 1 µs, while above a negative V_{th} instability occurs. Thereby, an increase up to 50 mV at 1 ms can be observed, while for durations above, the instability tends to saturate, too. The cause of that behavior is similar to applying higher V_{bias} and, although lower, still relevant at nominal V_{GS} operation.

Impact of the gate-driving conditions on the Schottky-gate device

In Fig. 5.14, similar measurements varying V_{bias} and t_{bias} are shown, but now for the Schottky-gate DUT. Looking at the variation of V_{bias} with short durations of 100 ns in Fig. 5.14(a), an V_{th} increase from 1.1 V to approximately 1.2 V occurs. Furthermore, for long durations of 10 s this can even increase to 1.5 V resulting in a positive V_{th} instability of 400 mV. As shown for a high negative V_{bias} of −10 V in Fig. 5.14(b), the V_{th} is already lifted at small durations but eventually increases at 100 ms similarly to the onset of the saturation in case of the ohmic-gate DUT.

Compared to the ohmic-gate DUT, the Schottky barrier of the Schottky-gate DUT is larger, shifting the onset of hole injection to much higher voltages. It is assumed that hole injection does not occur within the measurement range of the negative V_{bias}, meaning below −10 V. On the other hand, holes within the p-GaN

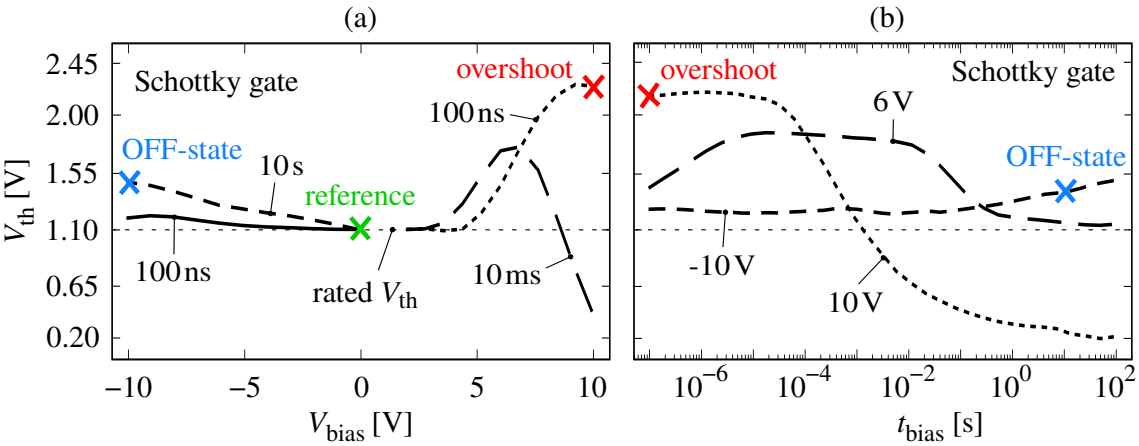

Figure 5.14: V_{th} for a sweep of the bias duration t_{bias}. The marked voltages demonstrate the applied V_{bias}. Note the different timescales for V_{th} in both subplots.

region can be removed from acceptor or trap states which subsequently accumulate at the Schottky barrier. Then, the depletion of holes from the p-GaN reduces the effective gate charge, which does not immediately reset after turn-on due to the very low gate current. Thus, a positive V_{th} instability occurs that is not counteracted by additional hole injection, as it is the case for the ohmic-gate DUT. Apart from that, electron trapping occurs in the AlGaN barrier with an onset at around $-5\,\mathrm{V}$ similar to the ohmic-gate DUT. Furthermore, hole depletion and accumulation require about 100 ms, as the hole injection of the ohmic-gate DUT.

Apart from that, the *overshoot* condition of the Schottky-gate DUT depicted in Fig. 5.14(a) does show a tremendous V_{th} increase already at low duration of 100 ns, while applying a V_{bias} above 4 V. Here, an increase from 1.1 V to 2.3 V can be observed which results in a positive V_{th} instability of around 1.2 V. However, applying a high V_{bias} of 10 V with durations above 10 µs results in the positive V_{th} instability to decrease and ultimately becoming negative starting from 1 ms, as shown in Fig. 5.14(b). Thereby, V_{th} reaches its minimum of 0.2 V at 1 s, resulting in a negative V_{th} instability of 900 mV that remains constant for even higher durations. However, looking at the duration of 10 ms in Fig. 5.14(a), the negative V_{th} instability does not appear for voltages prior to 7 V, which is above the nominal V_{GS}.

Applying a positive voltage above 4 V causes electrons from the 2DEG to be trapped in the AlGaN barrier (cf. Fig. 3.8). This results in a deficiency and depletion of the 2DEG and ultimately a positive V_{th} instability. Apart from that, high V_{GS} can also cause the injection of holes into the gate stack. The injected holes either neutralize the electron deficiency by getting trapped in the AlGaN barrier or accumulate at the AlGaN barrier, causing an additional positive charge. However, both effects cause a temporal increase of the 2DEG and, therefore, a negative V_{th} instability. Looking at Fig. 5.14(a), the hole injection of the Schottky-gate DUT seems to appear slightly above the nominal V_{GS} at 7 V at increased durations. Compared to this, the hole injection of the ohmic-gate DUT already occurs at voltages below the nominal V_{GS} of 3.5 V, concealing electron trapping in the first place.

Lastly, in Fig. 5.13(b) the V_{th} behavior for nominal V_{GS} of 6 V is shown, varying the duration. Below 10 µs a linear V_{th} increase from 1.3 V up to 1.9 V is observable. Above this the positive V_{th} instability remains relatively constant until 10 ms, where it starts to diminish down to zero at about 300 ms. Again, the cause of that behavior

is similar to higher V_{bias}, but in case of the Schottky-gate DUT, much more relevant for the nominal V_{GS} operation.

In conclusion, applying a positive V_{GS} causes electron trapping and depletion, yielding a positive V_{th} instability. However, for increased durations and an operation at nominal V_{GS} can result in hole injection. These holes either neutralize trapped electrons, are trapped themselves, or accumulate within the gate stack, which consequently causes a negative V_{th} instability. On the other hand, a negative V_{GS} can result in electron trapping, which yields a positive V_{th} instability. As in forward operation, this can be neutralized by hole injection with subsequent accumulation and trapping. However, this strongly depends on the Schottky barrier and is only observed for the ohmic-gate DUT where it causes a negative V_{th} instability.

5.2 Relevance

The GaN HEMT is a promising candidate for future PEs applications, especially in the area of high-frequency operation. In order to realize high-frequency switching, improved gate-driving concepts need to be utilized, allowing maximum efficiency. Consequently, aside from the HEMT itself, a key factor is the development of suitable gate drivers. An emerging trend is to evolve from discrete drivers towards a monolithic integration alongside the power device. Nonetheless, whether discrete or integrated, the design and functionality of the driver are essential.

Traditional gate drivers typically use active switching stages such as CMOS in conjunction with a passive driver network. Still up in 2023, prominent GaN HEMT manufacturers recommend the usage of a passive RRC network in conjunction with their drivers [111, 112]. Besides this, more advanced approaches utilize active driving solutions such as switched sources or resistances [113] to further improve switching efficiency. However, both solutions could cause unexpected reliability concerns, considering the impact of particular switching conditions.

Two prominent switching conditions are the V_{GS} overshoot at the turn-on and a turn-on from a negative V_{GS} after a long off-state duration. As shown in Sec. 5.1.4, both the *overshoot* and *OFF-state* (cf. Tab. 4.2) show a significant impact on V_{th}. Since V_{th} is affected by the gate-driving conditions, it can be assumed that similar

conditions can impact robustness. In order to evaluate this, the short circuit robustness is investigated in Sec. 5.2.1 for different driving conditions. Furthermore, V_{th} could be utilized as a health monitoring indicator, see Sec. 5.2.2.

5.2.1 Short Circuit Robustness

For the investigation of the short circuit(SC) capability, the HBS (cf. Sec. 4.2.1) is used and extended by a SC detection and shutdown unit. The main functionality of the SC unit is to measure I_{D} and to decouple the DUT (by HS switch-off) above a certain current threshold avoiding setup destruction in case of failure as well as to prevent an explosion of the DUT itself. Here, the SC unit is set to trigger above 100 A, which, as soon as detected, results in a decoupling within about 1 µs.

In Fig. 5.15, the results of the SC investigation are shown, comparing the impact of the gate-driving conditions on the maximum withstand capability. The measurement is done in a consecutive manner starting from $V_{\mathrm{DS}} = 300\,\mathrm{V}$ which is gradually increased in steps of 10 V until a SC failure occurred. To investigate the SC capability, a SC duration of 10 µs is utilized, which is a standard benchmark for conventional devices (e.g., IGBTs). However, GaN HEMTs can withstand this duration for voltages up to 80% of their maximum voltage, depending on the gate

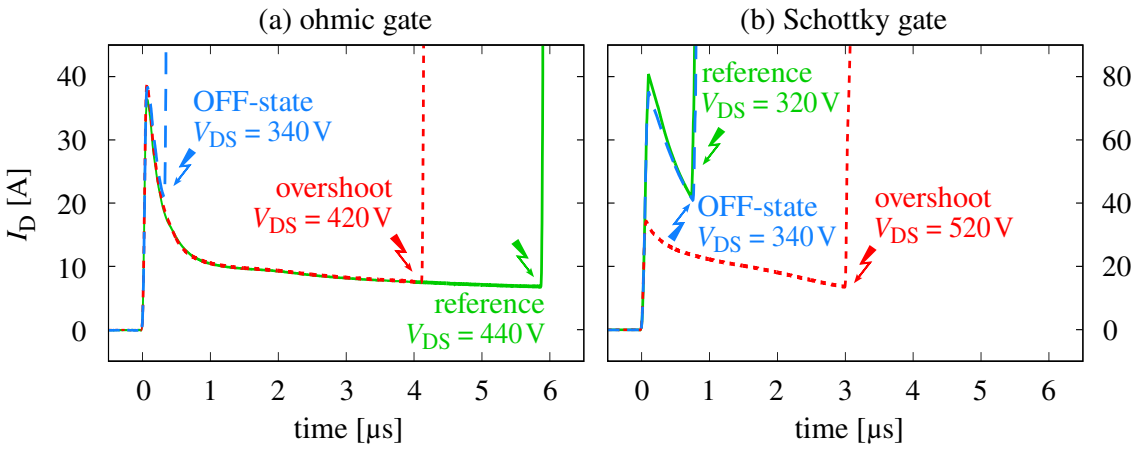

Figure 5.15: Short circuit current waveforms of both DUTs, comparing the impact of different gate-driving conditions (cf. Tab. 4.2) on the maximum withstand capability. The robustness is acquired at $V_{\mathrm{GS,nom}}$, applying V_{DS} only during on-state (FUL).

driving. In any case, after each non-destructive pulse, an off-state of 100 s is set for cooldown and *neutralization*. After this, V_{DS} is increased before triggering the subsequent measurement. Note that all SC measurements are done with the FUL condition (cf. Fig. 4.9) and by applying the nominal V_{GS} during the on-state.

Looking at the *reference* condition of the ohmic-gate DUT in Fig. 5.15(a), a failure occurs at 440 V which appears to be the maximum capability. Applying an *overshoot* can already affect the capability, which in case of the *OFF-state* condition results in a reduction of 100 V down to only 340 V. On the other hand, the *reference* condition of the Schottky-gate DUT in Fig. 5.15(b) appears to be the minimum capability with 320 V. Comparing this to the ohmic-gate DUT, the *reference* is already 120 V lower, but in turn tends to increase with the driving conditions. Utilizing a gate *overshoot* can result in a significant increase of up to 200 V, which raises the maximum capability to 520 V. Here, it should be noted that the initial I_{D} peak halves, resulting in a height comparable with the ohmic-gate DUT.

Applying the *OFF-state* condition on the ohmic-gate DUT results in a hole accumulation in the gate-stack which enhances the 2DEG, thus yielding a negative V_{th} instability (cf. Fig. 5.13). Assuming a homogeneous distributed 2DEG density below the gate stack, the electrical field peak induced by V_{DS} during on-state occurs on the drain-sided gate-edge [114]. Then, increasing V_{DS}, the electrical field will eventually hit the critical field strength of GaN (cf. Tab. 2.1). Consequently, an avalanche carrier generation occurs, resulting in an almost instantaneous breakdown. The field shape is steeper for an enhanced 2DEG, thus a reduced capability to withstand V_{DS}. Consequently, hole accumulation yields a negative V_{th} instability and reduces the SC capability. This does not occur in the Schottky gate because there is no hole injection (cf. Sec. 3.3.2).

Besides this, applying a gate *overshoot* causes electron trapping (cf. Fig. 5.14), which yields a positive V_{th} instability. Thereby, the 2DEG depletes and consequently increases the SC capability. However, this does not account for the ohmic gate since electron trapping is neutralized by hole injection.

Summarizing this, the configuration of a gate driver can result in *OFF-state* and gate *overshoot* conditions that eventually yield a V_{th} instability. The mechanisms leading to this alter the 2DEG below the gate stack, which impacts the capability to withstand high electrical fields. Consequently, the gate driver does not only cause

an unstable V_{th} but also significantly impact the SC capability. Thus, the driver design must be tailored to the utilization in a PE application.

5.2.2 Short Circuit Degradation

Apart from an instantaneous SC failure, repetitive stress with a reduced load can lead to degradation and subsequent destruction. Repetitive SC stress on the Schottky-gate DUT is shown to cause a I_{D} reduction depending on the number of pulses [115, 116]. Here, the behavior appears to be linked to a V_{th} shift in a positive direction that is accompanied by a reduction of the gate-leakage I_{G}. Apart from typical SC stress, a similar behavior is observed for repetitive reverse freewheeling stress, exposing a permanent increase of V_{th} and a decrease of I_{G} [20].

Since repetitive SC stress causes a degeneration accompanied by a positive V_{th} shift, it is very likely that the mechanisms causing V_{th} to shift alter too. In other words, if V_{th} could be accurately measured during operation, it would be possible to estimate the relative degradation and thus predict the device health. Furthermore, using V_{th} as a health indicator would allow for predictive maintenance of the GaN HEMTs used in PE applications and therefore reduce the overall downtime costs.

Investigating the impact of repetitive SC stress, the same setup configuration is used to evaluate the SC capability (cf. Sec. 5.2.1), but now with drastically reduced

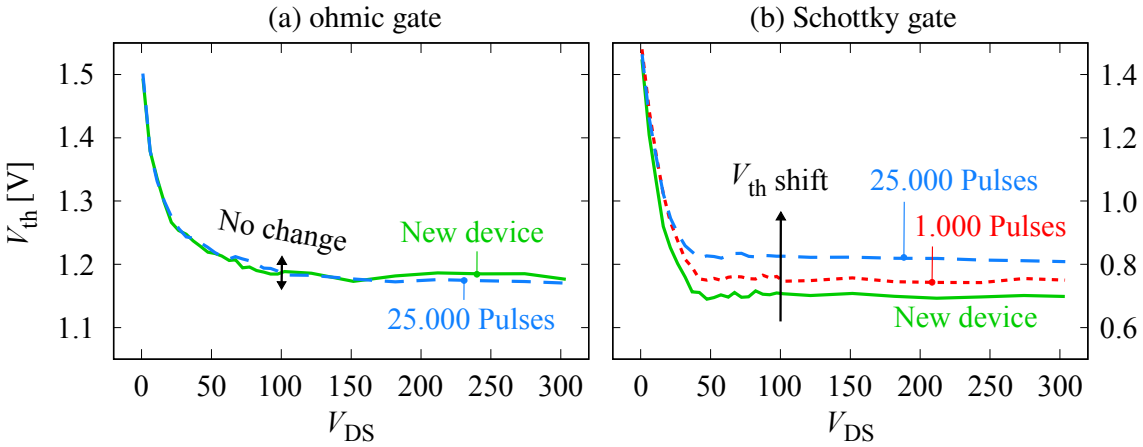

Figure 5.16: The behavior of V_{th} showing the impact of repetitive SC stress. In case of the Schottky-gate DUT, a permanent V_{th} increase is observable.

V_{DS} to prevent premature destruction. The repetitive SC stress for the ohmic-gate DUT is set to 250 V applied for 10 µs which results in a I_D peak of around 35 A. In turn, the Schottky-gate DUT already offers a around 100 V reduced SC capability, thus the V_{DS} stress is set to 150 V resulting in I_D peak of 70 A. The difference in I_D is based on the difference in nominal V_{GS}. Note that the investigation of both DUTs is based on the *reference* condition without any additional gate stress, while only on-state V_{DS} (FUL) is used preventing an unintentional V_{th} instability.

In Fig. 5.16, the impact of repetitive SC stress is shown on the behavior of V_{th}. Here, the repetitive cycles are structured around an initial health monitoring sequence followed by 1.000 stress pulses with 10 s off-state in-between for cooldown. As health monitoring indications, the transient, the DC transfer and output characteristics, and the V_{th} behavior are measured. Afterward, the stress pules are applied, and the whole cycle is repeated until a DUT failure occurs.

Looking at the results of the ohmic-gate DUT in Fig. 5.16(a), no impact on the V_{th} behavior can be observed. On the other hand, evaluating the transient measurements, a reduction of the initial I_D peak can be observable. Apart from that, no significant change in I_G or $R_{DS,on}$ occurs. In turn, for the Schottky-gate DUT in Fig. 5.16(b), a repetition of 1.000 pulses already results in a noticeable increase of V_{th}. Furthermore, this positive V_{th} shift tends to increase until 25.000 pulses, while above sudden DUT failure occurred. Similar to the ohmic-gate DUT, the I_D peak reduction is observable while I_G and $R_{DS,on}$ remain relatively unchanged.

Chapter 6

Compact Model

A large part of the power electronic development involves designing and testing new applications within a simulation tool prior to assembling the physical prototype. Thus, many critical conditions and interferences can be identified and counteracted already during the design process. In order to sufficiently identify these issues, it is mandatory to utilize accurate simulator models for each circuit component of the power electronic application to develop. For the vast majority of components such as passives or e.g. conventional Si-based MOSFETs, many precise models exist and can be utilized. However, in comparison, the GaN HEMT is a relatively new technology that involves a completely different operating principle.

In the early stages of development, conventional MOSFET models have been tailored to fit the functional behavior of GaN HEMT, which, however, are prone to mispredict HEMT-specific phenomena. In recent years, several GaN HEMT models have been developed that include many aspects of their unique operating principle, which helped to push their accuracy and predictability, as discussed in Sec. 6.1. However, until today, no unified HEMT model fully covers all operations and relevant effects. Furthermore, every manufacturer provides their own models, which are only to some extent comparable with the others. Finally, the undesired effect of the threshold voltage shift and instability are among the newer phenomena which are only partly covered and have yet to be included in available models.

To accurately predict the behavior of modern p-gate GaN HEMTs, it is necessary to develop a model including the threshold voltage V_{th} behavior. Since many of the available models are significantly different, developing a unified model that is scalable for various devices is mandatory. In order to tailor the unified model for a wide variety of available devices from different manufacturers, a parameter extraction strategy is developed. This strategy is integral to the model development and can create a fitting solely from datasheet information.

Many of the physical mechanisms causing the V_{th} behavior have already been identified (cf. Sec. 3.2 and Sec. 3.3), thus a physical-based approach is proposed and

assembled for the core model in Sec. 6.2. The vast majority of these mechanisms emerge within or at least interfere with the gate-stack region, which is why it appears as a vital point to include the V_{th} behavior. Here, the physical mechanisms that determine the current flow through the gate region are included and adjusted to cover both the functionality of the ohmic and Schottky gate in a single approach, see Sec. 6.3. The V_{th} shift is based on the capacitive coupling into the gate-stack (cf. Sec. 3.2), thus, the behavior of the parasitic capacitances in Sec. 6.4 are utilized as the foundation for the V_{th} shift model in Sec. 6.5. Finally, the V_{th} instability is included in Sec. 6.6 using time-depended functions for e.g., the trapping of states. Apart from that, many of the extensive physical equations are simplified, creating a compact model that is still accurate but fast in calculation.

Apart from that, the actual usage of such a model can typically take place in various simulation tools such as LTspice [117], SIMetrix [118], or Cadence [119]. However, every simulation tool usually uses its own model language and syntax, making it nearly impossible to maintain a cross-platform product. For this purpose, the model is developed in Verilog-A [120], which is considered a universal model language. The massive benefit of Verilog-A is that many simulators, such as Cadence can directly operate on it, while for LTspice, the code can be translated.

6.1 GaN Modeling

In literature, a large variety of GaN HEMTs model approaches can be found, which in turn can be categorized into four different types, as they are listed in Tab. 6.1. In terms of performance, these model types mainly differ in aspects of operational speed, output accuracy, and predictability. Here, the operational speed refers to the duration the simulation tool requires to load the model and to calculate the output. The output accuracy represents the qualitative match of simulation and measurement results in various operational conditions and characteristics. Predictability reflects the ability to adapt to changes in physical properties such as device scaling. This becomes particularly important when altering the current and voltage ratings of the model or even by adjusting to a new device generation.

The behavioral type model resembles an approach entirely built around equivalent circuits and non-physical mathematical functions. Typically, these models are high in speed since they only consist of a small number of equations without physical meaning, whereas they suffer in accuracy and predictability. These performances can be increased by adding or supplementing some physical equations, which leads to semi-physical models. Subsequently, building up the model foundation based on physical equations that describe the functional behavior of the material and technology itself results in physical-based type models. Typically, these physical equations are derived from differential equations and simplified to analytical equations, which are much faster to calculate. Finally, utilizing the differential equations itself results in numerical models, which are often quite complex and time-consuming to calculate, while on the other hand being the most accurate and predictable. However, aiming for an accurate model offering decent simulation speed, the physical-based approach is most suitable for creating a compact model that includes the V_{th} behavior.

Table 6.1: Overview of model approaches, comparing criteria of performance.

Type	Speed	Accuracy	Predictability
Behavioral	++	−−	−−
Semi-Physical	+	−	−
Physical-Based	−	+	+
Numerical	−−	++	++

The fundamental structure of behavioral, semi-physical, and physical-based models are usually equivalent circuit components using analytical equations, which is why they can be used in common simulation tools. Looking at the history, the first models that have been used or adapted for GaN HEMTs are the Curtice-Cubic GaAs FET model (CFET) [121] in 2004 and the EEsof scalable nonlinear HEMT model (EEHEMT) [122] in 2006. These are behavioral-type models set up from empirically determined equivalent circuits. While both consider the nonlinear electrical characteristics, the EEHEMT contains an additional thermal equivalent circuit.

An improvement in terms of behavioral models has been achieved with the introduction of the Angelov GaN FET model (Angelov-GaN) [123], which became one

of the first industrial standard compact models in 2013. Around the same time, the MIT Virtual Source GaN FET model (MVSG) [124] has been introduced, which initially was developed for Si-MOSFETs. Although developed for a different technology, it was quickly adapted for HEMTs by considering fundamental GaN-specific material properties and physical mechanisms. Finally, in 2018 the Advanced Spice Model for HEMTs (ASM-HEMT) [125] has been released, which is fundamentally set up as a physical GaN HEMT model based on the surface potential.

Table 6.2: Overview of the most relevant GaN HEMT models.

Name	Description	Release	Type
CFET	Curtice-cubic GaAs FET model	2004	Behavioral
EEHEMT	EEsof scalable nonlinear HEMT	2006	Behavioral
Angelov-GaN	Angelov GaN FET model	2013	Behavioral
MVSG	MIT Virtual Source GaN FET	2014	Semi-Physical
ASM-HEMT	Advanced Spice Model for HEMTs	2018	Physical-Based

6.2 Drain Model

The drain model is the center part of the developed compact model, which is assembled using the equations provided by the physically-based approach of the ASM-HEMT [125]. Many of the physical mechanisms of the V_{th} behavior are already identified (cf. Sec. 3.2 and Sec. 3.3), thus, they can be embedded into the drain model at a later stage. The drain model fundamentally calculates the surface potential, as described in Sec. 6.2.1. Here, the surface potential is used to determine the 2DEG carrier density in the AlGaN/GaN heterojunction by a closed-form analytical calculation of the Fermi-level E_{F}, which is valid in all regions of operation. Based on this, the sheet carrier density forming the 2DEG in the region below the gate stack can be determined based on the applied voltages V_{GS} and V_{DS}. The drain current I_{D} is calculated in Sec. 6.2.2 considering material-specific properties such as carrier mobility and velocity. Finally, the parameter extraction procedure of the drain model is showcased and verified in Sec. 6.2.3.

The drain model is illustrated in Fig. 6.1, indicating the components and locations within the device structure. Additionally to the HEMT model, which is based on the surface-potential approach, there are additional access and drift resistances R_G, R_D, and R_S to consider. Theoretically, R_D and R_S correspond to the 2DEG concentration of the drift regions, but these are simplified as resistances assuming that the 2DEG does not significantly change with V_{GS} in that region anyway. On the other hand, R_G depends on the doping concentration of the p-GaN region and is part of the gate model in Sec. 6.3. The resistances connect the internal HEMT model with the external nodes (g), (d), and (s). Consequently, the external nodes are considered as the input of the model, where applying the voltages V_{DS} and V_{GS} results in the calculation and flow of the currents I_D and I_G as the output.

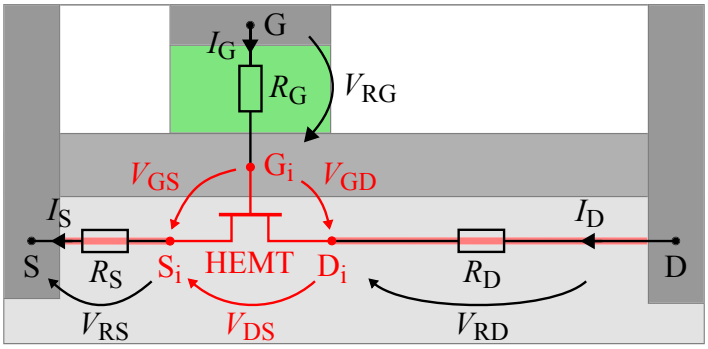

Figure 6.1: Simplified cross-section (cf. Fig. 2.8) showing structure of the drain model. The core part consists of the HEMT model, which is based on a surface-potential approach surrounded by the drift resistances R_G, R_D and R_S.

In order to accurately calculate the output current I_D in the HEMT model, the external potentials V_D and V_S applied on the input nodes D and S need to be translated into the internal voltage V_{DS}. However, internal voltages V_{DS} and V_{GS} appear to be dependent on the output current I_D itself, as they are defined as

$$\begin{aligned} V_{DS} &= (V_D - V_S) - V_{RD} - V_{RS} \\ \Rightarrow V_{DS} &= (V_D - V_S) - I_D \cdot (R_D + R_S) - I_G \cdot R_S \end{aligned} \tag{1}$$

and

$$\begin{aligned} V_{GS} &= (V_G - V_S) - V_{RG} - V_{RS} \\ \Rightarrow V_{GS} &= (V_G - V_S) - I_G \cdot (R_G + R_S) - I_D \cdot R_S. \end{aligned} \tag{2}$$

This issue might be difficult to solve or to simplify using typical interpreters such as Matlab [126], or Phyton [127]. Since these work in a sequential operating flow, creating a loop calculation would be required to find an iterative solution. On the other hand, the compiler of simulation tools such as LTspice [117], which translates and processes the model code, usually contains a built-in iterative solver.

6.2.1 Surface Potential

In a first attempt to generate a physical-based model for GaN HEMTs, the formation of the 2DEG sheet charge has been described as a function of the applied gate bias [128]. However, one of the major challenges in modeling the 2DEG derives from the complicated variation of the Fermi-level position E_{F} in the quantum well. Assuming a triangular-shaped well, a self-consistent solution of the Schroedinger's and Poisson's equations has been expressed by [129]. However, the solutions are transcendental equations and can not be solved analytically but require numerical solvers, resulting in an unsatisfactory operational speed for calculation.

To acquire a compact model, analytical equations of E_{F} have been developed, which are valid in all particular regions of operation [130]. Subsequently, these analytical equations are unified to a single closed-form equation of E_{F} that can be used to determine the resulting surface potential (SP). Here, the SP links the E_{F} to the respective location at which it is calculated e.g., at source- or drain-side of the HEMT structure. Finally, considering the current continuity and several real device effects such as mobility and velocity saturation, the unified SP can be utilized to calculate the drain current I_{D}. Note that the following SP and thus the drain model is largely obtained from [125]. A universal equation for the SP Φ_{SP} is given as

$$\Phi_{\mathrm{SP}} = E_{\mathrm{F,uni}} + V_{\mathrm{x}}, \tag{3}$$

where Φ_{SP} is defined by the unified $E_{\mathrm{F,uni}}$ and the voltage V_{x} at the point x at which they are calculated. For the calculation of I_{D}, the SP determination is split into two major sections. The first part considers the SP at the source-sided potential of the HEMT $\Phi_{\mathrm{SP,S}}$, along with the dependency of the gate bias. In turn, the SP at the drain-sided potential $\Phi_{\mathrm{SP,D}}$ corresponds to the drain bias dependency.

For the determination of SP at the source side, the voltage drop over the source-sided resistance $R_\mathrm{G} \approx 0\,\Omega$ is neglected, resulting in $\Phi_\mathrm{SP,S} = E_\mathrm{F,uni}$. Accordingly, the SP can be calculated by the closed-form equation of $E_\mathrm{F,uni}$, which is defined as

$$E_\mathrm{F,uni} = V_\mathrm{ov} - \frac{2 \cdot v_\mathrm{t} \cdot \ln\left(1 + \exp\left(\frac{V_\mathrm{ov}}{2 \cdot v_\mathrm{t}}\right)\right)}{\frac{1}{H_\mathrm{SP}} + \frac{C_\mathrm{g}'}{q \cdot N_\mathrm{DOS}} \cdot \exp\left(-\frac{V_\mathrm{ov}}{2 \cdot v_\mathrm{t}}\right)}. \tag{4}$$

Here, the gate bias is considered in the gate overdrive voltage $V_\mathrm{ov} = V_\mathrm{GS} - V_\mathrm{th}$ as well as in the 2DEG bias dependency that is defined as H_SP. Apart from that, the thermal voltage is taken into account, which is defined as $v_\mathrm{t} = (k_\mathrm{B} \cdot T)/q$, considering the Boltzmann constant k_B, the elementary charge q and the temperature T at which the model is calculated. Furthermore, the density of states in the GaN region N_DOS and the gate sheet capacitance C_g', originating from the AlGaN barrier, defined as

$$C_\mathrm{g}' = (\epsilon_0 \cdot \epsilon_\mathrm{AlGaN})/d_\mathrm{AlGaN} \tag{5}$$

are considered. Here, the ϵ_0 and ϵ_AlGaN are the vacuum and the relative permittivity of the AlGaN barrier layer, while d_AlGaN is the corresponding layer thickness.

The 2DEG bias dependency H_SP needed for the calculation of $E_\mathrm{F,uni}$ is given by

$$H_\mathrm{SP} = \frac{V_\mathrm{ov}^* + v_\mathrm{t} \cdot \left(1 - \ln\left(\frac{C_\mathrm{g}'}{q \cdot N_\mathrm{DOS} \cdot v_\mathrm{t}} \cdot V_\mathrm{ov}^*\right)\right) - \frac{1}{3} \cdot G_\mathrm{SP} \cdot \left(\frac{C_\mathrm{g}' \cdot V_\mathrm{ov}^*}{q}\right)^{\frac{2}{3}}}{V_\mathrm{ov}^* + v_\mathrm{t} + \frac{2}{3} \cdot G_\mathrm{SP} \cdot \left(\frac{C_\mathrm{g}' \cdot V_\mathrm{ov}^*}{q}\right)^{\frac{2}{3}}}. \tag{6}$$

In comparison to $E_\mathrm{F,uni}$ in (4), an effective overdrive voltage V_ov^* is required, defined by

$$V_\mathrm{ov}^* = 0.5 \cdot (V_\mathrm{ov} + \sqrt{V_\mathrm{ov}^2 + V_\mathrm{min}^2}). \tag{7}$$

Here, the restatement from V_ov to V_ov^* is necessary since the $\ln(x)$-function is undefined for negative values and thus would cause an error in computation. Consequently, negative V_ov values are replaced by a minimum overdrive V_min allowing for a

consistent calculation. Apart from that, an interpolation function is needed to unify the results of the Schroedinger's equation, aiming for a smooth transition between the different areas of operation. The source-sided interpolation G_{SP} is calculated as

$$G_{\mathrm{SP}} = \gamma_1 + \left(\frac{\gamma_1 + \gamma_2}{2} - \gamma_1\right) \cdot \tanh\left(\frac{V_{\mathrm{ov}}}{V_{\mathrm{th}}}\right). \tag{8}$$

Here, the constants γ_1 and γ_2 represent the quantization of charge which are derived from cyclotron-resonance measurements by [131].

For the determination of SP at the drain side, the drain-dependent overdrive voltage $V_{\mathrm{dov}} = V_{\mathrm{ov}} - V_{\mathrm{DS,sat}}$ needs to be considered, resulting in $\Phi_{\mathrm{SP,D}} = E_{\mathrm{F,uni}} - V_{\mathrm{dov}}$. Here, the drain-induced saturation $V_{\mathrm{DS,sat}}$ is defined by

$$V_{\mathrm{DS,sat}} = V_{\mathrm{DS}} \cdot \left(1 + \left(\frac{V_{\mathrm{DS}}}{V_{\mathrm{dsat}}}\right)^{\texttt{SAT1}}\right)^{-\frac{1}{\texttt{SAT2}}} \tag{9}$$

with

$$V_{\mathrm{dsat}} = \frac{V_{\mathrm{ov}}^* \cdot v_{\mathrm{sat}}}{v_{\mathrm{sat}} + V_{\mathrm{ov}} \cdot \dfrac{\mu_0}{2 \cdot L}}. \tag{10}$$

The impact of the drain bias is included based on the applied drain-source voltage V_{DS} as well as saturation voltage V_{dsat} and can be adjusted by the fitting parameters `SAT1` and `SAT2`. The saturation voltage V_{dsat} is defined as (10) and considers the saturation velocity v_{sat}, low field mobility μ_0, and gate region length L.

As for the source side, the determination of $E_{\mathrm{F,uni}}$ at the drain side is done using (4), but now considering a drain-dependent overdrive voltage $V_{\mathrm{dov}} = V_{\mathrm{ov}} - V_{\mathrm{DS,sat}}$. Similar to this, calculating H_{SP} and G_{SP} as (6) and (8), the overdrive needs to be replaced by V_{dov}. Furthermore, for the calculation of H_{SP} an effective overdrive is necessary which is equally defined as (7), but now with V_{dov}. Finally, the unified SP $\Phi_{\mathrm{SP,uni}}$ is determined by the source- and drain-sided potentials as

$$\Phi_{\mathrm{SP,uni}} = \Phi_{\mathrm{SP,dif}} \cdot (V_{\mathrm{dov}}^* - \Phi_{\mathrm{SP,avg}} + v_{\mathrm{t}}). \tag{11}$$

Thereby, the calculation contains the results of the differential SP as $\Phi_{\mathrm{SP,dif}} = \Phi_{\mathrm{SP,D}} - \Phi_{\mathrm{SP,S}}$ as well as the average SP with $\Phi_{\mathrm{SP,avg}} = \left(\Phi_{\mathrm{SP,D}} - \Phi_{\mathrm{SP,S}}\right)/2$.

6.2.2 Drain Current

With the unified surface potential $\Phi_{\mathrm{SP,uni}}$ defined in (11), the 2DEG carrier density can be determined, which is controlled by the applied bias voltages V_{GS} and V_{DS} (cf. Fig. 6.1). Now, to derive the current flow through the HEMT, the carrier transport mechanisms need to be considered. The primary transport mechanisms are carrier drift due to the electrical field and carrier diffusion based on the gradient in density. With an increase in the electrical field induced by the applied voltages, carriers can be scattered by phonons which results in a reduction in mobility and, thus, a carrier velocity saturation. Consequently, the drain current I_{D} is defined as

$$I_{\mathrm{D}} = \frac{W}{L} \cdot \Phi_{\mathrm{SP,uni}} \cdot C'_{\mathrm{g}} \cdot \mu_{\mathrm{deg}} \cdot \mu_{\mathrm{sat}}. \tag{12}$$

Here, the $\Phi_{\mathrm{SP,uni}}$ in conjunction with the gate sheet capacitance C'_{g} from (5) determines the 2DEG carrier density, which can be scaled by the gate width to length ratio W/L. Finally, the current is determined considering the mobility degradation μ_{deg} and subsequent saturation μ_{sat}.

The mobility of carriers in the 2DEG tends to reduce with an increased electrical field in the HEMT. Here, the electrical field is a consequence of the applied voltage V_{GS}, as well as the resulting SP $\Phi_{\mathrm{SP,uni}}$. However, the carrier mobility is already needed to determine $\Phi_{\mathrm{SP,uni}}$ within (10), causing a calculation loop within the model. In order to avoid this, $\Phi_{\mathrm{SP,uni}}$ is calculated only utilizing the low-field mobility μ_0, while the mobility degradation μ_{deg} is considered using the additional term

$$\mu_{\mathrm{deg}} = \frac{1}{1 + \mathtt{M1} \cdot (V_{\mathrm{ov}} - \Phi_{\mathrm{SP,avg}}) + \mathtt{M2} \cdot (V_{\mathrm{ov}} - \Phi_{\mathrm{SP,avg}})^2} \tag{13}$$

that modifies the resulting I_{D}. Additionally, the V_{DS} does also impact the mobility of 2DEG carriers. A similar effect occurs, but now due to the carrier velocity saturation based on lattice scattering. Thus, a mobility saturation μ_{sat} is defined as

$$\mu_{\mathrm{sat}} = \frac{1}{\sqrt{1 + \mathtt{SAT1}^2 \cdot \Phi^2_{\mathrm{SP,dif}}}}. \tag{14}$$

6.2.3 Parameter Extraction and Verification

One major goal of the model development is the universal applicability for different commercially available devices. In order to tailor the model towards different technologies e.g., an ohmic- or Schottky-type gate structure or different voltage and current ratings, a reliable parameterization strategy is mandatory. For this purpose, a Phyton-based tool is developed, which is used for the parameter extraction and optimization procedure. This procedure involves the digitization of datasheet information and characteristics, which can be supplemented or fully replaced by additional measurement results. Then, the digitized information is used to create an initial set of model parameters that is subsequently adjusted by a sequential least square optimization. Here, the optimizer compares the model output with the datasheet or measurement curves (e.g., transfer characteristics) to find a set of parameters that causes the slightest difference between them.

In Fig. 6.2, the parameter extraction and optimization procedure is exemplarily illustrated for the DC transfer characteristics. As a starting point, the model requires several datasheet information such as the rated current $I_{\mathrm{D,nom}}$, the nominal gate-source voltage $V_{\mathrm{GS,nom}}$, and the drain-source drift resistance $R_{\mathrm{DS,on}}$. These parameters can either be directly taken from the datasheet tables or extracted from the DC characteristics in the respective operational point. Then, in the first step,

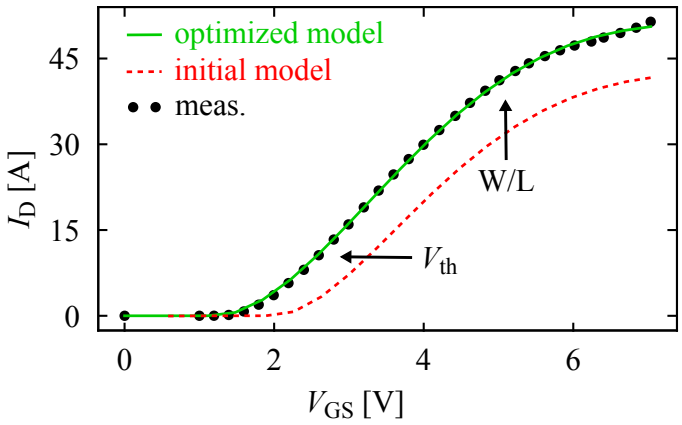

Figure 6.2: Illustration of the sequential parameter optimization on the example of the DC transfer characteristics, comparing model and measurement results.

the threshold voltage V_{th} is optimized to match the appropriate V_{GS}, which can differ between technologies or manufacturing tolerances. Afterward, as a second step, the W/L-ratio is adjusted to fit the model to the corresponding current rating.

The gate width to length ratio W/L is a typical design variable for semiconductor devices, which relates the applied input voltage V_{GS} through the transconductance to the respective output current I_{D}. From the manufacturer's perspective, the W/L-ratio is known information that is, to some extent, used in their model development. However, this is typically confidential information and is thus unavailable for commercial devices. Consequently, the only way to acquire the W/L-ratio is by estimating it through a model approach using known equations and parameters.

As shown in Sec. 6.2.1, the model equations of the GaN HEMT are fairly complex and thus unsuitable for that purpose. A solution for this is the usage of simple MOSFET equations, which do not perfectly fit but are more than sufficient to acquire an initial value. The W/L-ratio is calculated by

$$\frac{W}{L} = \frac{I_{\mathrm{D,nom}}}{\mu_0 \cdot C'_{\mathrm{g}} \cdot \left((V_{\mathrm{GS,nom}} - V_{\mathrm{th}}) \cdot I_{\mathrm{D,nom}} \cdot \frac{R_{\mathrm{DS,on}}}{2} - \frac{(I_{\mathrm{D,nom}} \cdot \frac{R_{\mathrm{DS,on}}}{2})^2}{2} \right)} \tag{15}$$

and derived from the MOSFET equation of the linear (triode) region [132]. To solve this, the values of $I_{\mathrm{D,nom}}$, $V_{\mathrm{GS,nom}}$, V_{th} and $R_{\mathrm{DS,on}}$ can be taken from datasheet information. Here, the voltage drop over the channel region is calculated as $V_{\mathrm{DS}} = I_{\mathrm{D,nom}} \cdot R_{\mathrm{DS,on}}/2$, assuming the channel resistance to account for half of the overall value. Apart from that, the MOSFET gate oxide capacitance is assumed to be similar to the HEMT gate sheet capacitance as C'_{g} from (5).

Several parameters are needed to calculate the W/L-ratio and subsequently the SP and I_{D} itself. Since the model aims for a physical-based approach, many equations are centered around physical constants, listed in Tab. 6.3. Apart from that, an additional set of parameters is utilized in the drain model, see Tab. 6.4. To some extent, these parameters are considered physical because they describe conditions such as temperature and geometry but also limitations. However, these parameters are equally used to generate the models for both DUTs.

Table 6.3: Physical parameters of the drain model, from [125].

Parameter	Description	Unit	Value
q	Elementary charge	C	$1.6 \cdot 10^{-19}$
k_B	Bolzmann constant	eV/K	$8.636 \cdot 10^{-5}$
ϵ_0	Vacuum permitivity	F/m	$8.854 \cdot 10^{-12}$
ϵ_AlGaN	Relative permitivity of AlGaN	-	9.2
N_DOS	Density of states in GaN	m^{-2}	$3.24 \cdot 10^{17}$
μ_0	Low-field mobility	m^2/Vs	0.17
v_sat	Saturation velocity	m/s	$1.9 \cdot 10^5$

Table 6.4: Constant parameters that are assumed to be equal for both DUTs.

Parameter	Description	Unit	Value
T_amb	Ambient temperature	K	298
L	Gate length	m	$250 \cdot 10^{-9}$
d_AlGaN	Thickness of AlGaN layer	m	$25 \cdot 10^{-9}$
R_S	Source-side drift resistance	Ω	$1 \cdot 10^{-3}$
γ_1	Schroedinger-Poisson constant 1	-	$2.12 \cdot 10^{-12}$
γ_2	Schroedinger-Poisson constant 2	-	$3.73 \cdot 10^{-12}$
V_min	Minimum overdrive	V	$10 \cdot 10^{-3}$
I_min	Minimum leakage current	A	$10 \cdot 10^{-12}$

In order to adjust the model regarding the difference in DUTs, a set of fitting parameters is used, as listed in Tab. 6.5. Since each dimension of the gate structure is necessary to know for the determination of the gate model in Sec. 6.3, the W/L-ratio is translated to the fitting variable W assuming a fixed L. Now, W is used to fit the model towards a specific current rating, along with the drift resistance R_D. Finally, the parameters `M1`, `M2` , `SAT1` and `SAT2` belong to the effects of mobility degradation and saturation from Sec. 6.2.2.

After fitting V_th and W, the additional parameters `M1`, `M2`, and `SAT1` must also be adjusted in the sequential optimization procedure. Here, the initial `M1`, `M2` are set low starting without mobility degradation, while the initial saturation is defined

Table 6.5: Fitting parameters used to optimize the drain model.

Parameter	Description	Unit	Ohmic gate	Schottky gate
W	Gate width	m	$6.481 \cdot 10^{-3}$	$5.063 \cdot 10^{-3}$
R_D	Drain-side resistance	Ω	$160.2 \cdot 10^{-3}$	$109.43 \cdot 10^{-3}$
`M1`	Mobility fitting 1	V^{-1}	$261.688 \cdot 10^{-3}$	$1.33 \cdot 10^{-6}$
`M2`	Mobility fitting 2	V^{-2}	$62.676 \cdot 10^{-3}$	$25.186 \cdot 10^{-3}$
`SAT1`	Saturation fitting 1	V^{-1}	1.789	2.924
`SAT2`	Saturation fitting 2	V^{-1}	1.257	1.396

as $\texttt{SAT1} = \mu_0/(v_\mathrm{sat} \cdot L)$. The outcome of fitting these five parameters is depicted in Fig. 6.3, comparing the model and measurement results for both DUTs. Note that both curves in each plot are equal, but one is linear and the other in a semilogarithmic scale. However, despite the significant difference in the current behavior of each DUT, the optimization generates accurate models for each device.

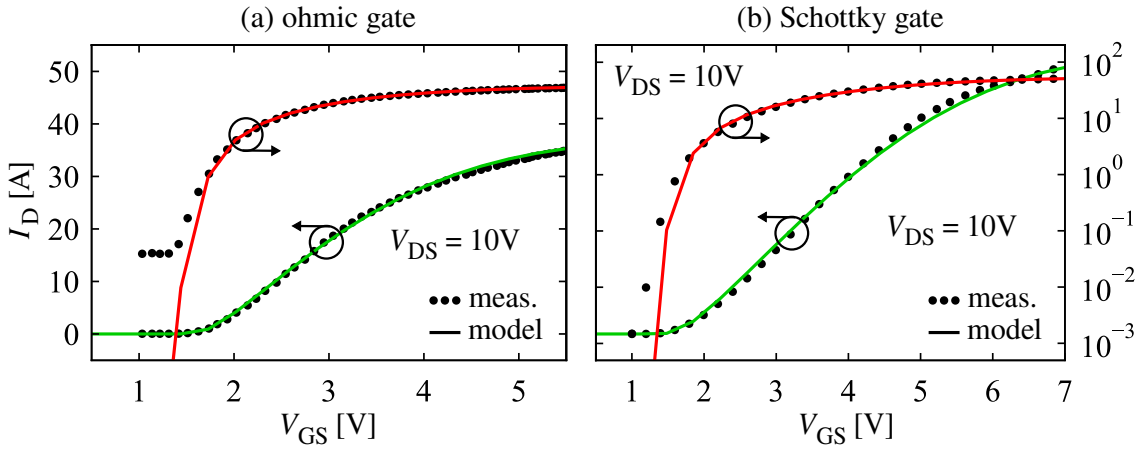

Figure 6.3: DC transfer characteristics of the (a) ohmic-gate and (b) Schottky-gate DUT, comparing the results of the measurements with the compact model. Note that I_D on the left is in linear and the right in logarithmic scale.

The fitting of the transfer characteristics is typically executed for measurements or datasheet curves representing an operation in saturation. In order to adjust the linear region, the output characteristics can be utilized, as shown in Fig. 6.4. Similar to the transfer characteristics, these are the final results of the model optimized for

both DUTs. The linear region is mainly impacted by the $R_{DS,on}$ of the device, which in turn depends on the resistance of the channel region and the drift region. Since the channel resistance is somewhat known from the I_D calculation, the drift resistance R_D is used to fit the overall on-state resistance. The parameter `SAT2` is also used to tailor the transition from the linear towards the saturation operation.

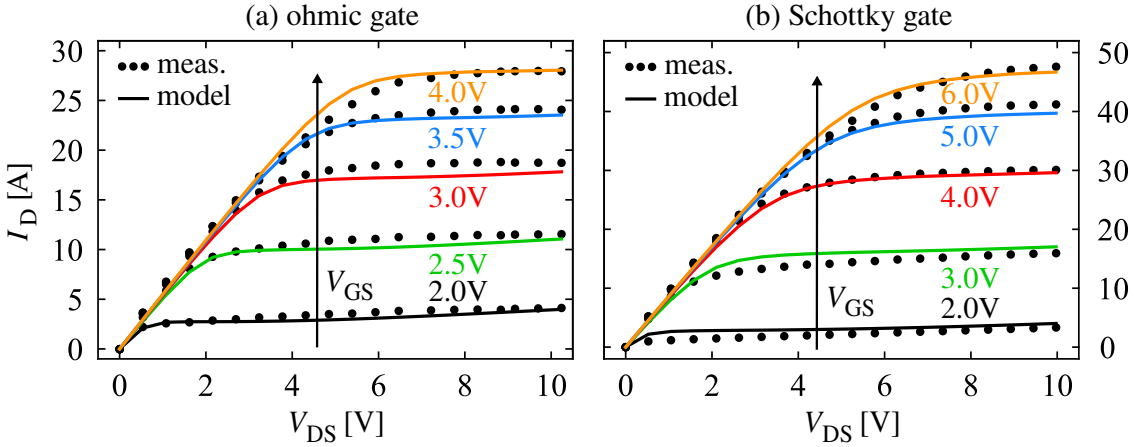

Figure 6.4: DC output characteristics in forward operation of the (a) ohmic-gate and (b) Schottky-gate DUT, comparing measurement and model results.

6.3 Gate Model

The drain model accounts for the relation between the input voltages V_{GS} and V_{DS} with the output current I_D, thus comprising the DC transfer and output characteristics. However, in comparison to a MOSFET, the HEMT does not have an oxide-based gate structure, which is why the DC input characteristics and thus the gate current I_G can not be neglected. Furthermore, the undesired effects of the V_{th} shift (cf. Sec. 3.2) as well as the V_{th} instability (cf. Sec. 3.3), appear in or at least correlate with the gate stack of p-gate GaN HEMTs. Since the SP-based drain model does not sufficiently cover the gate behavior, an appropriate gate model is developed, including interlinks with the V_{th} model developed in Sec. 6.5 and 6.6.

The structure of the gate stack in a p-gate GaN HEMT forms a Schottky contact (metal/p-GaN) or rather a reverse biased Schottky diode followed by a p-i-n diode (p-GaN/AlGaN/2DEG). The resulting structure of the gate model is illustrated in

Fig. 6.5. In addition to the Schottky diode D_{SC} and the p-i-n diode D_{PN}, the gate resistance R_G considers the drift region through the p-doped GaN layer.

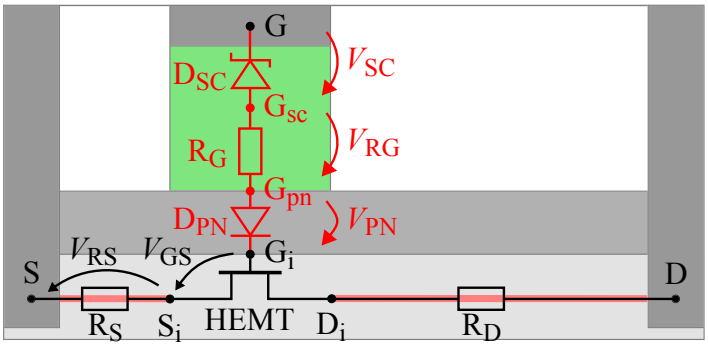

Figure 6.5: Cross-section showing the drain model that is extended by the elements of the gate model: Schottky diode D_{SC}, drift resistance R_G and p-i-n diode D_{PN}.

In order to calculate the gate model, the external potentials V_G and V_S applied on the input nodes G and S need to be translated into the internal voltages, which are mandatory to determine the output current I_G. These internal voltages are the voltage in space charge region (SCR) of the Schottky contact V_{SC}, defined as

$$V_{SC} = (V_G - V_S) - V_{RG} - V_{PN} - V_{GS} - V_{RS}, \tag{16}$$

the voltage drop over the gate drift-resistance V_{RG}, specified by

$$V_{RG} = I_G \cdot R_G, \tag{17}$$

and lastly the SCR voltage in the p-i-n diode V_{PN}, which is

$$V_{PN} = V_{BI}. \tag{18}$$

However, the determination of these voltages does require the knowledge of I_G itself and thus an iterative solution, similar to the drain model (cf. Sec. 6.2).

In forward operation ($V_{GS} > 0\,\mathrm{V}$), D_{SC} is reverse and D_{PN} forward biased. Thus the Schottky contact dominates the behavior of the current I_G. The limiting factor of current flowing through D_{SC} is the height of the Schottky barrier in the metal/p-GaN interface. In turn, this depends on the difference between the vacuum energies of the

p-GaN layer and the metallization. Since the contact metal is assumed to be equal for both DUTs (cf. Sec. 2.4.3), the barrier height is determined by the energy of the p-GaN layer, which depends on the doping concentration N_A. Apart from this, N_A does also determine the drift resistance R_G of the p-GaN region [31], defined as

$$R_\mathrm{G} = \frac{d_\mathrm{pGaN}}{W \cdot L \cdot q \cdot \mu_0 \cdot N_\mathrm{A}}. \tag{19}$$

In forward operation, the voltage drop over a p-i-n diode depends on the built-in voltage of the space charge region V_BI [31], which is

$$V_\mathrm{BI} = v_\mathrm{t} \cdot \ln\left(\frac{N_\mathrm{A}}{N_\mathrm{I}}\right). \tag{20}$$

Similar to the barrier and R_G, the V_BI also depends on N_A and the relation of N_A to its intrinsic carrier concentration N_I. Consequently, the current flow through the gate stack appears to be significantly determined by p-GaN doping N_A. Thus the gate model construction is centered around this variable.

In order to model the current flow through the gate stack, all mandatory mechanisms contributing to I_G need to be defined. In forward operation, the current conduction is dominated by the Schottky contact, which is calculated by

$$I_\mathrm{G} = I_\mathrm{PF} + I_\mathrm{FN} + I_\mathrm{TE} + I_\mathrm{min} \tag{21}$$

utilizing the mechanisms of Poole-Frenkel (PF) emission I_PF, Fowler-Nordheim (FN) tunneling I_PF, and thermionic emission (TE) I_TE. Additionally, a minimum leakage current I_min is considered.

As shown by the input characteristic in Fig. 6.6, all conduction mechanisms do simultaneously contribute to I_G but differ in their on-set as well as their extent. For voltages below the nominal operation $V_\mathrm{GS} < V_\mathrm{GS,nom}$, the PF emission appears to be the dominant effect which is further explained in Sec. 6.3.1. Afterward, the FN tunneling through the Schottky barrier takes over, leading to an increased I_G, see Sec. 6.3.2. Finally, as described in Sec. 6.3.3, reaching a maximum forward voltage, a breakdown of the Schottky barrier occurs. Thus I_G is given by the TE through the AlGaN barrier. Note that the TE breakdown current is limited by R_G.

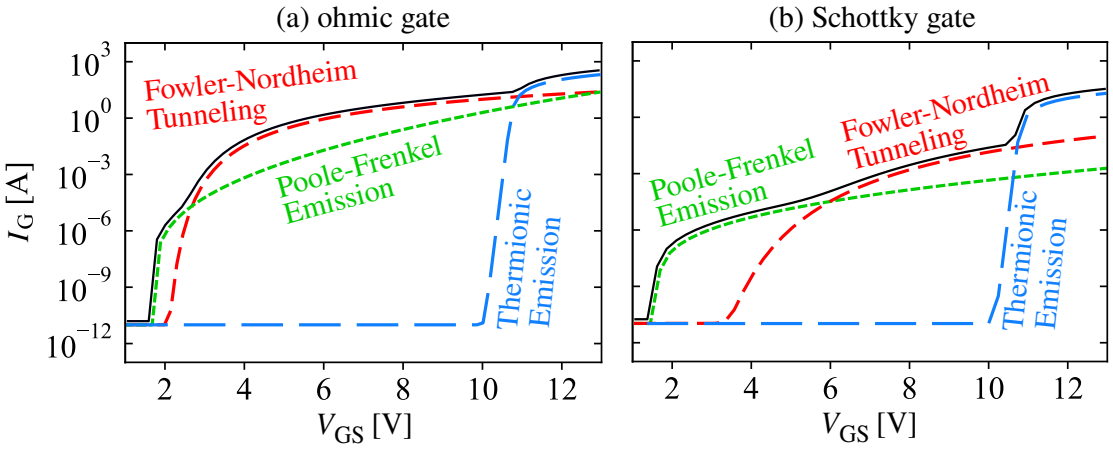

Figure 6.6: Simulated input characteristics of the (a) ohmic- and (b) Schottky-gate DUT, illustrating the distribution of the I_G conduction mechanisms: Poole-Frenkel (PF) emission, Fowler Nordheim (FN) tunneling, and thermionic emission (TE).

6.3.1 Poole-Frenkel Emission

The electrical field resulting from an applied voltage or temperature can cause the emission of electrons from trap states generating mobile carriers and conductive dislocation [133]. This phenomenon is called the Poole-Frenkel (PF) emission, which is a common mechanism responsible for the reverse leakage current in Schottky-contact GaN HEMTs [134]. Due to this, the PF current I_{PF} is calculated as

$$I_{PF} = E_{sc} \cdot \exp\left(-\frac{\Phi_E}{v_t} + \sqrt{\texttt{GP} \cdot \frac{E_{sc}}{v_t}}\right), \tag{22}$$

considering the barrier height for electron emission from trap states Φ_E and the electrical field at the Schottky contact E_{sc}. The calculation of I_{PF} is simplified, resulting in a fitting constant `GP` that is used to adjust the model while also considering the thermal voltage v_t similar to the drain model.

Applying a constant voltage V_{SC} on the SCR of the Schottky contact, which i supposed to be free of charge, a triangular shaped electrical field E_{sc} can be assumed that is calculated along its width x_{SC}, as

$$E_{sc} = \frac{V_{SC}^*}{x_{SC}} \cdot \frac{q}{\epsilon_0 \cdot \epsilon_{GaN}}. \tag{23}$$

Here, an effective voltage V_{SC}^{*} is used to determine E_{sc}, thus preventing a computation error as similarly done for the overdrive voltage in (7). Furthermore, the p-GaN permittivity ϵ_{GaN} is considered for the SCR field.

In the metal/p-GaN junction, the SCR mainly penetrates the p-GaN layer due to its lower carrier concentration compared to the metal. Based on this, the SCR distribution and thus its width x_{SC} can be estimated by

$$x_{\mathrm{SC}} = \sqrt{\frac{2 \cdot \epsilon_0 \cdot \epsilon_{\mathrm{GaN}} \cdot V_{\mathrm{SC}}^{*}}{q \cdot N_{\mathrm{A}}}}, \tag{24}$$

only considering the p-GaN doping concentration N_{A} and the voltage V_{SC}^{*} that is stored in it.

6.3.2 Fowler Nordheim Tunneling

For increasing voltages, electrons can start moving through the Schottky barrier, commonly known as electron field emission or Fowler-Nordheim (FN) tunneling. This phenomenon can occur in structures with very thin electrical isolating layers and is proven to be evident in GaN HEMTs already at room temperature [135]. The FN current I_{FN} can be calculated as

$$I_{\mathrm{FN}} = \frac{N_{\mathrm{O}}}{N_{\mathrm{A}}} \cdot \frac{E_{\mathrm{sc}}^{2}}{\Phi_{\mathrm{SC}}} \cdot \exp\left(-\frac{(\mathtt{GF} \cdot \Phi_{\mathrm{SC}})^{3/2}}{E_{\mathrm{sc}}}\right), \tag{25}$$

by the relation of an applied electrical field E_{sc} defined in (23) and the effective Schottky barrier Φ_{SC} [136], which is defined as

$$\Phi_{\mathrm{SC}} = \Phi_{\mathrm{B}} + \Delta\Phi_{\mathrm{X}}(N_{\mathrm{O}}) - \Delta\Phi_{\mathrm{X}}(N_{\mathrm{A}}). \tag{26}$$

Note that I_{FN} in (25) is simplified, using a weighting factor $N_{\mathrm{O}}/N_{\mathrm{A}}$ which considers the ratio of the actual p-GaN doping concentration N_{A}, an estimated doping N_{O} that would result in an ohmic contact and a fitting constant `GF`. This ratio reflects that the impact of FN tunneling reduces for devices with increased ohmic-type behavior. For a concentration of N_{A} close to N_{O}, the FN tunneling decreases resulting in PF emission remaining the dominant mechanism even for increased voltages.

The Schottky barrier Φ_{SC} from (26) is defined as an effective value [136]. Here, the gate-metal barrier Φ_{B} is considered as an offset, while $\Delta\Phi_{\mathrm{X}}$ reflects a doping-dependent modification. Assuming Φ_{B} to be the minimum barrier, the $\Delta\Phi_{\mathrm{X}}(N_{\mathrm{O}})$ corresponds to the estimated barrier height that must be overcome to achieve an ohmic contact. Consequently, the barrier reduction induced by the p-GaN doping $\Delta\Phi_{\mathrm{X}}(N_{\mathrm{A}})$ is defined as

$$\Delta\Phi_{\mathrm{X}}(N_{\mathrm{A}}) = q \cdot N_{\mathrm{A}} \cdot \frac{x_{\mathrm{SC}}^2}{2 \cdot \epsilon_0 \cdot \epsilon_{\mathrm{GaN}}}. \tag{27}$$

Similar to the PF emission, the resulting SCR width x_{SC} is determined by (24). Note that the SCR width obviously needs to be recalculated considering an ohmic-type doping N_{O}, which is necessary to acquire $\Delta\Phi_{\mathrm{X}}(N_{\mathrm{O}})$ using (27).

6.3.3 Thermionic Emission

In the forward operation of a diode, the effect of thermionic emission (TE) appears to be the dominant conduction mechanism [133]. Similar to PF emission, the TE considers an emission of electrons but here coming from lattice states and are induced by the thermal energy. The impact of temperature can also result in the generation of mobile carriers and conductive dislocations.

Nevertheless, in forward operation of the gate stack, the Schottky diode D_{SC} (cf. Fig. 6.5) is reverse biased and thus dominated by PF emission and FN tunneling. If the applied V_{GS} exceeds a limitation, a forward breakdown of the Schottky barrier can occur, resulting in a significant current increase. Then, the current conduction is determined by the p-i-n diode D_{PN}, which is actually in forward operation. Consequently, the TE current I_{TE} is considered for an operation exceeding the breakdown voltage V_{F} and defined as

$$I_{\mathrm{TE}} = I_{\mathrm{min}} \cdot \exp\left(\frac{V_{\mathrm{GS}} - V_{\mathrm{F}}}{v_{\mathrm{t}}}\right). \tag{28}$$

Similar to the PF and the FN equations, the TE current I_{TE} is greatly simplified, only considering a minimum value I_{min} instead of a temperature-dependent equation. However, this is sufficient since I_{TE} only determines the breakdown, which is not

examined in terms of temperature. Apart from that, the increase of I_{TE} or rather I_{G} is limited by the gate drift resistance R_{G}, which is defined in (19).

For a negative voltage on the gate stack, the signs turn, resulting in a reverse operation of D_{PN}, which then tends to dominate the current conduction. Since the Schottky barrier no longer determines I_{G}, the mechanisms of PF emission and FN tunneling can be neglected. However, increased voltages can result in a reverse breakdown of D_{PN}, similar to the forward direction. Once again, this is described by the TE current, resulting in a reverse I_{G} that is calculated as

$$I_{\mathrm{G}} = -I_{\mathrm{min}} \cdot \exp\left(\frac{-V_{\mathrm{GS}} - V_{\mathrm{R}}}{\mathtt{GT} \cdot v_{\mathrm{t}}}\right). \tag{29}$$

Compared to the forward I_{G} from (21), the reverse breakdown voltage V_{R} and a fitting constant `GT` are included for adjustment.

6.3.4 Parameter Extraction and Verification

As for the drain model (cf. Sec. 6.2.3), the development of the gate model is based on a unified parameter extraction and optimization procedure. For the calculation of the PF emission, FN tunneling, and TE, several physical constants are required, listed in Tab. 6.6. The intrinsic carrier concentration N_{I} of GaN is acquired by [137] and shown to be much lower compared to Si, since in GaN almost no carriers are released into the conduction band. Besides, the barrier constants Φ_{E} and Φ_{B} are given by the definition of the PF emission [133] and FN tunneling [136].

Table 6.6: Physical parameters of the gate model.

Parameter	Description	Unit	Value
ϵ_{GaN}	Relative permitivity of GaN	-	9.5
N_{I}	Intrinsic carrier concentration	cm^{-3}	$1 \cdot 10^{-10}$
Φ_{E}	Electron emission barrier	eV	0.35
Φ_{B}	Gate-metal barrier	eV	1.2

Several other constants are needed, which are listed in Tab. 6.7. Here, the p-GaN thickness d_{pGaN} and doping concentration N_{O} are estimated to the best of

our knowledge. On the other hand, the forward breakdown voltage V_{F} corresponds to the maximum value approved by the manufacturers as listed in the datasheets.

Table 6.7: Constant parameters of the gate model.

Parameter	Description	Unit	Value
d_{pGaN}	Thickness of the p-GaN layer	m	$1 \cdot 10^{-6}$
N_{O}	Ohmic doping concentration	cm^{-3}	$1 \cdot 10^{20}$
V_{F}	Gate forward breakdown	V	10

In order to adjust the model regarding the difference in the DUT structure resulting in either an ohmic gate or a Schottky gate, some fitting parameters are used as listed in Tab. 6.8. As intended in the design process of the gate model, the most relevant part of the fitting is done in forward operation by optimizing the p-GaN doping N_{A}. The fitting constants `GP` and `GF` are empirically determined, offering a decent match for both gate types. Note that all parameters are equally used to generate models for both DUT and remain constant throughout the optimization. The reverse operation is also adjusted using the breakdown voltage V_{R} and fitting constant `GT`.

Table 6.8: Fitting parameters used to optimize the gate model.

Parameter	Description	Unit	Ohmic gate	Schottky gate
N_{A}	p-GaN doping concentration	cm^{-3}	$2.42 \cdot 10^{19}$	$4.23 \cdot 10^{17}$
`GP`	PF fitting constant	m	0.57	0.57
`GF`	FN fitting constant	1/m	1	1
V_{R}	Gate reverse breakdown	V	3.37	13.46
`GT`	TE fitting constant	-	$63.43 \cdot 10^{-3}$	$68.96 \cdot 10^{-3}$

The optimized results of the gate model are shown in Fig. 6.7 for the forward and in Fig. 6.8 for the reverse operation. Here, the measured input characteristics are compared with simulated results of the optimized models of each DUT, which appear to align accurately for a wide range of operation.

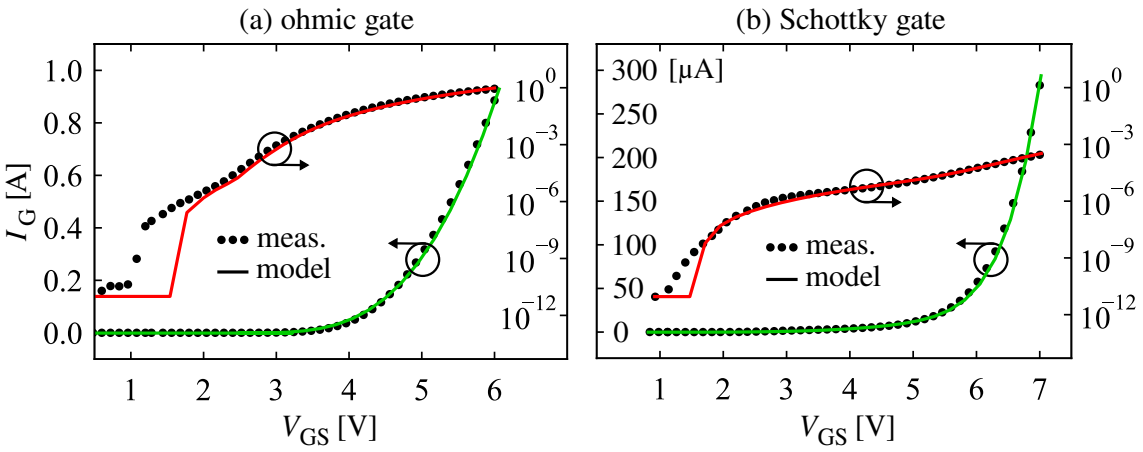

Figure 6.7: Forward input characteristics of the (a) ohmic-gate and (b) Schottky-gate DUT, comparing the results of the measurements with the compact model. Note that, I_G on the left is in linear and the right in logarithmic scale.

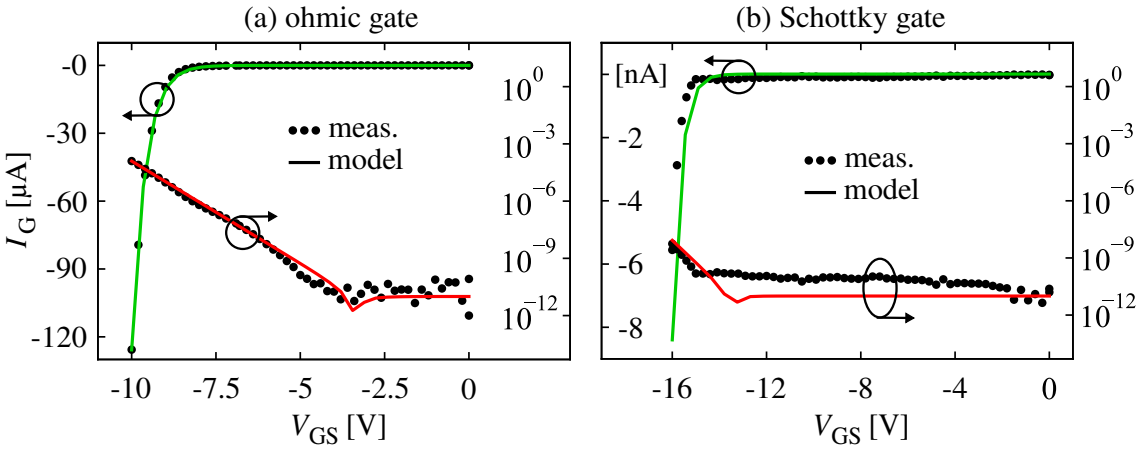

Figure 6.8: Reverse input characteristics, comparing measurements with the model.

6.4 Capacitance Model

The effect of the V_{th} shift (cf. Sec. 3.2) is related to the applied voltage that couples into the parasitic capacitances of the SCR in the gate stack (cf. Fig. 3.6). More specifically, the V_{th} shift correlates to the gate-drain capacitance C_{GD} and thus its dependency on the drain-source voltage V_{DS}. In order to include the V_{th} shift into

the drain and gate model, a specifically tailored capacitance model extension is developed, illustrated in Fig. 6.9. Thus, the formation of C_{GD} is considered as a series of capacitances that is composed by the SCRs of the Schottky contact C_{SC} and the p-i-n diode C_{PN}. On the other hand, the drain- and gate-source capacitances C_{DS} and C_{GS} are considered independent of the SCRs for simplification.

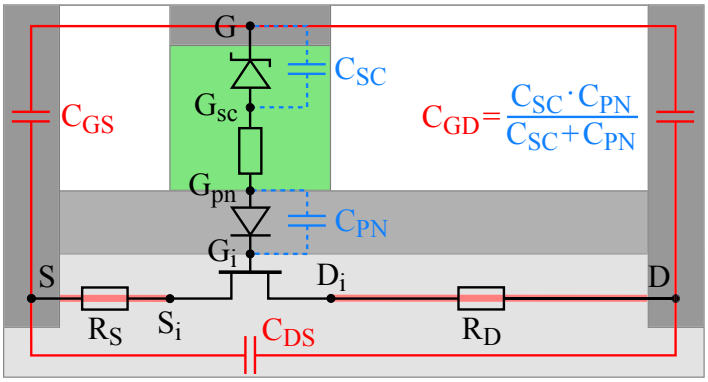

Figure 6.9: Cross-section showing the drain and gate model extended by the elements of the capacitance model: The series of Schottky and p-i-n diode SCR capacitances C_{SC} and C_{PN} forming C_{GD} as well as the parasitic capacitances C_{DS} and C_{GS}.

For a forward operation of the gate stack, the current conduction is dominated by the reversed SCR of the Schottky contact. However, looking at the distribution of a voltage applied between the gate and the drain contact V_{GD}, it will divide over both SCR capacitances C_{SC} and C_{PN} due to their series connection. Consequently, the resulting gate-drain capacitance C_{GD} is defined as

$$C_{\mathrm{GD}} = \frac{C_{\mathrm{SC}} \cdot C_{\mathrm{PN}}}{C_{\mathrm{SC}} + C_{\mathrm{PN}}}, \tag{30}$$

where C_{PN} relates to the gate sheet capacitance, defined in (5), scaled to the DUT dimensions using $C'_{\mathrm{g}} \cdot W/L$ (cf. Sec. 6.2.2). Hence, C_{PN} is much higher and thus less dominant in the series connection with C_{SC}.

Applying a positive voltage V_{GD} on the gate stack increases the electrical field-induced drift of carriers within the SCR, which results in a widening of the depletion region and thus a SCR widening. Based on the charge neutrality in this region, the SCR junction of the Schottky contact C_{SC} can be assumed as a capacitance that is

described by the depletion approximation [138] as

$$C_{\mathrm{SC}} = (C_{\mathrm{GD0}} - C_{\mathrm{GD1}}) \cdot \frac{1}{1 - \dfrac{V_{\mathrm{GD}}}{\mathtt{CAP1}}} + C_{\mathrm{GD1}}. \tag{31}$$

Here, the capacitance is parameterized by C_{GD0} and C_{GD1}, which correspond to an operation at low and high voltages. These parameters can be acquired by either the datasheet or measurement results. Additionally, the fitting constant `CAP1` is used to shape and adjust the model during the optimization procedure.

In comparison to C_{GD} or rather C_{SC}, the capacitances of the drain- and gate-source region C_{DS} and C_{GS} are assumed independent of the SCR. Here, different approaches could be implemented, while utilizing a simple mathematical equation can already result in a decent accuracy which is for C_{DS} exemplarily defined as

$$C_{\mathrm{DS}} = (C_{\mathrm{DS0}} - C_{\mathrm{DS1}}) \cdot \frac{\mathtt{CAP3}}{\sqrt{V_{\mathrm{DS}}^2 + \mathtt{CAP3}^2}} + C_{\mathrm{DS1}}. \tag{32}$$

Note that one reason for not just using the SCR definition from [138] is that the resulting value becomes infinite for $V_{\mathrm{DS}} = \mathtt{CAP3}$. For C_{GD} this issue appears to be negligible, but for C_{DS} and C_{GS} it occurs within the operational range.

For the parameterization of the capacitance model, their behavior needs to be extracted from either the datasheet or measurement results. The capacitance behavior is typically indicated and acquired by a voltage sweep, also known as the C-V profile. Here, specific wiring configurations are used to determine the capacitances. Consequently, the reverse capacitance C_{RSS} can be used to determine C_{GD} as

$$C_{\mathrm{RSS}} = C_{\mathrm{GD}} \quad \rightarrow \quad C_{\mathrm{GD}} = C_{\mathrm{RSS}}, \tag{33}$$

the input capacitance C_{ISS} together with C_{RSS} to gather C_{GS} as

$$C_{\mathrm{ISS}} = C_{\mathrm{GD}} + C_{\mathrm{GS}} \quad \rightarrow \quad C_{\mathrm{GS}} = C_{\mathrm{ISS}} - C_{\mathrm{RSS}}, \tag{34}$$

and finally the output capacitance C_{OSS} with C_{RSS} to extract C_{DS} with

$$C_{\mathrm{OSS}} = C_{\mathrm{DS}} + C_{\mathrm{GD}} \quad \rightarrow \quad C_{\mathrm{DS}} = C_{\mathrm{ISS}} - C_{\mathrm{RSS}}. \tag{35}$$

For example, executing a C-V measurement between the gate and source contact while the drain and source contact are shortened results in acquiring $C_{\mathrm{GD}} + C_{\mathrm{GS}}$ due to their parallel connection. Consequently, all capacitances are determined by measurements and subsequently translated for the model.

The resulting parameters used in the capacitance model are listed in Tab. 6.9. Here, the C_{GD0} corresponds to the maximum capacitance that occurs applying a voltage of 0 V, while C_{GD1} is the minimum extracted at 600 V. Although these values differ for each DUT, they remain constant throughout the optimization.

For optimization, the fitting parameters `CAP1`, `CAP2`, and `CAP3` are used, as listed in the lower half of Tab. 6.9. These parameters define the transition slope between the high and low values of the voltage-dependent capacitances. Note that `CAP2` remains unchanged for both DUTs since it has no significant impact on C_{ISS}.

Table 6.9: Constant (up) and fitting (down) parameters of the capacitance model.

Parameter	Description	Unit	Ohmic gate	Schottky gate
C_{GD0}	C_{GD} at 0 V	F	$6.69 \cdot 10^{-11}$	$3.19 \cdot 10^{-11}$
C_{GS0}	C_{GS} at 0 V	F	$1.41 \cdot 10^{-10}$	$9.9 \cdot 10^{-11}$
C_{DS0}	C_{DS} at 0 V	F	$8.66 \cdot 10^{-11}$	$2 \cdot 10^{-10}$
C_{GD1}	C_{GD} at 600 V	F	$1.48 \cdot 10^{-13}$	$7.52 \cdot 10^{-13}$
C_{GS1}	C_{GS} at 600 V	F	$1.55 \cdot 10^{-10}$	$1.14 \cdot 10^{-10}$
C_{DS1}	C_{DS} at 600 V	F	$2.75 \cdot 10^{-11}$	$2.6 \cdot 10^{-11}$
`CAP1`	C_{GD} fitting	V	7.75	16.04
`CAP2`	C_{GS} fitting	V	1	1
`CAP3`	C_{DS} fitting	V	81.04	103.9

The optimized results of the capacitance model are shown in Fig. 6.10. Here, the capacitance-voltage behavior (C-V profile) is depicted by comparing the datasheet curves with the optimized models of each DUT. It can be seen that the models do already fit quite accurately to the measurements. However, the datasheet C_{RSS} appears to shows a non-linear shape in the range of 20 V up to 200 V, which the model does not cover. In any case, the V_{th} model in Sec. 6.5 the capacitance model is sufficient to reproduce the V_{th} shift.

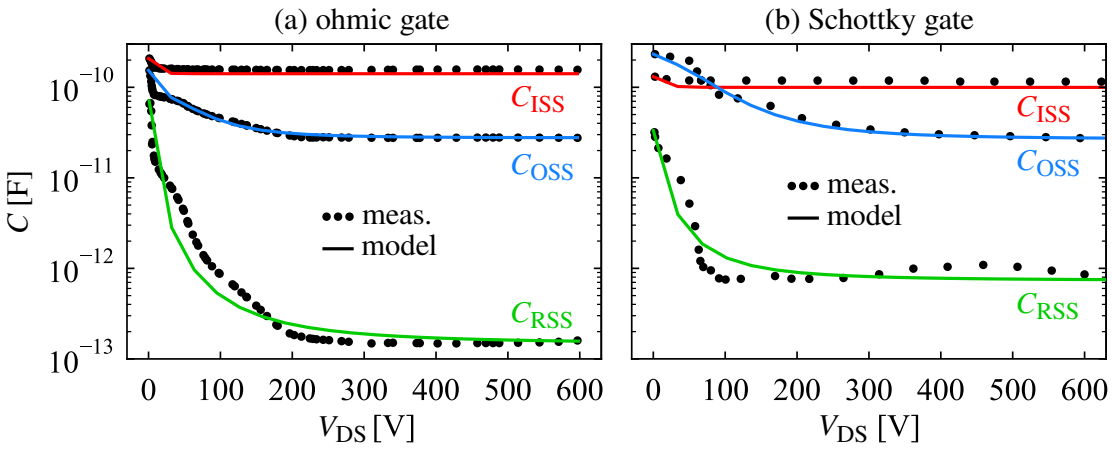

Figure 6.10: DC Capacitance-Voltage (C-V) behavior, comparing measurement and model results. Note that the results are in a semi-logarithmic scale.

6.5 Threshold Voltage Shift

The threshold voltage shift (cf. Sec. 3.2) is based on the capacitive coupling of V_{DS} into the SCRs of the gate stack (cf. Fig. 3.6). Applying a positive V_{GS} on the gate results in a reverse-biased Schottky and forward-biased p-i-n diode. Both of these diodes are built around a SCR, which can be considered as a voltage-dependent capacitance that increases or decreases relative to the applied V_{DS} (cf. Sec. 6.4). Here, the reverse-biased SCR capacitance C_{SC} tends to incorporate the largest amount of V_{GS} as well as the proportion of V_{DS} that couples through the series connected p-i-n capacitance C_{PN}. Consequently, a SCR widening occurs, resulting in a reduction of C_{SC} and thus a potential elevation in the floating p-GaN region, which is centered between C_{SC} and C_{PN}. However, the p-GaN potential determines the depth of the potential well forming the 2DEG and consequently the V_{GS} required for turn-on, which ultimately leads to the observation of a V_{th} shift [19].

In the current state-of-the-art, no model considers the V_{th} shift by its physical relation with the gate stack capacitances. As a novelty, a simple approach is developed which considers the actual shift calculation V_{shift} as well as the occurrence of a weakening effect V_{weak} to create an analytical V_{th} shift model, with

$$V_{th} = V_{shift} + V_{weak}. \tag{36}$$

According to the physical correlations, the V_{shift} should consider the floating p-GaN potential and its interaction with the 2DEG. On the other hand, the SP and consequently the drain model solely utilize the resulting V_{th} value as an input. However, to still incorporate some physical meaning, the V_{DS}-dependency of the SCR capacitances can be utilized. Hence, the actual shift V_{shift} is defined as

$$V_{\text{shift}} = (V_{\text{th,max}} - V_{\text{th,min}}) \cdot \frac{C_{\text{GD}}}{C_{\text{GD0}}} + V_{\text{th,min}}, \tag{37}$$

considering the SCR-dependent gate capacitance C_{GD} and its relative deviation from the initial value C_{GD0}. Consequently, a V_{DS}-induced change of C_{GD} or rather C_{SC} results in a change of V_{shift}, which covers at least one aspect of the physical mechanism. The parameterization of the resulting shift and its remaining offset is done based on measurements, as similarly realized for the other models. To remain a straightforward approach only the maximum and minimum V_{th} values are required, where $V_{\text{th,max}}$ is extracted at around 1 V and $V_{\text{th,min}}$ above 100 V (cf. Fig. 5.8).

The ohmic- and Schottky-gate DUT do mainly differ in the margin of the V_{th} shift, while in case of the ohmic device, a weakening of the shift is observable for voltages above 500 V. This could originate from an additional injection of holes coming from the hybrid drain (cf. Fig. 3.5), which is only integrated in case of the ohmic-gate DUT. These supplementary holes move along the 2DEG, where they can subsequently be injected through the AlGaN barrier and into the floating p-GaN or even the SCR capacitance. Within the capacitance, the holes counteract the drift-induced depletion, resulting in a width shortening of a SCR. A SCR widening corresponds to a V_{th} shift. Hence a shortening results in a shift weakening.

The hybrid drain was initially introduced to suppress the occurrence of current collapse by additional hole injection and is shown to do so for voltages above 550 V [14]. If measurement uncertainties and manufacturing tolerances are considered, the V_{th} shift weakening could be assigned to the hole injection from the hybrid drain. For this purpose, the shift weakening V_{weak} can be formulated as

$$V_{\text{weak}} = (V_{\text{th,hv}} - V_{\text{th,min}}) \cdot \frac{1}{2} \cdot \left(\tanh\left(\frac{V_{\text{DS}} - V_{\text{HI}}}{\texttt{WEAK}} \right) + 1 \right). \tag{38}$$

In addition to $V_{\mathrm{th,min}}$, the V_{th} value occuring at the maximum voltage $V_{\mathrm{th,hv}}$ is extracted at 600 V. To correlate the model to its physical origin, the effect is shifted towards the on-set of hole injection at 500 V using V_{HI}. Finally, the fitting parameter `WEAK` is used to adjust the slope of the V_{th} shift weakening.

The resulting V_{th} shift model parameters are listed in Tab. 6.10. As already mentioned, the $V_{\mathrm{th,max}}$, $V_{\mathrm{th,min}}$ and $V_{\mathrm{th,hv}}$ are extracted from measurements of each DUT. The same accounts for the on-set of hole injection V_{HI}, while the weakening constant `WEAK` is determined empirically. Note that for both DUTs, the same V_{HI} and `WEAK` are used, which is viable since V_{weak} of the Schottky-gate DUT is almost zero due to $V_{\mathrm{th,hv}} \approx V_{\mathrm{th,min}}$.

Table 6.10: Constant parameters of the V_{th} shift model.

Parameter	Description	Unit	Ohmic gate	Schottky gate
$V_{\mathrm{th,max}}$	Maximum V_{th} at 1 V	V	1.527	1.408
$V_{\mathrm{th,min}}$	Minimum V_{th}	V	1.312	0.695
$V_{\mathrm{th,hv}}$	High voltage V_{th} at 600 V	V	1.413	0.708
V_{HI}	On-set of hole injection	V	500	500
`WEAK`	Fitting of V_{th} shift weakening	V	50	50

The outcome of the V_{th} shift model is shown in Fig. 6.11, comparing the measurement with the model results for both DUTs. In case of the ohmic-gate DUT, the model almost perfectly covers the course of the V_{th} shift, except a variation between 300 V to 450 V which in comparison to the overall fit appears to be negligible. For the Schottky-gate DUT, the model also aligns with the measurement but does show a considerably larger difference for voltages between 20 V and 150 V. The reason for this is that the model is based on the behavior of the SCR capacitance C_{SC}, defined in (31), which is fitted in the capacitance model (cf. Fig. 6.10). This appears to be sufficient in the case of the ohmic-gate DUT. In turn, for the Schottky-gate DUT, this is less suitable since the transition is much steeper and already saturates at 50 V. However, the associated misalignment remains below 200 mV and only appears at the transition, which is acceptable for such a simple approach.

The impact of the V_{th} shift is demonstrated by the DC output characteristics that are depicted in Fig. 6.12, comparing the measurement with the model results

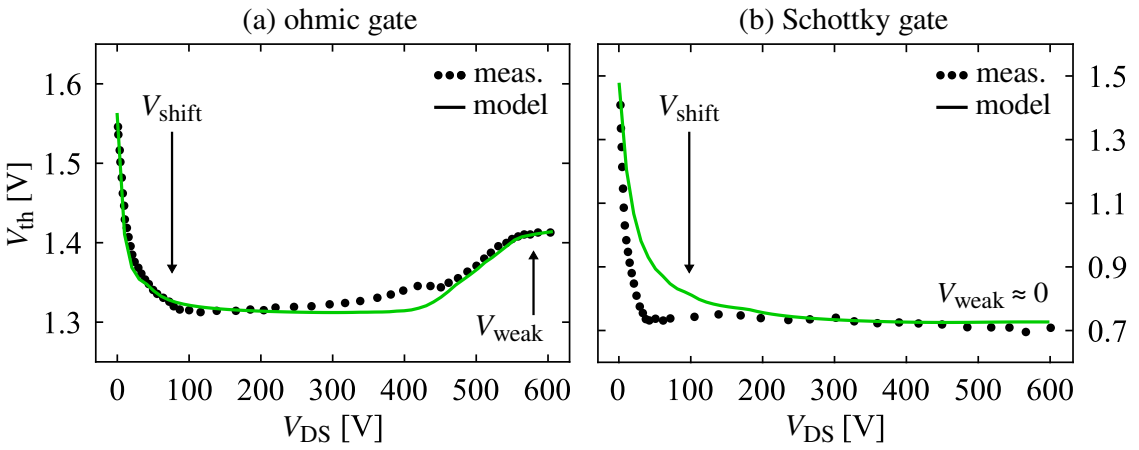

Figure 6.11: Behavior of the threshold voltage V_{th} showing the V_{DS}-induced V_{th} shift and a weakening effect that is only visible for the ohmic gate DUT.

for both DUTs. More precisely, the measurements are compared to the drain model, which initially only considers a constant V_{th} and later includes the V_{th} shift approach. Both models appear to align for voltages below operation in saturation, but a spread can be observed by looking at higher V_{DS} and lower currents.

In an ideal transistor, the current should remain constant for operation in saturation due to the occurrence of a pinch-off in the channel region that arises from carrier velocity saturation. Initially, the carrier velocity rises with an increasing field

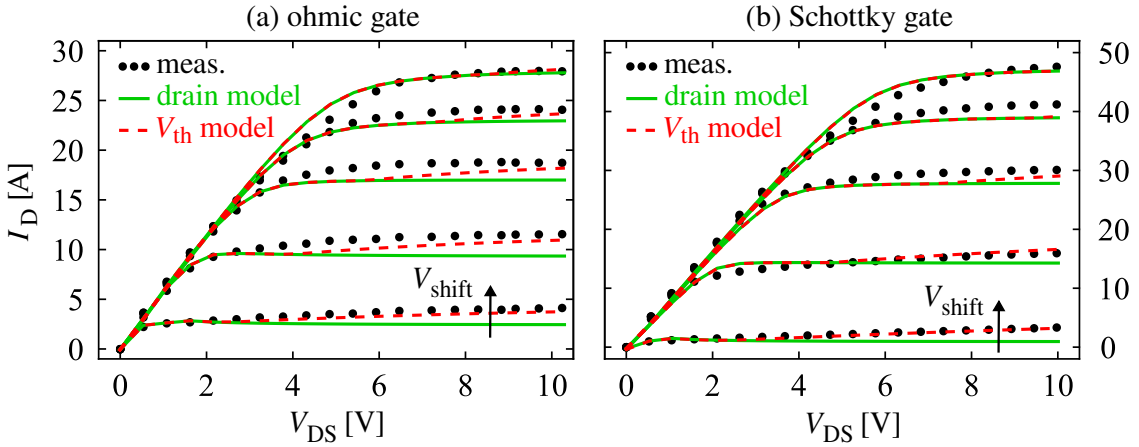

Figure 6.12: Impact of the V_{th} shift on the DC output characteristics, comparing the drain model with constant V_{th} as well as considering the V_{th} model.

induced by V_{DS} but eventually saturates due to a scattering at atoms or impurities [31]. However, real devices such as the bipolar transistor or the MOSFET can show an increase of the current even in saturation. In case of the MOSFET this occurs due to channel-length modulation causing a shortening of the effective channel length and thus an increase of I_{D}.

Although this might also be true for a HEMT, this would mean that the increase of I_{D} would occur for all values of V_{GS}. However, looking at the measurement results in Fig. 6.12, the I_{D} increase tends to only appear for low V_{GS}. The actual reason for this is the occurrence of the V_{th} shift induced by V_{DS}, which can clearly be seen comparing both models. Consequently, the advanced model, including the V_{th} shift, does cover the non-ideal deviation of I_{D} that occurs for increasing V_{DS} at low V_{GS}. Furthermore, this is observable in the presented measurements and in the datasheet curves of the respective manufacturers [96, 97].

6.6 Threshold Voltage Instability

The integration of static effects such as the V_{th} shift is done by simply adding the respective equation to the model. In order to take transient effects into account, a differential-equation approach can be utilized, which is implemented using the Verilog-A ddt()-function. Within the simulation, the function approximates the time derivative of the input value by calculating its incremental change concerning the previous time step. In other words, the function responds to a change in the input value, which is necessary for the implementation of capacitances and inductances. The resulting current is defined as

$$I_{\mathrm{D}} = C_{\mathrm{DS}} \cdot \mathrm{ddt}(V_{\mathrm{DS}}), \tag{39}$$

which serves as an example for the parasitic capacitance C_{DS} in the drain path. Applying a square-pulsed V_{DS} would result in a sudden jump of I_{D} between the time steps where V_{DS} rises, which then falls back to zero as soon as V_{DS} reaches a steady state. If this function is subsequently combined with a resistance, the typical RC-type charging and discharging characteristics can be reproduced.

The ddt()-function is utilized for the implementation of all parasitic components, such as the elements of the capacitance model as well as considering bond wire inductances. However, an occasional computation error was encountered during implementation if the constants e.g., C_{DS} were placed inside the functions. Thus, the constants are recommended to be placed outside, as shown in (39), resulting in comparable results without any error.

Looking at the results of the V_{th} instabilities in Sec. 5.1.4, very long time constants are observed, which exceed typical on-state durations by far. Many of the observed characteristics indicate that the mechanisms require a specific bias for a certain duration in order to appear as a transient change in the first place. For example, no impact is observable applying a negative V_{GS} of $-10\,\mathrm{V}$ for a duration below 100 ms, while after about 100 ms a quite noticeable V_{th} instability (cf. Sec. 5.1.4) occurs. Furthermore, as soon as the underlying mechanisms are charged, it can take up to 100 s for them to converge or rather disappear again. Consequently, it could be claimed that the V_{th} instabilities are a memory phenomenon.

Apart from that, the behavior of the V_{th} instabilities V_{inst} and V_{weak} are proven to add on top of the V_{th} shift (cf. Fig. 5.9), thus they can simply be added to the V_{shift} from (36) as

$$V_{\mathrm{th}} = V_{\mathrm{shift}} + V_{\mathrm{weak}} + V_{\mathrm{inst}} \tag{40}$$

creating a unified V_{th} model. In order to include the behavior of the V_{th} instabilities into the model, the observable memory effect needs to be reproduced utilizing a time- and bias-dependent approach. For this purpose, an exemplary model is developed covering the behavior of the V_{DS}-induced V_{th} instability.

The origin of V_{th} instabilities can be ascribed to carrier trapping, accumulation, and depletion mechanisms, which alter the effective charge within the gate stacks (cf. Sec. 3.3). This charge determines the potential of the p-GaN layer that directly correlates with the potential well forming the 2DEG density. However, these effects are temporal, so their emergence and disappearance must be memorized depending on the applied bias and its duration. For this purpose, an auxiliary voltage V_{M} is introduced that covers the memory effect, which is defined as

$$V_{\mathrm{M}} = V_{\mathrm{DS,in}} - \tau_{\mathrm{DS,in}} \cdot \mathrm{ddt}(V_{\mathrm{M}}). \tag{41}$$

In order to actually store the information, an additional Verilog-A simulation node is included in the model, serving as the reference point of the memory voltage V_{M}. Now, the behavior and the value of the V_{M} storage can be adjusted by the voltage-dependent change $V_{\mathrm{DS,in}}$ and its time dependency $\tau_{\mathrm{DS,in}}$.

The margin of change can be estimated by looking at the measurement results investigating the V_{DS}-induced V_{th} instability in Fig. 5.9. Here, the impact applying V_{DS} for 100 s during the off-state (HSF) is compared with an application during the on-state (FUL), as detailed in Fig. 4.9. The result of this is that in both cases an initial V_{th} shift occurs, which tends to spread out for voltages above $V_{\mathrm{DS}} > 50\,\mathrm{V}$. Although the results of both DUTs behave slightly differently, the mismatch between HSF and FUL ends by about 100 mV at high voltages for both. Aiming for a unified model approach, the resulting description of the voltage-dependent change $V_{\mathrm{DS,in}}$ is

$$V_{\mathrm{DS,in}} = \Delta V_{\mathrm{DS,in}} \cdot \left(\frac{1}{2} \cdot \big(\tanh(V_{\mathrm{DS}} - V_{\mathrm{TVI}}) + 1 \big) \right). \tag{42}$$

Here, it is assumed that there is no V_{th} instability for voltages below $V_{\mathrm{DS}} = V_{\mathrm{TVI}}$ of 50 V which then rises to $\Delta V_{\mathrm{DS,in}} = 100\,\mathrm{mV}$ and remains constant until the maximum V_{DS}. Here, the overall change is defined as $\Delta V_{\mathrm{DS,in}}$ and the onset as V_{TVI}.

Although the V_{DS}-induced V_{th} instability largely depends on the drain bias, several measurements have shown that its duration correlates with the gate bias V_{GS}, see Sec. 5.1.1. For an operation with a low V_{GS} that is close to V_{th} this duration is found to be around 100 ms (cf. Fig. 5.1). On the other hand, at the nominal V_{GS}, this can decrease to 1 ms or eventually even further for increased voltages (cf. Fig. 5.4). Thus, the time-dependency of the V_{th} instability $\tau_{\mathrm{DS,in}}$ is defined as

$$\tau_{\mathrm{DS,in}} = \Delta \tau_{\mathrm{DS,in}} \big(\tanh(-V_{\mathrm{GS}}) + 1 \big) \tag{43}$$

The necessary parameters of the V_{th} instability model are listed in Tab. 6.11. Similar to the V_{th} shift model, all parameters are acquired by measurements or determined empirically and remain unaffected by the optimization procedure.

The V_{DS}-induced V_{th} instability is demonstrated by transient I_{D} simulations depicted in Fig. 6.13, comparing both DUTs. To showcase the impact of the V_{th} instability, two V_{DS} driving conditions FUL and HSF are compared. Here, the HSF

Table 6.11: Constant parameters of the V_{th} instability model.

Parameter	Description	Unit	Value
$\Delta V_{\mathrm{DS,in}}$	Maximum change of $V_{\mathrm{DS,in}}$	V	$100 \cdot 10^{-3}$
$\Delta \tau_{\mathrm{DS,in}}$	Maximum change of $\tau_{\mathrm{DS,in}}$	s	1
V_{TVI}	Onset of V_{th} instability	V	50

corresponds to an off-state duration of 100 s and FUL to 0 s. Furthermore, each DUT is simulated at three different V_{GS}, and V_{DS} is set to 100 V to actually obtain results. Finally, $\Delta V_{\mathrm{DS,in}}$ is significantly increased to 500 mV for illustrative purposes, which allows to observe the differences up to high voltages.

The results show that the transient I_{D} without applying any off-state bias (FUL) is initially high but then drops down after a V_{GS}-dependent duration to a lower value. In comparison, the I_{D} with off-state stress (HSF) does remain constant for the whole duration. Consequently, it can be stated that the applied V_{DS} during the on-state causes some charging mechanism that ultimately lowers the overall current. This observation goes well with the fact that the uncharged-state I_{D} (FUL) does eventually converge with the current representing the charged-state (HSF).

Apart from applying very long on- and off-state durations, the impact of the V_{DS}-induced V_{th} instability can also be observed in a pulsed operation. For this

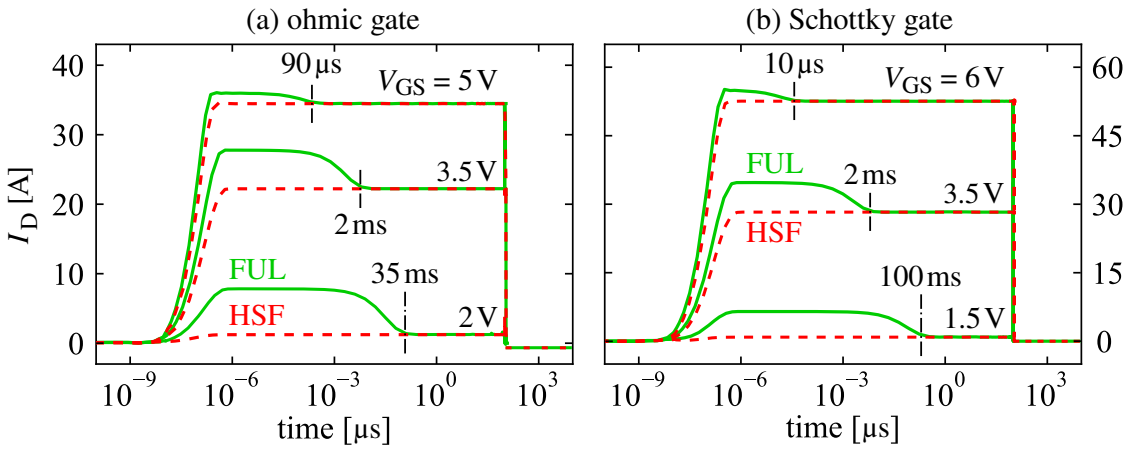

Figure 6.13: Transient I_{D} simulation, showing the impact of the V_{th} instability by comparing the application of on-state V_{DS} (FUL) with off-state V_{DS} (HSF) at 100 V.

purpose, a constant V_{DS} of 100 V is applied in FUL operation while pulsing V_{GS} with a constant on-state duration t_{on} of 1 µs, comparing the impact of two different off-state durations t_{off}, as shown in Fig. 6.14(a). Looking at the respective transient current waveforms in Fig. 6.14(b), with a very short t_{off} of only 0.2 µs the I_D tends to drop from 30 A to 28 A within about 400 µs of operation. However, with a ten times increase t_{off} of only 2 µs this increases to about 1 ms. For an increased t_{off}, the total duration for charge storage shrinks, while the stored charge eventually discharges. This behavior appears sufficiently covered by the memory voltage V_M.

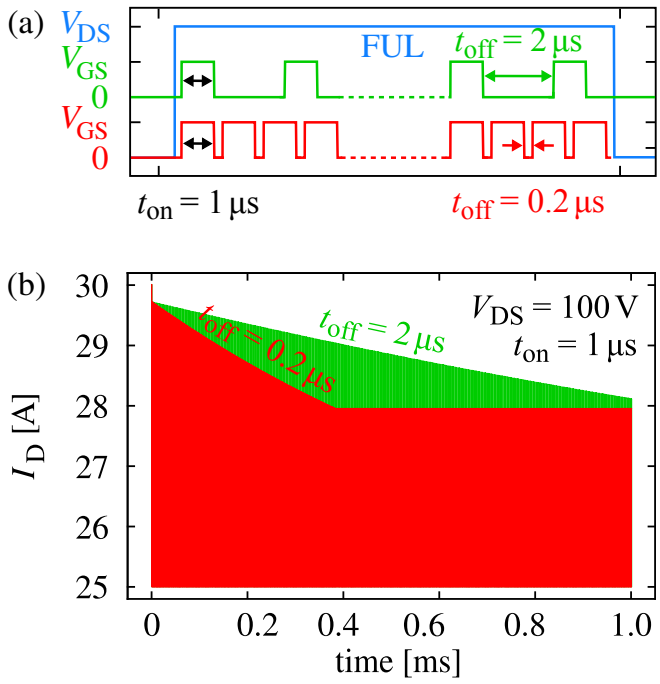

Figure 6.14: Transient I_D simulation, showing the impact of the V_{th} instability by comparing the a pulse operation with different off-state durations t_{off}.

Finally, implementing the V_{th} model can significantly increase runtime if done wrong. Since the model consists of mathematical equations that describe the effects, it might be obvious to define a model variable V_{th} and assign all equations to it. Then, during e.g., the translation from Verilog-A to LTspice, all assigned equations would be deployed in every other equation containing V_{th}. However, this can be circumvented by defining V_{th} as a virtual node, which yields a runtime of 2.5 s.

Although the duration is already quite acceptable, the model is further streamlined by setting the Schroedinger's transition functions G_{SP} defined as (8) in the drain model to zero. However, this is justifiable since the streamlined model does not necessarily reduce accuracy while its simulation speed significantly increases. Consequently, this results in a total runtime duration of 1.5 s, which is quite competitive compared to other compact models. Lastly, all shown simulation results are actually acquired using the streamlined model.

Chapter 7

Conclusion and Future Work

In order to investigate the V_{th} behavior of commercially available state-of-the-art p-gate GaN HEMTs, a custom pulse setup is developed offering high-resolution fast-switching measurements for pulse durations from 100 ns up to 100 s. For the investigation, a three-level gate driver is developed, improving the measurement possibilities. Furthermore, a thermal model is utilized to exclude the impact of self-heating, which recalculates its impact for elevated operation.

The applied drain-source voltage V_{DS} can yield a static V_{th} shift caused by a capacitive coupling into the gate stack resulting in a potential elevation with subsequent gate barrier lowering. Consequently, the 2DEG density below the gate increases, resulting in less gate-source voltage V_{GS} required for the turn-on. The V_{th} shift is shown to occur in the range of low V_{DS} up to 100 V, which tends to saturate afterward, remaining constant up to the maximum of 600 V. In case of the ohmic-gate DUT, a shift of about 200 mV is observable, which, in turn, reaches up to 700 mV for the Schottky-gate DUT. Furthermore, for the ohmic DUT, a weakening of the V_{th} shift is observed that appears to correlate with the onset of hole injection that origins from its additional hybrid drain structure.

If V_{DS} is applied for a long duration (e.g., during off-state), a dynamic V_{th} instability can appear, which is also observable for and even appears to correlate with V_{GS}. Here, the instability is caused by mechanisms of carrier trapping, accumulation, and depletion that occur in the gate stack, which subsequently impact the 2DEG too. These mechanisms tend to converge to a neutral state over time, which accelerates at increased on-state V_{GS}. However, at nominal V_{GS} the convergence can still require durations between 10 µs to 1 ms, which substantially increases up to 100 s for operation close to the threshold.

Considering the observations of the measurements, the behavior of the V_{th} instabilities can be correlated to their physical mechanisms. Applying a positive V_{GS} causes electron trapping and depletion, which yields a positive V_{th} instability. For increased durations and operation at nominal V_{GS}, holes can be injected, which either

neutralize electrons or get trapped, too, causing a negative V_{th} instability. Negative V_{GS} can result in electron trapping and a positive V_{th} instability, which might be neutralized by hole injection. In turn, at negative V_{GS}, the injection depends on the Schottky barrier and does only occur for the ohmic-gate DUT, which then yields a negative V_{th} instability. However, the impact on the Schottky-gate DUT is much more severe, leading to an overall V_{th} instability that can change in the range of 2 V depending on the applied V_{GS}. In comparison, for the ohmic-gate DUT the range is only 200 mV. Apart from that, the V_{GS} conditions causing an V_{th} instability appear also to impact the short-circuit capability. Furthermore, the V_{th} shift is observed to alter with device degradation during repetitive short-circuit measurements.

Since none of the available p-gate GaN HEMTs models include the V_{th} behavior, a physically-based compact model is developed considering the V_{th} shift and the V_{DS}-induced instability. The model development is done in Verilog-A and aims for scaleability toward different devices, currents, and voltages. This can be adjusted utilizing a parameter extraction strategy to create fitting models from information available in datasheets of the DUTs.

The model core is developed from a surface-potential approach covering the drain path that is extended by Poole-Frenkel emission and Fowler-Nordheim tunneling covering the conduction in the gate stack. The developed V_{th} shift model is based on the gate SCR capacitances and also covers the weakening effect due to hole injection. Finally, a time-dependent approach demonstrates the impact of the V_{DS}-induced V_{th}-instability. In the end, the developed V_{th} model shows a satisfying agreement with the measurement results while maintaining a simple and physically-based approach that can easily be implemented in analytical compact models.

Extensive Experimental Investigation

In order to improve the quality of the model, the estimation of the parameter extraction, and the accuracy of the optimization strategy, it is suggested to extend the experimental investigation. The investigation should cover more devices with different current and voltage ratings and those available from other manufacturers. Furthermore, the temperature impact needs to be investigated and included in the model, which remains an open task to complement the model predictability.

Since reliability concerns are shown to correlate with V_{th}, more emphasis should be placed on understanding the fundamental physical mechanisms. An extensive investigation of the V_{th}-depended short-circuit save operating could help to predict fail-save operations. Furthermore, the degradation is shown to be accompanied by an additional V_{th} shift, which could be used for health monitoring, preemptively preventing aging-induced failures. However, for that purpose, a live V_{th} measurement needs to be developed in the first place. This could indirectly be done by determining the Miller-plateau during inductive switching, which has been shown to correlate with mechanisms causing a V_{th} shift in SiC MOSFETs [139].

Improvement of the Compact Model

In order to improve the physical validity of the model, some fundamental assumptions should be reviewed or extended. The behavior of the V_{th} shift is modeled by the SCR capacitances but solely parameterized from measurements. In order to predict the V_{th} behavior for devices with different voltage or current ratings, parameters such as $V_{\mathrm{th,min}}$ or $V_{\mathrm{th,max}}$ should be determined by their physical relation. This could be done by correlating the floating p-GaN potential with the 2DEG density. Furthermore, the p-GaN potential should also depend on its doping N_{A}, which could be modified by the effective charge of the V_{th} instabilities.

The approach of the V_{DS}-induced V_{th} instability shows that it is possible to integrate the bias- and time-dependent functionality into the model, while considering the memory effect. Since the results appear to be sufficient, the approach is also proposed to integrate the V_{GS}-induced V_{th} instabilities.

Abbrevations

2DEG	Two-Dimensional Electron Gas
AC	Alternating Current
Al	Aluminum
Al_2O_3	Aluminum Oxide
AlGaN	Aluminum Gallium Nitride
AlN	Aluminium Nitride
Angelov-GaN	Angelov GaN FET model
ASM-HEMT	Advanced Spice Model for HEMTs
Au	Gold
AWG	Arbitrary Waveform Generator
C	Carbon
CFET	Curtice-Cubic GaAs FET model
CMOS	Complementary Metal-Oxide-Semiconductor
DC	Direct Current
DIBL	Drain-Induced Barrier Lowering
DUT	Device Under Test
EEHEMT	EEsof scalable nonlinear HEMT model
Fe	Iron
FN	Fowler-Nordheim
FUL	Fault Under Load
Ga	Gallium
GaAs	Gallium Arsenid
GaN	Gallium Nitride
GDCBL	Gate/Drain Coupled Barrier Lowering
GIT	Gate Injection Transistor
HBS	Half-Bridge Supply
HEMT	High Electron Mobility Transistor
HNO_3	Nitric Acid
HS	High Side

HSF	Hard Switching Fault
IGBT	Insulated Gate Bipolar Transistor
LS	Low Side
MIS	Metal Insulator Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MVSG	MIT Virtual Source GaN FET model
N	Nitrogen
Ni	Nickel
PE	Power Electronic
PF	Poole-Frenkel
SC	Short Circuit
SCR	Space Charge Region
Si	Silicon
Si_3N_4	Silicon Nitride
SiC	Silicon Carbide
SiN	Silicon Mononitride
SMU	Source Measure Unit
SP	Surface Potential
TE	Thermionic Emission
Ti	Titanium
WBG	Wide Band Gap

Symbols

a	Crystal lattice constant (nm)
c	Crystal unit cell size (nm)
C_{DC}	DC-link capacitance (F)
C_{DS}	Drain-source capacitance (F)
C_{DS0}	Drain-source vapacitance at 0 V (F)
C_{DS1}	Drain-source capacitance at 600 V (F)
C'_{g}	Gate sheet capacitance ($\mathrm{F/m^2}$)
C_{GD}	Gate-drain capacitance (F)
C_{GD0}	Gate-drain capacitance at 0 V (F)
C_{GD1}	Gate-drain capacitance at 600 V (F)
C_{GS}	Gate-source capacitance (F)
C_{GS0}	Gate-source capacitance at 0 V (F)
C_{GS1}	Gate-source capacitance at 600 V (F)
C_{ISS}	Input capacitance (F)
C_{OSS}	Output capacitance (F)
C_{PN}	Space charge capacitance of the p-i-n diode (F)
C_{RSS}	Reverse capacitance (F)
C_{SC}	Space charge capacitance of the Schottky contact (F)
`CAP1`	Fitting constant of the gate-drain capacitance (V)
`CAP2`	Fitting constant of the gate-source capacitance (V)
`CAP3`	Fitting constant of the drain-source capacitance (V)
d_{AlGaN}	Thickness of the AlGaN layer (m)
d_{pGaN}	Thickness of the p-GaN layer (m)
D_{PN}	p-i-n diode ()
D_{SC}	Schottky diode ()
E_{C}	Conduction band energy (eV)
E_{crit}	Critical electrical field (MV/cm)
E_{F}	Fermi energy (eV)
$E_{\mathrm{F,uni}}$	Unified fermi energy (eV)
E_{G}	Bandgap energy (eV)

E_{sc}	Electrical field in the Schottky contact (eV)
ϵ_0	Vacuum permitivity (F/m)
$\epsilon_{\mathrm{AlGaN}}$	Relative permitivity of aluminium gallium nitride ()
ϵ_{GaN}	Relative permitivity of gallium nitride ()
G_{SP}	Interpolation for Schroedinger Poisson solution ()
γ_1	Constant for Schroedinger-Poisson solution 1 ()
γ_2	Constant for Schroedinger-Poisson solution 2 ()
`GF`	Fitting constant for Fowler-Nordheim tunneling ()
`GP`	Fitting constant for Poole-Frenkel emission ()
`GT`	Fitting constant for thermionic emission ()
H_{SP}	Bias dependency of the 2DEG ()
I_{D}	Drain current (A)
$I_{\mathrm{D,nom}}$	Nominal drain current (A)
I_{FN}	Gate current by Fowler-Nordheim tunneling (A)
I_{G}	Gate current (A)
$I_{\mathrm{G,nom}}$	Nominal gate current (A)
I_{min}	Minimum leakage current (A)
I_{PF}	Gate current by Poole-Frenkel emission (A)
I_{TE}	Gate current by thermionic emission (A)
k_{B}	Boltzmann constant (eV/K)
L	Gate length (m)
`M1`	Fitting constant for mobility degradation 1 (V^{-1})
`M2`	Fitting constant for mobility degradation 2 (V^{-2})
μ_0	Electron low-field mobility (cm^2/Vs)
μ_{deg}	Mobility degradation ()
μ_{sat}	Mobility velocity saturation ()
N_{A}	Doping concentration (cm^{-3})
N_{DOS}	Desity of states in the GaN (cm^{-2})
N_{I}	Intrinsic carrier concentration (cm^{-3})
N_{O}	Ohmic-contact doping (cm^{-3})
P_{PE}	Piezoelectric polarization ($\mathrm{C/m}^2$)
P_{SP}	Spontaneous polarization ($\mathrm{C/m}^2$)

$\Phi_{\mathrm{SP,avg}}$	Average surface potential (V)
Φ_{B}	Gate-metal barrier (eV)
$\Phi_{\mathrm{SP,dif}}$	Differential surface potential (V)
Φ_{E}	Electron emission barrier (eV)
Φ_{SC}	Effective Schottky contact barrier (eV)
Φ_{SP}	Surface potential (V)
$\Phi_{\mathrm{SP,D}}$	Drain-sided surface potential (V)
$\Phi_{\mathrm{SP,S}}$	Source-sided surface potential (V)
$\Phi_{\mathrm{SP,uni}}$	Unified surface potential (V)
$\Delta\Phi_{\mathrm{X}}$	Doping-dependend gate-barrier shift (eV)
q	Electron charge (C)
R_{D}	Drain-region drift and contact resistance (Ω)
$R_{\mathrm{DS,on}}$	Drain-source resistance at on-state (Ω)
R_{G}	Gate-region drift and contact resistance (Ω)
R_{S}	Source-region drift and contact resistance (Ω)
`SAT1`	Fitting constant for saturation 1 (V^{-1})
`SAT2`	Fitting constant for saturation 2 (V^{-1})
T_{amb}	Ambient temperature (K)
t_{bias}	Duration of the biasing phase (s)
$\tau_{\mathrm{DS,in}}$	Time-dependency of the threshold voltage instability (s)
T_{DUT}	Temperature of the device under test (K)
t_{meas}	Duration of the measurement phase (s)
t_{ntr}	Duration of the neutralization phase (s)
t_{off}	Off-state duration (s)
t_{on}	On-state duration (s)
V_{BI}	Built-in voltage (V)
V_{bias}	Gate-driver voltage during biasing phase (V)
V_{D}	Drain potential (V)
V_{DC}	DC-link supply voltage (V)
V_{dov}	Drain-dependent overdrive voltage (V)
V_{DS}	Drain-source voltage (V)
V_{dsat}	Saturation voltage (V)

$V_{\mathrm{DS,in}}$	Voltage-dependency of the threshold voltage instability (V)
$V_{\mathrm{DS,sat}}$	Drain-source saturation voltage (V)
V_{F}	Gate foward breakdown voltage (V)
V_{G}	Gate potential (V)
V_{GD}	Gate-drain voltage (V)
V_{GS}	Gate-source voltage (V)
$V_{\mathrm{GS,nom}}$	Nominal gate-source voltage (V)
V_{HI}	On-set voltage of hybrid-drain-induced hole injection (V)
V_{inst}	Threshold voltage instability (V)
V_{M}	Auxiliary voltage covering the memory effect (V)
V_{meas}	Gate-driver voltage during measurement phase (V)
V_{min}	Minimum bias voltage (V)
V_{ntr}	Gate-driver voltage during neutralization phase (V)
V_{ov}	Overdrive voltage (V)
V_{PN}	Space charge voltage of the p-i-n diode (V)
V_{R}	Gate reverse breakdown voltage (V)
V_{RD}	Voltage-drop over drain drift-resistance (V)
V_{RG}	Voltage-drop over gate drift-resistance (V)
V_{RS}	Voltage-drop over source drift-resistance (V)
V_{S}	Source potential (V)
v_{sat}	Electron saturation velocity (cm/s)
V_{SC}	Space charge voltage of the Schottky contact (V)
V_{shift}	Threshold voltage shift (V)
v_{t}	Thermal voltage (V)
V_{th}	Threshold voltage (V)
$V_{\mathrm{th,hv}}$	Threshold voltage at 600 V (V)
$V_{\mathrm{th,max}}$	Maximum threshold voltage at 1 V (V)
$V_{\mathrm{th,min}}$	Minimum threshold voltage (V)
V_{TVI}	Onset of the threshold voltage instability (V)
V_{weak}	Weakening of the threshold voltage shift (V)
W	Gate width (m)
`WEAK`	Fitting constant of threshold voltage weakening (V)

x_{SC}	Width of the gate space charge region (m)

Bibliography

[1] *Global Energy Review 2021 - Renewables*. https://www.iea.org/reports/global-energy-review-2021/renewables. Accessed: 23-02-2023.

[2] *Unsere Energiewende: sicher, sauber, bezahlbar*. https://www.bmwk.de/Redaktion/DE/Dossier/energiewende.html. Accessed: 23-02-2023.

[3] *HVDC PLUS – the decisive step ahead*. https://assets.siemens-energy.com/siemens/assets/api/uuid:9b6dd359-01b4-4356-9de2-6e7dbb1bb0d0/2022-03-11-hvdc-plus.pdf?ste_sid=6caf0519bc33fd706f19392496824442. Accessed: 23-02-2023.

[4] Infineon. *CoolGaN™ the new power paradigm*. 2019. URL: https://www.infineon.com/dgdl/Infineon-GalliumNitride_CoolGaN_emode_HEMTs-ProductSelectionGuide-v01_01-EN.pdf?fileId=5546d46266f85d630167%200c286baf30a6 (visited on 06/19/2023).

[5] O. Ambacher et al. "Two-dimensional electron gases induced by spontaneous and piezoelectric polarization charges in N- and Ga-face AlGaN/GaN heterostructures". In: *Journal of Applied Physics* 85.6 (1999), pp. 3222–3233. DOI: 10.1063/1.369664.

[6] K. J. Chen et al. "GaN-on-Si Power Technology: Devices and Applications". In: *IEEE Transaction on Electron Devices* 64.3 (Mar. 2017), pp. 779–795. ISSN: 1557-9646. DOI: 10.1109/ted.2017.2657579.

[7] E. A. Jones, F. Wang, and B. Ozpineci. "Application-based review of GaN HFETs". In: *2014 IEEE Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*. Oct. 2014, pp. 24–29. DOI: 10.1109/wipda.2014.6964617.

[8] X. Hu et al. "Enhancement mode AlGaN/GaN HFET with selectively grown pn junction gate". English. In: *Electronics Letters* 36 (8 Apr. 2000), 753–754(1). ISSN: 0013-5194. DOI: 10.1049/el:20000557.

[9] Y. Uemoto et al. “Gate Injection Transistor (GIT) - A Normally-Off AlGaN/-GaN Power Transistor Using Conductivity Modulation”. In: *IEEE Transaction on Electron Devices* 54.12 (Dec. 2007), pp. 3393–3399. ISSN: 0018-9383. DOI: 10.1109/ted.2007.908601.

[10] N. E. Posthuma et al. “An industry-ready 200 mm p-GaN E-mode GaN-on-Si power technology”. In: *2018 IEEE 30th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*. May 2018, pp. 284–287. DOI: 10.1109/ispsd.2018.8393658.

[11] M. A. Khan et al. “Current/voltage characteristic collapse in AlGaN/GaN heterostructure insulated gate field effect transistors at high drain bias”. English. In: *Electronics Letters* 30 (25 Dec. 1994), 2175–2176(1). ISSN: 0013-5194.

[12] R. Vetury et al. “The impact of surface states on the DC and RF characteristics of AlGaN/GaN HFETs”. In: *IEEE Transactions on Electron Devices* 48.3 (Mar. 2001), pp. 560–566. ISSN: 1557-9646. DOI: 10.1109/16.906451.

[13] S.C. Binari et al. “Trapping effects and microwave power performance in AlGaN/GaN HEMTs”. In: *IEEE Transactions on Electron Devices* 48.3 (Mar. 2001), pp. 465–471. ISSN: 1557-9646. DOI: 10.1109/16.906437.

[14] K. Tanaka et al. “Suppression of current collapse by hole injection from drain in a normally-off GaN- based hybrid-drain-embedded gate injection transistor”. In: *Appl.Phys.Lett.* 107 (Oct. 2015). DOI: 10.1063/1.4934184.

[15] L. Efthymiou et al. “Understanding the Threshold Voltage Instability During OFF-State Stress in p-GaN HEMTs”. In: *IEEE Electron Device Letters* 40.8 (Aug. 2019), pp. 1253–1256. ISSN: 1558-0563. DOI: 10.1109/led.2019.2925776.

[16] J. Chen et al. “OFF-state Drain-voltage-stress-induced VTH Instability in Schottky-type p-GaN Gate HEMTs”. In: *IEEE Journal of Emerging and Selected Topics in Power Electronics* (2020), pp. 1–1. ISSN: 2168-6785. DOI: 10.1109/jestpe.2020.3010408.

[17] L. Sayadi et al. “Threshold Voltage Instability in p-GaN Gate AlGaN/-GaN HFETs”. In: *IEEE Transaction on Electron Devices* 65.6 (June 2018), pp. 2454–2460. ISSN: 1557-9646. DOI: 10.1109/ted.2018.2828702.

[18] A. Stockman et al. “Threshold Voltage Instability Mechanisms in p-GaN Gate AlGaN/GaN HEMTs”. In: *2019 31st International Symposium on Power Semiconductor Devices and ICs (ISPSD)*. May 2019, pp. 287–290. DOI: 10.1109/ispsd.2019.8757667.

[19] Muqin Nuo et al. “Gate/Drain Coupled Barrier Lowering Effect and Negative Threshold Voltage Shift in Schottky-Type p-GaN Gate HEMT”. In: *IEEE Transactions on Electron Devices* 69.7 (July 2022), pp. 3630–3635. ISSN: 1557-9646. DOI: 10.1109/TED.2022.3175792.

[20] S. Li et al. “Reliability Concern of 650-V Normally-OFF GaN Devices Under Reverse Freewheeling Stress”. In: *IEEE Transaction on Electron Devices* 67.8 (Aug. 2020), pp. 3492–3495. ISSN: 1557-9646. DOI: 10.1109/ted.2020.2999026.

[21] Y. Q. Chen et al. “Degradation Behavior and Mechanisms of E-Mode GaN HEMTs With p-GaN Gate Under Reverse Electrostatic Discharge Stress”. In: *IEEE Transaction on Electron Devices* 67.2 (Feb. 2020), pp. 566–570. ISSN: 1557-9646. DOI: 10.1109/ted.2019.2959299.

[22] X. Tang et al. “Mechanism of Threshold Voltage Shift in p-GaN Gate AlGaN/GaN Transistors”. In: *IEEE Electron Device Letters* 39.8 (June 2018), pp. 1145–1148. ISSN: 1558-0563. DOI: 10.1109/led.2018.2847669.

[23] Xueyang Li et al. “Charge trapping related channel modulation instability in p-GaN gate HEMTs”. In: *Microelectronics Reliability* 65 (2016), pp. 35–40. ISSN: 0026-2714. DOI: 10.1016/j.microrel.2016.07.040.

[24] Y. Shi et al. “Carrier Transport Mechanisms Underlying the Bidirectional VTH Shift in p-GaN Gate HEMTs Under Forward Gate Stress”. In: *IEEE Transaction on Electron Devices* 66.2 (Feb. 2019), pp. 876–882. ISSN: 1557-9646. DOI: 10.1109/ted.2018.2883573.

[25] S. Huang et al. “Characterization of Vth-instability in Al2O3/GaN/AlGaN/-GaN MIS-HEMTs by quasi-static C-V measurement”. In: *physica status solidi c* 9.3-4 (2012), pp. 923–926. DOI: 10.1002/pssc.201100302.

[26] Kalparupa Mukherjee et al. “Analysis of threshold voltage instabilities in semi-vertical GaN-on-Si FETs”. In: *Applied Physics Express* 13.2 (Jan. 2020), p. 024004. DOI: 10.35848/1882-0786/ab6ddd.

[27] A. Toriumi, M. Iwase, and M. Yoshimi. “On the performance limit for Si MOSFET’s: experimental study”. In: *IEEE Transactions on Electron Devices* 35.7 (July 1988), pp. 999–1003. ISSN: 1557-9646. DOI: 10.1109/16.3357.

[28] F. Assad et al. “On the performance limits for Si MOSFETs: a theoretical study”. In: *IEEE Transactions on Electron Devices* 47.1 (Jan. 2000), pp. 232–240. ISSN: 1557-9646. DOI: 10.1109/16.817590.

[29] Noriyuki Iwamuro. “Recent progress of power semiconductor devices and their futures”. In: *2017 IEEE CPMT Symposium Japan (ICSJ)*. Nov. 2017, pp. 191–194. DOI: 10.1109/ICSJ.2017.8240114.

[30] *Odyssey Semi - Why GaN?* https://www.odysseysemi.com/technology. Accessed: 24-02-2023.

[31] Josef Lutz et al. *Semiconductor Power Devices*. Chemnitz, Germany: Springer, 2017.

[32] Noriyuki Iwamuro. “Recent Progress of SiC-MOSFETs and Their Futures-Competion with state-of-the-art Si-IGBT-”. In: *2019 International Conference on Electronics Packaging (ICEP)*. Apr. 2019, pp. 260–264. DOI: 10.23919/ICEP.2019.8733597.

[33] *Automotive GaN FETs engineered for high frequency and robustness in HEV/EVs*. https://e2e.ti.com/blogs_/b/powerhouse/posts/charge-faster-and-drive-farther-with-gan-based-onboard-charger-in-electric-vehicles. Accessed: 24-02-2023.

[34] Noriyuki Iwamuro and Thomas Laska. “IGBT History, State-of-the-Art, and Future Prospects”. In: *IEEE Transactions on Electron Devices* 64.3 (Mar. 2017), pp. 741–752. ISSN: 1557-9646. DOI: 10.1109/TED.2017.2654599.

[35] R. Dingle et al. “Electron mobilities in modulation-doped semiconductor heterojunction superlattices”. In: *Applied Physics Letters* 33.7 (1978), pp. 665–667. DOI: 10.1063/1.90457.

[36] Christian De Brida. “Gallium Nitride simulations using Sentaurus software”. dissertation. University of Padova, 2010.

[37] Rüdiger Quay. *Gallium Nitride Electronics*. Freiburg, Germany: Springer, 2008.

[38] Hannes Behmenburg. “Comprehensive study on MOVPE of InAlN/GaN HEMT structures and GaN nanowires”. dissertation. Rheinisch-Westfälischen Technischen Hochschule Aachen, 2013.

[39] C. X. Ren. “Polarisation fields in III-nitrides: effects and control”. In: *Materials Science and Technology* 32.5 (2016), pp. 418–433. DOI: 10.1179/1743284715Y.0000000103.

[40] Gerrit Lükens. “Normally-off Transistor Topologies in Gallium Nitride Technology”. dissertation. Rheinisch-Westfälischen Technischen Hochschule Aachen, 2020.

[41] Olivier Jardel et al. “Electrical performances of AlInN/GaN HEMTs. A comparison with AlGaN/GaN HEMTs with similar technological process”. In: *International Journal of Microwave and Wireless Technologies* 3.3 (2011), pp. 301–309. DOI: 10.1017/S1759078711000419.

[42] J. P. Ibbetson et al. “Polarization effects, surface states, and the source of electrons in AlGaN/GaN heterostructure field effect transistors”. In: *Applied Physics Letters* 77.2 (2000), pp. 250–252. DOI: 10.1063/1.126940.

[43] Sten Heikman et al. “Polarization effects in AlGaN/GaN and GaN/AlGaN/-GaN heterostructures”. In: *Journal of Applied Physics* 93.12 (2003), pp. 10114–10118. DOI: 10.1063/1.1577222.

[44] Takashi Mimura et al. “A New Field-Effect Transistor with Selectively Doped GaAs/n-AlxGa1-xAs Heterojunctions”. In: *Japanese Journal of Applied Physics* 19.5 (May 1980), pp. L225–L227. DOI: 10.1143/jjap.19.l225.

[45] Malay Trivedi and Krishna Shenai. "Performance evaluation of high-power wide band-gap semiconductor rectifiers". In: *Journal of Applied Physics* 85.9 (1999), pp. 6889–6897. DOI: 10.1063/1.370208.

[46] H. Wang et al. "Maximizing the Performance of 650-V p-GaN Gate HEMTs: Dynamic RON Characterization and Circuit Design Considerations". In: *IEEE Transactions on Power Electronics* 32.7 (July 2017), pp. 5539–5549. ISSN: 1941-0107. DOI: 10.1109/TPEL.2016.2610460.

[47] Thomas Butcher and Teresa Brown. "Gallium". In: *Critical Metals Handbook*. John Wiley & Sons, Ltd, 2014. Chap. 7, pp. 150–176. ISBN: 9781118755341. DOI: https://doi.org/10.1002/9781118755341.ch7.

[48] "Bücher". In: *International Journal of Materials Research* 92.5 (2001), pp. 505–507. DOI: doi:10.3139/ijmr-2001-0101.

[49] *Toyoda Gosei Succeeds in Making Larger GaN Substrates for Next-Generation Power Devices*. https://www.toyoda-gosei.com/news/detail/?id=306. Accessed: 06-12-2022.

[50] Michael Marks, Zainuriah Hassan, and K.Y. Cheong. "Ultrathin Wafer Pre-Assembly and Assembly Process Technologies: A Review". In: *Critical Reviews in Solid State and Materials Sciences* 40 (May 2015), pp. 1–40. DOI: 10.1080/10408436.2014.992585.

[51] *HexaTech Investment Accelerates 100 mm Diameter Aluminum Nitride Substrate Program*. https://www.prnewswire.com/news-releases/hexatech-investment-accelerates-100-mm-diameter-aluminum-nitride-substrate-program-301639906.html. Accessed: 08-12-2022.

[52] *SiC Power Devices: Lowering Costs to Drive Adoption*. https://www.powerelectronicsnews.com/sic-power-devices-lowering-costs-to-drive-adoption/. Accessed: 08-12-2022.

[53] Armin Dadgar. "Sixteen years GaN on Si". In: *physica status solidi (b)* 252.5 (2015), pp. 1063–1068. DOI: https://doi.org/10.1002/pssb.201451656.

[54] D. Marcon, Y. N. Saripalli, and S. Decoutere. “200mm GaN-on-Si epitaxy and e-mode device technology”. In: *2015 IEEE International Electron Devices Meeting (IEDM)*. Dec. 2015, pp. 16.2.1–16.2.4. DOI: 10.1109/IEDM.2015.7409709.

[55] Xiaoguang He et al. “Step-Graded AlGaN vs superlattice: role of strain relief layer in dynamic on-resistance degradation”. In: *Applied Physics Express* 15.1 (Dec. 2021), p. 011001. DOI: 10.35848/1882-0786/ac3dc0.

[56] Eldad Bahat-Treidel et al. “AlGaN/GaN/GaN:C Back-Barrier HFETs With Breakdown Voltage of Over 1 kV and Low Ron/A”. In: *IEEE Transactions on Electron Devices* 57.11 (Nov. 2010), pp. 3050–3058. ISSN: 1557-9646. DOI: 10.1109/TED.2010.2069566.

[57] Johan Bergsten et al. “AlGaN/GaN high electron mobility transistors with intentionally doped GaN buffer using propane as carbon precursor”. In: *Japanese Journal of Applied Physics* 55.5S (Mar. 2016), 05FK02. DOI: 10.7567/JJAP.55.05FK02.

[58] M. Asif Khan et al. “GaN-AlxGa1−xN Heterostructures Deposition by Low Pressure Metalorganic Chemical Vapor Deposition for Metal Insulator Semiconductor Field Effect Transistor (Misfet) Devices”. In: *MRS Proceedings* 281 (1992), p. 769. DOI: 10.1557/PROC-281-769.

[59] Yong Cai et al. “High-performance enhancement-mode AlGaN/GaN HEMTs using fluoride-based plasma treatment”. In: *IEEE Electron Device Letters* 26.7 (July 2005), pp. 435–437. ISSN: 1558-0563. DOI: 10.1109/LED.2005.851122.

[60] Rongming Chu et al. “1200-V Normally Off GaN-on-Si Field-Effect Transistors With Low Dynamic on -Resistance”. In: *IEEE Electron Device Letters* 32.5 (May 2011), pp. 632–634. ISSN: 1558-0563. DOI: 10.1109/LED.2011.2118190.

[61] Nobuo Kaneko et al. “Normally-off AlGaN/GaN HFETs using NiOx gate with recess”. In: *2009 21st International Symposium on Power Semiconductor Devices (ISPSD)*. June 2009, pp. 25–28. DOI: 10.1109/ISPSD.2009.5157992.

[62] K. Ota et al. “A normally-off GaN FET with high threshold voltage uniformity using a novel piezo neutralization technique”. In: *2009 IEEE International Electron Devices Meeting (IEDM)*. Dec. 2009, pp. 1–4. DOI: 10.1109/IEDM.2009.5424398.

[63] Arno Stockman and Peter Moens. “ON-State Gate Stress Induced Threshold Voltage Instabilities in p-GaN Gate AlGaN/GaN HEMTs”. In: *2020 IEEE International Integrated Reliability Workshop (IIRW)*. Oct. 2020, pp. 1–4. DOI: 10.1109/IIRW49815.2020.9312869.

[64] Hao Lu et al. “Improved Ohmic Contact Performance on Undoped AlGaN/-GaN HEMTs Using by Ternary Alloy Predeposition”. In: *2021 18th China International Forum on Solid State Lighting & 2021 7th International Forum on Wide Bandgap Semiconductors (SSLChina: IFWS)*. Dec. 2021, pp. 65–67. DOI: 10.1109/SSLChinaIFWS54608.2021.9675188.

[65] Tohru Oka et al. “Over 10 a operation with switching characteristics of 1.2 kV-class vertical GaN trench MOSFETs on a bulk GaN substrate”. In: *2016 28th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*. June 2016, pp. 459–462. DOI: 10.1109/ISPSD.2016.7520877.

[66] Chirag Gupta et al. “In Situ Oxide, GaN Interlayer-Based Vertical Trench MOSFET (OG-FET) on Bulk GaN substrates”. In: *IEEE Electron Device Letters* 38.3 (Mar. 2017), pp. 353–355. ISSN: 1558-0563. DOI: 10.1109/LED.2017.2649599.

[67] Min Sun et al. “High-Performance GaN Vertical Fin Power Transistors on Bulk GaN Substrates”. In: *IEEE Electron Device Letters* 38.4 (Apr. 2017), pp. 509–512. ISSN: 1558-0563. DOI: 10.1109/LED.2017.2670925.

[68] Dinesh Ramanathan. “Re-inventing Power Electronics: NexGen Power Systems with Vertical GaN(TM)”. In: *PCIM Europe 2022; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*. May 2022, pp. 1–8. DOI: 10.30420/565822137.

[69] T.A. Fjeldly and M. Shur. "Threshold voltage modeling and the subthreshold regime of operation of short-channel MOSFETs". In: *IEEE Transactions on Electron Devices* 40.1 (Jan. 1993), pp. 137–145. ISSN: 1557-9646. DOI: 10.1109/16.249436.

[70] G. Meneghesso et al. "Surface-related drain current dispersion effects in AlGaN-GaN HEMTs". In: *IEEE Transactions on Electron Devices* 51.10 (Oct. 2004), pp. 1554–1561. ISSN: 1557-9646. DOI: 10.1109/TED.2004.835025.

[71] Hideki Hasegawa et al. "Mechanisms of current collapse and gate leakage currents in AlGaN/GaN heterostructure field effect transistors". In: *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena* 21.4 (2003), pp. 1844–1855. DOI: 10.1116/1.1589520.

[72] T. Mizutani et al. "A study on current collapse in AlGaN/GaN HEMTs induced by bias stress". In: *IEEE Transactions on Electron Devices* 50.10 (Oct. 2003), pp. 2015–2020. ISSN: 1557-9646. DOI: 10.1109/TED.2003.816549.

[73] S.C. Binari et al. "Fabrication and characterization of GaN FETs". In: *Solid-State Electronics* 41.10 (1997). Proceedings of the Topical Workshop on Heterostructure of Microlectronics, pp. 1549–1554. ISSN: 0038-1101. DOI: https://doi.org/10.1016/S0038-1101(97)00103-2.

[74] P. B. Klein et al. "Observation of deep traps responsible for current collapse in GaN metal–semiconductor field-effect transistors". In: *Applied Physics Letters* 75.25 (1999), pp. 4016–4018. DOI: 10.1063/1.125523.

[75] Kazushige Horio et al. "Physics-based simulation of buffer-trapping effects on slow current transients and current collapse in GaN field effect transistors". In: *Journal of Applied Physics* 98.12 (2005), p. 124502. DOI: 10.1063/1.2141653.

[76] Naohiro Tsurumi et al. "AlN Passivation Over AlGaN/GaN HFETs for Surface Heat Spreading". In: *IEEE Transactions on Electron Devices* 57.5 (May 2010), pp. 980–985. ISSN: 1557-9646. DOI: 10.1109/TED.2010.2044675.

[77] P. Moens et al. “An industrial process for 650V rated GaN-on-Si power devices using in-situ SiN as a gate dielectric”. In: *2014 IEEE 26th International Symposium on Power Semiconductor Devices IC's (ISPSD)*. June 2014, pp. 374–377. DOI: 10.1109/ISPSD.2014.6856054.

[78] Michael J. Uren, Janina Moreke, and Martin Kuball. “Buffer Design to Minimize Current Collapse in GaN/AlGaN HFETs”. In: *IEEE Transactions on Electron Devices* 59.12 (Dec. 2012), pp. 3327–3333. ISSN: 1557-9646. DOI: 10.1109/TED.2012.2216535.

[79] Hou-Yu-Wang et al. “Effects of the Fe-doped GaN buffer in AlGaN/GaN HEMTs on SiC substrate”. In: *2015 IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC)*. June 2015, pp. 645–648. DOI: 10.1109/EDSSC.2015.7285198.

[80] M.J. Uren et al. “Punch-through in short-channel AlGaN/GaN HFETs”. In: *IEEE Transactions on Electron Devices* 53.2 (Feb. 2006), pp. 395–398. ISSN: 1557-9646. DOI: 10.1109/TED.2005.862702.

[81] Wataru Saito et al. “Influence of electric field upon current collapse phenomena and reliability in high voltage GaN-HEMTs”. In: *2010 22nd International Symposium on Power Semiconductor Devices IC's (ISPSD)*. June 2010, pp. 339–342.

[82] A. Koudymov et al. “Mechanism of current collapse removal in field-plated nitride HFETs”. In: *IEEE Electron Device Letters* 26.10 (Oct. 2005), pp. 704–706. ISSN: 1558-0563. DOI: 10.1109/LED.2005.855409.

[83] Yasuhiro Uemoto et al. “A Normally-off AlGaN/GaN Transistor with R=2.6mΩ and BV=640V Using Conductivity Modulation”. In: *2006 International Electron Devices Meeting*. Dec. 2006, pp. 1–4. DOI: 10.1109/IEDM.2006.346930.

[84] Kenichiro Tanaka et al. “Effects of Deep Trapping States at High Temperatures on Transient Performance of AlGaN/GaN Heterostructure Field-Effect Transistors”. In: *Japanese Journal of Applied Physics* 52.4S (Apr. 2013), 04CF07. DOI: 10.7567/jjap.52.04cf07.

[85] Saichiro Kaneko et al. “Current-collapse-free operations up to 850 V by GaN-GIT utilizing hole injection from drain”. In: *2015 IEEE 27th International Symposium on Power Semiconductor Devices IC's (ISPSD)*. May 2015, pp. 41–44. DOI: 10.1109/ISPSD.2015.7123384.

[86] A.A. Mutlu and M. Rahman. “Two-dimensional analytical model for drain induced barrier lowering (DIBL) in short channel MOSFETs”. In: *Proceedings of the IEEE SoutheastCon 2000. 'Preparing for The New Millennium' (Cat. No.00CH37105)*. Apr. 2000, pp. 340–344. DOI: 10.1109/SECON.2000.845589.

[87] Mojtaba Allaei, Majid Shalchian, and Farzan Jazaeri. “Modeling of Short-Channel Effects in GaN HEMTs”. In: *IEEE Transactions on Electron Devices* 67.8 (Aug. 2020), pp. 3088–3094. ISSN: 1557-9646. DOI: 10.1109/TED.2020.3005122.

[88] K. Murukesan, L. Efthymiou, and F. Udrea. “Gate stress induced threshold voltage instability and its significance for reliable threshold voltage measurement in p-GaN HEMT”. In: *2019 IEEE 7th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*. Oct. 2019, pp. 177–180. DOI: 10.1109/wipda46397.2019.8998859.

[89] J. He, G. Tang, and K. J. Chen. “VTH Instability of p-GaN Gate HEMTs Under Static and Dynamic Gate Stress”. In: *IEEE Electron Device Letters* 39.10 (Oct. 2018), pp. 1576–1579. ISSN: 1558-0563. DOI: 10.1109/led.2018.2867938.

[90] S. Yang et al. “Identification of Trap States in p-GaN Layer of a p-GaN/AlGaN/GaN Power HEMT Structure by Deep-Level Transient Spectroscopy”. In: *IEEE Electron Device Letters* 41.5 (May 2020), pp. 685–688. ISSN: 1558-0563. DOI: 10.1109/led.2020.2980150.

[91] Chi Zhang et al. “Electrical Degradations of p-GaN HEMT under High Off-state Bias Stress with Negative Gate Voltage”. In: *2019 IEEE 26th International Symposium on Physical and Failure Analysis of Integrated Circuits (IPFA)*. July 2019, pp. 1–4. DOI: 10.1109/IPFA47161.2019.8984885.

[92] A. Stockman et al. “Gate Conduction Mechanisms and Lifetime Modeling of p-Gate AlGaN/GaN High-Electron-Mobility Transistors”. In: *IEEE Transaction on Electron Devices* 65.12 (Dec. 2018), pp. 5365–5372. ISSN: 1557-9646. DOI: 10.1109/ted.2018.2877262.

[93] B. Bakeroot et al. “Analytical Model for the Threshold Voltage of p-(Al)GaN High-Electron-Mobility Transistors”. In: *IEEE Transaction on Electron Devices* 65.1 (Jan. 2018), pp. 79–86. ISSN: 1557-9646. DOI: 10.1109/ted.2017.2773269.

[94] M. Ruzzarin et al. “Degradation Mechanisms of GaN HEMTs With p-Type Gate Under Forward Gate Bias Overstress”. In: *IEEE Transaction on Electron Devices* 65.7 (July 2018), pp. 2778–2783. ISSN: 1557-9646. DOI: 10.1109/ted.2018.2836460.

[95] M. Ge et al. “Gate Reliability of p-GaN Gate AlGaN/GaN High Electron Mobility Transistors”. In: *IEEE Electron Device Letters* 40.3 (Mar. 2019), pp. 379–382. ISSN: 1558-0563. DOI: 10.1109/led.2019.2893290.

[96] Infineon. *IGT60R190D1S - 600V CoolGaN™ enhancement-mode Power Transistor*. 2020. URL: https://www.infineon.com/dgdl/Infineon-IGT60R190D1S-DataSheet-v03_12-EN.pdf?fileId=5546d46265f064ff016685fa29796520 (visited on 05/20/2022).

[97] GaN Systems. *GS66504B - Bottom-side cooled 650 V E-mode GaN transistor*. 2018. URL: https://gansystems.com/wp-content/uploads/2018/04/GS66504B-DS-Rev-180422.pdf (visited on 05/20/2022).

[98] Keysight. *B1505A Power Device Analyzer / Curve Tracer*. 2022. URL: https://www.keysight.com/de/de/assets/7018-02115/data-sheets/5990-3853.pdf (visited on 03/01/2023).

[99] Keysight. *33500B and 33600A Series Trueform Waveform Generators*. 2022. URL: https://www.keysight.com/de/de/assets/7018-05928/data-sheets/5992-2572.pdf (visited on 03/01/2023).

[100] Toshiba. *Photocouplers GaAs Infrared LED & Photo IC - TLP5771*. 2018. URL: https://toshiba.semicon-storage.com/info/TLP5771_datasheet_en_20180306.pdf?did=53276&prodName=TLP5771 (visited on 03/01/2023).

[101] Infineon. *OptiMOS 2 + OptiMOS-P 2 Small Signal Transistor*. 2015. URL: https://www.infineon.com/dgdl/Infineon-BSD235C-DS-v02_04-EN.pdf?fileId=db3a30433580b371013585a2d0d53326 (visited on 03/01/2023).

[102] Diodes Incorporated. *DMG4800LSD - DUAL N-CHANNEL ENHANCEMENT MODE MOSFET*. 2022. URL: https://www.diodes.com/assets/Datasheets/DMG4800LSD.pdf (visited on 03/01/2023).

[103] Teledyne LeCroy. *HDO4000A Oscilloscopes Fact Sheet*. 2017. URL: https://cdn.teledynelecroy.com/files/pdf/hdo4000a-oscilloscopes-datasheet.pdf (visited on 03/01/2023).

[104] Pico. *TA045 - 200 MHz 60 V Differential Probe - User's Manual*. 2008. URL: https://www.picotech.com/download/manuals/ta045-differential-probe-users-guide.pdf (visited on 03/01/2023).

[105] Teledyne LeCroy. *High Voltage Differential Probes HVD3605A, HVD3220, HVD3206A, HVD310xA*. 2021. URL: https://cdn.teledynelecroy.com/files/pdf/hvd3000a-probes-datasheet.pdf (visited on 03/01/2023).

[106] Teledyne LeCroy. *Current Probes*. 2017. URL: https://cdn.teledynelecroy.com/files/pdf/current-probes-datasheet.pdf (visited on 03/01/2023).

[107] Rohm. *SCT3080KL - N-channel SiC power MOSFET*. 2022. URL: https://fscdn.rohm.com/en/products/databook/datasheet/discrete/sic/mosfet/sct3080kl-e.pdf (visited on 03/01/2023).

[108] Keysight. *N5700 Series System DC Power Supplies*. 2022. URL: https://www.keysight.com/de/de/assets/7018-01235/data-sheets/5989-1330.pdf (visited on 03/01/2023).

[109] Textronix Keithley. *SourceMeter SMU Instrument 1000 Watts, 10 Amps Pulse, 7 Amps DC*. 2022. URL: https://download.tek.com/datasheet/2461-DataSheet.pdf (visited on 03/01/2023).

[110] D. C. Wunsch and R. R. Bell. "Determination of Threshold Failure Levels of Semiconductor Diodes and Transistors Due to Pulse Voltages". In: *IEEE Transactions on Nuclear Science* 15.6 (Dec. 1968), pp. 244–259. ISSN: 1558-1578. DOI: 10.1109/TNS.1968.4325054.

[111] Infineon. *Infineon EiceDRIVER*. 2021. URL: https://www.infineon.com/dgdl/Infineon-1EDF5673F-DataSheet-v02_04-EN.pdf?fileId=5546d46266a498f50166c9b590b52264 (visited on 02/07/2023).

[112] GaN Systems. *GaN Systems EiceDRIVER*. 2022. URL: https://gansystems.com/wp-content/uploads/2022/07/GN010-ENG-EZDrive-Solution-for-GaN-Systems-GaN-Transistors-Rev.220720.pdf (visited on 02/07/2023).

[113] Dawei Liu et al. "Full Custom Design of an Arbitrary Waveform Gate Driver With 10-GHz Waypoint Rates for GaN FETs". In: *IEEE Transactions on Power Electronics* 36.7 (July 2021), pp. 8267–8279. ISSN: 1941-0107. DOI: 10.1109/TPEL.2020.3044874.

[114] Gang Xie et al. "An AlGaN/GaN HEMT with a reduced surface electric field and an improved breakdown voltage". In: *Chinese Physics B* 21.8 (Aug. 2012), p. 086105. DOI: 10.1088/1674-1056/21/8/086105.

[115] He Li et al. "Robustness of 650-V Enhancement-Mode GaN HEMTs Under Various Short-Circuit Conditions". In: *IEEE Transactions on Industry Applications* 55.2 (Mar. 2019), pp. 1807–1816. ISSN: 1939-9367. DOI: 10.1109/TIA.2018.2879289.

[116] Sheng Li et al. "Understanding Electrical Parameter Degradations of P-GaN HEMT Under Repetitive Short-Circuit Stresses". In: *IEEE Transactions on Power Electronics* 36.11 (Nov. 2021), pp. 12173–12176. ISSN: 1941-0107. DOI: 10.1109/TPEL.2021.3077128.

[117] Analog Devices. *LTspice*. 2023. URL: https://www.analog.com/en/design-center/design-tools-and-calculators/ltspice-simulator.html (visited on 05/24/2023).

[118] SIMetrix Technologies. *SIMetrix*. 2023. URL: https://www.simetrix.co.uk/products/simetrix.html (visited on 05/24/2023).

[119] Cadence. *Cadence Virtuoso*. 2023. URL: https://www.cadence.com/en_US/home/tools/ic-package-design-and-analysis/ic-package-design-flows/virtuoso-system-design-platform.html (visited on 05/24/2023).

[120] Verilog-AMS. *Introduction to Verilog-A*. 2023. URL: https://verilogams.com/tutorials/vloga-intro.html (visited on 05/25/2023).

[121] W. R. Curtice and M. Ettenberg. "A Nonlinear GaAs FET Model for Use in the Design of Output Circuits for Power Amplifiers". In: *IEEE Transactions on Microwave Theory and Techniques* 33.12 (Dec. 1985), pp. 1383–1394. ISSN: 0018-9480. DOI: 10.1109/TMTT.1985.1133229.

[122] keysight technologies. *EE HEMT1 Model (EEsof Scalable Nonlinear HEMT Model)*. 2023. URL: https://edadocs.software.keysight.com/pages/viewpage.action?pageId=6063102 (visited on 05/24/2023).

[123] I. Angelov et al. "An empirical table-based FET model". In: *IEEE Transactions on Microwave Theory and Techniques* 47.12 (Dec. 1999), pp. 2350–2357. ISSN: 1557-9670. DOI: 10.1109/22.808981.

[124] Ujwal Radhakrishna et al. "MIT virtual source GaNFET-high voltage (MVSG-HV) model: A physics based compact model for HV-GaN HEMTs". In: *physica status solidi (c)* 11.3-4 (2014), pp. 848–852. ISSN: 1610-1642. DOI: 10.1002/pssc.201300392.

[125] ASM GROUP - IIT Kanpur. *Advanced Spice Model for High Electron Mobility Transistors*. 2023. URL: https://iitk.ac.in/asm/ (visited on 05/24/2023).

[126] MathWorks. *Math. Graphics. Programming.* 2023. URL: https://de.mathworks.com/products/matlab.html (visited on 05/25/2023).

[127] Phyton. *Python is powerful... and fast, plays well with others,runs everywhere,is friendly & easy to learn,is Open.* 2023. URL: https://www.python.org/ (visited on 05/25/2023).

[128] Sourabh Khandelwal, Nitin Goyal, and Tor A. Fjeldly. "A Physics-Based Analytical Model for 2DEG Charge Density in AlGaN/GaN HEMT Devices". In: *IEEE Transactions on Electron Devices* 58.10 (Oct. 2011), pp. 3622–3625. ISSN: 1557-9646. DOI: 10.1109/TED.2011.2161314.

[129] S. Kola, J. M. Golio, and G. N. Maracas. “An analytical expression for Fermi level versus sheet carrier concentration for HEMT modeling”. In: *IEEE Electron Device Letters* 9.3 (Mar. 1988), pp. 136–138. ISSN: 0741-3106. DOI: 10.1109/55.2067.

[130] Sourabh Khandelwal, Yogesh Singh Chauhan, and Tor A. Fjeldly. “Analytical Modeling of Surface-Potential and Intrinsic Charges in AlGaN/GaN HEMT Devices”. In: *IEEE Transactions on Electron Devices* 59.10 (Oct. 2012), pp. 2856–2860. ISSN: 1557-9646. DOI: 10.1109/TED.2012.2209654.

[131] Ho Ki Kwon et al. “Radiative recombination of two-dimensional electrons in a modulation-doped Al0.37Ga0.63N/GaN single heterostructure”. In: *Applied Physics Letters* 75.18 (Nov. 1999), pp. 2788–2790. ISSN: 0003-6951. DOI: 10.1063/1.125150.

[132] Berkeley University of California. *1. MOSFET equations*. 2023. URL: https://inst.eecs.berkeley.edu/~ee105/fa05/handouts/discussions/Discussion5.pdf (visited on 06/05/2023).

[133] Sudip Ghosh et al. “Surface-Potential-Based Compact Modeling of Gate Current in AlGaN/GaN HEMTs”. In: *IEEE Transactions on Electron Devices* 62.2 (Feb. 2015), pp. 443–448. ISSN: 1557-9646. DOI: 10.1109/TED.2014.2360420.

[134] Sreenidhi Turuvekere et al. “Gate Leakage Mechanisms in AlGaN/GaN and AlInN/GaN HEMTs: Comparison and Modeling”. In: *IEEE Transactions on Electron Devices* 60.10 (Oct. 2013), pp. 3157–3165. ISSN: 1557-9646. DOI: 10.1109/TED.2013.2272700.

[135] Sreenidhi Turuvekere et al. “Evidence of Fowler–Nordheim Tunneling in Gate Leakage Current of AlGaN/GaN HEMTs at Room Temperature”. In: *IEEE Transactions on Electron Devices* 61.12 (Dec. 2014), pp. 4291–4294. ISSN: 1557-9646. DOI: 10.1109/TED.2014.2361436.

[136] Wenshen Li et al. “Thermionic emission or tunneling? The universal transition electric field for ideal Schottky reverse leakage current: A case study in -Ga2O3”. In: *Applied Physics Letters* 117.22 (Dec. 2020). 222104. ISSN: 0003-6951. DOI: 10.1063/5.0029348.

[137] Dalvir K. Saini. “Gallium Nitride: Analysis of Physical Properties and Performance in High-F in High-Frequency P equency Power Electr ower Electronic Cir onic Circuits”. dissertation. Wright State University, 2015.

[138] P. Van Halen and M.H. Habib. “A new model for the p-n junction space charge region capacitance”. In: *[1993] Proceedings of the Tenth Biennial University/Government/Industry Microelectronics Symposium*. 1993, pp. 126–130. DOI: 10.1109/UGIM.1993.297022.

[139] Christian Unger and Martin Pfost. “Determination of the Transient Threshold Voltage Hysteresis in SiC MOSFETs after Positive and Negative Gate Bias”. In: *2019 31st International Symposium on Power Semiconductor Devices and ICs (ISPSD)*. May 2019, pp. 195–198. DOI: 10.1109/ISPSD.2019.8757661.

Appendix

A Verilog-A Model

```
// Autor: Thorsten Sezgin-Oeder
// TU Dortmund University - Chair of Energy Conversion
// GaNiusVth model, supported by DFG Priority Program 2312
//############################################################
// INCLUDE disciplines.vams
//############################################################
nature voltage
    access = V;
    units = "V";
    abstol = 0.0004321;
endnature
nature current
    access = I;
    units = "A";
    abstol = 0.001234;
endnature
discipline electrical
    potential voltage;
    flow current;
enddiscipline

//############################################################
// STRUCTURE
//############################################################
module HEMT (g,d,s);
// External nodes
    electrical g,d,s;
// Internal nodes
    electrical gp,gi,di,si,x;
// Drain path
    branch (d,di)   ad;
    branch (gi,di)  gd;
    branch (gi,si)  gs;
    branch (di,si)  ds;
```

```
    branch (si,s)   as;
// Gate path
    branch (g,gi)   ag;
    branch (gi,gp)  sc;
    branch (gp,si)  pn;

//#########################################################
// PARAMETER - DRAIN MODEL
//#########################################################
//---------------------------------------------------------
// PHYSICAL
//---------------------------------------------------------
// Elementary charge [C]
    parameter real Q        = 1.602e-19      from  (0:inf);
// Boltzmann constant [J/K]
    parameter real KB       = 1.381e-23      from  (0:inf);
// Vaccum permittivity [F/m]
    parameter real EPS0     = 8.854e-12      from  (0:inf);
// Dielectric permittivity of AlGaN [As/Vm]
    parameter real EPSALGAN = 9.2            from  (0:inf);
// Density of states in GaN [1/(m^2*V)]
    parameter real DOS      = 3.24e+17       from  (0:inf);
// Low-field mobility of 2DEG [m^2/Vs]
    parameter real M0       = 0.17           from  (0:inf);
// Carrier saturation velocity [m/s]
    parameter real VSAT     = 190000.0       from  (0:inf);
//---------------------------------------------------------
// CONSTANTs
//---------------------------------------------------------
// Nominal temperature [K]
    parameter real TNOM     = 298.0          from  (0:inf);
// Ambient temperature [K]
    parameter real TAMB     = 298            from  (0:inf);
// Gate length [m] (Channel length)
    parameter real L        = 2.5e-07        from  (0:inf);
// AlGaN thickness [m]
    parameter real DALGAN   = 2.5e-08        from  (0:inf);
// Source-side drift-resistance
    parameter real RS       = 0.001          from  (0:inf);
```

```
// Schroedinger-Poisson solution variable
    parameter real G1       = 2.12e-12       from  (0:inf);
// Schroedinger-Poisson solution variable
    parameter real G2       = 3.73e-12       from  (0:inf);
// Minimum overdrive [V]
    parameter real VMIN     = 0.01           from  (0:inf);
// Minimum current [A]
    parameter real IMIN     = 1e-11          from  (0:inf);
//-------------------------------------------------------
// FITTING
//-------------------------------------------------------
// Gate width [m]
    parameter real W        = 0.006430738    from  (0:inf);
// Drain-side drift-resistance [Ohm]
    parameter real RD       = 0.07           from  (0:inf);
// 1st order mobility degradation [1/V]
    parameter real M1       = 0.2510308414   from  (0:inf);
// 2nd order mobility degradation [1/V^2]
    parameter real M2       = 0.06387144347  from  (0:inf);
// Velocity saturation parameter
    parameter real SAT1     = 1.789473684    from  (0:inf);
// Transition of saturation region
    parameter real SAT2     = 1              from  (0:inf);
//-------------------------------------------------------
// VARIABLEs
//-------------------------------------------------------
    real Vds,Vgs,Vgd,vt,Vov,Vove;
    real Cg,beta,Gs,Hs,Ns,Qs,EFs,SPs;
    real mu,Vdsat,Vdsate,Vdov,Vdove,Gd,Hd,Nd,Qd,EFd,SPd;
    real SPdif,SPavg,SPuni,mdeg,msat,Ids;

//#########################################################
// PARAMETER - GATE MODEL
//#########################################################
//-------------------------------------------------------
// PHYSICAL
//-------------------------------------------------------
// Dielectric permittivity of GaN [As/Vm]
    parameter real EPSGAN   = 9.5            from  (0:inf);
```

```
// Intrinsic carrier concentration [cm-3]
    parameter real NI       = 1e-10          from  (0:inf);
// Barrier height for electron emission [eV]
    parameter real PE       = 0.35           from  (0:inf);
// Barrier hight [eV]
    parameter real PB       = 1.2            from  (0:inf);
//-----------------------------------------------------------
// CONSTANTs
//-----------------------------------------------------------
// p-GaN thickness [m]
    parameter real DPGAN    = 1e-06          from  (0:inf);
// Optimim ohmic doping concentration [cm-3]
    parameter real NO       = 1e+20          from  (0:inf);
// Gate forward-breakdown voltage [V]
    parameter real VF       = 10.0           from  (0:inf);
//-----------------------------------------------------------
// FITTING
//-----------------------------------------------------------
// P-GaN doping concentration [cm-3]
    parameter real NA       = 2.5147e+19     from  (0:inf);
// Ideality factor (forward)  [m]
    parameter real GP       = 0.57           from  (0:inf);
// Gate reverse-breakdown voltage [V]
    parameter real VR       = 3.346          from  (0:inf);
// Ideality factor (reverse)
    parameter real GR       = 0.0631         from  (0:inf);
//-----------------------------------------------------------
// VARIABLEs
//-----------------------------------------------------------
    real Ni,Na,No,Vb0,Vb1,xb0,xb1,Pb0,Pb1,Psc,Vsc,Esc;
    real Ipf,Ifn,Ite,Isc,Rg,Vbi,Ipn;

//###########################################################
// PARAMETER - CAPACITANCE MODEL
//###########################################################
//-----------------------------------------------------------
// CONSTANTs
//-----------------------------------------------------------
// Initial capacitances
```

```
    parameter real CGD0     = 6.695e-11       from (0:inf);
    parameter real CGS0     = 1.411e-10       from (0:inf);
    parameter real CDS0     = 8.657e-11       from (0:inf);
// HighVds capacitances
    parameter real CGD1     = 1.482e-13       from (0:inf);
    parameter real CGS1     = 1.546e-10       from (0:inf);
    parameter real CDS1     = 2.747e-11       from (0:inf);
//-----------------------------------------------------------
// FITTING
//-----------------------------------------------------------
// Gradient of the capacitances
    parameter real CAP1     = 5.862           from (0:inf);
    parameter real CAP2     = 1.0             from (0:inf);
    parameter real CAP3     = 82.534          from (0:inf);
// Parasitic Inductance
    parameter real LP       = 1e-08           from (0:inf);
//-----------------------------------------------------------
// VARIABLEs
//-----------------------------------------------------------
    real Csc,Cpn,Cgd,Cgs,Cds;

//###########################################################
// PARAMETER - THRESHOLD MODEL
//###########################################################
//-----------------------------------------------------------
// CONSTANTs
//-----------------------------------------------------------
// Max Vth @ 0V [V], Min Vth [V], Vth @ 600V [V]
    parameter real VTHMAX   = 1.54571        from  (0:inf);
    parameter real VTHMIN   = 1.31261        from  (0:inf);
    parameter real VTHHV    = 1.41284        from  (0:inf);
// On-set of hole injection
    parameter real VHI      = 500            from  (0:inf);
// Vth shift weakening
    parameter real WEAK     = 50             from  (0:inf);
// Maximum change of Vdsin
    parameter real DVDSIN   = 100e-3         from  (0:inf);
// Maximum change of tdsin
    parameter real DTDSIN   = 1              from  (0:inf);
```

```
// Onset of the Vth instability
    parameter real VTVI     = 50             from  (0:inf);
//-------------------------------------------------------
// VARIABLEs
//-------------------------------------------------------
    real Vspace,Vweak,Vshift,Vdsin,tdsin,Vinst;
    real Vth (* node="Vth", func="limit(_,VTHMIN,VTHMAX)" *);

//#########################################################
// DRAIN MODEL
//#########################################################
analog begin
// Thermal voltage
    vt      = KB*TAMB/Q;
// Overdrive
    Vov     = V(gs)-Vth;
// Effective GS overdrive (subslope limit)
    Vove    = 0.5*(Vov+sqrt(pow(Vov,2)+VMIN));
//-------------------------------------------------------
// FERMI-NIVEAU @ SOURCE SIDE
//-------------------------------------------------------
// Interpolation for Schroedinger Poisson solution
    Cg      = EPS0*EPSALGAN/DALGAN;
    beta    = Cg/(Q*DOS*vt);
    Gs      = 0;
// Bias depependence of the 2DEG Fermi-level
    Hs      = (Vove+vt*(1-ln(beta*Vove))-Gs/3*
              pow(Cg*Vove/Q,2/3))/
              (Vove+vt+Gs*2/3*pow(Cg*Vove/Q,2/3));
// 2DEG Charge Density
    Ns      = Cg/Q*2*vt*ln(1+exp(Vov/(2*vt)))/
              (1/Hs+(Cg/(Q*DOS))*exp(-Vov/(2*vt)));

// Unified Fermi-level
    EFs     = Vov-Q*Ns/Cg;
//-------------------------------------------------------
// FERMI-NIVEAU @ DRAIN SIDE
//-------------------------------------------------------
```

```
// Velocity saturation
    Vdsat   = Vove*VSAT/(VSAT+Vov*mu/(2*L));
// Fitting of saturation
    Vdsate  = V(ds)*(pow(1+pow(V(ds)/Vdsat,SAT2),-1/SAT2));
// Intrinisc GD saturation overdrive
    Vdov    = Vov-Vdsate;
// Effective GD sat. overdrive (subslope limit)
    Vdove   = 0.5*(Vdov+sqrt(pow(Vdov,2)+VMIN));
// Interpolation for Schroedinger Poisson solution
    Gd      = 0;
// Bias dependency of the 2DEG Fermi-level
    Hd      = (Vdove+vt*(1-ln(beta*Vdove))-Gd/3*
              pow(Cg*Vdove/Q,2/3))/
              (Vdove+vt+Gd*2/3*pow(Cg*Vdove/Q,2/3));
// 2DEG Charge Density
    Nd      = Cg/Q*2*vt*ln(1+exp(Vdov/(2*vt)))/
              (1/Hd+(Cg/(Q*DOS))*exp(-Vdov/(2*vt)));
// Unified Fermi-level
    EFd     = Vdov-Q*Nd/Cg;
//-------------------------------------------------------
// UNIFIED SURFACE POTENTIAL
//-------------------------------------------------------
// Surface potential @ Source-side
    SPs     = EFs;
// Surface potential @ Drain-side
    SPd     = EFd+Vdsate;
// Differential surface potential
    SPdif   = SPd-SPs;
// Average surface potential
    SPavg   = 0.5*(SPd+SPs);
// Effective surface potential
    SPuni   = (Vdove-SPavg+vt)*SPdif;
//-------------------------------------------------------
// DRAIN CURRENT
//-------------------------------------------------------
// Mobility degradation
    mdeg    = 1/(1+M1*(Vov-SPavg)+M2*pow(Vov-SPavg,2));
// Mobility saturation
    msat    = 1/sqrt(1+pow(SAT1,2)*pow(SPdif,2));
```

```
// Effective current
    Ids     = W/L*SPuni*Cg*mdeg*msat;
//-----------------------------------------------------------
// OUTPUT
//-----------------------------------------------------------
    V(ad)   <+ RD*I(ad);
    I(ds)   <+ Ids+IMIN;
    V(as)   <+ RS*I(as);
    //V(as)   <+ LP*ddt(I(as));

//###########################################################
// GATE MODEL
//###########################################################
//-----------------------------------------------------------
// METAL/p-GaN CONTACT (forward operation)
//-----------------------------------------------------------
// Doping correlations [cm-3 -> m-3]
    Ni      = NI*1e+6;
    No      = NO*1e+6;
    Na      = NA*1e+6;
// Space charge region
    Vb0     = vt*(ln(No/Ni));
    Vb1     = vt*(ln(Na/Ni));
    xb0     = sqrt((2*EPS0*EPSGAN*Vb0)/Q/No);
    xb1     = sqrt((2*EPS0*EPSGAN*Vb1)/Q/Na);
// Schottky barrier
    Pb0     = Q*(No)*pow(xb0,2)/(2*EPS0*EPSGAN);
    Pb1     = Q*(Na)*pow(xb1,2)/(2*EPS0*EPSGAN);
    Psc     = PB+Pb0-Pb1;
// Electrical field
    Esc     = 0.5*(V(sc)+sqrt(pow(V(sc),2)))/
              xb1*Q/(EPS0*EPSGAN);
// Pool-Frenkel Emission (low Vgs)
    Ipf     = (Esc)*exp(-PE/vt+sqrt(GF*Esc)/vt);
// Fowler-Nordheim Tunneling (high Vgs)
    Ifn     = NO/NA*pow(Esc,2)/Psc*
              exp(-sqrt(pow(Psc,3))/Esc);
// Gate breakdown (very high Vgs)
    Ite     = IMIN*exp((V(gs)-VF)/vt);
```

```
//-------------------------------------------------------
// p-GaN Region
//-------------------------------------------------------
// Drift Resistance
    Rg      = DPGAN/(W*L*Q*MO*Na);
//-------------------------------------------------------
// p-GaN/AlGaN/2DEG (PIN) DIODE
//-------------------------------------------------------
    Vbi     = vt*(ln(Na/Ni));
    Ipn     = -IMIN*exp(GR*(-V(gs)-VR)/vt);
//-------------------------------------------------------
// OUTPUT
//-------------------------------------------------------
    V(ag)   <+ RS*I(ag);
    V(ag)   <+ Rg*I(ag);
    V(pn)   <+ Vbi;
    I(gs)   <+ Ipf+Ifn+Ite+Ipn+IMIN;

//#########################################################
// CAPACITANCE MODEL
//#########################################################
//-------------------------------------------------------
// CAPACITANCES
//-------------------------------------------------------
// Gate-Drain Capacitance
    Csc     = (CGD0-CGD1)/pow(1-V(gd)/CAP1,1)+CGD1;
    Cpn     = W/L*Cg;
    Cgd     = Csc*Cpn/(Csc+Cpn);
// Gate-Source Capacitance
    Cgs     = (CGS0-CGS1)*CAP2/
              sqrt(pow(V(gs),2)+pow(CAP2,2))+CGS1;
// Drain-Source Capacitance
    Cds     = (CDS0-CDS1)*CAP3/
              sqrt(pow(V(ds),2)+pow(CAP3,2))+CDS1;
//-------------------------------------------------------
// OUTPUT
//-------------------------------------------------------
    I(gd)   <+ Cgd*ddt(V(gd));
    I(gs)   <+ Cgs*ddt(V(gs));
```

```
    I(ds)   <+ Cds*ddt(V(ds));

//#############################################################
// THRESHOLD MODEL
//#############################################################
//-------------------------------------------------------------
// SHIFT
//-------------------------------------------------------------
    Vspace  = (VTHMAX-VTHMIN)*Cgd/CGD0+VTHMIN;
    Vweak   = (VTHHV-VTHMIN)*0.5*(tanh((V(ds)-500)/50)+1);
    Vshift  = Vspace+Vweak;
//-------------------------------------------------------------
// VDS INSTABILITY
//-------------------------------------------------------------
// Bias-dependend charge due to Vgs
    tdsin   = DTDSIN*(tanh(-V(g,s))+1);
// Bias-dependend charge due to Vds
    Vdsin   = DVDSIN*(0.5*(tanh(V(d,s)-VTVI)+1));
// Vds-induced Vth-instability
    V(x)    <+ Vdsin-tdsin*ddt(V(x));
    Vinst   = V(x);
//-------------------------------------------------------------
// OUTPUT
//-------------------------------------------------------------
// Threshold voltage
    Vth     = Vshift+Vinst;
end
endmodule
```

B List of Publications

[A] Thorsten Oeder, Alberto Castellazzi, and Martin Pfost. “Experimental study of the short-circuit performance for a 600V normally-off p-gate GaN HEMT”. In: *2017 29th International Symposium on Power Semiconductor Devices and IC's (ISPSD)*. May 2017, pp. 211–214. DOI: 10.23919/ISPSD.2017.7988925.

[B] Thorsten Oeder, Alberto Castellazzi, and Martin Pfost. “Electrical and thermal failure modes of 600V p-gate GaN HEMTs”. In: *Microelectronics Reliability* 76-77 (2017), pp. 321–326. ISSN: 0026-2714. DOI: 10.1016/j.microrel.2017.06.046.

[C] Alberto Castellazzi, Asad Fayyaz, Siwei Zhu, Thorsten Oeder and Martin Pfost “Single pulse short-circuit robustness and repetitive stress aging of GaN GITs”. In: *IEEE International Reliability Physics Symposium (IRPS)*. Mar. 2018, 4E.1-1-4E.1–10. DOI: 10.1109/IRPS.2018.8353593.

[D] F. D'Aniello, A. Fayyaz, A. Castellazzi, T. Oeder and M. Pfost. “Damage accumulation in GaN GITs exposed to repetitive short-circuit”. In: *2019 31st International Symposium on Power Semiconductor Devices and ICs (ISPSD)*. May 2019, pp. 451–454. DOI: 10.1109/ISPSD.2019.8757692.

[E] Thorsten Oeder and Martin Pfost. “Impact of Carrier Accumulation on the Transient Behavior of p-Gate GaN HEMTs”. In: *2019 31st International Symposium on Power Semiconductor Devices and ICs (ISPSD)*. May 2019, pp. 443–446. DOI: 10.1109/ ISPSD.2019.8757570.

[F] Thorsten Oeder and Martin Pfost. “Gate-Stress-Induced Threshold Voltage Instabilites, a Comparison of Ohmic and Schottky p-Gate GaN HEMTs”. In: *2020 IEEE Workshop on Wide Bandgap Power Devices and Applications in Asia (WiPDA Asia)*. Sept. 2020, pp. 1–5. DOI: 10.1109/WiPDAAsia49671.2020.9360288.

[G] Thorsten Oeder and Martin Pfost. “Gate-Induced Threshold Voltage Instabilities in p-Gate GaN HEMTs”. In: *IEEE Transaction on Electron Devices* Sept. 2021, pp. 4322–4328. ISSN: 1557-9646. DOI: 10.1109/ted.2021.3098254.

[H] Thorsten Oeder and Martin Pfost. “Threshold Voltage Behavior and Short-Circuit Capability of p-Gate GaN HEMTs Depending on Drain- and Gate-Voltage Stress”. In: *2022 IEEE 9th Workshop on Wide Bandgap Power Devices & Applications (WiPDA)*. Nov. 2022, pp. 73–76.
DOI: 10.1109/WiPDA56483.2022.9955266.

C List of Supervised Theses

[a] Simon Stehr. "Gegenüberstellung von material- und technologiebasierten Limitierungen moderner Leistungshalbleiter". *Fachwissenschaftliche Projektarbeit*. August 2018.

[b] Alem Basic. "Einfluss des Gate-Source-Widerstands auf die Gate-Charakteristik bei GaN-HEMTs". *Bachelor-Thesis*. October 2018.

[c] Yannik Bieker. "Entwicklung einer Temperaturregelung zur thermischen Charakterisierung moderner Leistungshalbleiter". *Bachelor-Thesis*. June 2019.

[d] Lukas Knappstein. "Development and Construction of a sequentially extendable Measurement Setup for Characterizing the Degradation of AlGaN/GaN HEMTs". *Master-Thesis*. January 2021.

[e] Lukas Ciesiolka. "Experimentelle Charakterisierung der Auswirkung von Gate-Stress induzierten Schwellspannungs-Instabilitäten bei p-Gate AlGaN/GaN HEMTs". *Master-Thesis*. March 2021.

[f] Refaat Al Nouri. "Entwicklung eines Prüfkonzepts und Validierung eines isolierten SiC-basierten DC/DC-Wandlers, für die Ladeinfrastruktur von Elektrofahrzeugen". *Master-Thesis*. July 2021.

[g] Bohua Zhang. "Development of a Surface-Potential-Based Compact Model for p-Gate GaN HEMTs in Verilog-A, involving a Measurement-Assisted Parameter Extraction Methodology". *Master-Thesis*. July 2021.

[h] Mohammad Harbaji. "Entwicklung eines analytischen Kompaktmodells der Gate-Struktur von p-Gate GaN HEMTs in Verilog-A". *Bachelor-Thesis*. August 2022.