

PAPER • OPEN ACCESS

Buried graphene heterostructures for electrostatic doping of low-dimensional materials

To cite this article: A Gumprich *et al* 2023 *Nanotechnology* **34** 265203

View the [article online](#) for updates and enhancements.

You may also like

- [Analysis on the Electrostatic Doping and Several Alternative Devices](#)
Chenxi Yu
- [First-principles calculation of gate-tunable ferromagnetism in magic-angle twisted bilayer graphene under pressure](#)
Xiao Chen, Shuanglong Liu, James N Fry et al.
- [Recent advances in two-dimensional p-type metal chalcogenides: synthesis, doping strategies and applications](#)
Jie Wu, Fuwei Zhuge, Huiqiao Li et al.

PRIME
PACIFIC RIM MEETING
ON ELECTROCHEMICAL
AND SOLID STATE SCIENCE

HONOLULU, HI
October 6-11, 2024

Joint International Meeting of
The Electrochemical Society of Japan (ECS)
The Korean Electrochemical Society (KECS)
The Electrochemical Society (ECS)

Early Registration Deadline:
September 3, 2024

MAKE YOUR PLANS NOW!

Buried graphene heterostructures for electrostatic doping of low-dimensional materials

A Gumprich¹ , J Liedtke¹, S Beck¹, I Chirca², T Potočník²,
J A Alexander-Webber² , S Hofmann²  and S Tappertzhofen^{1,*} 

¹ Chair for Micro- and Nanoelectronics, Department of Electrical Engineering and Information Technology, TU Dortmund University, Martin-Schmeisser-Weg 4-6, D-44227, Dortmund, Germany

² Department of Engineering, University of Cambridge, 9 JJ Thompson Avenue, Cambridge CB3 0FA, United Kingdom

E-mail: stefan.tappertzhofen@tu-dortmund.de

Received 23 November 2022, revised 17 January 2023

Accepted for publication 8 February 2023

Published 13 April 2023



CrossMark

Abstract

The fabrication and characterization of steep slope transistor devices based on low-dimensional materials requires precise electrostatic doping profiles with steep spatial gradients in order to maintain maximum control over the channel. In this proof-of-concept study we present a versatile graphene heterostructure platform with three buried individually addressable gate electrodes. The platform is based on a vertical stack of embedded titanium and graphene separated by an intermediate oxide to provide an almost planar surface. We demonstrate the functionality and advantages of the platform by exploring transfer and output characteristics at different temperatures of carbon nanotube field-effect transistors with different electrostatic doping configurations. Furthermore, we back up the concept with finite element simulations to investigate the surface potential. The presented heterostructure is an ideal platform for analysis of electrostatic doping of low-dimensional materials for novel low-power transistor devices.

Supplementary material for this article is available [online](#)

Keywords: low-dimensional materials, graphene-heterostructures, electrostatic doping, buried triple gates, steep slope transistors, carbon nanotube transistors

(Some figures may appear in colour only in the online journal)

1. Introduction

Among the most important challenges in modern transistor development is the reduction of the power dissipation. Almost all integrated circuits in consumer electronics are made of silicon-based metal oxide semiconductor field-effect transistors (MOSFET). Over the last decades the increase of

performance while decreasing the power dissipation has been achieved by scaling down the MOSFET's geometry. Eventually, this long-term scaling reached tremendous difficulties due to short channel effects, such as drain induced barrier lowering [1]. One approach to mitigate short channel effects are FinFET devices [2], which were successfully scaled down to the sub 22 nm regime. Recently, leading semiconductor companies like IBM introduced the 2 nm technology node, with a typical gate length of 14 nm and a 44 nm pitch. A key challenge thereby remains to maintain sufficient electrostatic gate control for ever smaller gate lengths and decreasing power. One approach is to design devices where the channel material and geometry are fundamentally different from state-of-the-art transistors [3–5]. Materials of lower dimensions,

* Author to whom any correspondence should be addressed.



Original content from this work may be used under the terms of the [Creative Commons Attribution 4.0 licence](#). Any further distribution of this work must maintain attribution to the author(s) and the title of the work, journal citation and DOI.

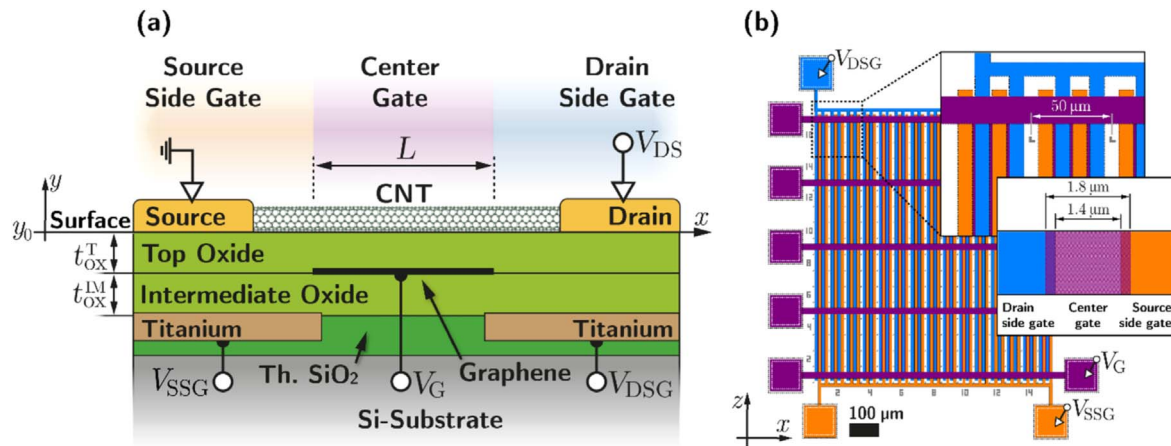


Figure 1. (a) Concept of the heterostructure depicted as a completed CNT-FET device. Titanium is used as side gate material embedded in thermal SiO₂ (Th. SiO₂) and complemented by a graphene center gate. (b) Lithography mask layout of a single heterostructure cell. The orange and blue layers are the side gates forming an interdigital comb-like architecture. The purple layer is the main gate or center gate.

such as one-dimensional (1D) materials like nanowires (NWs) or carbon nanotubes (CNTs), and two-dimensional transition metal dichalcogenides (2D-TMDs) offer new design opportunities [5–7]. These materials allow to drive relatively high currents despite their almost atomically constrained geometry. Furthermore, these 1D or ultra-thin channel materials enable excellent gate control and extreme scalability. There are a number of TMDs that exhibit very small bandgaps well below 1 eV, which makes them ideal candidates for novel low-power transistor devices. Examples of such new devices include steep slope transistors (SSTs), such as tunneling field-effect transistors (TFETs) and superlattice energy-filtering transistors (EF-FETs) [8–16].

Manufacturing of SSTs with 1D- or 2D-materials in transistor applications demands an adjustable doping profile along the channel. However, conventional doping using implanted impurities or chemical modification will negatively impact the carrier mobility, generates unwanted depletion effects, and is also rather difficult or simply impossible to realize [17, 18].

An alternative to provide a semiconductor with a high electron or hole density is electrostatic doping via mutually insulated gate electrodes [19, 20]. This allows for individually controllable potentials along a semiconductor channel region, which enables the fabrication of reconfigurable transistors [21–23]. For example, a TFET channel needs at least three individually controllable gate electrodes in close proximity to precisely define the source-channel-drain band configurations in order to control the band-to-band tunneling probability [6, 24–26]. A previous approach that allows electrostatic doping with a so-called triple gate architecture was reported by Müller *et al* [12, 26]. The architecture included a lateral design of buried v-shaped metal center gate electrodes surrounded by *n*-doped silicon side gate electrodes. The platform is based on sophisticated fabrication methods such as ion doping for the side gates and chemical mechanical polishing (CMP) for the required planarization of the surface. Moreover, the v-shaped center gate electrodes are prepared by anisotropic wet-chemical etching, which hinders further

downscaling of the lateral dimensions. Besides technical challenges during fabrication, a major drawback of the architecture is that the layout does not allow for a perfect overlap of the buried electrodes, which limits the steepness of the electrostatic doping profiles. Thus, fabrication of buried and individually controllable electrodes to achieve a field distribution with steep potential gradients along the channel remains an unresolved problem.

In this work, we report on the design and fabrication of a novel graphene/metal heterostructure with three mutually insulated and independently addressable gate electrodes. This heterostructure can be used as a platform for application and analysis of electrostatic doping of low-dimensional materials. The fabricated platform consists of structured graphene center gate electrodes buried by an oxide, on top of embedded titanium side gate electrodes and separated by an additional (intermediate) oxide. The use of 2D graphene as electrode provides a platform with high surface planarity. In contrast to the architecture reported by Müller *et al* [12, 26], our heterostructure is fabricated using much simpler methods. Furthermore, simulations highlight that much steeper electrical potential gradients between the gates can be achieved. The heterostructure allows symmetric *n–n* (*n*FET) and *p–p* (*p*FET) doping profiles, or asymmetric doping profiles for *n–p* or *p–n* band-to-band TFETs, respectively. For *npn* or *pnp*, two on-states are possible yielding a double tunneling barrier. We demonstrate the feasibility of our design utilizing CNTs as channel material with a channel length of 1.4 μm. Our design is versatile, and allows for the integration of almost any semiconducting 1D- or 2D-material and progressive scaling down to sub-100 nm dimensions.

2. Concept and layout

A simplified cross-sectional schematic of the platform is shown in figure 1(a). Titanium source side gates (SSG) and drain side gates (DSG) are embedded into an oxidized silicon substrate. The two side gates are buried beneath an

intermediate oxide with a slightly laterally overlapping center gate electrode on top. The stack is then buried again by another (top) oxide. Figure 1(a) shows a CNT-FET device with the channel length L as an example. The orange-colored background marks the influence of the SSG zone, blue the DSG zone and purple the center gate zone, respectively. Figure 1(b) illustrates a bird's eye view of the design by showing the layout of the lithography mask. The same color scheme as in figure 1(a) is used to indicate the different layers representing the buried gate electrodes. The layout of the side gates can be best described as an interdigital comb-like architecture. All gates are arranged in an alternating and repeating pattern covering a large amount of the sample's surface, thus providing a high probability for nano-objects, i.e. 1D or 2D materials, to span over all three gates. Since all gates are individually addressable by external voltage probes, the doping level can be fully controlled during operation.

The platform is designed to provide arbitrary electrostatic doping profiles for various steep slope devices including TFETs. This requires a very sharp potential barrier to realize steep transitions from the source/drain conduction band to the channel valence band in order to achieve a high band-to-band tunneling probability [8, 27]. That is, the steeper the potential transition, the higher the gate control for the device. The electrostatic potential distribution along the heterostructure has been investigated by finite element (FE) simulations using Comsol Multiphysics. The Fermi-level of the low dimensional material on top of the heterostructure can be shifted by electrostatic doping, which effectively results in tunable doping profiles. Thus, the gradient of the surface potential induced by the three buried electrodes is directly related to the local doping profile of the low dimensional channel material. Figure 2(a) shows the surface potential distribution along all three gates with different oxide thicknesses t_{ox} , respectively. We plotted the potential profiles in y -direction at the surface for $t_{\text{ox}} = 10$ nm, 20 nm, 30 nm, 50 nm and 100 nm (identical increment for intermediate and top oxide). Figure 2(b) illustrates the surface potential as a 2D plot with the corresponding electrodes. Voltages are arbitrarily chosen here and depend on the actual channel material. As expected, the sharpness of the potential decreases for greater vertical distances of the electrodes, thus weakening the band transitions. Therefore, the electrostatic doping gradients depend significantly on the oxides' thickness and should be as thin as possible.

The advantage of using graphene for the center gate electrode instead of using a conventional metal-based electrode is the ultra-thin thickness of the graphene layer. Replacing the graphene layer by a conventional metal layer (with a thickness of some tens to nanometers) would significantly increase the distance between the side gates and channel material. This would result in less sharp potential gradients. We expect that unintentional doping of the graphene from the side gate potentials is of no concern here. A noticeably decline of the density of states of the graphene center gate would appear by moving the Fermi-level to the very vicinity of the Dirac-point. A static potential configuration from the side gates coinciding with such event is

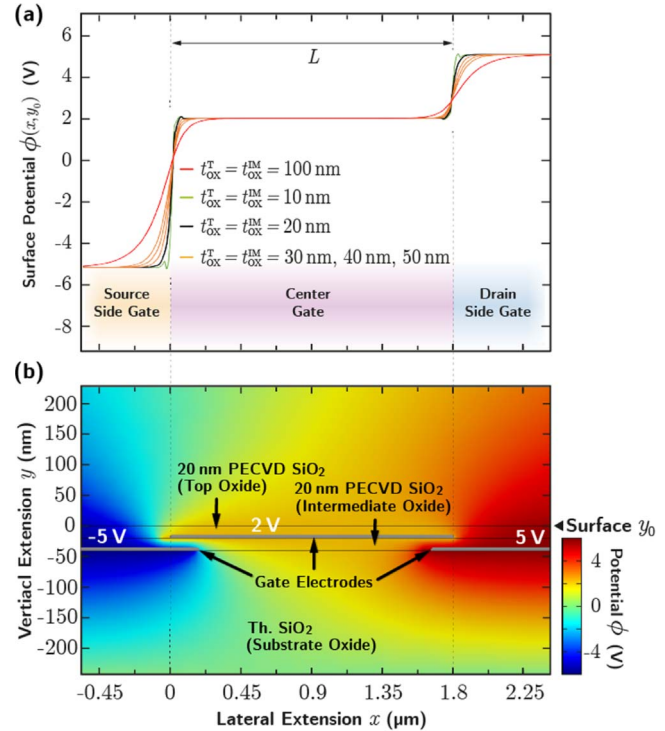


Figure 2. (a) FE simulations of the potential with different oxide thicknesses at the surface y_0 . Here we chose an equal increment for the intermediate and the top oxide, respectively. Note that voltages are chosen arbitrarily since they only scale the curves but do not affect the potential characteristic. (b) 2D FE simulation cross-section plot of the potential distribution of the heterostructure. The buried gate electrodes are drawn as gray bars.

highly unlikely and would be detectable in the transfer characteristics. A change of the graphene conductivity by unintentional electrostatic doping would also not affect the platform's functionality since the graphene is used as biasing electrode only and does not drive any significant current apart from leakage currents in the \sim pA range, see below. Furthermore, the contact to the intermediate oxide will result in chemically doping of the graphene, which provides available states for charge carriers at the interface.

Since we already mentioned the previously reported triple gate architecture by Müller *et al* [26], we also compared the potential transition between the two designs (figure 3). Due to the lateral structure used by Müller *et al* the electrode line-up is discontinuous. The simulations showed that a lateral formation of electrodes does not provide as much steepness as our approach of overlapping electrodes with an intermediate oxide. According to the simulation shown in figure 3, the width (10% to 90%) of the transition between the SSG and center gate, and center gate and DSG are 6 nm (1) and 13 nm (2) for our new platform (for 10 nm and 20 nm oxide thickness, respectively), and 37 nm (3) for the architecture reported by Müller *et al*. Thus, our concept allows for inherently steeper electrostatic doping profiles. The band-to-band tunneling probability depends exponentially on the length of this transition region, and thus the steepness of the potential gradients. Another disadvantage of Müller's platform is that it relied on n -doped silicon side gates (in this case

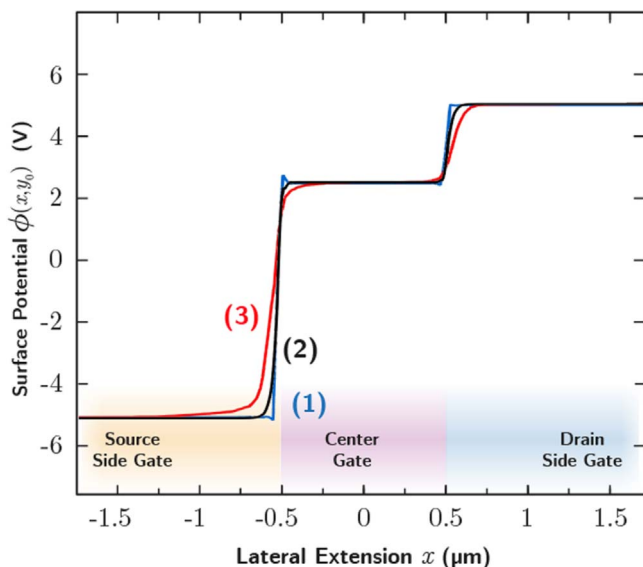


Figure 3. Potential distribution corresponding to the electrostatic doping profile of a channel material for different buried triple gate architectures: Steepest transition is shown by curve (1) and (2) representing our design with $t_{\text{ox}} = 10$ nm and $t_{\text{ox}} = 20$ nm, respectively (for both intermediate and top oxide thickness). The design by Müller *et al* [26] exhibits a noticeably weaker slope (3) in the potential transition (curves had been adjusted to match the channel dimensions of each platform). The curve (3) is reproduced with permission from [28]. © Verlagshaus Mainz (2015). Note, additional depletion effects of the Si side gates are not considered for slope (3).

the side gates could not be replaced by metal layers since the silicon is required for anisotropic etching). As a semi-conducting electrode the side gate edges exhibit a depletion zone for positive voltages adding to the issue of discontinuous potential transitions.

3. Experimental

3.1. Heterostructure platform fabrication

Fabrication of the heterostructure starts with the wet-thermal oxidation of a 4 inch silicon wafer. The targeted SiO_2 -thickness depends on the desire to improve optical visibility of the buried graphene layer. According to our previous simulations maximum visibility is achieved for a SiO_2 thickness of 72 nm [29]. For integration of the side gates into the heterostructure while still maintaining a nearly planar surface, a reactive ion etching (RIE) process etches 30 nm trenches into the SiO_2 which are filled with titanium in a subsequent sputtering deposition process. A CMP process for planarization is not required when the trench etching and metal sputtering process are precisely calibrated (see figure S1a in the supplementary data). Titanium is chosen because it exhibits a very low thermal expansion coefficient ($8.5 \cdot 10^{-6} \text{ K}^{-1}$), which is similar to the thermal expansion coefficient of SiO_2 ($5.1 \cdot 10^{-6} \text{ K}^{-1}$), and thus allows for a planar surface by preventing any damage of the substrate at elevated temperatures. This is important since the subsequent

plasma enhanced chemical vapor deposition (PECVD) is carried out at 350 °C for 30 s using an Oxford PlasmaLab 80Plus system in order to deposit 20 nm of SiO_2 onto the substrate. As a precursor gas we used 2% SiH_4 in He (flow rate 192 sccm, N_2O flow rate 355 sccm) a plasma power of 50 W and a pressure of 1.33 hPa. The Ti metallization limits our platform's temperature, which is in the range between cryogenic temperatures and at least up to 350 °C. Up to this point, all processes were carried out at wafer-level, which allows for high throughput fabrication. The main or center gates on top of the oxide are made of transferred graphene. We employ such transfer of graphene based on simplicity. Note that various direct growth approaches for graphene have been reported that potentially could allow transfer-free pathways [30]. However, our platform does not have stringent demands for a high electronic quality of the graphene layers. We used copper foil catalyzed chemical vapor deposition (CVD) of graphene and a subsequent simple PMMA-based wet-transfer as proposed by Deokar *et al* [31]. For this step, the wafers were diced into 1.2 cm × 1.2 cm sized samples to allow transfer of 1 cm × 1 cm sized graphene sheets. The transfer process causes a relatively high surface roughness of 8 nm (see figure S1(b) in the supplementary data). This roughness may lead to a non-perfect alignment of the CNT to the surface, and thus a limited transistor performance. By using an optimized transfer process, a much lower surface roughness could be achieved. For example, Zhang *et al* reported on a Rosin-enabled transfer yielding a graphene surface roughness of 0.66 nm [32]. However, for this proof-of-concept we do not focus on optimization or development of a new transfer process, and alternative methods such as wafer-scale transfer [33] or bubble transfer of graphene e.g. CVD-grown on germanium wafers [34] can also be used. Different from the process reported by Deokar *et al*, we found that a bake-out for five minutes on a hotplate at 70 °C removes the residual water on the substrate more efficiently. PMMA residues are then removed by acetone at 40 °C. Note that resist residuals are a general issue for PMMA based transfer methods [35]. In fact, resist residuals may significantly increase the contact resistance at the metal interface [36]. A cleaning with oxygen plasma would almost fully remove the PMMA, however, the graphene would be removed as well. Therefore, the substrate stays at least three hours in hot acetone (40 °C) to remove as much residues as possible. Thereafter, UV-lithography and a 30 s Ar/ O_2 -RIE process patterned the graphene into the slightly overlapping center gate structure. The 20 nm top oxide is subsequently deposited by the same PECVD process as carried out for the intermediate oxide. Exemplary images of the completed platforms are shown in figure 4. The overall gate length is 1.8 μm for 1.4 μm side gate separation, which is the smallest feature size on the platform allowing a processing sequence solely based on optical lithography. The entire process could alternatively be fabricated by any other high-resolution lithography method including electron beam lithography. This would allow to scale down to gate lengths below the 100 nm regime.

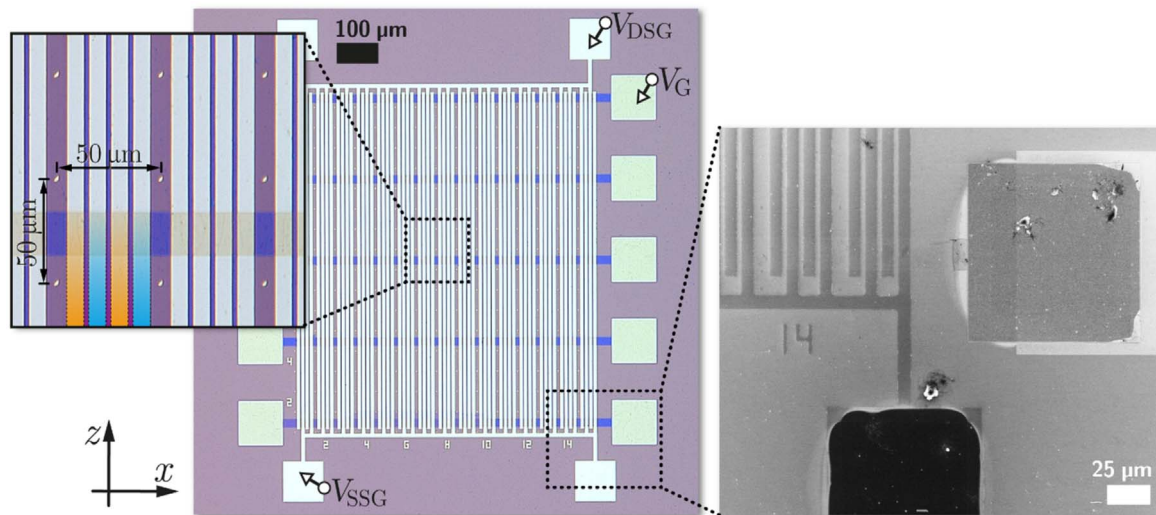


Figure 4. Optical (left) and scanning electron microscope (SEM, right) images of the completed platform with metal contact terminals before transistor fabrication: the upper and lower terminals connect to each pair of the titanium side-gates (silver-ish), terminals left and right connect to the graphene center gates (blue-colored electrodes). The graphene is barely visibly in the SEM microscope.

3.2. Transistor fabrication

As an experimental proof-of-concept we demonstrate the working principle of our new platform for arbitrary electrostatic doping profiles by using field effect transistors based on carbon nanotubes. Commercially available single wall CNTs were purchased from IoLiTec Ionic Liquids Technologies GmbH (Lot NCPCS009) and solved in isopropyl alcohol. The CNTs were then deposited onto the sample's surface by spin-on. Due to the high density of the triple gate areas, the chances are relatively high to find a suitable CNT laying across all three gates. This method however causes a randomized positioning of CNTs, which makes further contact fabrication with UV-lithography impossible. Therefore, source and drain contact terminals were patterned by electron beam lithography (EBL) using the CSAR62 resist (AR-P6200 by AllResist GmbH) and a Raith Pioneer System with 15 kV accelerating voltage. For the removal of the resist after metal deposition (lift-off) the exposure must cause the resist to exhibit a small undercut after developing. This is achieved by an exposure dose of $90 \mu\text{C cm}^{-2}$ eventually yielding very good lift-off results in dioxolane and acetone. Metal deposition (60 nm Au) was carried out by thermal evaporation to provide high deposition anisotropy. Figure 5 shows a completed CNT-FET device with deposited metal source and drain contacts. As an alternative to CNTs, which are randomly distributed after spin-on, 2D-TMDs such as 2D-WS₂ could be deposited using a transfer [37] or even low temperature growth process for example. In this case, alignment and layout of the transistor structures could be precisely prepared by conventional patterning processes including simple UV-lithography.

3.3. Metrology

Raman spectroscopy of graphene was performed with a Renishaw Raman InVia microscope using a 50× objective

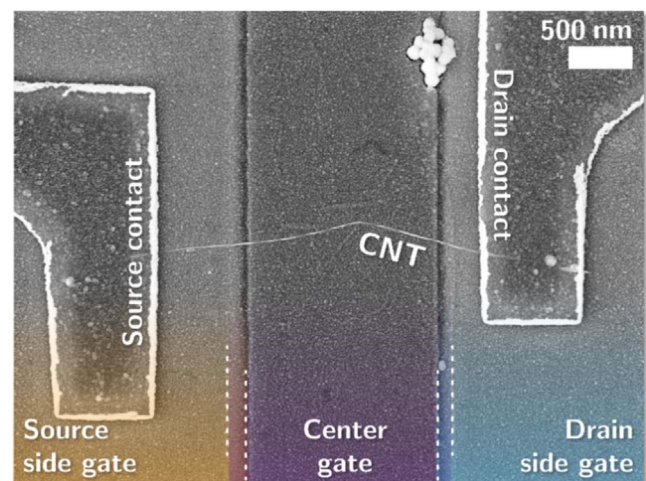


Figure 5. Completed CNT-FET on the substrate's surface: the example shows the metal S/D-contact terminals connected to the CNT laying across the center gate and both side gates on top of the heterostructure.

lens and a 532 nm laser excitation at 1% power (10 s exposure time, 3 accumulations). Scanning electron microscopy (SEM) images were obtained using a Zeiss Gemini Column within a Raith Pioneer System. For electrical characterization, a triaxial probe needle station with variable chuck temperature was used. The current/voltage characteristics were measured using an Agilent 4156C semiconductor analyzer (20 ms integration time).

4. Results and discussion

To evaluate the impact of plasma enhanced oxide deposition on the graphene layer, Raman measurements have been conducted. Figure 6 shows the Raman spectra before and after oxide deposition, respectively. The marked peaks reveal

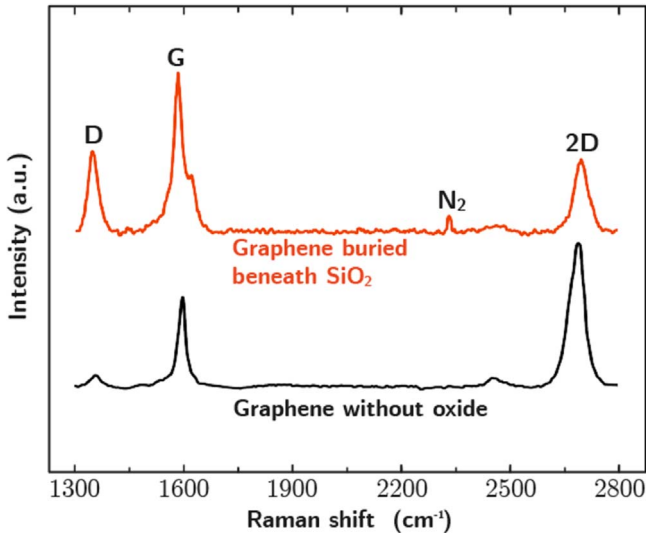


Figure 6. Characterization of the graphene center gate layer: Raman spectra of the transferred graphene sheet before (black curve) and after (orange curve) the oxide deposition. Note that both spectra are not equally scaled in intensity.

information about the graphene's morphology [38]. The D-peak reflects the likelihood of any scattering events happened with a lattice defect. Therefore, the smaller the D-peak, the smaller the defect concentration of the graphene [39]. Note that even for plain graphene without oxide deposition a D-peak appears, suggesting that the transferred graphene already exhibits some defects. However, an increase of defects after a wet-transfer of graphene is quite common and can be alleviated by time consuming procedures [35, 40]. The defect concentration is usually related to the quality of graphene, and the ratio of D- to G-peak makes a good indicator for evaluating the graphene's quality. Here, the D/G-ratio is 0.14 for the graphene before and 0.5 after the oxide deposition. According to Cançado *et al* this translates to approximated defect distances of $L_D > 24$ nm and >15 nm, respectively [41]. However, the Raman spectra suggest that even after oxide deposition, the graphene is still intact since the 2D-peak has only shifted by ~ 10 cm^{-1} from the graphene's characteristic signature 2D-peak at ~ 2674 cm^{-1} [39]. We also confirmed the presence of intact graphene by crossway electrical measurements throughout the structured graphene before and after the oxide deposition. We found that the electrical resistance increased by only 17% on average after oxide deposition. For our heterostructures, the electrical properties of the graphene layers are of minor importance, since the graphene is only used for electrostatic biasing and does not drive any significant electrical current. Thus, we conclude that the buried graphene layer is suitable enough to serve as gate electrode.

To verify the functionality of the fabricated device, output and transfer characteristics were measured at different temperatures. Figure 7(a) demonstrates the field effect transistor behavior based on the transfer characteristics (drain current I_D versus center gate voltage V_G) at room temperature (295 K), at 373 K and at 423 K, respectively, on a semi-logarithmic scale. Source side gate and drain side gate are set to 3 V and -3 V, respectively, implementing an asymmetric *pnn* and *ppn* doping

profile. As expected, the CNTs exhibits minimal *p*-type behavior due to the chemical doping effect of oxygen molecules adsorbed on their surface [42–44]. Since the side gates and the center gate are mutually aligned within the scope of optical lithography, a perfect overlap of the electrodes as suggested by FE simulations is not guaranteed for every sample. This and the non-optimized roughness of the graphene layer of 8 nm (see figure S1b in the supplementary data) results in an inverse subthreshold slope of 94 mV dec^{-1} and a threshold voltage of $V_{th} \approx -1$ V (see figure S3 in the supplementary data) at room temperature (295 K). A much better lateral alignment accuracy could be achieved by optimization of the UV mask layout or using EBL for platform fabrication. In this case we expect much smaller inverse subthreshold slopes.

The drain current I_D exhibits an on/off ratio of ~ 5 decades, which comes close to the recommendation of 6 decades by the International Roadmap for Devices and Systems (IRDS) [45]. With rising temperature, the on/off ratio reduces to ~ 4.2 decades at 373 K and ~ 3.3 decades at 473 K, respectively. This agrees to previous studies, which found that CNT-FET devices exhibit a lower dependence on temperature than MOSEFTs [46–48]. The overall center gate leakage current as illustrated in figure 7(b) is larger than for top gate architectures [49–51]. That is because the electrodes of source and drain cover a relatively large area on the surface all across the buried gate architecture, which eventually increases the possibility for leakage currents adding to the drain current at $V_G = 0$ V. This also contributes to the large inverse subthreshold slope and can be mitigated by improving the resistivity of the deposited oxides. However, the gate current here is still low enough for a proof-of-concept and has only a small impact on the drain current characteristic.

Figures 7(c) and (d) show the output characteristics for different gate voltages ranging from -3 to -1.5 V at different temperatures. We estimated the hole mobility μ_h (*p*-type, *ppn*) at room temperature from the transconductance $dI_D/dV_G = \mu_h(C/L^2)V_{DS}$ at $V_{DS} = 25$ mV. Where $L = 1.8$ μm is the CNT length, and C the capacity per unit length approximated by a cylindrical geometry, i.e. $C/L = 2\pi\epsilon_0\epsilon_{ox}/\ln(2d_{ox}/r)$. ϵ_0 is the permittivity of vacuum and r the CNT radius. According to the supplier of the CNTs, the radius is in-between $r = 1$ nm and $r = 2$ nm. Since the energetic alignment of the intrinsic region is controlled by the center gate we use $d_{ox} = 20$ nm, that is the thickness of the top oxide, and a relative permittivity for SiO_2 of $\epsilon_{ox} = 3.9$. From figures 7(c) and (d) we find $dI_D/dV_G = 5$ nA V^{-1} in the saturation regime. Thus, the calculated hole mobility is between $\mu_h = 49.6$ $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$ (for $r = 2$ nm) and $\mu_h = 61.1$ $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$ (for $r = 1$ nm), which is comparable to that of previous CNT-FET studies [52–54]. Additionally, we altered the doping configuration to a symmetric setup to investigate the impact of the side gates. Figure 7(e) shows how the performance is drastically reduced for *npn* to *nnn* and *pnp* to *ppp* configurations. In case of disabling (floating contacts) the side gates all along (figure 7(f)—blue curve) or in case of short-circuiting all side gates (figure 7(f)—red curve) the performance is better than for symmetric doping, but still inferior to asymmetric doping. The minimum I_D off-current at $V_G = 0$ V is about an order of

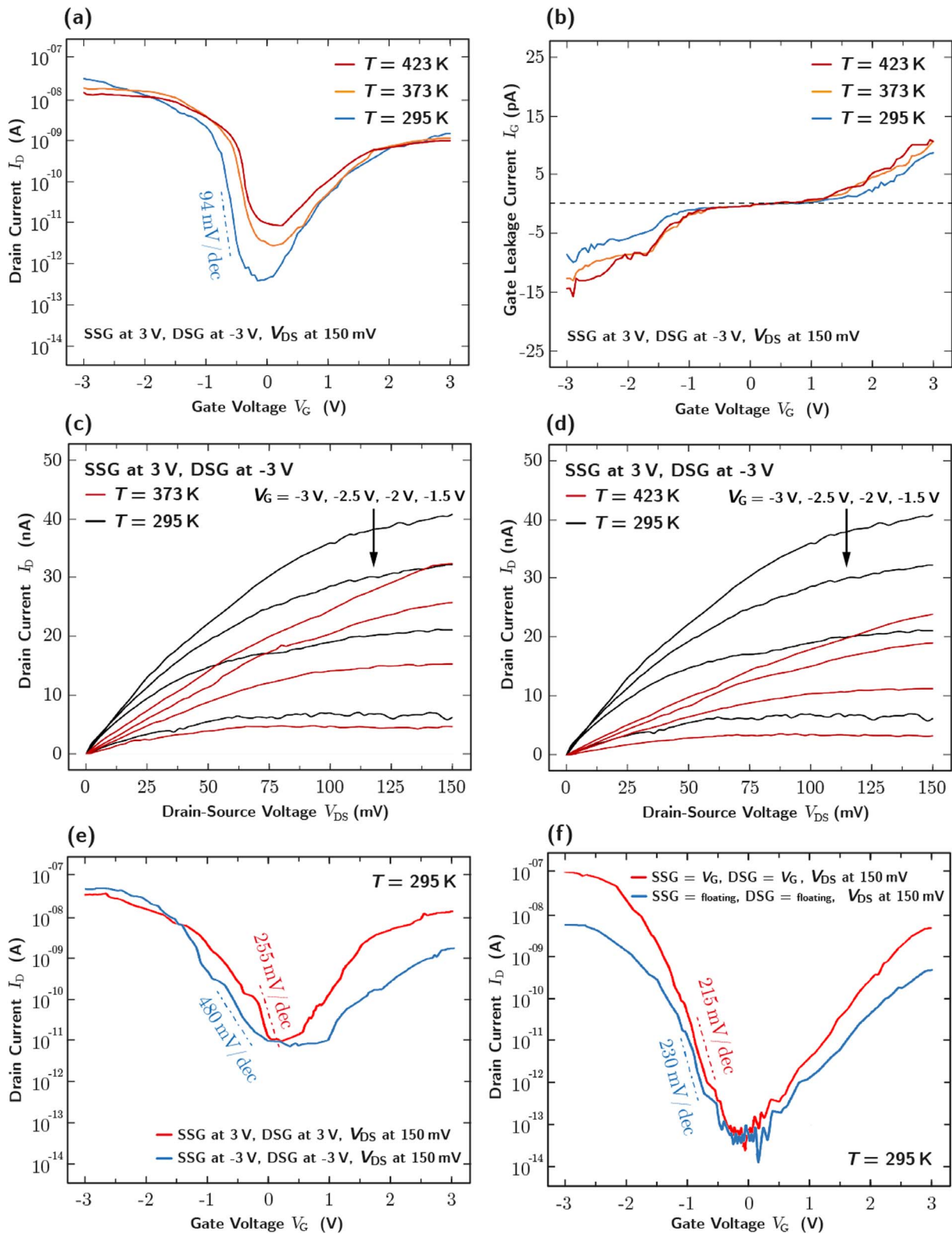


Figure 7. CNT-FET current/voltage measurements: (a) transfer characteristic at different temperatures on a semi-log scale, drain-source voltage was set to $V_{DS} = 150$ mV. Source side gate and drain side gate are setup in a static asymmetric configuration: $V_{SSG} = 3$ V, $V_{DSG} = -3$ V. (b) Corresponding gate leakage current I_G (center gate) versus V_G with a maximum absolute current of $I_G = 1.5 \cdot 10^{-11}$ A. (c), (d) Output characteristic at different temperatures for different gate voltages ranging from -3 to -1.5 V with the same side gate configuration. (e) Transfer characteristic for a symmetric doping profile (red curve: $V_{SSG} = V_{DSG} = 3$ V, blue curve: $V_{SSG} = V_{DSG} = -3$ V). (f) Transfer characteristic for floating side gates (blue curve) and for a gate union $V_{SSG} = V_{DSG} = V_G$.

Table 1. Comparison of recent studies on similar devices, with sgFET = single gated field effect transistor, TFET = tunnel field effect transistor, BTG = buried tripe gate and BSG = buried single gate. The characteristics of the single-gated CNT with BSG platform is shown in figure S2 in the supplementary data.

| Channel material | S^{-1} (mV dec ⁻¹) | $I_{D,On}$ (A) | $I_{D,Off}$ (A) | Contact material | Platform | References |
|------------------|----------------------------------|---------------------------|--------------------------|-------------------|-----------------|------------|
| CNT | 94 | $\sim 3.5 \times 10^{-8}$ | $\sim 5 \times 10^{-13}$ | Au | TFET, BTG | This study |
| WSe ₂ | 180 | $\sim 1 \cdot 10^{-6}$ | $\sim 9 \times 10^{-12}$ | Ni | TFET, BTG | [58] |
| CNT | 198 | $\sim 10^{-8}$ | $\sim 2 \times 10^{-14}$ | Au | sgFET, BSG | This study |
| CNT | 85 | $\sim 2 \times 10^{-6}$ | $\sim 3 \times 10^{-9}$ | Co-Mo alloy | sgFET, Top-Gate | [55] |
| CNT | 73 | $\sim 8 \times 10^{-6}$ | $\sim 5 \times 10^{-10}$ | Ti/Au to graphene | sgFET, Top-Gate | [56] |
| Si-NW | 90 | $\sim 2 \times 10^{-6}$ | $\sim 4 \times 10^{-15}$ | NiSi ₂ | Double Top-Gate | [57] |

magnitude lower since the side gate potential does no longer contribute to the overall channel potential. A similar performance is observed for a single-gated CNT as shown in figure S2 in the supplementary data. In this configuration the subthreshold behavior is dominated by the thermally broadened Fermi distribution, which results in a much larger inverse subthreshold slope of $S^{-1} = 198$ mV dec⁻¹ compared to 94 mV dec⁻¹ for triple-gated asymmetric doping. Obviously, the asymmetric doping has a strong impact on the transistor performance. In this context it is important to note, that the inverse subthreshold slope with asymmetric doping is also not affected by the temperature (see figure 7(a)). Therefore, we conclude that the charge transport for a CNT with asymmetric doping is indeed dominated by band-to-band tunneling. Further optimization of the platform (such as better alignment of the CNT to the surface, thinner top and intermediate oxide, and replacement of SiO₂ by an oxide with larger ϵ_{ox} like Al₂O₃) may allow to further decrease the inverse subthreshold slope potentially even below the thermoionic limit of 60 mV dec⁻¹ at room temperature.

To put our research into perspective, table 1 lists a comparison of similar devices with respect to the inverse subthreshold slope S^{-1} , the maximum drain on- and minimum off-current $I_{D,On}$ and $I_{D,Off}$, respectively, the channel and contact-material, and the platform used for gating. Note, the table makes no claim to completeness and in general comparison between difference devices is difficult due to different device geometries, CNT/NW radius, oxide thickness, etc. Relatively small S^{-1} are reported for top-gated CNTs in this table [55, 56]. However, for these devices, the ratio $I_{D,On}:I_{D,Off}$ is only 2–3 orders of magnitude, which is considered to be too low for most applications. A much larger $I_{D,On}:I_{D,Off}$ of 9 orders of magnitude has been reported for a double top-gated silicon nanowire (Si-NW) with an inverse subthreshold slope of 90 mV dec⁻¹ [57], which is comparable to our asymmetrically doped CNT. In this device, one gate electrode is used to control the field effect while the other gate electrode can be used to electrostatically program the device into *n*-type or *p*-type operation. However, similar to single-gated configuration and in contrast to the here proposed heterostructure, the minimum inverse subthreshold slope that can be achieved is fundamentally limited to the thermally broadened Fermi distribution.

The CNT-FET measurements demonstrated the working principle of our new heterostructure for electrostatic doping of low-dimensional materials. The platform is universal and can

be used for application and analysis of electrostatic doping of various 1D- and 2D-materials. As a proof-of-concept, the heterostructures were fabricated using UV-lithography, demonstrating that steep electrostatic potential gradients can be achieved using even very simple patterning technologies. In contrast to the concept reported by Müller *et al* [12, 26], further improvement and lateral downscaling well below the 100 nm lateral dimensions can be obtained using mask optimization or high-resolution patterning technologies, including electron-beam lithography. In addition, the steepness of the doping gradient strongly depends on the oxide thicknesses (see figure 3). For simplification of the fabrication process, we used relatively thick (20 nm) SiO₂ layers prepared by a well-established PECVD process, to ensure low leakage currents from the buried gate electrodes to the source- and drain-contact pads. Further optimization of the SiO₂ PECVD process may allow for much thinner oxide layers. Instead of PECVD, ozone-enhanced thermal atomic layer deposition of ultra-thin and highly insulating oxides (well below 10 nm) on graphene could also be used providing even sharper potential gradients [52, 59]. Moreover, in follow-up studies, the simple graphene transfer process could be replaced by a high-quality wafer-scale transfer or (potentially) even direct growth of graphene on oxides for complete wafer-scale fabrication of the heterostructures. We also note that recently established techniques using computer vision to find isolated CNTs, followed by automated electrode routing, could be used to increase the manufacturing throughput of these randomly distributed CNT devices [60].

5. Conclusions

In this study we demonstrated the feasibility of a graphene heterostructure to implement an individually configurable electrostatic doping profile for a CNT-FET device. Fabrication of the platform was done by conventional UV-lithography partially on wafer-scale to establish a simple and reproducible process while still being able to convey fabrication to high resolution patterning technologies. Proof-of-concept electrical measurements of CNT-FET devices demonstrated field-effect transistor characteristics with an inverse subthreshold slope down to 94 mV dec⁻¹. Smaller inverse subthreshold slopes may be achievable by optimizing the patterning process, the intermediate oxide thicknesses and

buried electrode overlapping. Increasing the temperature showed a decrease in performance, however, less pronounced than for conventional MOSFET devices. A variation in the doping profile was successfully shown for a number of possible configurations, such as asymmetric doping (*pnn*, *ppn*) and symmetric doping (*npn*, *nnn* and *pnp*, *ppp*). The demonstrated platform can be used for application and analysis of electrostatic doping of emerging low-dimensional materials including 2D dichalcogenides such as WS₂ or WSe₂ and may unlock their application potential for novel steep slope transistor devices.

Acknowledgments

JAA-W acknowledges the support of his Royal Society Dorothy Hodgkin Research Fellowship. SH acknowledges funding from EPSRC (EP/P005152/1).

Data availability statement

The data that support the findings of this study are openly available at the following URL/DOI: <http://hdl.handle.net/2003/41227>.

ORCID iDs

A Gumprich  <https://orcid.org/0000-0002-5858-1149>

J A Alexander-Webber  <https://orcid.org/0000-0002-9374-7423>

S Hofmann  <https://orcid.org/0000-0001-6375-1459>

S Tappertzhofen  <https://orcid.org/0000-0003-3747-5627>

References

- [1] Troutman R R 1979 VLSI limitations from drain-induced barrier lowering *IEEE J. Solid-State Circuits* **14** 383–91
- [2] Sell B, An S, Armstrong J, Bahr D, Bains B, Bamberg R and Young N 2022 Intel 4 CMOS technology featuring advanced FinFET transistors optimized for high density and high-performance computing 2022 *IEEE Symp. on VLSI Technology and Circuits (VLSI Technology and Circuits)* (IEEE) pp 282–3
- [3] Skotnicki T, Hutchby J A, King T J, Wong H S and Boeuf F 2005 The end of CMOS scaling: toward the introduction of new materials and structural changes to improve MOSFET performance *IEEE Circuits Devices Mag.* **21** 16–26
- [4] Knoch J, Bjork M T, Riel H, Schmid H and Riess W 2008 One-dimensional nanoelectronic devices-towards the quantum capacitance limit 2008 *Device Research Conf.* (IEEE) pp 173–6
- [5] Knoch J 2009 Optimizing tunnel FET performance-Impact of device structure, transistor dimensions and choice of material 2009 *Int. Symp. on VLSI Technology, Systems, and Applications* pp 45–6
- [6] Knoch J, Mantl S and Appenzeller J 2007 Impact of the dimensionality on the performance of tunneling FETs: bulk versus one-dimensional devices *Solid-State Electron.* **51** 572–8
- [7] Kallis K T, Müller M R, Knoch J, Gumprich A and Merten D 2017 Electrostatic doping of 2D-materials—from single devices toward circuitry exploration *Quantum Matter* **6** 45–9
- [8] Appenzeller J, Lin Y M, Knoch J and Avouris P 2004 Band-to-band tunneling in carbon nanotube field-effect transistors *Phys. Rev. Lett.* **93** 196805
- [9] Gnani E, Reggiani S, Gnudi A and Baccarani G 2011 Steep-slope nanowire FET with a superlattice in the source extension *Solid-State Electron.* **65** 108–13
- [10] Richter S, Blaesser S, Knoll L, Trelenkamp S, Fox A, Schäfer A and Mantl S 2014 Silicon–germanium nanowire tunnel-FETs with homo- and heterostructure tunnel junctions *Solid-State Electron.* **98** 75–80
- [11] Burke A M, Carrad D J, Gluschke J G, Storm K, Fahlvik Svensson S, Linke H and Micolich A P 2015 InAs nanowire transistors with multiple, independent wrap-gate segments *Nano Lett.* **15** 2836–43
- [12] Müller M R, Salazar R, Fathipour S, Xu H, Kallis K, Künzelmann U and Knoch J 2016 Gate-controlled WSe₂ transistors using a buried triple-gate structure *Nanoscale Res. Lett.* **11** 1–6
- [13] Grap T, Riederer F, Gupta C and Knoch J 2017 Buried multi-gate InAs-nanowire FETs 2017 *47th European Solid-State Device Research Conf. (ESSDERC)* (IEEE) pp 82–5
- [14] Sridevi R and Pravin J C 2021 Two-dimensional transition metal dichalcogenide (TMD) materials in field-effect transistor (FET) devices for low power applications *Semiconductor Devices and Technologies for Future Ultra Low Power Electronics* (Boca Raton, FL: CRC Press) pp 253–88
- [15] Bhuwarka K K, Born M, Schindler M, Schmidt M, Sulima T and Eisele I 2006 P-channel tunnel field-effect transistors down to sub-50 nm channel lengths *Jpn. J. Appl. Phys.* **45** 3106
- [16] Huang R, Huang Q, Chen S, Wu, C, Wang J, An X and Wang Y 2014 High performance tunnel field-effect transistor by gate and source engineering *Nanotechnology* **25** 505201
- [17] Yu W J and Lee Y H 2011 Strategy for carrier control in carbon nanotube transistors *ChemSusChem* **4** 890–904
- [18] Björk M T, Schmid H, Knoch J, Riel H and Riess W 2009 Donor deactivation in silicon nanostructures *Nat. Nanotechnol.* **4** 103–7
- [19] Gupta G, Rajasekharan B and Huetting R J 2017 Electrostatic doping in semiconductor devices *IEEE Trans. Electron Devices* **64** 3044–55
- [20] Prete D, Demontis V, Zannier V, Rodriguez-Douton M J, Guazzelli L, Beltram F and Rossella F 2021 Impact of electrostatic doping on carrier concentration and mobility in InAs nanowires *Nanotechnology* **32** 145204
- [21] Heinzig A, Slesazek S, Kreupl F, Mikolajick T and Weber W M 2012 Reconfigurable silicon nanowire transistors *Nano Lett.* **12** 119–24
- [22] Mikolajick T, Heinzig A, Trommer J, Baldauf T and Weber W M 2017 The RFET—a reconfigurable nanowire transistor and its application to novel electronic circuits and systems *Semicond. Sci. Technol.* **32** 043001
- [23] Kim T, Lim D, Son J, Cho K and Kim S 2022 Reconfiguration of operation modes in silicon nanowire field-effect transistors by electrostatic virtual doping *Nanotechnology* **33** 415203
- [24] Knoch J and Mueller M R 2014 Electrostatic doping—controlling the properties of carbon-based FETs with gates *IEEE Trans. Nanotechnol.* **13** 1044–52
- [25] Finge T, Riederer F, Mueller M R, Grap T, Kallis K and Knoch J 2017 Investigations on field-effect transistors based on two-dimensional materials *Ann. Phys.* **529** 1700087
- [26] Mueller M R, Gumprich A, Schuette F, Kallis K, Kuenzelmann U, Engels S and Knoch J 2014 Buried triple-gate structures for advanced field-effect transistor devices *Microelectron. Eng.* **119** 95–9

- [27] Knoch J and Appenzeller J 2010 Modeling of high-performance p-type III–V heterojunction tunnel FETs *IEEE Electron Device Lett.* **31** 305–7
- [28] Müller M R 2015 Buried triple-gate structures for tunnel FETs based on emerging research *Materials Verlagshaus Mainz* (Süsterfeldstraße 83, 52072 Aachen, Germany: Druck-und Verlagshaus Mainz GmbH) p 86
- [29] Müller M R, Gumprich A, Ecik E, Kallis K T, Winkler F, Kardynal B and Knoch J 2015 Visibility of two-dimensional layered materials on various substrates *J. Appl. Phys.* **118** 145305
- [30] Pang J, Mendes R G, Wrobel P S, Wlodarski M D, Ta H Q, Zhao L and Rummeli M H 2017 Self-terminating confinement approach for large-area uniform monolayer graphene directly over Si/SiO_x by chemical vapor deposition *ACS Nano* **11** 1946–56
- [31] Deokar G, Avila J, Razado-Colambo I, Codron J L, Boyaval C, Galopin E and Vignaud D 2015 Towards high quality CVD graphene growth and transfer *Carbon* **89** 82–92
- [32] Zhang Z, Du J, Zhang D, Sun H, Yin L, Ma L and Ren W 2017 Rosin-enabled ultraclean and damage-free transfer of graphene for large-area flexible organic light-emitting diodes *Nat. Commun.* **8** 1–9
- [33] Sutter P W, Flege J I and Sutter E A 2008 Epitaxial graphene on ruthenium *Nat. Mater.* **7** 406–11
- [34] Wang R, Whelan P R, Braeuninger-Weimer P, Tappertzhofen S, Alexander-Webber J A, Van Veldhoven Z A and Hofmann S 2016 Catalyst interface engineering for improved 2D film lift-off and transfer *ACS Appl. Mater. Interfaces* **8** 33072–82
- [35] Ullah S, Yang X, Ta H Q, Hasan M, Bachmatiuk A, Tokarska K and Rummeli M H 2021 Graphene transfer methods: a review *Nano Res.* **14** 3756–72
- [36] Macintyre D S, Ignatova O, Thoms S and Thayne I G 2009 Resist residues and transistor gate fabrication *J. Vac. Sci. Technol. B* **27** 2597–601
- [37] Delabie A, Caymax M, Groven B, Heyne M, Haesevoets K, Meererschaut J and Thean A 2015 Low temperature deposition of 2D WS₂ layers from WF₆ and H₂S precursors: impact of reducing agents *Chem. Commun.* **51** 15692–5
- [38] Ferrari A C, Meyer J C, Scardaci V, Casiraghi C, Lazzeri M, Mauri F and Geim A K 2006 Raman spectrum of graphene and graphene layers *Phys. Rev. Lett.* **97** 187401
- [39] Narula R and Reich S 2008 Double resonant Raman spectra in graphene and graphite: a two-dimensional explanation of the Raman amplitude *Phys. Rev. B* **78** 165422
- [40] Park H, Lim C, Lee C J, Kang J, Kim J, Choi M and Park H 2018 Optimized poly (methyl methacrylate)-mediated graphene-transfer process for fabrication of high-quality graphene layer *Nanotechnology* **29** 415303
- [41] Cañado L G, Jorio A, Ferreira E M, Stavale F, Achete C A, Capaz R B and Ferrari A C 2011 Quantifying defects in graphene via Raman spectroscopy at different excitation energies *Nano Lett.* **11** 3190–6
- [42] Martel R, Derycke V, Lavoie C, Appenzeller J, Chan K K, Tersoff J and Avouris P 2001 Ambipolar electrical transport in semiconducting single-wall carbon nanotubes *Phys. Rev. Lett.* **87** 256805
- [43] Derycke V, Martel R, Appenzeller J and Avouris P 2002 Controlling doping and carrier injection in carbon nanotube transistors *Appl. Phys. Lett.* **80** 2773–5
- [44] Yamada T 2004 Publisher's Note: Modeling of carbon nanotube Schottky barrier modulation under oxidizing conditions [Phys. Rev. B 69, 125408 (2004)] *Phys. Rev. B* **69** 159901
- [45] IRDS; International Roadmap for Devices and Systems 2021 Process Integration, Devices, and Structures (PIDS); Online; URL (<https://aeneas-office.org/2021/11/18/international-roadmap-for-devices-and-systems-irds-2021-edition-available/>) (as of 2022)
- [46] Sinha S K and Chaudhury S 2014 Comparative study of leakage power in CNTFET over MOSFET device *J. Semiconduct.* **35** 114002
- [47] Sinha S K and Chaudhury S 2013 Impact of temperature variation on CNTFET device characteristics *2013 Int. Conf. on Control, Automation, Robotics and Embedded Systems (CARE)* (Piscataway, NJ: IEEE) pp 1–5
- [48] Marani R and Perri A G 2021 Temperature Dependence of IV Characteristics in CNTFET Models: A Comparison *Int. J. Nanosci. Nanotechnol.* **17** 33–9
- [49] Pei T, Zhang Z, Wang Z, Ding L, Wang S and Peng L M 2011 Temperature performance of doping-free top-gate CNT field-effect transistors: potential for low-and high-temperature electronics *Adv. Funct. Mater.* **21** 1843–9
- [50] Nihey F, Hongo H, Yudasaka M and Iijima S 2002 A top-gate carbon-nanotube field-effect transistor with a titanium-dioxide insulator *Jpn. J. Appl. Phys.* **41** L1049
- [51] Wind S J, Appenzeller J, Martel R, Derycke V P P A and Avouris P 2002 Vertical scaling of carbon nanotube field-effect transistors using top gate electrodes *Appl. Phys. Lett.* **80** 3817–9
- [52] Alexander-Webber J A, Sagade A A, Aria A I, Van Veldhoven Z A, Braeuninger-Weimer P, Wang R and Hofmann S 2016 Encapsulation of graphene transistors and vertical device integration by interface engineering with atomic layer deposited oxide *2D Mater.* **4** 011008
- [53] Xiao K, Liu Y, Hu P A, Yu G, Wang X and Zhu D 2003 High-mobility thin-film transistors based on aligned carbon nanotubes *Appl. Phys. Lett.* **83** 150–2
- [54] Martel R, Schmidt T, Shea H R, Hertel T and Avouris P 1998 Single-and multi-wall carbon nanotube field-effect transistors *Appl. Phys. Lett.* **73** 2447–9
- [55] Cao Q, Tersoff J, Farmer D B, Zhu Y and Han S J 2017 Carbon nanotube transistors scaled to a 40-nanometer footprint *Science* **356** 1369–72
- [56] Qiu C, Zhang Z, Xiao M, Yang Y, Zhong D and Peng L M 2017 Scaling carbon nanotube complementary transistors to 5-nm gate lengths *Science* **355** 271–6
- [57] Heinzig A, Slesazek S, Kreupl F, Mikolajick T and Weber W M 2012 Reconfigurable silicon nanowire transistors *Nano Lett.* **12** 119–24
- [58] Riederer F, Grap T, Fischer S, Mueller M R, Yamaoka D, Sun B and Knoch J 2018 Alternatives for doping in nanoscale field-effect transistors *Phys. Status Solidi (a)* **215** 1700969
- [59] Aria A I, Nakanishi K, Xiao L, Braeuninger-Weimer P, Sagade A A, Alexander-Webber J A and Hofmann S 2016 Parameter space of atomic layer deposition of ultrathin oxides on graphene *ACS Appl. Mater. Interfaces* **8** 30564–75
- [60] Potocnik T, Christopher P J, Mouthaan R, Albrow-Owen T, Burton O J, Jagadish C and Alexander-Webber J A 2022 Automated computer vision-enabled manufacturing of nanowire devices *ACS nano* (<https://doi.org/10.1021/acsnano.2c08187>)