Optimized Commutation Circuit for Improved Utilization of SiC

A thesis approved for the academic degree of

Doktor der Ingenieurwissenschaften (Dr.-Ing.)

at the

Faculty of Electrical Engineering and Information Technology

TU Dortmund University

by

M.Sc. Michael Schlüter
born on 08.07.1986
in Büren

Supervisor: Univ.-Prof. Dr.-Ing. Martin Pfost, TU Dortmund University
Co-Advisor: Univ.-Prof. Dr.-Ing. Andreas Lindemann, Otto-von-Guericke-Universität

Day of Oral Examination: 08.12.2023

Contents

1 Introduction **1**
1.1 Thematic Classification . . . 2
1.2 Problem Description . . . 2
1.3 Hypothesis and Research Questions . . . 5
1.4 Structure of the Thesis . . . 5

2 Basics and Technology Review **7**
2.1 Power Semiconductor Devices . . . 7
2.1.1 A Short Introduction to Semiconductor Materials . . . 7
2.1.2 Introduction to Diodes . . . 8
2.1.3 Introduction to MOSFETs . . . 10
2.2 Parasitic Inductances in Power Electronics . . . 13
2.2.1 Basic Geometries and Their Characteristics . . . 13
2.2.2 Consequences for Low- and High-Power Applications . . . 14
2.3 Hard and Soft Switching . . . 15
2.3.1 Description of the Turn-On Event . . . 17
2.3.2 Description of the Turn-Off Event . . . 18
2.3.3 Resonant Switching . . . 19
2.4 Introduction to Snubbers . . . 22
2.4.1 DC-Snubber . . . 22
2.4.2 Turn-Off Snubber . . . 25
2.4.3 Power Loss Estimation . . . 25
2.5 Ceramic Capacitors . . . 26
2.5.1 Mechanical Construction . . . 27
2.5.2 Dielectric Materials . . . 27
2.5.3 Electrical Characteristics . . . 29

3 Introduction and Modeling of an Optimized Commutation Circuit **31**
3.1 Optimized Circuit Introduction . . . 32
3.2 Operation at Turn-On and Diode Recovery . . . 33
3.3 Operation at Turn-Off . . . 36
3.4 Modeling the Turn-On Event . . . 39
3.5 Modeling the Turn-Off Event . . . 43

4 Model Validation and Application **48**
4.1 Module Assembly and Measurement Description . . . 48
4.1.1 Capacitor Selection . . . 48
4.1.2 Conventional Halfbridge . . . 50
4.1.3 Halfbridge with DC-Snubber . . . 50
4.1.4 Halfbridge with Active Snubber . . . 52
4.2 Turn-On Model Validation for High Operation Currents . . . 53
4.3 Turn-On Model Validation for Low Operation Currents . . . 58
4.4 Turn-Off Model Validation for High Operation Currents . . . 62

4.5 Turn-Off Model Validation for Low Operation Currents . . . 68
4.6 Continuous Operation at High Load Current . . . 74
4.7 Continuous Operation at Low Load Current . . . 77
4.8 Continuous Operation at Sinusoidal Load Current . . . 80

5 Setup Comparison 84
5.1 Finding Appropriate Gate Resistors . . . 84
5.1.1 Turn-Off Event . . . 84
5.1.2 Turn-On and Diode Recovery . . . 86
5.2 Comparing Switching Waveforms . . . 89
5.2.1 Comparison of the Turn-Off Event . . . 89
5.2.2 Comparison of the Turn-On Event . . . 95
5.2.3 Comparison of the Diode-Recovery Event . . . 98
5.3 Behavior within Operation Range . . . 100
5.3.1 Voltage Gradients . . . 100
5.3.2 Reverse Recovery Peak Current . . . 103
5.3.3 Switching Losses . . . 104
5.3.4 Damping Losses . . . 107
5.3.5 On-State Resistance . . . 109
5.4 Achievable Output Power for Inverter Operation . . . 109
5.4.1 Evaluation of Losses . . . 110
5.4.2 Achievable Inverter Output Power . . . 113
5.4.3 Inverter Efficiency . . . 114

6 Operation with Pulsed LC filter 117
6.1 Active Filter Introduction . . . 117
6.2 Filter Dimensioning . . . 119
6.3 Discharge Pulse . . . 120
6.4 Charge Pulse . . . 121
6.5 Comparison to IGBT-Setup . . . 123

7 Summary and Outlook 127
7.1 Summary . . . 127
7.2 Outlook . . . 129

A Mathematical derivations 131
A.1 Calculation of Density of States . . . 131
A.2 Equations of an RLC Circuit . . . 132
A.3 Analytical Derivation of Active Snubber Turn-On . . . 134
A.3.1 Fundamental Equations . . . 134
A.3.2 Solution for the First Interval . . . 135
A.3.3 Solution for the Second Interval . . . 136
A.3.4 Solution for the Third Interval . . . 137
A.3.5 Solution for the Fourth Interval . . . 139
A.4 Analytical Derivation of Active Snubber Turn-Off . . . 142
A.4.1 Fundamental Equations . . . 142
A.4.2 Solution for the First Interval . . . 144
A.4.3 Solution for the Second Interval . . . 145

A.4.4 Solution for the Third Interval . . . 150
A.5 Determining the Thermal Resistance . . . 156
A.6 Inverter Calculation Scheme . . . 159

B Detailed Setup Description **162**
B.1 Gate Driver . . . 162
B.2 Basic Measurement Setup . . . 164

C Documented Data **166**
C.1 Model Coefficients for Loss Estimation . . . 166

List of Figures **167**

List of Tables **170**

List of Symbols **171**

List of Abbreviations **179**

Bibliography **180**

List of own Publications **193**

Kurzfassung

MOSFETs aus Siliziumcarbid setzen sich zunehmend als sinnvoller Ersatz für etablierte Silizium-IGBTs durch. Dennoch kann als großer Nachteil die weiterhin hohe Defektdichte im Rohmaterial genannt werden. Um die Ausnutzung des Halbleitermaterials zu verbessern, bietet sich insbesondere die Reduktion von Halbleiterverlusten an. Diese setzen sich aus Schaltverlusten und Durchlassverlusten zusammen. Hierbei sind die Durchlassverluste durch den Einschaltwiderstand abhängig von der Durchbruchspannung des Bauteils und die Schaltverluste von der erreichbaren Schaltgeschwindigkeit. Letztere ist dabei limitiert durch die maximale Abschaltüberspannung, welche ebenfalls von der Durchbruchspannung sowie der Streuinduktivität abhängt. Somit ist bei signifikanter Reduktion der Streuinduktivität eine Reduktion der Gesamthalbleiterverluste zu erwarten.
In dieser Arbeit werden dabei zunächst der Stand der Technik dargelegt und wesentliche Bauteileigenschaften und Aufbaulimitierungen erklärt. Entscheidende Limitierungen in der Reduktion der Streuinduktivität stellen dabei dessen Verteilung auf Zwischenkreis und Leistungsmodul, die Verbindung zwischen beiden sowie Anforderungen an automatisierte Fertigung dar. Als mögliche Lösung werden DC-Snubber diskutiert, wobei diese durch hohe Dämpfungsverluste für höhere Ströme uninteressant werden.
Darauf aufbauend wird ein aktiv gesteuerter Snubber vorgestellt und dessen Betriebsweise am Beispiel einer Halbbrücke beschrieben. Die Schaltung erlaubt dabei eine starke Reduktion der Streuinduktivität im Abschaltmoment, wodurch Abschaltverluste und Durchlassverluste verbessert werden. Zudem besitzt die Schaltung eine große Streuinduktivität im Einschaltvorgang, wodurch Einschaltverluste vernachlässigbar werden. Desweiteren wird die Betriebsweise analytisch beschrieben, wodurch sich Optimierungsmöglichkeiten für zero-current-switching des Hilfsschalters aufzeigen.
Anschließend wird das hergeleitete Modell mit Messungen validiert, mit dessen Hilfe das Schaltungsverhalten für aufeinanderfolgende Schaltvorgänge berechnet und mit einem DC-Snubber verglichen. Hierbei zeigt sich, dass die Spannung des Snubber-Kondensators alternierend um einen stabilen Endwert konvergiert und für gleiche maximale Kondensatorspannung die Snubberkapazität der Hälfte eines DC-Snubbers entspricht.
Für eine Bewertung der Ausnutzung werden exemplarisch Drei-Phasen-Inverter mit Hilfe messtechnisch bestimmer Charakterisierungsdaten für Schaltfrequenzen von 10 kHz und 30 kHz ausgelegt. Neben einer konventionellen Halbbrücke, einer Halbbrücke mit DC-Snubber und der Schaltung mit aktivem Snubber werden Setups für optimiertes Durchlassverhalten abgeschätzt. Um unbekannte Temperatureinflüsse optimierter Halbleiter zu vernachlässigen, wird dabei nur die Stromabhängigkeit des Einschaltwiderstandes berücksichtigt. Für 10 kHz zeigt sich dabei eine mögliche Steigerung der Ausgangsleistung von 35 % für nicht optimierten MOSFET und von 59 % für optimierten MOSFET.
Zuletzt wird mit der vorgestellten Schaltung ein LC-Filter aktiv angesteuert. Dabei soll der Einsatz für Anwendungen mit Begrenzungen in der Spannungssteilheit und ein Austausch konventioneller IGBTs geprüft werden. Hierbei konnte ein Zusammenhang mit der Snubberspannung und dem Timing des Pulsmusters für den Filter festgestellt werden. Ein Vergleich der Schaltverluste zu einem IGBT-Setup ähnlicher Leistung zeigte dabei eine Verlustreduktion von bis zu Faktor 20 bei gleichzeitig flacherer Flanke. Als nachteilig zeigte sich jedoch das Timing des aktiven Snubbers für die Minimierung des Filters.

Abstract

Silicon carbide MOSFETs have gained popularity over established silicon IGBTs. However, a major drawback is a still high defect density in the raw material. To improve the utilization of the semiconductor material, especially the reduction of semiconductor losses is reasonable. The semiconductor losses can be separated into conduction and switching losses. The conduction losses with the on-state resistance are dependent on the device breakdown voltage and switching losses from the achievable switching speed. Latter is limited by the maximum turn-off voltage overshoot, which is also dependent on the breakdown voltage and from the system stray inductance. Hence, significantly reducing the stray inductance impacts both conduction and switching losses.
In this work, the current state-of-the-art is stated, important device properties and setup limitations are outlined. It is shown that the distribution of the stray inductance above the DC-link, the power module and the interconnection of both as well as requirements for automated production are major limitations for its reduction. As a potential solution DC-snubbers are discussed but due to increasing damping losses they become uninteresting for higher currents.
Considering this, an active controlled snubber is introduced and its manner of operation with a halfbridge is described. The setup allows a strong reduction of the stray inductance for turn-off, which allows improvement of turn-off and conduction losses. Additionally, the setup provides a large stray inductance for turn-on, whereby the turn-on losses become negligible. Further, the manner of operation is described analytically, which shows opportunities for zero-current-switching of the auxiliary switch. Afterwards, the derived model is validated using measurements and is used to predict the behavior for subsequent switching events.
The results are compared with a similar DC-snubber setup. It could be found that the snubber voltage shows an alternating but stable behavior and, a maximum snubber voltage, which is half of that of a similar DC-snubber.
To judge the utilization, three-phase inverters have been designed for switching frequencies of 10 kHz and 30 kHz based on data measured with reference designs. In addition to a conventional halfbridge, a halfbridge with DC-snubber and the active snubber setup, further setups with an optimized conduction behavior are estimated. To neglect unknown temperature dependencies of hypothetically optimized semiconductors, only the current dependency is considered. For a switching frequency of 10 kHz, a possible increase in the inverter output power of 35 % could be found for a non-optimized semiconductor and 59 % for an optimized MOSFET.
Finally, the introduced setup is used to actively drive a small LC-filter. Here, the usage in applications with restrictions on the maximum voltage slope shall be evaluated. A dependency of the snubber voltage and the timing of the filter pulses could be found. A comparison to a state-of-the-art IGBT setup with similar output power showed a reduction in switching losses by a factor of 20 with a simultaneously lower voltage slope. However, it could be found that the time constants of the snubber circuit limit the minimization of the LC-filter.

1 Introduction

Power electronics are a key technology for efficient processing of electrical energy. In the past, increasing energy costs were a major driver for continuous improvements in semiconductor and material technology. Today, the increasing awareness of resource depletion and environmental pollution together with the increasing demand for energy presupposes the use of evolved energy conversion and storage technologies. This has led to a transformation process from using fossil-based energy sources to electrification powered by renewable energies, see [1]. Power electronics is a key technology for increased energy efficiency and e-mobility is an accelerator for further technology development, see [2]. While in most applications power electronic devices are used as switches, this allows an efficient processing of electrical energy, which is a major driver for success of power electronics in recent decades. During the development of a power electronic device the reduction of losses is one of the most important goals because it affects the achievable output power and efficiency immediately. Besides the conduction losses of a turned-on semiconductor, the switching losses are relevant, especially in applications with higher switching frequencies. Today, in most low-voltage applications up to approximately 1 kV metaloxide-semiconductor field-effect-transitors (MOSFETs) are the preferred switches. Because of low switching losses, it allows the highest switching frequencies, but the conduction losses caused by a high on-state resistance increase if the device is rated for higher voltages, see [3, 4].
For higher voltage ratings up to approximately 6.5 kV the insulated gate bipolar transistor (IGBT) shows acceptable conduction losses. Because of the bipolar behavior, conduction losses for high current operation points are lower. To limit the overall losses, an IGBT used at high switching frequencies must be rated for low current and voltage, [4] S.3ff.
As in other areas, silicon (Si) is still the most commonly used material for power semiconductors, see [5]. It is the most mature material in terms of production, technical expertise and low cost. Nevertheless, the physical characteristics of silicon make further significant improvements challenging. Devices made from silicon show some important limitations in switching speed, the capability of blocking voltage and the maximum operation temperature.
Since several years, materials with higher bandgap, such as silicon carbide (SiC) or gallium nitride (GaN) are subject of research or are even available on the market. Their advantages compared to silicon are well known, cf. [5–7]. Due to the availability of vertical SiC-MOSFET devices allowing higher breakdown voltages compared to lateral GaN devices, SiC is interesting for higher power applications [8]. Nevertheless, excessive material cost, cf. [9], and a strong tendency to oscillations, cf.[10], may limit the possible substitution of Si-IGBTs in many classic applications with SiC-MOSFET devices. Therefore, several laborious approaches are considered to increase the output power per chip area or the power density respectively. One approach is a better cooling structure, which allows higher losses and in conclusion, a higher power output per volume. Power modules as assemblies of several semiconductor dies usually soldered on a ceramic substrate with advanced cooling structures such as PinFin base plates and double-sided cooled devices or combinations have been topic of research and are available on the market [11, 12]. Other approaches for loss reduction are to influence the switching behavior, see e.g. [13, 14], or

optimizing the commutation circuit, e.g. [15, 16]. For example, a reduction of the stray inductance has a positive effect towards a clean switching event [17] with less ringing and reduction of voltage overshoot at turn-off. Hence, the switching speed can be increased - with similar overvoltage - to reduce switching losses, or an operation at higher DC-link voltage can be allowed to improve the possible power output of an inverter.
Because the stray inductance of the switching cell consists of several partial inductances, like the equivalent series inductor (ESL) of the DC-link capacitor, the inductance of the power module and the connection between both, a reduction is challenging. Major challenges are e.g. the suitable assembly technologies or materials and creepage distances for higher voltage classes. Additionally, acceptable efforts for production and space limitations, have a significant influence on the total production cost. Therefore, for an optimal result the collaboration of capacitor and power module vendors might be required.

1.1 Thematic Classification

This work belongs to the field of electrical engineering with a focus on power electronics. It deepens the topics of minimizing switching losses and characteristics of SiC-MOSFETs and optimization of the switching behavior related to circuit parasitics at higher power classes. The overall goal is to develop an improved switching cell for the used switching technology at fastest switching for highest possible power output and efficiency. To achieve this goal, this work concerns with the corresponding technologies, e.g. trade-offs in semiconductor device dimensioning, optimizing circuit parasitics and the usage of snubber capacitors. Finally, an optimized commutation circuit is proposed focusing to enhance the achievable power output by allowing both higher switching speed and simultaneously higher DC-Link voltage.

1.2 Problem Description

As already mentioned, SiC-MOSFETs are a reasonable substitute for Si-IGBT in many applications. Since several years, SiC-MOSFETs have been available on the market [18]. Compared to Si-IGBTs in the 1.2 kV class, SiC-MOSFETs allow much faster switching speed and lower conduction and switching losses. However, while common system assemblies are designed for IGBTs, a simple replacement of the semiconductor dies may not lead to the optimal utilization of the expensive SiC-material. This is mainly related to the stray inductance of the switching cell limiting the switching performance as explained below for a common drive inverter.

A drive inverter consists of at least a power semiconductor arrangement, cf. Fig. 1.1 (green), connected to the driver electronic (orange), and a control unit (red). Depending on the application and power range, the connection (gray) to a DC capacitor (blue) can be carried out directly or through an arrangement such as a printed circuit board (PCB) (low-power) or a copper plate busbar arrangement (mostly high-power). The most common power semiconductor arrangement for this application is a three phase-leg configuration consisting of three halfbridges, see Fig. 1.1. For power levels above 10 kW power module assemblies are available, which provide a more compact design compared to a discrete assembly and usually a better cooling structure.

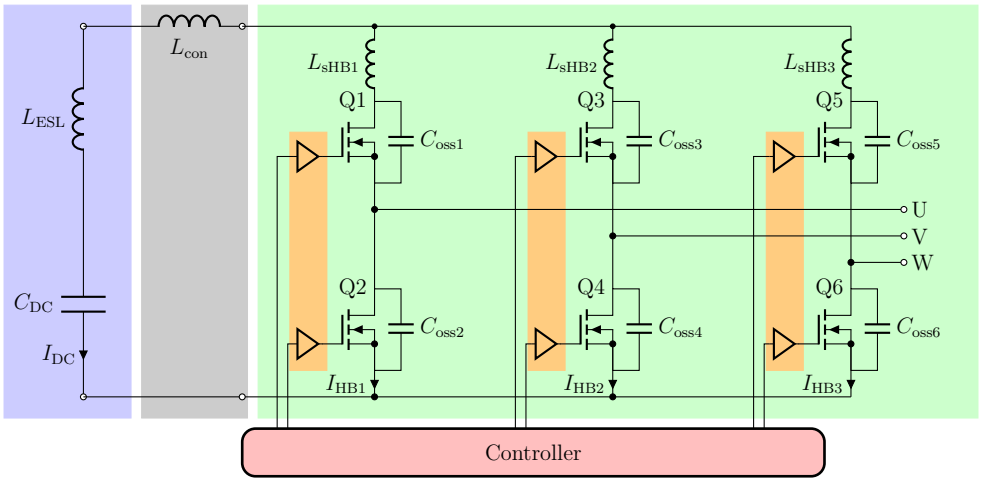


Figure 1.1: Basic inverter schematic with components

An important goal during construction is a low stray inductance between the DC-link capacitance C_{DC} and the semiconductor being a key factor for clean switching [17] and low voltage overshoot [19]. A major challenge in reducing stray inductance is that this inductance is distributed over the capacitor, connection and the power module halfbridge. Confer Fig. 1.1, with the ESL of the capacitor L_{ESL}, the connection inductance L_{con} and the inductance of a halfbridge L_{sHBn}, which is depicted as a lumped inductance. Because the inductance of a common planar conductor arrangement, cf. Fig. 2.6b, increases with conductor length and with the distance between the conductors or decreases with the width of a conductor, cf. Sect. 2.2.1, the problem can be derived by rationality. An inductance goal of zero can be achieved in theory by reducing distance and length to zero and increasing the width to infinity. Because of an infinite width immediately leads to an infinite effort in terms of material, cost and space, a widening of the width is very limited. Similarly, the minimum distance is usually limited by the maximum insulation voltage. Hence, further reduction relates also to the availability of better insulation material. In conclusion, only a reduction in the distance between the DC-link capacitor and the power semiconductor described by the conductor length is a reasonable solution.
However, the dimensioning of DC-link capacitance is related to the allowed current ripple and voltage ripple and the switching frequency [20]. Thus, common DC-link capacitors are comparatively large, see [21] and a small proximity between the capacitor and the semiconductor might be hard to achieve considering the requirement for a manageable inverter assembly into account. In summary, an optimal design is limited by the available capacitor technology, the design of the power module and a connection technology which must be acceptable for series production in terms of effort and costs. Thus, a close collaboration between capacitor supplier, power semiconductor supplier and potential customer is necessary.

For improved switching performance, on the one hand, a low stray inductance reduces the voltage overshoot during the negative current slope and thus, enabling faster switching at turn-off, the use of a higher DC-link voltage or alternatively a semiconductor technology with lower breakdown voltage and lower on-state resistance. On the other hand, a lower stray inductance increases the switching losses at turn-on [22, 23]. While a high stray inductance leads to a voltage drop during turn-on, this voltage drop is lower with a small

inductance. Hence, the semiconductor voltage during the current slope is higher with lower stray inductance and the losses are increased.
Consequently, for optimal efficiency, a compromise between switching and conduction losses, electromagnetic interference (EMI), DC-link voltage and acceptable manufacturing effort has to be made.
Another limitation of further switching loss reduction is the voltage slope allowed by the electric motor. A high voltage slope leads to stress on motor windings [24] as well as higher bearing currents [25] with a negative effect on the motor lifetime. Additionally, depending on the cable length between the motor and inverter, an edge reflection may occur on the motor terminals, leading to high peak voltages [26] and also higher insulation stress.
In conclusion, besides the allowed voltage slope, the energy in the stray inductance as root cause of overvoltage and ringing is one of the major obstacles for optimized switching behavior in terms of losses and oscillations.
In this work, a setup is presented, which actively makes use of this energy to significantly reduce the voltage overshoot, oscillation amplitude and switching losses. This allows a higher DC-link voltage and a better utilization of the wide-bandgap material (WBM) semiconductor device. Furthermore, it separates the requirements of a high capacitance and low inductance of the DC-link capacitor and therefore, it allows the usage of a less advanced DC-link capacitor and connection technology with higher stray inductance. Furthermore, it is shown that the proposed setup is compatible with the actively pulsed filter presented by [27]. Thus, it is also suitable for applications with a demand for very slow voltage slopes.

1.3 Hypothesis and Research Questions

In this chapter, the research hypotheses are derived from the problem description mentioned above. The research questions serve as a basis for the investigations carried out in this work.

- An optimized switching behavior can be achieved by an active management of the energy stored in the stray inductance.
- This has a significant contribution to increasing the efficiency and output power.
- Through the active energy management the semiconductor utilization is increased.
- With an active management of the energy stored in the stray inductance, concepts with larger stray inductance are possible and reasonable.
- The switching losses can be reduced and thus, higher switching frequencies and the operation of filters actively driven by the halfbridge for a reduced voltage slope are possible.

The above-listed hypotheses allow the formulation of the research questions.

- How can the energy in the stray inductance be used actively for improved switching characteristics?
- What influence does the found method have on the switching behavior?
- How large is the achievable influence on the system performance?
- Are the additional measures disadvantageous for the application?

Goal of this work is to develop a system with significantly increased performance, efficiency and improved utilization of WBM semiconductors. The system shall serve as a substitute for conventional power semiconductor modules used in inverters, as outlined in Chapter 1.2.

1.4 Structure of the Thesis

At this point, a short overview of the following chapters shall be given.
First, an introduction into related topics and technology is given with focus on effects and characteristics which are relevant for this work.
Subsequently, an optimized commutation circuit is presented. Further, its principle of operation to manage the energy in the stray inductance is described and a mathematical model for the turn-on and turn-off event is derived.
Then, the power modules used for measurements are introduced, two module variants serving as reference types and the module with the introduced optimized commutation circuit. Afterwards, the mathematical models are compared with measurements, and significant effects are discussed. Subsequently, the derived mathematical model is used to predict the circuit behavior during different types of operation.
The next chapter compares the characteristics of two reference module variants with the optimized type. The switching behavior is compared at different operation points and the achievable output power during inverter operation is estimated by calculation.

The next to last chapter shows the operation of a LC-filter actively driven by the optimized circuit to present a substitute for conventional IGBT inverters where, due to a switching speed constraint, WBM semiconductors may not be reasonable. Therefore, a comparison with a state-of-the-art IGBT module is given.
Finally, a summary of the work and it's important findings is given and an outlook shall point out future research directions.

2 Basics and Technology Review

2.1 Power Semiconductor Devices

For a better understanding of the effects observed in this work, a basic introduction in common power semiconductors, the materials and their properties is given below. First, semiconductor materials with their characteristics which are important for power applications are outlined with special focus on the advantages of WBM compared to Si. Afterwards, characteristics of bipolar diodes as well as MOSFETs are described. In particular, attention was paid on device related effects which might have a strong influence in the circuit presented in this work and which should be considered for proper dimensioning.

2.1.1 A Short Introduction to Semiconductor Materials

In power electronics, Si is still the most common material. Its characteristics are well-known and as a result the technology is well established. However, silicon shows some limitations, cf. Tab. 2.1, effecting the achievable performance of the semiconductor device. To overcome these limitations, WBM are an interesting and emerging solution. In the recent years, silicon carbide in 4H configuration (4H-SiC) and GaN have gained popularity and are the most suitable wide-bandgap materials in terms of technological maturity. Nevertheless, both materials are still facing problems in material quality [3, 28]. However, SiC has the highest level of development for vertical devices allowing higher breakdown voltages, see [5], which makes it the preferred material for higher power devices.
In Table 2.1 some important material properties of the mentioned semiconductors are listed. However, it should be mentioned that the material parameters strongly variate for WBM in the literature which might be explained by variances in the quality of the investigated material.

Table 2.1: Semiconductor properties at 300K

	Si	4H-SiC	GaN
W_G [eV]	1.12^D	3.25^D	3.44^C
E_crit *[V/cm]	$200\mathrm{k}^\mathrm{A}$,$300\mathrm{k}^\mathrm{C}$	$2\ \mathrm{M}^\mathrm{A}$, $3.18\ \mathrm{M}^\mathrm{C}$	$3\mathrm{M}\text{-}3.5\mathrm{M}^\mathrm{C}$
v_sat [cm/s]	$1.05 \cdot 10^{7\,\mathrm{A}}$	$2 \cdot 10^{7\,\mathrm{A}}$	$2.5 \cdot 10^{7\,\mathrm{A}}$
μ_n [cm^2/Vs]	1400^C	500^B, 1000^A	900^C, 2000^B
μ_p [cm^2/Vs]	470^A	50^B, 115^A	10^C
ε_r [1]	11.8^B	9.8^B	7.8^B
CTE [$1 \cdot 10^{-6}$ °C]	2.59^A	4.3^A	$5.4\text{-}7.2^\mathrm{C}$

* E_crit is a function of doping. Thus, it should be understood as an estimation.
References: A:[4], B:[28], C:[29], D: Appendix A.1

A higher bandgap between valence and conduction band makes the semiconductor more robust against thermal charge carrier generation and other extrinsic influences like an electric field. This results in a significantly lower intrinsic concentration of charge carriers

at a given temperature. According to [30] p.21ff, the intrinsic carrier concentration can be calculated with a known density-of-states in the conduction, N_C, and valence band, N_V, with

$$n_i = \sqrt{N_C N_V} e^{-\frac{W_G}{2k\vartheta}} \tag{2.1}$$

where k is the Boltzmann constant, W_G is the bandgap energy and ϑ is the absolute temperature. Figure 2.1 shows the intrinsic carrier concentration as a function of temperature for silicon and SiC with the density of states calculated in Appendix A.1.

In Fig. 2.1 it can be seen that with an exemplary chosen doping concentration of $1 \cdot 10^{15}\,\mathrm{cm}^{-3}$, see [4, 30], the intrinsic charge generation becomes significant for a silicon device at temperatures above 300 °C. In comparison, SiC allows higher temperatures and thus, - due to a higher temperature gradient - a higher heat dissipation and power density. However, a possible limitation might be the robustness against high temperatures of the used packaging materials.

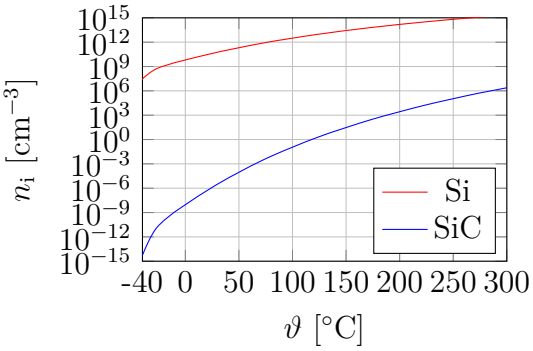


Figure 2.1: Intrinsic carrier concentration

2.1.2 Introduction to Diodes

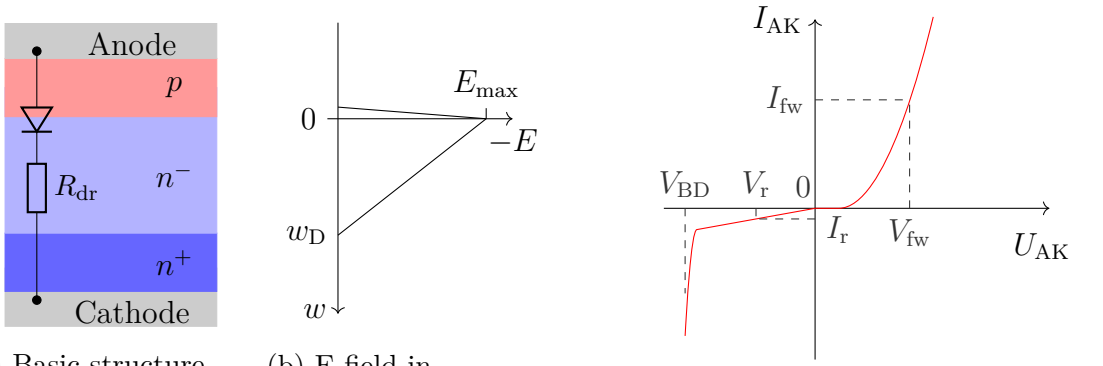
By combining a P and N doped semiconductor an abrupt PN junction is formed. The concentration of donor and acceptor atoms, N_D and N_A, which are for silicon usually ionized at room temperature [30], leads to a diffusion current and a charge displacement. This results in an electric field which drives a current in the opposite direction. For a P-N junction without external current and field, the diffusion and field driven current cancel each other out, so that a diffusion voltage can be calculated along the P-N junction width. By using n_i the diffusion potential for an abrupt P-N junction can be calculated according to [30] p.81 with

$$V_{diff} \approx \frac{k\vartheta}{q} \ln\left(\frac{N_D N_A}{n_i^2}\right). \tag{2.2}$$

For the exemplary chosen doping concentrations $N_D = N_A = 1 \cdot 10^{15}\,\mathrm{cm}^{-3}$ the diffusion voltage at 300 K can be calculated for a Si and SiC junction to $V_{diff,Si} = 0.6\,\mathrm{V}$ and $V_{diff,SiC} = 2.5\,\mathrm{V}$. Hence, the conduction losses can be expected to be much higher with SiC. Furthermore, bipolar structures like diodes made from silicon carbide suffer from severe aging mechanisms such as bar-shaped stacking faults [31]. Thus, SiC bipolar diodes - and SiC-MOSFET body diodes - are not a reasonable choice for free-wheeling operation yet.

Compared to normal diodes, PIN-diodes have an intrinsic region between the P and N doped sides. Because a PIN-diode as a substructure of a MOSFET, its characteristics are explained in this chapter. The intrinsic n^- zone, cf. Fig. 2.2a, increases the blocking capability compared to a simple P-N junction. The characteristic is given in Figure 2.2c. At a defined forward current I_{fw}, a forward voltage drop V_{fw} from anode to cathode can be

measured. At reverse voltage operation the reverse blocking current I_r flows from cathode to anode. For high reverse voltages the devices breaks down at a voltage of V_{BD}.



(a) Basic structure of a PIN-diode

(b) E-field in blocking state

(c) Characteristic (different negative and positive scales)

Figure 2.2: PIN Diode

Blocking state

By applying a reverse voltage to the diode, an electric field is formed similar to Fig. 2.2b. Due to the lower carrier density the n^- zone the field strength decreases slower. Hence, in case the field does not enter the n^+ zone, the width of the intrinsic zone w_B, determines the blocking capability of the diode. According to [30], the width as a function of the applied voltage V_{AK} can be calculated with

$$w_D = \sqrt{\frac{2\varepsilon_s}{qN_D}\left(V_{diff} - V_{AK} - \frac{2k\vartheta}{q}\right)}, \tag{2.3}$$

while N_D is the donor concentration in the n^- region, q the unit charge and ε_s is the semiconductor permittivity, see also Table 2.1. Additionally, the depletion layer capacitance per area can be written as

$$C_D = \frac{\varepsilon_s}{w_D} = \sqrt{\frac{q\varepsilon_s N_D}{2\left(V_{diff} - V_{AK} - \frac{2k\vartheta}{q}\right)}}. \tag{2.4}$$

Conduction and reverse recovery

As explained by [4] p.39, the forward voltage at the PN junction at a current density of $10\,A/cm^2$, which is comparatively low, is similar to the diffusion voltage V_{diff}. Thus, considering the voltage drop over the drift region resistance, which is a function of the charge carrier concentrations μ_n and μ_p, cf. Fig. 2.2a R_{dr}, the forward voltage V_{fw} can be estimated with

$$V_{fw} \approx V_{diff} + R_{dr}(\mu_n, \mu_p) I_{fw}. \tag{2.5}$$

During forward bias operation, the intrinsic region is swamped with charge carriers, Fig. 2.3 t_0. By applying a negative voltage on the flooded PN junction, these carriers are extracted during the interval $t_0 < t < t_3$. First, for $t \leq t_1$, the carrier concentration at the

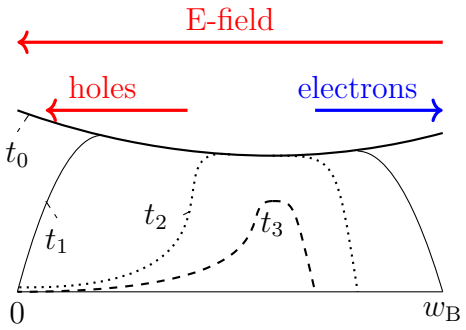


Figure 2.3: Carrier distribution in the drift region after [32] for a strong reverse current

corners (0 and w_B) drops to the state of thermal equilibrium. Later, from $t_1 < t \leq t_3$ the space-charge zone widens and the device voltage decrease to higher negative values. The extraction current can be measured as a reverse current as will be described in Section 3.4 and may cause significant losses.
As already mentioned, the PIN-structure is included in a MOSFET structure, cf. Fig. 2.2a with Fig. 2.5a. It is important to notice that at commercial free wheeling Si-PIN diodes it is common to modify the charge carrier life time to achieve an improved conduction behavior as well as a tail current during reverse recovery and thus a clean switching event with low voltage overshoot [33–35]. However, it is well known that the MOSFET intrinsic diode is not optimal. Thus, if the body diode is used as a free wheeling diode - as it is done in this work - the reverse recovery behavior might reduce the achievable device performance.

Forward recovery behavior
By applying a high current slope in conduction direction of a diode, the device might show a forward voltage V_{fr} [36–38]. This effect, depicted in Fig. 2.9, has a very similar influence as a stray inductance and might limit the achievable switching speed. A worst-case estimation is given by [4], with the assumption of an infinite current slope and a device without swamped base, the maximum voltage can be calculated as

$$V_{frm} = \frac{w_B \cdot j}{q\mu_n N_D} \tag{2.6}$$

while μ_n is the carrier mobility in the n^- region and j the current density. It should be mentioned that this effect has been evaluated for the used SiC-MOSFETs with the result of a negligible forward recovery voltage.

2.1.3 Introduction to MOSFETs

The MOSFET is the most important switching device in electronics. It is capable of operating at highest switching frequencies compared to other power semiconductors. However, silicon devices are only available for comparatively low voltages and current levels which is related to the dependence of the on-state resistance R_{on} to the breakdown voltage, cf. Fig. 2.4. Considering that the drift region has a significant fraction, of the total on-state

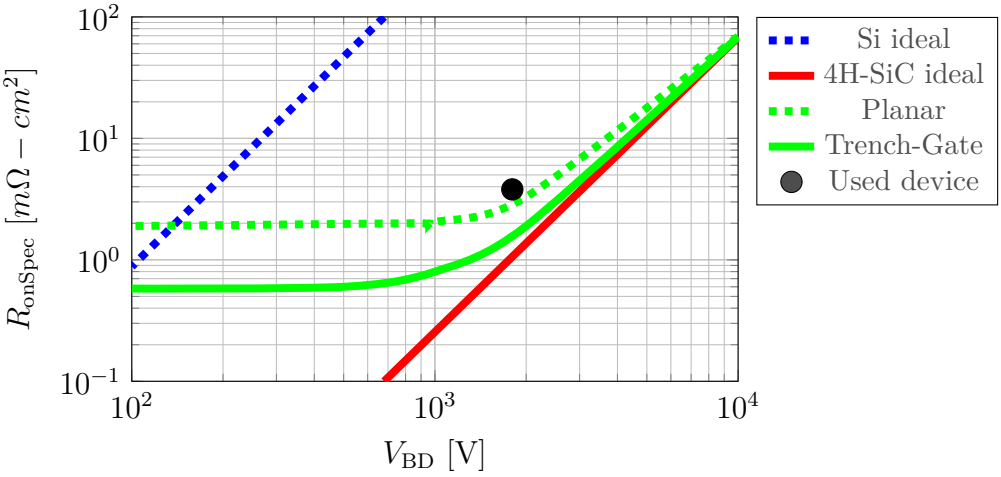


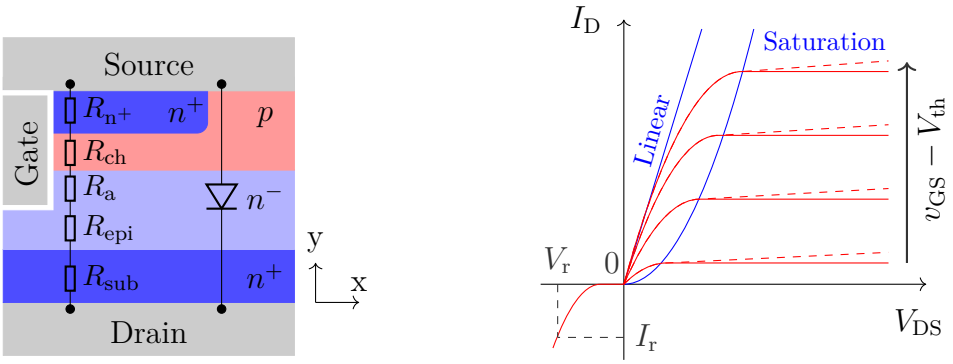
Figure 2.4: Ideal specific on-state resistance over breakdown voltage after [39]

resistance, a rough estimation on the dependence of the implemented breakdown voltage can be found in [39] p. 15 with

$$R_{\mathrm{on-ideal}} = \frac{4V_{\mathrm{BD}}^2}{\varepsilon_{\mathrm{s}}\mu_{\mathrm{n}}E_{\mathrm{crit}}^3}. \tag{2.7}$$

Here, the semiconductor properties are considered by ε_{S} as the semiconductor dielectric constant, μ_{n} as the electron mobility and E_{crit} as the critical electric field. Due to the cubic dependence on the critical electric field, this equation indicates the strong benefits of wide-bandgap materials which is illustrated in Fig. 2.4.
Since the availability of wide-bandgap materials the MOSFET is reasonable for applications at voltages above 1 kV. The first SiC-MOSFET with a rated break down voltage of 1 kV was commercially introduced by Cree [18] in 2011. For power electronics, higher blocking and current-carrying capability can be achieved with a vertical trench gate structure as depicted in Fig. 2.5a compared to a planar structure. It can be seen that the right-hand-side arrangement of the device equates to a PIN-diode structure. This body diode results in a reverse conductive capability which is considered with the negative quadrant of the characteristic in Fig. 2.5b. However, a body diode has some significant disadvantages compared to a dedicated anti-parallel diode in both dynamic and static behavior, cf. [40]. Additionally, for SiC-MOSFETs, as mentioned above, the bipolar structure suffers from significant aging mechanisms like bar-shaped stacking faults [31, 41, 42]. Therefore, it is not reasonable to use the body diode as a free wheeling diode as it is done with paralleled IGBT-diode combination.

Further, it has been found that the breakdown voltage of the structure shown in Fig. 2.5a is limited by the high electric field strength at the bottom side of the gate trench. According to [43] p. 496, this limitation can be overcome by implementing a shielding plate at the trench bottom. Further, the drift region has still a major contribution to the total specific on-resistance, cf. [44] p. 501. By applying a positive voltage V_{GS} from Gate to Source, the conductivity of the p-region near the Gate can be modulated. A positive voltage increases the electron concentration and decreases the hole concentration in this region and for a voltage higher than a specific threshold voltage V_{th} a conductive channel can be achieved.



(a) Basic MOSFET structure

(b) Characteristic with
solid: long channel, dashed: short channel

Figure 2.5: Vertical trench MOSFET

Channel modulation through Gate voltage

As described in [30] in detail, with the condition that the electric field strength in x-direction, cf. 2.5a, is much larger compared to the field in y-direction, and the assumption of a constant mobility the current-voltage-characteristic can be estimated as follows.

$v_{DS} \ll (v_{GS} - V_{th})$**:** For a very low v_{DS} and a gate voltage above the threshold voltage, the charge distribution in the channel near the gate is nearly homogeneous. Thus, the channel operates in the linear region, cf. Fig. 2.5b, and behaves like a resistor R_{ch} which is a function of the gate voltage

$$R_{ch} = \frac{l_{ch}}{w_{ch}\mu_n C_{ox}(v_{GS} - V_{th} - v_{DS}/2)}. \tag{2.8}$$

Here, the channel length and width are l_{ch} and w_{ch} respectively and the capacitance between gate and semiconductor is C_{ox}. From (2.8) the drain current can be estimated with

$$i_D = \frac{w_{ch}}{l_{ch}}\mu_n C_{ox}(v_{GS} - V_{th} - v_{DS}/2)v_{DS}. \tag{2.9}$$

$v_{DS} \approx (v_{GS} - V_{th})$**:** If the drain voltage is in the range of $(v_{GS} - V_{th})$, the charge becomes reduced at the drain end. Therefore, the behavior becomes non-linear.

$v_{DS} \gg (v_{GS} - V_{th})$**:** For high drain-source voltages, the electric field along the channel accelerates the electrons towards the drain with saturation velocity v_{sat}. Due to the higher saturation velocity of wide-bandgap materials like SiC and GaN compared to Si, cf. Tab. 2.1, such devices show a higher saturation current at equal gate voltages. By reaching v_{sat} the drain current becomes independent of the drain-source voltage, cf. Fig. 2.5b solid line. According to [30], the saturation current can be calculated with

$$I_{Dsat} = \frac{w_{ch}}{2l_{ch}M}\mu_n C_{ox}(V_{GS} - V_{th})^2, \tag{2.10}$$

where M is a function of doping concentration and oxide thickness.

Short channel effects
The equations previously mentioned are valid for long channels where the field caused by the gate bias is much higher compared to the drain bias. With reduced channel length for reduced R_{ch}, the influence from the field in y-direction has to be considered. The field in the channel becomes two-dimensional which results in many undesirable forms of electric behavior [30]. In literature, this can be found as drain-induced-barrier-lowering (DIBL) [45–47]. One remarkable effect for this work is that the drain current does not saturate with drain bias. Thus, in saturation region the drain current is also a function of drain voltage which is exemplary illustrated by a dashed line in Figure 2.5b.

2.2 Parasitic Inductances in Power Electronics

The parasitic inductance in the commutation loop - or switching cell - is an important parameter in a hard switching power semiconductor application. With the usage of controllable semiconductors with significantly high $\mathrm{d}i/\mathrm{d}t$ and current density, the parasitic inductance become topic of research, see e.g. [48, 49]. In the commutation loop, the parasitic inductance leads to a voltage overshoot at turn-off, e.g. [50] and may contribute to high frequency oscillations with the output capacitance of the switching device [51]. Because the optimization of the stray inductance is a major topic in this work, a brief introduction shall be given in this section.

2.2.1 Basic Geometries and Their Characteristics

The inductance is the relation between the total magnetic flux Φ_{t} to the current I

$$L = \frac{\Phi_{\mathrm{t}}}{I}. \tag{2.11}$$

The magnetic flux is the integral of the magnetic flux density B over a surface A under the assumption of a scalar permeability μ to be calculated with

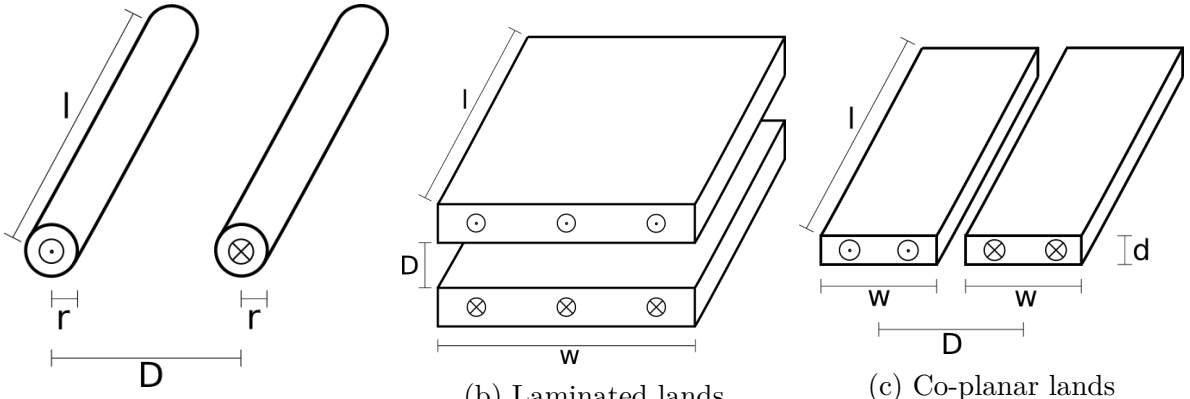
$$\Phi = \mu \int \boldsymbol{H} \mathrm{d}\boldsymbol{A}, \tag{2.12}$$

see [52]. Hence, the inductance is also a function of geometry and thus, this section shall give a brief overview of common geometries shown in Figure 2.6. Further, their appropriateness to minimize the stray inductance is outlined. The mathematical description of the inductance is a complex task which can be derived from the history of literature comparing Maxwell's "A Treatise on Electricity and Magnetism" [53] with Rayleigh's improvements [54] on the example of parallel cylinders, Fig. 2.6a, to the actual state of knowledge, see e.g. [55]. For parallel cylinders, the formula

$$L_{\mathrm{cyl}} = \frac{\mu_0}{2\pi} \ln\left(\frac{D}{2r} + \sqrt{\left(\frac{D}{2r}\right)^2 - 1}\right). \tag{2.13}$$

can be obtained. Here, D is the distance between the center of the two cylinders with the radius r and the length l.
Another common geometry is a conductor arrangement shown in Fig. 2.6b with laminated lands also referred to as bus bar. The equation for the inductance according to e.g. [56], as

$$L_{\mathrm{lam}} = \mu_0 l \frac{D}{w} \tag{2.14}$$



(a) Parallel cylinders (b) Laminated lands (c) Co-planar lands

Figure 2.6: Common conductor geometries

describes the relation as a fraction of the inner distance D of both conductors and their width w.

The final structure is a co-planar conductor arrangement according to Figure 2.6c with a mathematical description assuming $d = 0$ found in [57], as

$$L_{\text{coplan}} = \begin{cases} \frac{120l}{c_0} \ln\left(2\frac{1+\sqrt{k}}{1-\sqrt{k}}\right), & \frac{1}{\sqrt{2}} \leq k \leq 1 \\ \frac{120\pi^2 l}{c_0 \ln\left[2(1+\sqrt{k'})/(1-\sqrt{k'})\right]}, & 0 \leq k \leq \frac{1}{\sqrt{2}} \end{cases} . \tag{2.15}$$

Here, with the coefficients defined as

$$k = \frac{D}{D+2w} \quad \text{and} \quad k' = \sqrt{1-k^2}. \tag{2.16}$$

From Figure 2.6a and (2.13) it can be derived that the inductance can be minimized by increasing the radii or reducing the distance. Considering wire insulation, a higher voltage necessitates thicker insulation and is a limiting factor for minimizing the geometry inductance.
Similarly, minimizing the distance D in the co-planar arrangement is limited by the insulation material as well and therefore, by the target voltage in the application. Contrary to both previous setups, the laminated lands in Fig. 2.6b offer the opportunity in case of a limited D to increase the width w of the arrangement and therefore further minimization of the inductance L_{lam}.
Indeed, while the laminated lands are the best choice for low inductance applications, in practice the usability is often limited by further constraints like e.g. manufacturability or design requirements on interfaces between components.

However, it should be mentioned that the inductance as well as the resistance of a conductor arrangement is also a function of frequency caused by skin- and proximity effect [58–60]. A comprehensive study can be found in [61].

2.2.2 Consequences for Low- and High-Power Applications

In typical hard switching power semiconductor applications, minimizing the stray inductance between the DC-link capacitor and the semiconductor is a major design goal limiting

the voltage overshoot at turn-off and ringing amplitude and simultaneously enabling faster switching speeds, see e.g. [17, 62, 63]. Further, with the availability of semiconductors based on WBM, the efforts of investigation in minimizing the stray inductance has risen. Indeed, depending on the requirements for the application, minimizing the stray inductance to an affordable value might not be possible or reasonable in terms of effort.
Common approaches focus on making use of the structure shown in Fig. 2.6b with novel assembly technologies like chip-embedding, see e.g. [64], which allows very low stray inductances. Other common approaches are using foils as interconnection material [65], further optimize established interconnection technology [60] or using ceramic capacitors close to the switching semiconductor.
Several options to deal with the stray inductance have been evaluated in the literature. In [66] the product of stray inductance L_σ and nominal current I_{nom} as the magnetic flux Φ_{t}, cf. 2.11 is mentioned as a rating parameter. The Φ_{t} of several setups found in the literature have been analyzed and clustered in three current classes. Table 2.2 shows the range of found $L_\sigma \cdot I_{\mathrm{nom}}$ products for the total setup including DC-link capacitor or only for the package from the semiconductor to the power module connection. With presupposed similar rise and fall times and with the known relation

$$v \propto \frac{\mathrm{d}\Phi_{\mathrm{t}}}{\mathrm{d}t}, \tag{2.17}$$

Table 2.2: Application current class analysis of $L_\sigma \cdot I_{\mathrm{nom}}$

Current class	$L_\sigma \cdot I_{\mathrm{nom}}$ Package	$L_\sigma \cdot I_{\mathrm{nom}}$ Total setup	**References**
$<= 50\,\mathrm{A}$	$< 0.007\,\mu\mathrm{Vs} - 0.08\,\mu\mathrm{Vs}$	$< 0.007\,\mu\mathrm{Vs} - 0.22\,\mu\mathrm{Vs}$	[64, 67, 68]
$<= 500\,\mathrm{A}$	$0.4\,\mu\mathrm{Vs} - 2.8\,\mu\mathrm{Vs}$	$< 1.3\,\mu\mathrm{Vs} - > 9\,\mu\mathrm{Vs}$	[69–73]
$> 500\,\mathrm{A}$	$0.84\,\mu\mathrm{Vs} - 10.2\,\mu\mathrm{Vs}$	$< 5.4\,\mu\mathrm{Vs} - > 111\,\mu\mathrm{Vs}$	[65] [17, 50, 62]

Table 2.2 indicates that setups for higher current rating have to deal with higher turn-off overvoltage. Thus, the switching speed must be decreased or devices with higher breakdown voltage and higher specific on-resistance have to be used. Both leads to higher losses with increasing nominal current. Therefore, fast switching WBM semiconductors cannot be utilized as optimal as in lower current applications. An alternative option compared to a conventional DC-link setup as in above analyzed setups is the use of snubber capacitors which are further discussed in Section 2.4.

2.3 Hard and Soft Switching

Outgoing from non-ideal semiconductor devices described in the Sections 2.1.2 and 2.1.3, the turn-on and turn-off switching event is explained by a simplified commutation circuit as depicted in Figure 2.7. This circuit represents a very common power semiconductor configuration on which most dynamic effects relevant in this work can be described schematically. Because the parasitic elements have a significant impact on the switching

performance and behavior especially at very fast switching speeds, this influence is described for turn-on and turn-off in the following chapters.
Following assumptions shall be made for the description:

- The inductance in the gate circuit is small and thus, it is neglected
- The driver has an infinite voltage slope and zero impedance
- The load current I_{Load} and the voltage source V_{DC} are time invariant
- Magnetic couplings are neglected
- All oscillations caused by previous switching events have been damped

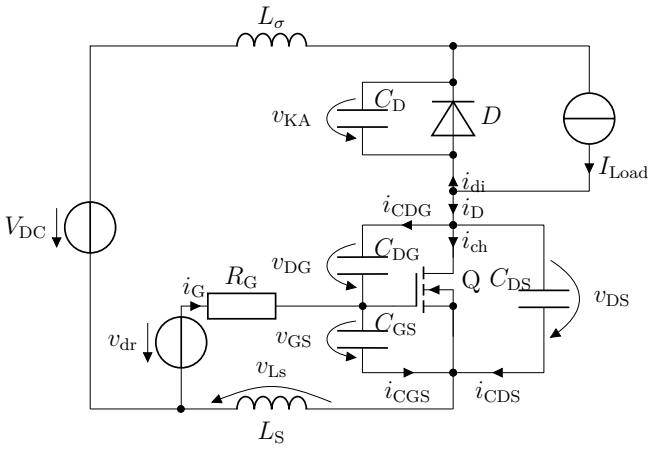


Figure 2.7: Basic commutation circuit

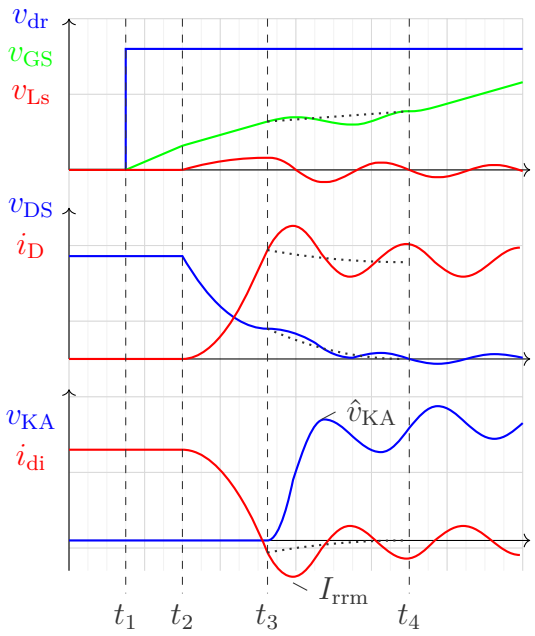


Figure 2.8: Turn-on event

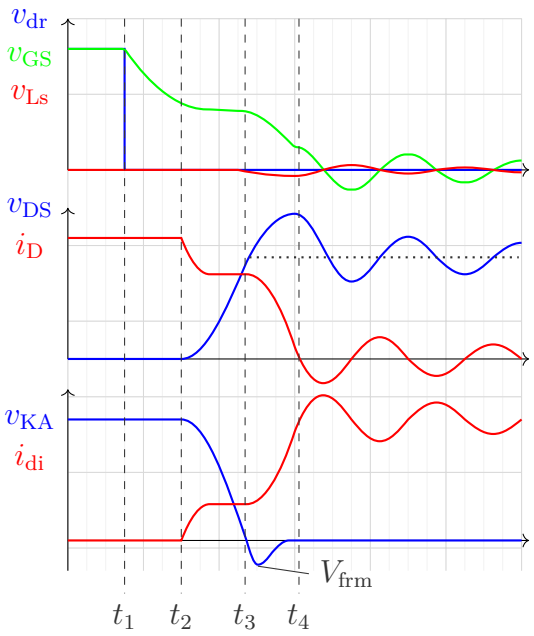


Figure 2.9: Turn-off event

2.3.1 Description of the Turn-On Event

The turn-on event is described with reference to Figure 2.8.

$t < t_1$: Before the switching event, the driver output voltage v_{dr} is low and thus, the MOSFET Q is in blocking state. Therefore, the load current I_{Load} is flowing through the diode D. Hence, the PN junction is flooded with charge carriers and the voltage from anode to cathode v_{KA} equates to the negative forward voltage V_{fw}, see (2.5).

$t_1 < t < t_2$: At t_1 the driver voltage v_{dr} rises to high value. The resulting gate charge current i_{G} is limited by the gate resistor R_{G} and charges the input capacitance

$$C_{\mathrm{iss}} = C_{\mathrm{GS}} + C_{\mathrm{DG}}. \tag{2.18}$$

Because the MOSFET channel is not controlled yet, the drain-source voltage v_{DS} remains nearly constant. Therefore, the drain-gate capacitance displacement current i_{CDG} is negligible. As a result, the gate voltage v_{GS} increases as an exponential function with negative exponent.

$t_2 < t < t_3$: At the beginning, the gate voltage reaches the MOSFET's threshold voltage V_{th}. The MOSFET channel starts opening and the drain-source current i_{D} increases. The changing current causes a voltage drop over L_σ and hence, C_{DS} discharges. Additionally, the displacement current i_{CDG} cannot be neglected. i_{CDG} is superimposed to i_{G} and leads to a negative feedback which reduces the gate discharge and thus, the switching speed. Another negative feedback is caused by the parasitic inductance L_{S} shared by the gate and power path. The induced voltage $v_{\mathrm{Ls}} \approx L_{\mathrm{S}} \frac{di_{\mathrm{D}}}{dt}$ results effectively in a reduced driver voltage $v_{\mathrm{dr}} - v_{\mathrm{Ls}}$. As mentioned in Sect. 4.1.2, this effect is used to improve dynamic current sharing for paralleled MOSFET dies. For $v_{\mathrm{DS}} \gg v_{\mathrm{GS}}$ the MOSFET operates in the saturation region, cf. Fig. 2.5b. After i_{D} is equal to I_{load}, the diode current becomes negative and the charge carriers start recovering.
Hard switching: In case of a very small stray inductance L_σ, the v_{DS} voltage drop may become negligible. This results in high power dissipation $P_{\mathrm{loss}} = v_{\mathrm{DS}} \cdot i_{\mathrm{D}}$ and is defined as a hard switching event.
Quasi soft switching: For very fast switching events, e.g. in case the gate resistor is very small, the gate driver is able to counteract the displacement current through C_{DG}. Thus, the MOSFET channel is opened very fast. The voltage drop across L_σ may increase to V_{DC} level in this interval already at low drain current values. As a result, the current gradient is no more controlled by the MOSFET but only by the stray inductance and the DC-link voltage. This results in a significant reduction of P_{loss} and a softer switching event with higher efficiency, see [74].

$t_3 < t < t_4$: For $t = t_3$, i_{di} crosses zero. Subsequently, the PN junction depletes and the diode voltage v_{KA} increases. After the maximum reverse current I_{rrm} occurred, the voltage over L_σ changes rapidly and leads to a maximum diode voltage $\hat{v}_{\mathrm{KA}}$. Without an adequate tail-current shape, this triggers an oscillation between L_σ and the PN junction capacitance C_{D}. Furthermore, C_{DS} and C_{DG} have been partially discharged in the previous interval as a result of the voltage drop over L_σ. The remaining voltage v_{DS} discharges until t_4. Similarly to the previous interval, the

gate current i_G is superimposed by the displacement current i_{CDG}. Therefore, the gate capacitance is charged much slower and hence, this reduces the voltage slope. Depending on the diode softness, this interval can be very short, which can lead to much higher voltage slopes and higher $\hat{v}_{KA}$.

$t > t_4$: After the diode has taken the voltage and the MOSFET channel is opened, energy remains in the commutation circuit in terms of a current through L_σ and a charge in C_D. This energy oscillates and is damped by parasitic resistances or is radiated and may cause electromagnetic interference.
The gate voltage has reached a level at which the influence on the channel is very small. The MOSFET operates at linear region. Thus, for low gradient oscillations the negative feedback might be neglected. The gate capacitance charges up to the high level of the driver voltage.

2.3.2 Description of the Turn-Off Event

The turn-off event is described with reference to Figure 2.9.

$t < t_1$: For a time $t < t_1$, the gate and driver voltage v_{GS} and v_{dr} are at high level. Therefore, the MOSFET channel is opened and thus, the load current I_{Load} equals to i_{ch}. Furthermore, the diode voltage v_{KA} is equal to the DC-link voltage and the capacitance C_D is charged.

$t_1 < t < t_2$: At t_1 the driver voltage v_{dr} decreases to low value. The gate capacitor C_{GS} discharges through the gate resistor R_G. The MOSFET operates in linear region until $t = t_2$.

$t_2 < t < t_3$: In this interval, the MOSFET enters the non-linear region, cf. Fig. 2.5b. Therefore, the channel is modulated by the gate voltage. The voltage v_{DS} increases and the output capacitance

$$C_{oss} = C_{DS} + C_{DG} \tag{2.19}$$

is charged.
Similar to the turn-on event, the drain-source voltage slope causes a displacement current i_{CDG}, which superimposes the gate current. Hence, the discharge process of the gate capacitance slows down and the gate voltage slope flattens. The positive voltage slope leads to a displacement current in the diode capacitance according to $C_{oss}\frac{dv_{DS}}{dt}$. Due to the relation $I_{Load} = i_{di} + i_D$, the drain current is reduced.
Hard switching: Usually, the parasitic capacitances C_D and C_{oss} are small and as mentioned previously, the desirable voltage slope might be limited by the application. In this case, the displacement current may be very small and i_D remains nearly constant in this interval. Hence, the power dissipation is high, which causes a defined hard switching event.
Quasi soft switching: In case the application allows a high voltage gradient, the switching speed can be increased. Assuming a rapidly closed MOSFET channel, i_{ch} decreases to zero before I_{Load} has charged C_{oss} to a significant voltage. Hence, the dissipated losses in the MOSFET channel became small and the switching event becomes soft. However, it is important to mention that this cannot be measured because the measurable drain current always include the displacement current through

C_{oss}. Further, it is important to mention that for a closed channel, I_{Load} charges C_{oss} and simultaneously discharges C_D. Hence, the C_{oss} displacement current is a fraction of I_{Load} depending on the voltage dependency of C_{oss} and its state of charge.

$t_3 < t < t_4$: After C_D is discharged, the current commutates into the diode junction. As described in Section 2.1.2, the device might need time to take the current. Therefore, a voltage peak V_{frm} might be measured between the anode and cathode.
In case the gate resistor is comparatively high and the displacement current through C_{oss} at $t = t_3$ is negligible, the channel current is still significant. Because v_{DG} gets in the range of V_{DC} and due to the voltage dependency of C_{DG}, its negative feedback weakens and the displacement current i_{CDG} reduces. Therefore, the driver further discharges the gate capacitance, which closes the channel until v_{GS} equals V_{th}. The closing channel leads to a negative current gradient of i_D, that causes a positive voltage at the stray inductance $L_\sigma + L_S$. This voltage adds to the DC-link voltage and charges C_{oss}.

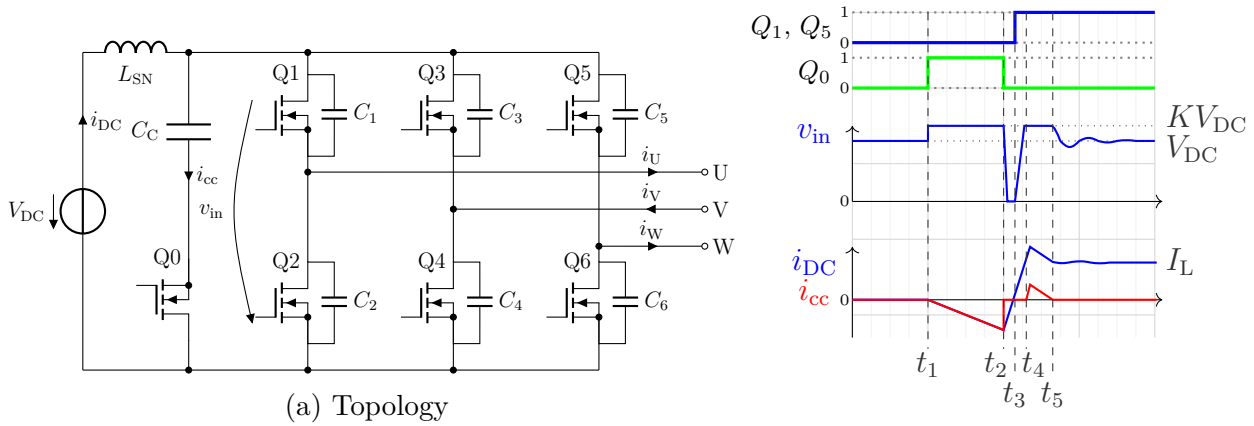
$t > t_4$: At $t = t_4$, the gate voltage reaches the threshold voltage. Thus, the MOSFET channel is closed. The energy remaining in C_{oss} leads to an oscillation with $L_\sigma + L_S$. Similarly to the turn-on event, this energy oscillates and is damped by parasitic resistances or is radiated and may cause EMI.
Because the driver voltage is lower than v_{GS}, the gate capacitance further discharges. Due to the voltage feedback characteristic of C_{DG}, the oscillation couples to the gate voltage, which must be controlled by the driver to avoid an unstable behavior at which the channel might be turned on again.

2.3.3 Resonant Switching

As described in the previous sections, for fast switching the parasitics in the commutation circuit are able to reduce the switching losses. A large stray inductance at turn-on leads to a voltage drop at turn-on, and a large capacitance leads to a current drop at turn-off so that the switching losses are lower than for a hard switching event.
Goal of resonant switching is a soft switching transition at zero or low current or voltage respectively. All concepts share the approach of ensuring a zero voltage or zero current switching by an external condition e.g. designing a circuit with resonance and switching synchronously to the zero crossings. A classification and an overview is given in [75], where topologies are differentiated into load resonant, link resonant, quasi and transition resonant.
Due to the variety of concepts and the circuit similarity to this work, only the notch commutated 3 phases PWM zero voltage switching (ZVS) inverter is described below to allow the reader a better differentiation.

Notch commutated 3 phases ZVS inverter
This concept depicted in Fig. 2.10a has been introduced by [76]. The circuit consist of the DC-link voltage source V_{DC}, a dedicated snubber inductor L_{SN}, the storage-voltage clamp capacitor C_C, the auxiliary notch-switch Q_0 and the three-halfbridge setup Q_1-Q_6. For all switches the internal body diode is not depicted separately. The switch capacitors C_1 to C_6 were assumed to be parasitic or small discrete devices. Similarly to the description in Section 2.3.2, it was considered that the turn-off becomes soft since the switch capacitor

provides zero voltage. Because the capacitor has a negative effect on the turn-on losses, cf. Section 2.3.1, a notch is introduced at this particular moment by the auxiliary circuit. This prevents dissipation of capacitor energy in the main inverter switches Q_1 to Q_6.



(a) Topology

(b) Timing diagram

Figure 2.10: Notch commutated 3-phase PWM ZVS inverter

In Figure 2.10b, the diagram is shown. In the upside diagram the gating signals of Q_0, Q_1 and Q_5 are depicted. Q_3 is not shown due to the reason that the current direction of i_V leads to a commutation into the body diode. Therefore, the channel is not controlled. The voltage at the three phase inverter state v_{in} and the currents i_{DC} and i_{cc} are shown in the coordinate system in Fig. 2.10b.

$t < t_1$: For describing the principle of operation, the initial state is assumed to be as follows. The main switches Q_1, Q_3 and Q_5 are in blocking state. Hence, the corresponding capacitors C_1, C_3 and C_5 are charged to v_{in}. With the direction of currents given in Fig. 2.10a this means that the current i_U is flowing through the body diode of Q_2 and i_W is flowing through the body diode of Q_6 similarly. The current i_V is flowing through the channel of the turned on Q_4.
Furthermore, it is assumed that the energy in L_{SN} from previous events has been transferred to C_C so a voltage higher than V_{DC} can be measured at the capacitor. The notch switch Q_0 is in blocking state.

$t_1 \leq t < t_2$: At $t = t_1$, the notch switch is activated. The Voltage v_{in} increases to the higher voltage of C_C, which is KV_{DC} with $K > 1$. This leads to a voltage over L_{SN}, which results in a negative current slope of the DC-link current i_{DC}.

$t_2 \leq t < t_3$: After reaching t_2, the notch switch is turned-off. Hence, the current through the DC bus snubber inductor L_{SN} - flowing in opposite i_{DC} direction - is forced to flow over the 3 phase inverter. The still charged capacitors C_1, C_3 and C_5 are discharged and the current is flowing through the body diodes of the main switches Q_1 to Q_6. This results in a voltage notch with $v_{in} = 0$. Because the DC-link voltage V_{DC} is applied to L_{SN}, the DC current starts increasing linearly.

$t_3 \leq t < t_4$: For $t = t_3$, the previously negative DC-link current becomes zero and further increases. At this point the main switches Q_1 and Q_5 are turned on. The increasing i_{DC} charges the capacitors C_2, C_3 and C_6.

$t_4 \leq t < t_5$: i_{DC} reaches the level of the inverter input current I_{L}. The remaining energy in L_{SN} commutates into the clamp capacitor and thus, the inverter input voltage v_{in} is clamped to the clamp capacitor voltage KV_{DC}.

$t > t_5$: The DC bus snubber inductor oscillates with the effective capacitance of the inverter which is the sum of C_2, C_3 and C_6.

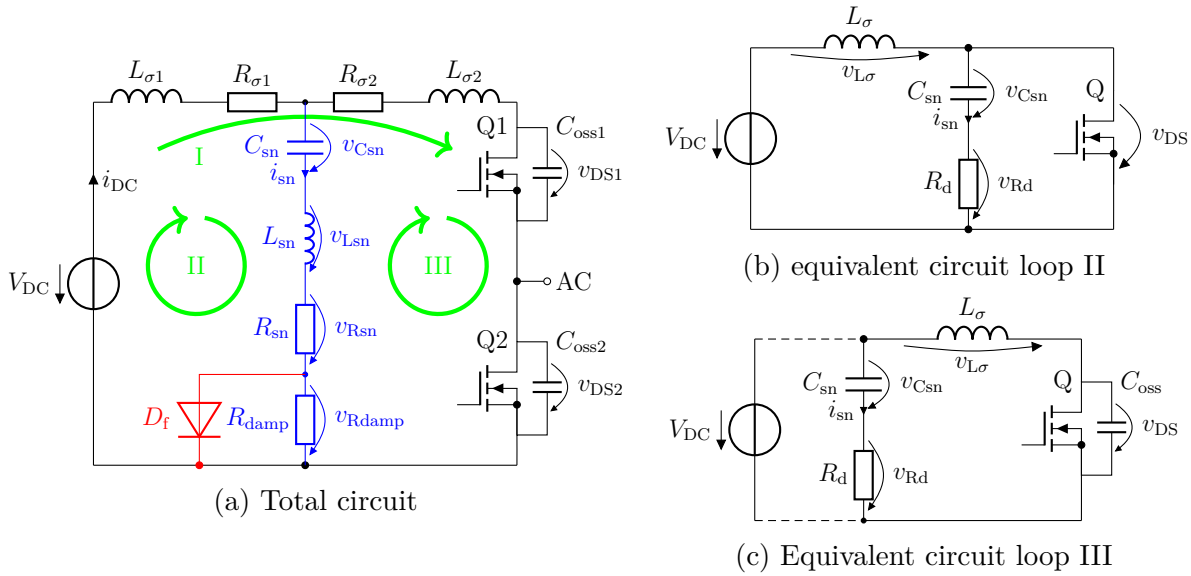
In the mentioned publication [76], the circuit is described with a dedicated large inductor L_{SN} of a few micro Henry which is disadvantageous in terms of conduction losses or achievable power density.

2.4 Introduction to Snubbers

Snubber circuits are common in power electronics since decades, see e.g. [77]. In General a snubber is a device which is capable of damping oscillations or reducing the stress on the switching device, see [78–80]. Optimize the design and analyze the influence of the snubber circuit on the switching event was targeted in various publications, e.g. [81–85]. Several approaches have been analyzed like a dedicated damping resistor magnetically coupled to the stray inductance [86]. However, the effectiveness for this approach strongly depends on the magnetic coupling. Even a MOSFET with intrinsic snubber has been considered [87]. Since the availability of wide-bandgap semiconductors further research has been done to reduce the ringing behavior or to reduce the voltage overshoot at higher switching speeds, cf. [16, 88].
Because only capacitive snubbers are relevant in this work, inductive snubber concepts presented by e.g. [89, 90] are not described in the continuation.

2.4.1 DC-Snubber

A DC-snubber or decoupling capacitor is a small capacitor compared to the DC-link capacitor which is connected at the DC terminals closer and thus, with lower inductance, to the semiconductor. Therefore, the stray inductance $L_\sigma = L_{\sigma1} + L_{\sigma2}$ between the DC-link voltage source V_{DC} and the power semiconductor is divided into two subinductors, cf. Fig. 2.11a. Thus, multiple harmonic frequencies can be observed which may cause EMI, cf.[83, 91]. The resistors $R_{\sigma1}$ and $R_{\sigma2}$ represent the losses in the subcircuits and considering skin and proximity effect they are frequency dependent [61].
Basically, there are two approaches to design a DC-snubber. The first is to optimize the ringing behavior by optimized damping in the subcircuit while secondly the overvoltage reduction is goal of optimization.



(a) Total circuit

(b) equivalent circuit loop II

(c) Equivalent circuit loop III

Figure 2.11: DC-snubber equivalent circuits

The basic DC-snubber circuit for halfbridge application is depicted in Fig. 2.11a (blue). The Snubber capacitor is C_{sn}, while L_{sn} represents the inductive part consisting of the

capacitor ESL as well as the inductance of the snubber connection. R_{sn} is the resistive part of the capacitor as the equivalent series resistor (ESR) and the parasitic connection respectively. However, the inductive part may be reduced by effective magnetic coupling under dedicated circumstance, see [91, 92]. R_{damp} is a dedicated and optional damping resistor. To reduce the voltage drop v_{Rdamp} during commutation, an optional free-wheeling diode D_{f} (red) can be applied. The placement of the DC-snubber leads to three possible oscillation loops, cf. Fig. 2.11a (green). The first loop is the loop which is present without snubber. The second loop is formed by the DC-link and the snubber itself, while the third loop includes the snubber and the semiconductor capacitance.

Design for optimized oscillation damping
Depending on the oscillation loop chosen for optimization different equivalent circuits can be derived from Fig. 2.11a. To analyze the complex system a common approach is a reduction to a second order system, see [16, 88]. For deriving the equations it is assumed that one body diode of either $Q1$ or $Q2$ is in conduction state. Hence, the voltage at the diode is treated to be zero. Furthermore, it is assumed that L_σ represents the dominating parasitic inductance. Additionally C_{oss} is treated to be much smaller than C_{sn}.

In case the snubber shall be optimized for oscillation loop III, cf. Fig. 2.11c, the resonant angular frequency can be calculated with the assumptions previously made as derived in Chapter A.2

$$\omega_0 = \frac{1}{\sqrt{L_\sigma C_{\mathrm{oss}}}}. \tag{2.20}$$

An optimal damping can be achieved by selecting the damping resistor as

$$R_{\mathrm{d}} = 2\sqrt{\frac{L_\sigma}{C_{\mathrm{oss}}}}. \tag{2.21}$$

In [16] as well as [88] the snubber capacitor value is obtained by using the resonant angular frequency and the damping resistor as given above with

$$C_{\mathrm{sn}} = \frac{1}{\omega_0 R_{\mathrm{d}}}. \tag{2.22}$$

Additionally, in [16] an additional capacitor without damping resistor was connected in parallel to the DC-snubber. It has been found that the approach given above does not lead to optimal damping with this setup and the values of C_{sn} and R_{d} have been adjusted manually. As a reason it is assumed by the authors that the additional capacitor lead to interference which is not taken into account in the equations. Moreover, it has been found that the presence of the DC-snubber with resistor has no influence on the total switching losses.

Another approach for dimensioning the snubber assuming the equivalent circuit in Fig. 2.11b is adapted from [80]. With the baseline capacitance and baseline resistance

$$C_{\mathrm{base}} = L_\sigma \left(\frac{I_{init}}{V_{\mathrm{DC}}}\right)^2, \tag{2.23}$$

$$R_{\mathrm{base}} = \frac{V_{DC}}{I_{init}}, \tag{2.24}$$

where I_{init} is the initial DC-link current before switching, the maximum voltage of v_{DS} appearing at $t = t_{\text{m}}$ and can be calculated with

$$v_{\text{DSmax}} = v_{\text{DC}} \cdot \left[1 + e^{-\alpha t_{\text{m}}} \sqrt{1 + \frac{C_{\text{base}}}{C_{\text{sn}}} + \frac{R_{\text{d}}}{R_{\text{base}}} - 0.75 \left(\frac{R_{\text{d}}}{R_{\text{base}}} \right)^2} \right]. \tag{2.25}$$

Here, α and t_{m} can be calculated with the following set of equations

$$\omega_a = \sqrt{\omega_0^2 - \alpha^2}, \quad \alpha = \frac{R_{\text{d}}}{2L_\sigma} \tag{2.26}$$

$$\phi = \arctan\left(\frac{v_{\text{DC}} - I_{init} R_{\text{d}}/2}{\omega_a L_\sigma I_{init}} \right), \quad \gamma = \arctan \frac{\omega_a}{\alpha}, \quad t_{\text{m}} = \frac{\phi - \gamma - \pi/2}{\omega_a}. \tag{2.27}$$

According to [80], the maximum voltage becomes minimal in case $C_{\text{sn}} = C_{\text{base}}$ and $R_{\text{d}} = 1.3 \cdot R_{\text{base}}$. Due to the configuration as depicted in Fig. 2.11a the initial voltage of C_{sn} before the switching event is equal to the voltage in case all oscillations have been damped. With respect to the rule of energy conservation and neglecting semiconductor losses the losses damped in R_{d} can be estimated as given in [80] p.674 with

$$W_{\text{Rd}} = \frac{1}{2} L_\sigma I_{init}^2. \tag{2.28}$$

Design for overvoltage suppression

For an effective suppression of overvoltage during turn-off and diode recovery the parasitic inductance between the snubber and the halfbridge has to be very small. Thus, Fig. 2.11b is assumed as equivalent circuit. Because a load current flowing through L_σ, commutation into the snubber path would lead to a voltage drop over R_{d}, the resistor is treated to be a lumped resistor representing the parasitics in Fig. 2.11a.

The maximum capacitor voltage change $\Delta v_{\text{Csn,max}}$ in an LC circuit can be calculated by considering the energy stored in L_σ as well as the energy E_{DC} provided by the DC-voltage source V_{DC} and leads to

$$\Delta v_{\text{Csn,max}} = \sqrt{\frac{L_\sigma}{C_{\text{sn}}} I_{init}^2 + \frac{2W_{\text{DC}}}{C_{\text{sn}}}}. \tag{2.29}$$

Here, I_{init} is the initial current through L_σ. A low-resistive design with $R_{\text{d}}(f = 0\,\text{Hz}) \approx 0$ results in an initial snubber voltage $v_{\text{Csn0}} \approx V_{\text{DC}}$ and with (A.4)ff., the necessary capacitance with a given allowed voltage increase over the DC-link voltage $\kappa V_{\text{DC}} = V_{\text{DSmax}} - V_{\text{DC}}$ with a fraction of V_{DC} as $\kappa < 1$ can be calculated with

$$C_{\text{sn}} = L_\sigma \left(\frac{I_{init}}{\kappa V_{\text{DC}}} \right)^2. \tag{2.30}$$

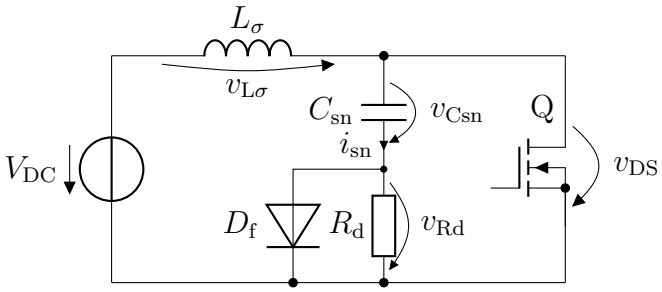


Figure 2.12: Turn-off snubber equivalent circuit

2.4.2 Turn-Off Snubber

A turn-off snubber is similar to the DC-snubber from the analytical point of view. However, the RC combination is directly connected to a power switch minimizing the stray inductance, see Fig. 2.12.
The diode D_{f} ensures a low impedance conduction path if the semiconductor turns-off. The energy in L_σ commutates into C_{sn} which keeps the voltage low. Thus, the turn-off event becomes soft as described in Section 2.3.2.
Due to the direct connection the capacitor is totally charged up to V_{DC} after turn-off. Considering that the turn-on time is much less than the snubber time constant $C_{\mathrm{sn}} \cdot R_{\mathrm{d}}$, the energy stored in C_{sn} is dissipated in the resistor at each turn-on event. Thus, according to [93] (2.28) has to be extended to

$$W_{\mathrm{Rd}} = \frac{1}{2} L_\sigma I_{init}^2 + \frac{1}{2} C_{\mathrm{sn}} V_{DC}^2 \tag{2.31}$$

Hence, the capacitance chosen for a turn-off snubber shall be as small as possible to keep the losses in an acceptable range.

2.4.3 Power Loss Estimation

Similarly to the previous chapters, the worst case damping losses for a DC-snubber setup can be estimated with (2.28) and for a turn-off snubber with (2.31). With an oscillation triggered at every switching event, the mean damping losses are a function of switching frequency f_{sw}, the current I_{init} and L_σ and C_{sn} respectively. This leads to

$$P_{\mathrm{damp}} = W_{\mathrm{Rd}} f_{\mathrm{sw}}, \tag{2.32}$$

as a worst case assumption, while the energy W_{Rd} is damped on both turn-on and turn-off event.
An important factor that can lead to deviations in practical setups are the series elements in the snubber path, cf. Fig. 2.11a L_{sn}, R_{sn} and without D_{f} also R_{damp}. In case these elements are significantly large, they cause an increased semiconductor voltage during the turn-off. As a result, the effectiveness of overvoltage reduction is lower and the energy from (2.28) is now partially dissipated in the semiconductor.
As an example application with a stray inductance of $L_\sigma = 20\,\mathrm{nH}$ the worst case losses for a DC-snubber setup are depicted in Fig. 2.13. It can be noticed that the losses are

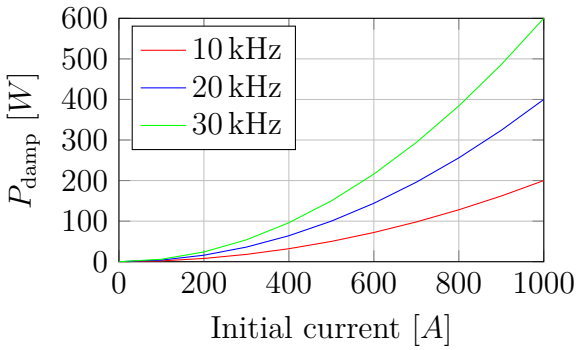


Figure 2.13: Exemplary DC-snubber worst case losses

significant for applications operating at higher current level.
However, in practical setups the parasitic resistors $R_{\sigma 1}$ and $R_{\sigma 2}$, cf. Fig. 2.11a show a significant damping contribution. Thus, the losses shown in Fig. 2.13 are not dissipated in the ESR at own but are distributed over all resistive components in the resonant circuit such as connections, conductors and the DC-link capacitor. This may lead to significant temperature increase and is targeted by e.g. [94] where an arrangement is introduced with compact dedicated damping resistors. The damping resistors are mounted on the ceramic substrate for improved loss dissipation and shall unburden the other components. Further, the application of a DC-snubber capacitor for overvoltage reduction influences the semiconductor losses as well. While such a DC-snubber reduces turn-off losses by overvoltage reduction, the buffering effect weakens the voltage drop over the stray inductance at turn-on similar to a conventional switching cell with DC-link capacitor and same stray inductance. Hence, it increases the turn-on losses. This influence on the losses has been analyzed and approved by [85, 95] for SiC-MOSFET application and by [96] for an IGBT setup where a large DC-snubber has been found to be unsuitable for higher power applications.

2.5 Ceramic Capacitors

Depending on the application, the optimal selection of the capacitor technology is essential. As already summarized by [97] in low frequency applications with a demand for high energy density, electrolytic capacitors are most common. Nevertheless, they suffer from a high ESR, low ripple current rating and wear out due to electrolytic evaporation. Metallized Polypropylene Film Capacitors have superior characteristics in many points as high voltage and ripple current capability as well as low loss and good properties at higher frequencies. However, less specific capacitance and low energy density as well as a relatively low temperature rating limit their use for applications where a comparably high capacitance has to be connected with very low inductance in close proximity to a semiconductor operating a temperatures close to 150 °C as it would be optimal for snubber circuits.
With good high frequency and loss characteristics as well as availability of devices rated for temperatures above 150 °C and good energy density, multilayer ceramic capacitors (MLCCs) are a more suitable choice for this application. Recent developments in energy density e.g. [98] or [99] show a promising development offering new solutions for high

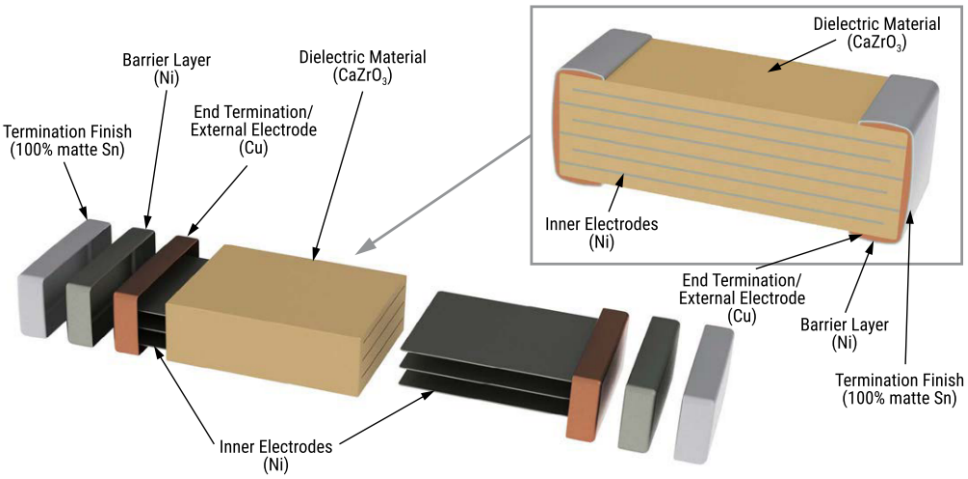


Figure 2.14: Exemplary assembly of a KC-Link capacitor [99]

integration. Therefore, this section shall tread important considerations influencing the device selection.

2.5.1 Mechanical Construction

Basically, the body of a MLCC consists of a stack of ceramic layers each coated with a metallization. The outer electrodes or termination are usually a combination of several interface layers but other types of electrodes like sintered metal plates are also available [98]. An assembly for a capacitor technology used in this work is given in Fig. 2.14 for an example. It can be seen that the inner electrodes are relatively thin compared to the ceramic material. Therefore, the assumption can be made that the ceramic material mainly determines the mechanical and heat dissipation behavior.
Failure modes can be divided in either extrinsic failure, mainly due to non-optimal processing, environmental influence or intrinsic failures due to device chemistry and physics [100, 101]. Mechanical stress may cause rupture of the ceramic body which can lead to a decreasing insulation resistance [102].

2.5.2 Dielectric Materials

For ceramic capacitors several material alloys are available for the dielectric. By applying an electric field to a dielectric, its insulating property prevents a charge transport from one electrode to the other. However, a short distance charge transport happens within an atom, molecule or small conductive areas and results in a dipole moment. Then, the material is called polarized. Depending on the characteristics ceramics are grouped into three classes as described in [103].

Class I dielectrics have a low relative permittivity of 5 to a few hundred and therefore, a low energy density. The dissipation factor $\tan\delta$ is very low ($<< 0.01$) and the temperature dependency is linear from zero to several thousand ppm/°C. Related modern materials are based on simple oxides like TiO_2, $CaTiO_3$ and modified $(Ca, Sr)(Zr, Ti)O_3$ [103]. According to [104], class I materials don't show a piezoelectric behavior. Due to its properties class I ceramics are used where low losses and linearity are required.

Class II dielectrics are usually based on Barium Titanate $BaTiO_3$ and $SrTiO_3$ and are available with a relative permittivity above 20.000. This is caused by its ferroelectric characteristic. According to [105], class II ceramic properties vary more with temperature, field strength and frequency than class I ceramics but their effects can be modified by doping with e.g. Ca,Zr or Sn. Furthermore, the dissipation factor is higher than those of class I ceramics with $\tan\delta < 0.03$ but can exceed this value at high AC load and in some temperature ranges. Additionally, class II materials are piezoelectric in their ferroelectric phase, see [104, 106]. This results in a change in mechanical dimensions by applying an electric field and vice versa.
Ferroelectric materials show domains with equal intrinsic electric field orientation Fig. 2.15.

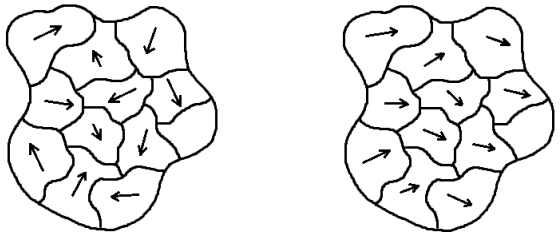


Figure 2.15: Areas with intrinsic field orientation
left:unpolarized, right: polarized

With an increasing electric field, more and more domains orient in field direction and store energy. A similar effect is known from the Weiss-domains in ferromagnetism from which the prefix 'ferro' is derived in ferroelectric.
Materials where each neighbor of a domain is oriented in opposite direction are called antiferroelectric. This results in a slightly different behavior than normal ferroelectric material as it can be seen in Fig. 2.16.

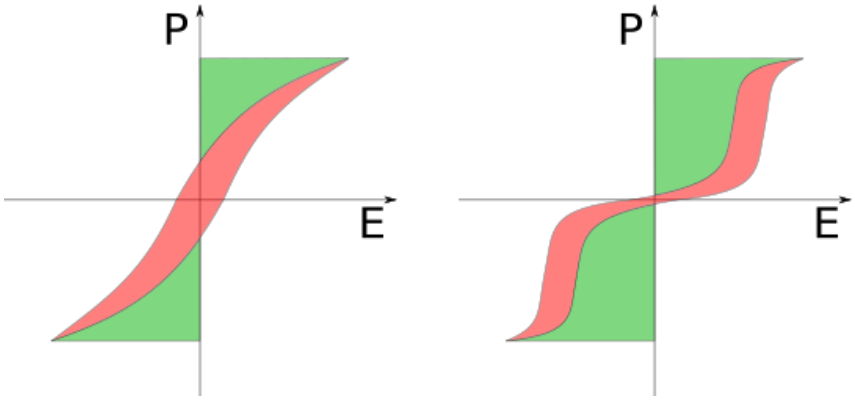


Figure 2.16: Scheme for polarization P over electric field E for relaxor ferroelectric (left) and antiferroelectric (right) material after [107]

Figure 2.16 shows the hysteresis of a relaxor ferroelectric and an antiferroelectric material. This hysteresis indicates the expectable capacitance/voltage behavior of the capacitor. Within a relaxor ferroelectric material many domains flip already at lower field-strength. Hence, the capacitance is going to be at its maximum at zero voltage. Contrariwise, at the antiferroelectric material, most domains will flip not until a specific field

strength is reached. As a result, such a capacitor will show its capacitance peak at a voltage different from zero, see [98, 106].

Class III dielectrics are processed in that manner that each grain has a conductive core insulated by a thin shell. Hence, the electric field only concentrates in the thin shells which results in very high specific capacitance values. It should be noted that due to the low shell thickness, these capacitors are only available for low voltages and therefore being unattractive for high power applications.

2.5.3 Electrical Characteristics

As mentioned above, ceramic material properties can vary with temperature, frequency and applied electric field strength. Hence, the ceramic properties have an immediate influence on the electric characteristic of a capacitor and the possible field of application. Further, the electrical properties vary also with the mounting direction.

With capacitor electrodes parallel to the mounting fixture, additional harmonics could be observed [108].
The capacitor can be modeled with the equivalent circuit shown in Fig. 2.17 (top). R_s is the serial resistance mainly caused by the connection. According to [109], it is very small up to the Megahertz range and then becomes significant due to skin effect. The ESL is the equivalent serial inductance and C the capacitance of the device. R_p describes the ceramic properties as well as the insulation resistance for DC bias.
Figure 2.17 (bottom) shows the simplified capacitor model with frequency, temperature and voltage dependent ESR and C. The equation of the simplified equivalent circuit is derived from the complete model and results in

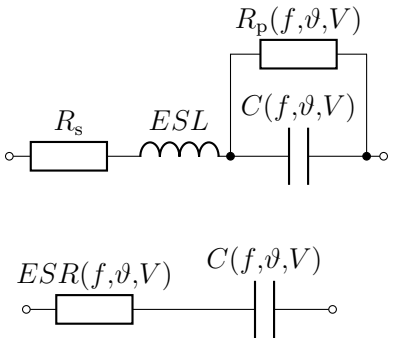


Figure 2.17: Complete capacitor equivalent circuit (top), simplified (bottom)

$$Z = R_s + \frac{R_p}{(\omega C R_p)^2 + 1} + j\left(\omega L - \frac{\omega C R_p^2}{(\omega C R_p)^2 + 1}\right). \tag{2.33}$$

Here, it is assumed that the capacitance is the dominant imaginary part over the target operation area. It should be noted that the linear model of (2.33) does not include the non-linear characteristics of the dielectrics mentioned in Section 2.5.2 which cause a more complex device response. These non-linear dependence of the ESR and C from voltage, temperature and frequency is well known and has been reported many times, see [110–114].

Breakdown behavior

Another application relevant point is the breakdown behavior of the ceramic material. There are long and short term effects. While especially foil capacitors show self healing property, ceramics don't. Therefore, the recommended voltage during application is about five times lower than the breakdown value [105].

A thermal breakdown is described with heating due to dielectric loss and the resulting decrease in insulation resistance which may result in thermal runaway and finally a breakdown.
Another effect is called discharge breakdown and describes a decreased breakdown voltage during charge and discharge. One hypothesis is given in [105]. At DC operation a high field concentrates at impurities and inhomogene pores in the dielectric material. If the critical field is reached, a discharge at this point occurs and leads to a local field reduction. The recharge process at DC takes time due to low leakage current and therefore, the interval between subsequent events is low. During AC operation, a discharge orrurs every half cycle contrary to DC when the leakage current causes the recharge. Hence, a breakdown at AC is more likely and the breakdown-voltage for AC load is lower. Another hypothesis is investigated by [115], where the lower breakdown is considered as a strain induced process. As mentioned above, some ceramic materials change their mechanical measurements in presence of electric field. As a result, the strain will change periodically with the applied AC field and may finally result in early breakdown due to e.g. interface separation or mechanical breakage.
Long term degradation is discussed in [105] and is explained with different mechanisms. E.g. environmental effects may cause rougher surfaces and lead to increased absorption of moisture and conductive impurities. Another effect is electrochemical action at DC condition and may lead to e.g. migration of silver on surfaces or along grain boundaries.

3 Introduction and Modeling of an Optimized Commutation Circuit

In this work, an optimized commutation circuit is presented and its manner of operation was patented in [116] and further investigated in [117] and [118]. In Section 2.1 it was mentioned that the wide-bandgap materials silicon carbide and gallium nitride are still suffering from poor raw material quality and high cost. Therefore, it is most reasonable to maximize their potential in the target application of medium and high power conversion at voltages above 500 V and currents above 100 A. Because silicon carbide has the highest state of development at the moment and it is the better choice for higher power ratings, it is chosen as the semiconductor material in this work. Basically, the proposed setup is also applicable for other semiconductor materials.

To maximize the utilization of SiC the losses must be decreased to a minimum. In Section 2.1.3, is has been shown that the on-state resistance is strongly dependent on the specified breakdown voltage of a MOSFET device. Additionally, a MOSFET must be selected with respect to the maximum expected drain-source voltage during operation, which usually appears at the negative current slope at turn-off, see Sect. 2.3. Hence, at a given current slope or switching speed respectively, a reduction of the turn-off overvoltage enables the choice of a device with lower breakdown-voltage and better on-state resistance or the operation at higher DC-link voltage. Both lead to lower losses per output power. But it has to be noted that this relationship couples the demand of low on-state resistance or high DC-link voltage to the achievable switching speed. As it can be derived from Sect. 2.3 the coupling factor is the setup's stray inductance. Therefore, a strong reduction of stray inductance is a mandatory goal for reducing the turn-off overvoltage and reduce either the on-state resistance or alternatively increasing the DC-link voltage respectively. As outlined in Sect. 2.2, for practical systems some important limitations make further minimization of the stray inductance challenging. Usually, the DC-link capacitor and the power module are developed and manufactured by different vendors and both components are assembled at customer side. This leads necessarily to a standardization of interfaces between the components or adaptations with the tacit requirement of easy assembly. These facts are strong inhibitors of reducing the stray inductance and limit the achievable over all system efficiency and in conclusion, better utilization of the power semiconductor.
Hence, a possible optimization in terms of stray inductance reduction and keeping the requirement of easy assembly for both dedicated components might be achieved by transferring the requirement of low stray inductance only to the power module.
Another important point to be considered is that a minimized stray inductance reduces the voltage drop at turn-on and would lead to higher turn-on losses at similar switching speed. It can be found in the literature that by keeping the switching speed constant, a change in the stray inductance has only a negligible effect on switching losses [22]. This results from the increase of turn-on losses and simultaneous reduction of turn-off losses.
By considering the above mentioned points the second important requirement can be made as a high stray-inductance at turn-on and a low stray inductance at turn-off. This

requirement for its own can be achieved by good approximation with the DC-snubber circuit shown in Fig. 2.11a with a large capacitor. By designing the stray inductance $L_{\sigma 2}$ very low, for example by integrating the snubber circuit inside the power module on substrate level, the low commutation relevant stray inductance for turn-off can be provided by the snubber. At turn-on, a large damping resistor R_{damp} and the free-wheeling diode D_{f} decouple the snubber and a larger stray inductance $L_{\sigma 1}$ would lead to the desired high voltage drop and low turn-on losses. However, the rule of energy conservation prescribes undesired damping losses with (2.28), which makes this solution uninteresting for higher power applications, cf. also [96].
To overcome this problem, a solution without or negligible damping losses would be reasonable. To keep the rule of energy conservation and do not dissipate the energy by damping, it must be actively converted to usable energy by transfer to the load or must be recovered into the DC-link capacitor.

In the following section a new setup and principle of operation is described successively which achieves the previously made requirements as presented by [117].

Further, a theoretical model for the setup is developed to evaluate characteristics which might not be easy to find with empirical studies and to gain a detailed understanding of the circuit. The model is validated and used for exemplary applications in Chapter 4. The goal of the active snubber with asymmetric stray inductance is to enable highest switching speed. As it will be shown, fastest switching speed allows to make use of some simplifications during modeling. In applications with limited switching speed, these simplifications may not be utilized and reduce the model application.

3.1 Optimized Circuit Introduction

In this section, the asymmetric active snubber circuit, see Fig. 3.1, its key features and the principle of operation is introduced, see also [117].
As described above, a reasonable optimization targets a large stray inductance during turn-on as well as a small stray inductance during turn-off. Further, the mentioned constraints for easy assembly might be achieved by transferring the requirement of a low inductive commutation cell to the power module. The circuit shown in Fig. 3.1 is designed with a DC-snubber like capacitor C_{sn} in practice carried out as a ceramic capacitor placed on substrate level inside the power module. This allows a very low commutation loop inductance for turn-off to be calculated with

$$L_{\sigma\mathrm{Off}} = L_{\mathrm{hb}} + \frac{L_{\mathrm{sn}} \cdot (L_{\mathrm{link}} + L_{\mathrm{con}})}{L_{\mathrm{sn}} + L_{\mathrm{link}} + L_{\mathrm{con}}} \tag{3.1}$$

To get a desired large stray inductance at turn-on $L_{\sigma\mathrm{On}}$, this snubber must be disconnected during turn-on, so the effective stray inductance at turn-on is given by

$$L_{\sigma\mathrm{On}} = L_{\mathrm{hb}} + L_{\mathrm{link}} + L_{\mathrm{con}}. \tag{3.2}$$

(3.2) can be simplified for $L_{\mathrm{hb}} \ll L_{\mathrm{link}} + L_{\mathrm{con}}$ to

$$L_{\sigma\mathrm{On}} \approx L_{\mathrm{link}} + L_{\mathrm{con}} = L_{\mathrm{main}} \tag{3.3}$$

with L_{main} for the inductance of the main DC-link circuit. Similarly, with $L_{\mathrm{sn}} \ll L_{\mathrm{link}} + L_{\mathrm{con}}$ (3.1) can be simplified to

$$L_{\sigma\mathrm{Off}} \approx L_{\mathrm{hb}} + L_{\mathrm{sn}}. \tag{3.4}$$

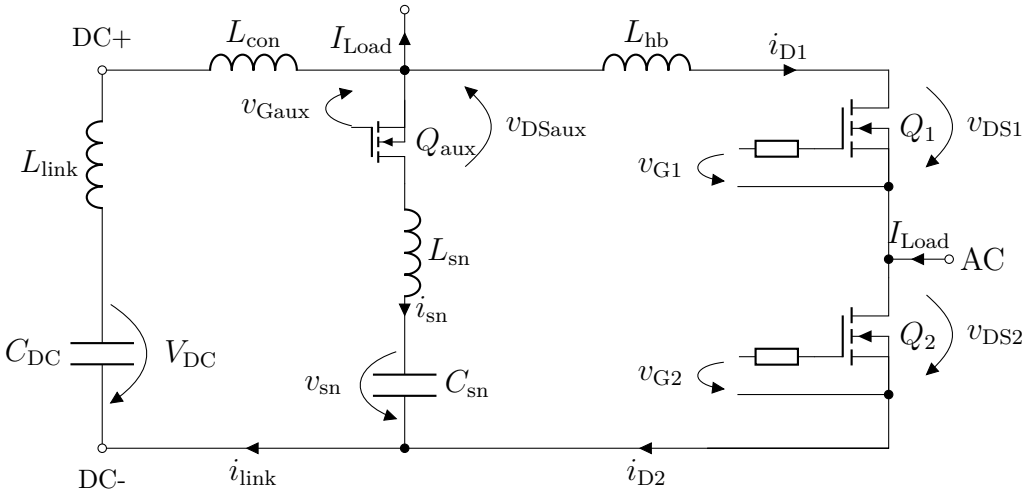


Figure 3.1: Setup equivalent circuit

Additionally, the damping losses must be controlled for total loss reduction. Both decoupling at turn-on as well as prohibiting resonant oscillation is done by placing a small switch with anti-parallel diode like a MOSFET, cf. Fig. 3.1 Q_{aux}, in series to the capacitor. This switch is only turned on during a short period during the switching events as described below.

3.2 Operation at Turn-On and Diode Recovery

In this section, a simplified description of the turn-on event with the setup above is given. The corresponding desired timing is shown in Figure 3.2.

$t < t_1$: Initially, the following assumptions are made. Q_2 is in blocking state and a constant load current I_{Load} is flowing into the AC terminal, here exemplary connected to the junction at Q_{aux}, cf. Fig. 3.1. Therefore, the body diode of Q_1 is in conduction state and its voltage v_{DS1} is close to zero. Additionally, it is assumed that the snubber capacitor C_{sn} is charged up - due to previous switching events - up to a voltage higher than the DC-link capacitor, $V_{\mathrm{sn0}} > V_{\mathrm{DC}}$. The auxiliary switch Q_{aux} is in blocking state, so its voltage is

$$v_{\mathrm{DSaux}}(t < t_1) = V_{\mathrm{sn0}} - V_{\mathrm{DC}}.$$

$t_1 \leq t < t_2$: At $t = t_1$, the gate signal of the blocking switch Q_2 is turned on and the load current starts commutating from Q_1 to Q_2. The increasing current gradient of i_{D2} and the deliberately large stray inductance $L_{\sigma\mathrm{On}}$ (see (3.2) and Fig. 3.1) result in a significant voltage drop down to zero. This results in a quasi soft behavior and the turn-on losses are very small. It has to be noted that in this interval, the chip capacitance C_{oss2} is discharged through the channel also. So the stored energy, calculated later with (3.15), is dissipated in the semiconductor but not measured which might not be negligible.
The increasing voltage over L_{main} also leads to a voltage drop over the auxiliary switch Q_{aux} which has to be taken into account for proper dimensioning and device selection. In case L_{hb} is very low compared to L_{main}, v_{DSaux} nearly reaches the snubber voltage v_{sn} with a difference of

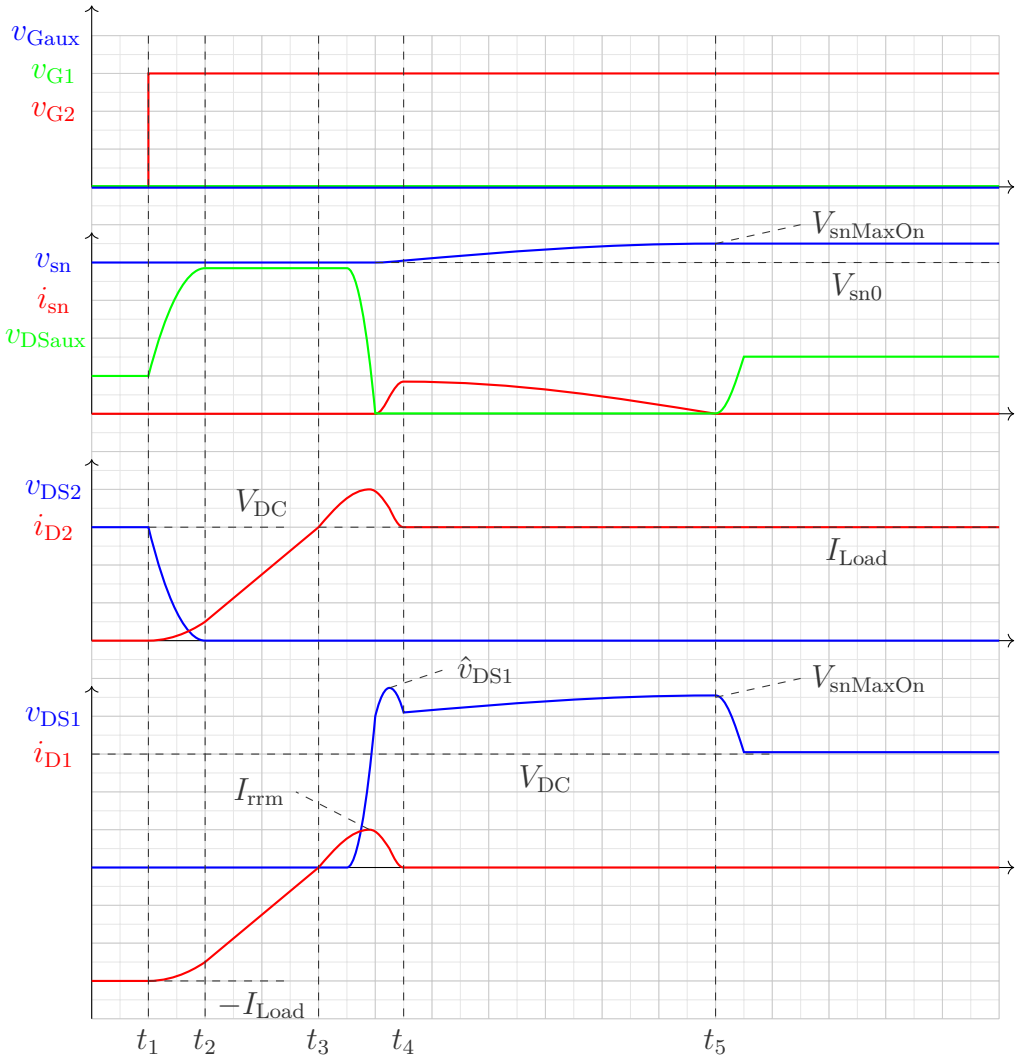


Figure 3.2: Turn-on event after [118]

$$v_{\mathrm{sn}} - v_{\mathrm{DSaux}} = L_{\mathrm{hb}} \cdot \frac{\mathrm{d}i_{\mathrm{D2}}}{\mathrm{d}t}.$$

$t_2 \leq t < t_3$: In this interval, the total DC-link voltage is across $L_{\sigma\mathrm{On}}$ and the current slope is determined by

$$\frac{\mathrm{d}i_{\mathrm{D2}}}{\mathrm{d}t} = \frac{v_{\mathrm{DC}}}{L_{\sigma\mathrm{On}}}$$

until i_{D2} is equal to the load current at $t = t_3$.

$t_3 \leq t < t_4$: After i_{D2} is equal to the load current, the charge in the body diode of Q_1 recovers and the reverse recovery current leads to a drain-source current higher than the load current. The voltage v_{DS1} increases until it reaches the snubber voltage v_{sn} level. Simultaneously, the voltage at the auxiliary switch v_{DSaux} decreases down to zero. It reaches zero slightly before the maximum peak voltage $\hat{v}_{\mathrm{DS1}}$ occurs.

It should be noted that the current in the DC-link i_{link} becomes positive due to the reverse recovery current. Hence, the stray inductance L_{main} contains an energy of

$$W_{\text{Lmain}} = \frac{1}{2} \cdot L_{\text{main}} \cdot i_{\text{link}}^2. \tag{3.5}$$

Further, as the voltage at the auxiliary switch v_{DSaux} becomes zero, its body diode gets in conduction state. As a result, for the diode turn-off, the commutation circuit changes in its effective stray inductance from $L_{\sigma\text{On}}$ to $L_{\sigma\text{Off}}$.
During this period of the diode turn-off, the voltage at Q_1 increases to its maximum $\hat{v}_{\text{DS1}}$ which is only determined by the very small effective stray inductance, the current gradient and the snubber voltage

$$\hat{v}_{\text{DS1}} = L_{\sigma\text{Off}} \cdot \frac{\mathrm{d}i_{\text{D1}}}{\mathrm{d}t}_{max} + v_{\text{sn}}. \tag{3.6}$$

Additionally, the current i_{link} driven by L_{main} starts commutating into the snubber capacitor. As a result, the remaining energy in L_{main} acc. (3.5) and the power provided by the DC-link begin to charge the snubber capacitor

$t_4 \leq t < t_5$: For $t = t_4$, the diode recovery process is finished. The cosinusoidal snubber current is determined by the resonant circuit consisting of C_{sn} and

$$L_{\text{res}} = L_{\text{main}} + L_{\text{sn}}. \tag{3.7}$$

Due to this comparatively large inductance and the large snubber capacitance, the resonant frequency of this circuit is comparatively low.
Due to the low frequency and the small value of $L_{\sigma\text{Off}}$, the voltage drop over this inductance L_{hb} becomes negligible. This results in a voltage over the turned-off switch Q_1 similar to the snubber

$$v_{\text{DS1}} \approxeq v_{\text{sn}}.$$

During this period, the energy W_{Lmain} and energy provided by the DC-link is transferred to the snubber capacitor until its voltage reaches its maximum at $t = t_5$ leading to an energy change in the capacitance of

$$\Delta W_{\text{Csn}} = \frac{1}{2} \cdot L_{\text{res}} \cdot i_{\text{sn}}^2(t_4) + W_{\text{DC}} \tag{3.8}$$

$$= \frac{1}{2} \cdot C_{\text{sn}} \cdot \Delta v_{\text{sn}}^2 \tag{3.9}$$

By inserting $\Delta v_{\text{sn}}^2 = v_{\text{sn}}^2(t_5) - v_{\text{sn}}^2(t_4)$ into the previous equation and rearranging to $v_{\text{sn}}(t_5)$ the peak snubber voltage V_{snMaxOn} can be estimated as

$$V_{\text{snMaxOn}} = \sqrt{\frac{L_{\text{res}}}{C_{\text{sn}}} i_{\text{sn}}^2(t_4) + v_{\text{sn}}^2(t_4) + \frac{2W_{\text{DC}}}{C_{\text{sn}}}}. \tag{3.10}$$

$t \geq t_5$: By entering this interval, the snubber current becomes zero and the body diode of Q_{aux} gets into blocking state. As a result, the snubber is disconnected and the voltage v_{DS1} reduces to the DC-link voltage V_{DC} again.

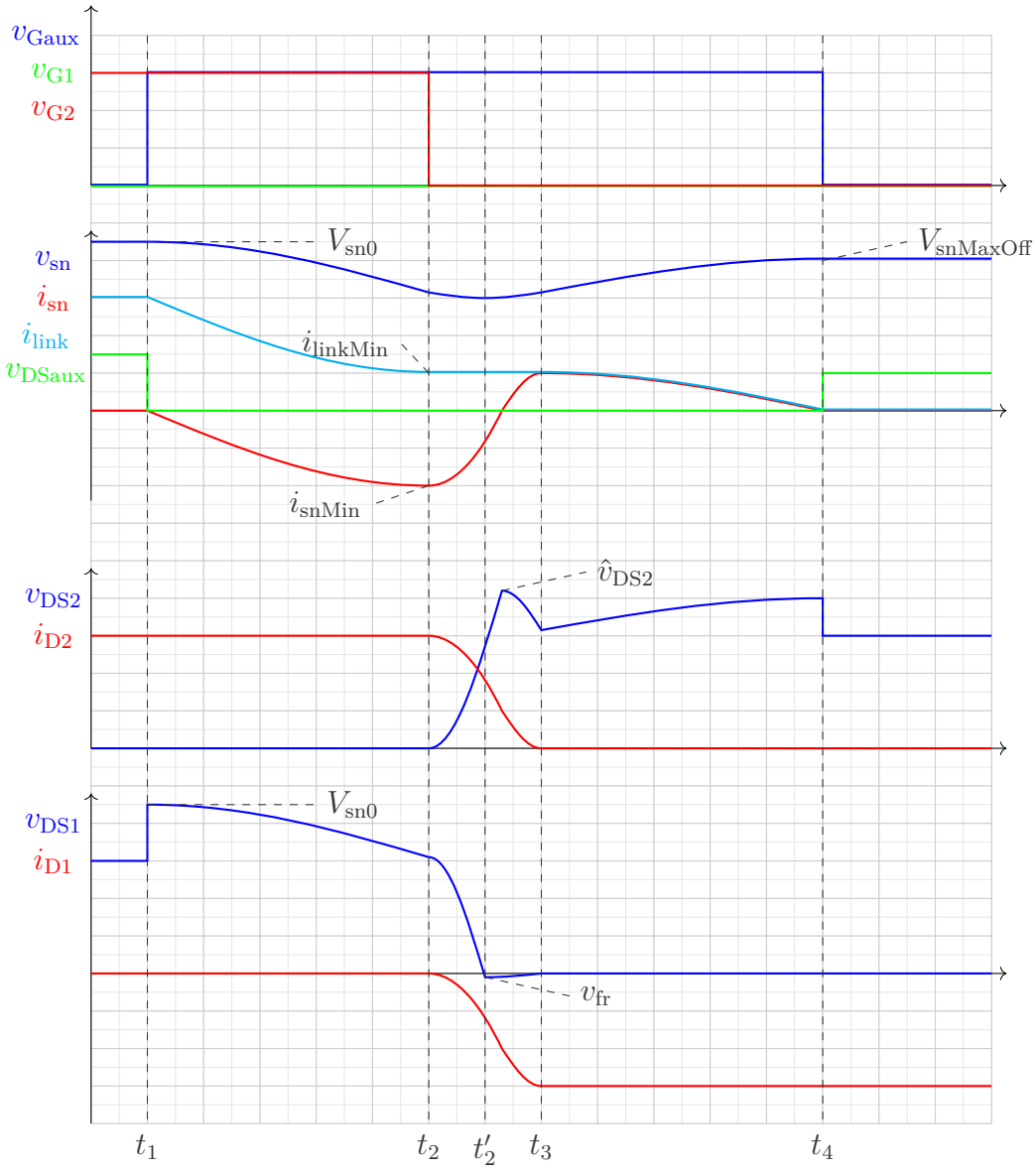


Figure 3.3: Turn-off event after [118]

3.3 Operation at Turn-Off

$t < t_1$: Similar to the turn-on event, it is assumed that previous switching events have charged the snubber capacitor to a voltage higher than the DC-link voltage $V_{\mathrm{sn0}} > V_{\mathrm{DC}}$. Before t_1, Q_{aux} is in blocking-state. Q_2 is in conduction state, so its drain current equals I_{Load}. Additionally, its voltage is zero, which results in a drain-source voltage of the complementary transistor Q_1 equal to V_{DC}.

$t_1 \leq t < t_2$: At $t = t_1$, the auxiliary switch Q_{aux} is turned on rapidly. Because the snubber current slope is mainly determined by the characteristics of the resonant circuit C_{sn} and L_{res} (see (3.7) and Fig. 3.1), the snubber current remains nearly zero during the turn-on event of Q_{aux}. Hence, it is turned on with zero current and therefore, negligible losses. It should be noted that the voltage of the blocking transistor v_{DS1} increases to V_{sn0}.

The higher snubber voltage v_{sn}, results in a sinusoidal discharge current. This discharge current reduces the DC-link current i_{link} by constant load current through Q_2. During this phase the snubber partially provides energy to the load and unburdens the main DC-link. As a result, energy that would be damped in a conventional DC-snubber setup according to Fig. 2.11a, is now fed to the load by reducing the provided power of the main DC-link.
At the end of this period timed by choosing t_2, the snubber current is approximately at its minimum i_{snMin} and $v_{\mathrm{sn}}(t_2) \approx V_{\mathrm{DC}}$. The retrievable energy stored in the snubber capacitor at previous switching events is nearly totally released. With $i_{\mathrm{sn}} = i_{\mathrm{link}} - i_{\mathrm{D2}}$ this results in the minimum achievable remaining DC-link current i_{linkMin} and the energy change in L_{main} can be calculated with

$$\Delta W_{\mathrm{Lmain}} = \frac{1}{2} \cdot C_{\mathrm{sn}} \cdot \Delta v_{\mathrm{sn}}^2 \tag{3.11}$$

$$= \frac{1}{2} \cdot L_{\mathrm{main}} \cdot \Delta i_{\mathrm{sn}}^2, \tag{3.12}$$

where $\Delta v_{\mathrm{sn}} = V_{\mathrm{sn0}} - v_{\mathrm{sn}}(t_2)$. Thus, the resulting snubber current at this point can be calculated by considering (3.12) and rearranging to

$$\Delta i_{\mathrm{sn}} = \sqrt{\frac{C_{\mathrm{sn}}}{L_{\mathrm{main}}}} \Delta v_{\mathrm{sn}}^2. \tag{3.13}$$

Now the remaining current in the DC-link can be calculated

$$i_{\mathrm{link}} = I_{\mathrm{Load}} - \Delta i_{\mathrm{sn}} \tag{3.14}$$

$t_2 \leq t < t_2'$: The turn-off event of the conducting power switch Q_2 is started at $t = t_2$ by decreasing the gate-voltage v_{G2} to low level.
In this description t_2 is chosen considering the snubber voltage is similar to the DC-link voltage $v_{\mathrm{sn}}(t_2) \approx V_{\mathrm{DC}}$. It should be noted that the selection of t_2 is a manner of optimization. A comprehensive examination is shown in Section 3.5.
Additionally, during this period the snubber voltage v_{sn} and the DC-link current i_{link} remain nearly constant, which is caused by the much larger oscillation period of the resonant circuit C_{sn} and L_{res} compared to the turn-off duration. Only a slight change is caused by the commutation current. Hence, the commutation current is mainly provided by the snubber capacitor. This results in the very small effective stray inductance according to (3.4).
The high voltage slope of v_{DS2} causes a displacement current in the parasitic capacitance of the complementary switch Q_1 which leads to a reduction of the drain current i_{D2}. Maximizing the switching speed can lead to a quasi soft turn-off as described in Section 2.3.2. The parasitic capacitance of Q_2 is charged with

$$W_{\mathrm{Coss2}} \approx \frac{1}{2} \cdot C_{\mathrm{oss2}} \cdot v_{\mathrm{sn}}(t_2')^2 \tag{3.15}$$

for a parasitic capacitance C_{oss2} assumed to be linear.

$t_2' \leq t < t_3$: At $t = t_2'$, the voltage of the switching device v_{DS2} equals the snubber voltage v_{sn} equal to the DC-link voltage. The voltage of the complementary switch v_{DS1}

becomes zero and the current starts flowing though its junction. Hence, according to Section 2.1.2 a forward recovery voltage v_{fr} might be measured which may limit the achievable switching speed of Q_2. The resulting voltage of Q_2 is described by a superposition of the slightly increasing snubber voltage, the forward voltage and the induced voltage in the small effective stray inductance $L_{\sigma\mathrm{Off}}$

$$v_{\mathrm{DS2}} = v_{\mathrm{sn}} + v_{\mathrm{fr}} + L_{\sigma\mathrm{Off}} \frac{\mathrm{d}i_{\mathrm{D2}}}{\mathrm{d}t}. \tag{3.16}$$

After reaching its maximum $\hat{v}_{\mathrm{DS2}}$, it approaches the snubber voltage v_{sn}.

$t_3 \leq t < t_4$: At the beginning of this period, the switching event of Q_2 is finished. Despite of the period $t_2 \leq t < t_2'$, now i_{D2} is zero. Hence, the snubber current becomes equal to the DC-link current $i_{\mathrm{sn}} = i_{\mathrm{link}}$. Very similar to the turn-on event period $t_3 \leq t < t_4$ the cosinusoidal snubber current is determined by the resonant circuit consisting of C_{sn} and L_{res}. However, due to the similarity of snubber- and DC-link voltage, the energy provided by the DC-link can be neglected in the calculation. The remaining energy in L_{main}, see (3.3), can be calculated with (3.5) which is transferred to the snubber capacitor. The snubber voltage at the end of this period, where the oscillating current crosses zero, can be calculated by adapting (3.10) to

$$v_{\mathrm{snMaxOff}} = \sqrt{\frac{L_{\mathrm{res}}}{C_{\mathrm{sn}}}} i_{\mathrm{linkMin}} + v_{\mathrm{sn}}(t_3). \tag{3.17}$$

$t \geq t_4$: At $t = t_4$, the snubber current reaches zero. The auxiliary switch is now turned off rapidly for zero current switching and for preventing further oscillation. Hence, its voltage raises to $v_{\mathrm{snMaxOff}} - V_{\mathrm{DC}}$. The energy from the stray inductance is now stored for subsequent turn-off events.

3.4 Modeling the Turn-On Event

In this section, the described turn-on event according to Section 3.2 is modeled mathematically. Similarly, it is assumed that the fall time of the drain-source voltage is much lower than the current rise time. Hence, a large effective stray inductance $L_{\sigma\mathrm{On}}$ is assumed. This results in an interval, where the total DC-link voltage is across this stray inductance and the turn-on event becomes quasi soft, cf. Sect. 2.3.1. Further, it will be shown under which conditions this assumption becomes invalid and the model shown starts deviating from measurements.
In addition, for the sake of a manageable model, it is based on some simplifications. It is known that the behavior of the body diode is a function of temperature, current gradient and forward current amplitude and dead-time, cf. [40, 119–122] as well as dependent on a possible parasitic turn-on [123]. One major simplification is lumping the reverse recovery charge as well as the behavior of the non-linear output capacitance [119, 120] into a single linear capacitance $C_{\mathrm{oss}*}$. Then, $C_{\mathrm{oss}*}$ models the bipolar current part as well as the capacitive displacement part of the diode, see also [124]. This simplification is valid if the carrier lifetime during diode recovery is not artificially increased, e.g. by carrier life-time modulation.
The switching behavior of the semiconductor is simplified with a linear decreasing voltage slope, which is sufficient at the desired high switching speed as it will be shown. Further, the auxiliary switch has an output capacitance assumed to be negligible. However, in a practical setup with very fast recovery diode behavior the displacement current in this output capacitance might be significant.
With respect to Figure 3.1 the inductance L_{hb} and L_{sn} are lumped into a single one L_{snhb}. This is valid for $L_{\mathrm{hb}} \ll L_{\mathrm{main}}$ to achieve a similar resonant frequency and turn-off overvoltage and results in an equivalent circuit shown in Fig. 3.4.

$$L_{\mathrm{sn}} \rightarrow L_{\mathrm{snhb}} = L_{\mathrm{sn}} + L_{\mathrm{hb}}. \tag{3.18}$$

Further, this simplification is suitable for practical setups in which L_{hb} is very small. Thus, in case the snubber capacitor is placed with higher inductance L_{sn}, e.g. on driver board, the model remains valid.
These simplifications allow a model derivation for subsequent intervals as depicted in Figure 3.2.
Finally, the model shall be used to calculate the damping losses during the intervals. Hence, the corresponding resistors are included in the circuit as well.

According to Fig. 3.4, the description relies on a turning on semiconductor Q_2. Hence, the body diode of Q_1 is initially in conduction state. An important point to mention is the frequency dependence of R_{main} - which models the losses in the connection to the DC-link capacitor and the capacitor itself - due to skin and proximity effect and capacitor loss factor. So for the continuous load current this resistance is very low and increases for the AC-signals in the further described intervals. Hence, the initial snubber voltage before the very first switching event is very similar to the DC-link voltage V_{DC}.
A complete mathematical successive solution including initial states and important complex derivation steps can be found in Appendix A.3.

Interval $t_1 \leq t < t_2$

Equal to Section 3.2, the semiconductor Q_2 starts turning on at $t_1 = 0$, cf. Fig. 3.1. Its drain-source voltage v_{DS2} is modeled as linear decreasing and due to the blocking

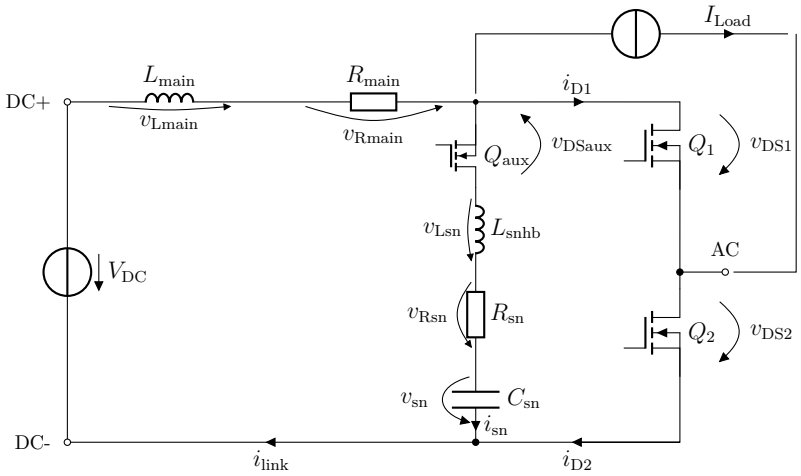


Figure 3.4: Model equivalent circuit

auxiliary switch, a circular current increases within the loop over the DC-link capacitor and its connection to the halfbridge. As a result, a voltage drop occurs across L_{main} and R_{main} in the first interval $t_1 \leq t < t_2$. The DC-link current can be calculated with

$$i_{\mathrm{link}}(t) = \frac{V_{\mathrm{DC}}}{t_{\mathrm{f12}} R_{\mathrm{main}}} \left(\frac{1}{2\delta_{14}} (e^{-2\delta_{14} t} - 1) + t \right), \tag{3.19}$$

where the voltage fall time is $t_{\mathrm{f12}} = t_2 - t_1$. To calculate the damping coefficient the following well-known equation, see also (A.33), is used

$$\delta_{14} = \frac{R_{\mathrm{main}}}{2L_{\mathrm{main}}}. \tag{3.20}$$

The indices -14- refer to a coefficient valid from t_1 to t_4.

Interval $t_2 \leq t < t_3$
After the channel of Q_2 is opened, its voltage v_{DS2} equals zero and the total DC-link voltage V_{DC} lies across L_{main} and R_{main}. Within this interval $t_2 \leq t < t_3$, the further current increase is almost linear for small R_{main} and can be described with

$$i_{\mathrm{link}}(t) = \frac{V_{\mathrm{DC}}}{t_{\mathrm{f12}} R_{\mathrm{main}}} \left(\frac{1}{2\delta_{14}} (e^{-2\delta_{14} t} - e^{-2\delta_{14}(t - t_{\mathrm{f12}})}) + t_{\mathrm{f12}} \right). \tag{3.21}$$

To calculate the point in time when i_{link} reaches the load current level, (3.21) can be rearranged to $t = t_3$ as

$$t_3 = -\ln \left(\frac{(\frac{I_{\mathrm{Load}} R_{\mathrm{main}}}{V_{\mathrm{DC}}} - 1) 2\delta_{14} t_{\mathrm{f12}}}{1 - e^{+2\delta_{14} t_{\mathrm{f12}}}} \right) / (2\delta_{14}). \tag{3.22}$$

Special case: Slow voltage slope or low load current
In case the voltage slope is smaller or the load current is comparatively low, i_{link} may reach the load current level before v_{DS2} becomes zero. In such a case, t_3 calculated with (3.22) is smaller than or equal to t_2. Hence, the first two intervals (or even further

intervals) overlap and the previously shown (3.21) is omitted. Furthermore, this means that v_{DS1} starts increasing before v_{DS2} has reached zero and thus, (3.19) becomes invalid. However, for a small difference between t_2 and the calculated t_3, (3.19) may be applicable with acceptable deviation, as it will be shown in Section 4.3. Appropriately, t_3 can be calculated by rearranging (3.19) to $t = t_3$ by using the Lambert-W-function

$$t_3 = \frac{\mathrm{W}\left(-e^{-K_*}\right) + K_*}{2\delta_{14}} \tag{3.23}$$

and by setting K_* to be

$$K_* = \frac{I_{\mathrm{Load}} R_{\mathrm{main}}^2}{V_{\mathrm{DC}} L_{\mathrm{main}}} t_{\mathrm{f12}} + 1. \tag{3.24}$$

Interval $t_3 \leq t < t_4$

For the following derivations, the initial assumption of a high voltage slope of v_{DS2} and a comparatively high load current shall be valid.

The DC-link current has reached the load current value at $t = t_3$ and hence, the recovery process of the Q_1 body diode starts. In this interval the current i_{D1}, see Fig. 3.4, is positive due the reverse recovery charge. The drain-source voltage of the passive switch, here Q_1, increases. Hence, its output capacitance $C_{\mathrm{oss}*}$ charges and as a result, the voltage across the auxiliary switch Q_{aux} decreases, see also Fig. 3.2. After the peak current I_{rrm} occurs, cf. Fig. 3.2, the current slope becomes negative and - caused by $L_{\sigma\mathrm{On}}$ - the voltage across the passive switch further increases until it becomes equal to the snubber voltage V_{sn0}. V_{sn0} is higher than V_{DC} caused by charging during former switching events as discussed in Sections 4.6. Thus, the body diode of the auxiliary switch becomes conductive. However, in a real setup, where the output capacitance of Q_{aux} might allow a significant displacement current, the parasitic elements in the snubber path, L_{snhb} and R_{sn}, may cause a measurable voltage drop which shall be neglected here.

Hence, the main stray inductance L_{main} and the output capacitance $C_{\mathrm{oss}*}$ result in a resonant circuit with the following parameters

$$\omega_{034} = \frac{1}{\sqrt{L_{\mathrm{main}} C_{\mathrm{oss}*}}} \quad \text{and} \tag{3.25}$$

$$\omega_{\mathrm{d34}} = \sqrt{\omega_{034}^2 - \delta_{14}^2}. \tag{3.26}$$

This allows the calculation of the DC-link current according to the following equation

$$i_{\mathrm{link}}(t) = A_{34} e^{-\delta_{14}(t-t_3)} \sin(\omega_{\mathrm{d34}}(t - t_3)) + I_{\mathrm{Load}}, \tag{3.27}$$

where A_{34} is very similar to the reverse recovery peak in case $e^{-\delta_{14}(t-t_3)} \approx 1$. Otherwise, A_{34} can be calculated under the condition of fast switching with $v_{\mathrm{Lmain}} = V_{\mathrm{DC}}$ in the interval $t_1 \leq t < t_2$ by

$$A_{34} = \frac{V_{\mathrm{DC}}}{t_{\mathrm{f12}} R_{\mathrm{main}} \omega_{\mathrm{d34}}} \left(e^{-2\delta_{14}(t_3 - t_2)} - e^{-2\delta_{14} t_3}\right), \tag{3.28}$$

which changes for low current values due to the skipped interval ($t_2 \leq t < t_3$) to

$$A_{34} = \frac{V_{\mathrm{DC}}}{(t_3 - t_1) R_{\mathrm{main}} \omega_{\mathrm{d34}}} \left(1 - e^{-2\delta_{14} t_3}\right). \tag{3.29}$$

The end of this interval at $t = t_4$, can be estimated with

$$t_4 = \arccos(K)/\omega_{\mathrm{d34}} + t_3, \tag{3.30}$$

in case the damping is negligible ($\delta_{14} << \omega_{\mathrm{d34}}$) and where K is given by

$$K = \frac{(V_{\mathrm{DC}} - V_{\mathrm{sn0}} - R_{\mathrm{main}} I_{\mathrm{Load}})\, 2\delta_{14} t_{\mathrm{f12}}}{V_{\mathrm{DC}}(e^{-2\delta_{14}(t_3 - t_2)} - e^{-2\delta_{14} t_3})}. \tag{3.31}$$

Interval $t_4 \leq t < t_5$
Considering a real setup, the conducting body diode of Q_{aux} yields to multiple resonant circuits sharing the snubber path. One is the resonant circuit formed by the main stray inductance L_{main} and L_{snhb}

$$L_{\mathrm{res}} = L_{\mathrm{snhb}} + L_{\mathrm{main}} \tag{3.32}$$

and the snubber capacitor C_{sn} with a comparatively low resonant frequency. In this circuit the resonance contains the major part of oscillating energy if $L_{\mathrm{main}} \gg L_{\mathrm{snhb}}$. The second resonance occurs between the output capacitance $C_{\mathrm{oss}*}$ of Q_1 and the snubber inductance L_{snhb} with smaller energy. Because goal is describing the snubber behavior and losses, latter resonance is neglected and not considered by the model. Hence, only the resonance between L_{res} and C_{sn} is analyzed further.
For further derivations, the peak value of the AC part of the oscillating DC-link current at $t = t_4$ is important and can be calculated by subtracting the load current from (3.27) resulting in

$$i_{\mathrm{linkAC}}(t_4) = A_{34} e^{-\delta_{14}(t_4 - t_3)} \sin(\omega_{\mathrm{d34}}(t_4 - t_3)). \tag{3.33}$$

Appropriately, the relevant parameters of the target resonant circuit are

$$\omega_{045} = \frac{1}{\sqrt{L_{\mathrm{res}} C_{\mathrm{sn}}}}, \tag{3.34}$$

$$\delta_{45} = \frac{R_{\mathrm{main}} + R_{\mathrm{sn}}}{2L_{\mathrm{res}}} \quad \text{and} \tag{3.35}$$

$$\omega_{\mathrm{d45}} = \sqrt{\omega_{045}^2 - \delta_{45}^2}. \tag{3.36}$$

These parameters and (3.33) allow the calculation of i_{link} in the last interval $t_4 \leq t < t_5$ resulting in

$$i_{\mathrm{link}}(t) = e^{-\delta_{45}(t - t_4)}[i_{\mathrm{linkAC}}(t_4)\cos(\omega_{\mathrm{d45}}(t - t_4)) + A_{45}\sin(\omega_{\mathrm{d45}}(t - t_4))] + I_{\mathrm{Load}} \tag{3.37}$$

with the parameter

$$A_{45} = \frac{(V_{\mathrm{DC}} - V_{\mathrm{sn0}} + R_{\mathrm{sn}} I_{\mathrm{Load}})}{L_{\mathrm{res}}\omega_{\mathrm{d45}}} - \frac{\delta_{45}}{\omega_{\mathrm{d45}}}(i_{\mathrm{linkAC}}(t_4) + 2I_{\mathrm{Load}}). \tag{3.38}$$

The end of the switching event occurs for $t = t_5$ when the DC-current crosses zero. t_5 can be estimated in case of negligible damping with

$$t_5 = \frac{\arctan\left(-\frac{A_{1\mathrm{t5}}}{A_{2\mathrm{t5}}}\right)}{\omega_{\mathrm{d45}}} + t_4, \tag{3.39}$$

where A_{1t5} and A_{2t5} are defined by

$$A_{1t5} = i_{\text{linkAC}}(t_4)\omega_{\text{d45}}L_{\text{res}} \quad \text{and} \tag{3.40}$$

$$A_{2t5} = V_{\text{DC}} - V_{\text{sn0}} + R_{\text{sn}}I_{\text{Load}} - L_{\text{res}}\delta_{45}(i_{\text{linkAC}}(t_4) + 2I_{\text{Load}}). \tag{3.41}$$

With the knowledge of t_5, the calculation of the snubber current within the last interval can be done with

$$\begin{aligned} i_{\text{sn}}(t) &= i_{\text{link}}(t) - I_{\text{Load}} \\ &= e^{-\delta_{45}(t-t_4)}[i_{\text{linkAC}}(t_4)\cos(\omega_{\text{d45}}(t-t_4)) \quad + A_{45}\sin(\omega_{\text{d45}}(t-t_4))]. \end{aligned} \tag{3.42}$$

This allows the calculation of the snubber voltage change by integration to obtain the charge and division by the snubber capacitance as

$$\begin{aligned} \Delta v_{\text{sn}} = &A_{45\text{Vsn1}}e^{-\delta_{45}(t-t_4)}\sin(\omega_{\text{d45}}(t-t_4)) \\ &+ A_{45\text{Vsn2}}\left(1 - e^{-\delta_{45}(t-t_4)}\cos(\omega_{\text{d45}}(t-t_4))\right), \end{aligned} \tag{3.43}$$

with the parameters

$$A_{45\text{Vsn1}} = \frac{i_{\text{linkAC}}(t_4) + 2I_{\text{Load}}}{\omega_{\text{d45}}C_{\text{sn}}} - 2\omega_{\text{d45}}L_{\text{res}}I_{\text{Load}} - \frac{\delta_{45}}{\omega_{\text{d45}}}(V_{\text{DC}} - V_{\text{sn0}} + R_{\text{sn}}I_{\text{Load}}) \quad \text{and} \tag{3.44}$$

$$A_{45\text{Vsn2}} = V_{\text{DC}} - V_{\text{sn0}} - R_{\text{main}}I_{\text{Load}}. \tag{3.45}$$

The end value of the snubber voltage can now be calculated with

$$v_{\text{sn}}(t_5) = V_{\text{snMaxOn}} = V_{\text{sn0}} + \Delta v_{\text{sn}}. \tag{3.46}$$

3.5 Modeling the Turn-Off Event

In this section, the model for the turn-off event is derived. Goal of the turn-off event is to describe the snubber current to enable loss estimation as well as snubber voltage change. For stability purposes, the snubber voltage change shall be calculable as a function of the load current, the switching speed and the initial snubber voltage before the switching event. This eases the assessment of stability during subsequent switching operation together with the turn-on model.
Because during the whole event the auxiliary switch is in conduction state, the oscillation circuit parameters are equal to

$$\omega_0 = \omega_{045}, \quad \delta = \delta_{45} \quad \text{and} \quad \omega_{\text{d}} = \omega_{\text{d45}} \tag{3.47}$$

as it is used in Appendix A.4 where a complete successive solution can be found similar to the turn-on. Additionally, the equivalent circuit according to Figure 3.4 can be used. However, the behavior of the turning off semiconductor Q_2 is not approximated by a linear voltage but a linear current slope.

Interval $t_1 \leq t < t_2$
Similar to the turn-on, t_1 is defined to be zero, cf. Fig. 3.3. Thus, the first interval is described by a simple damped oscillation according to

$$i_{\text{sn}}(t) = \frac{A_0}{\omega_d} \cdot e^{-\delta t} \cdot \sin(\omega_d t), \tag{3.48}$$

where

$$A_0 = \frac{V_{\mathrm{DC}} - V_{\mathrm{sn0}} - R_{\mathrm{main}} I_{\mathrm{Load}}}{L_{\mathrm{res}}} \tag{3.49}$$

is a constant and recurrent parameter used in further equations. Integration of (3.48) and division by the snubber capacitance leads to the equation for the snubber voltage change within this interval

$$\Delta v_{\mathrm{sn}}(t) = -A_0 L_{\mathrm{res}} \left[e^{-\delta t} \left(\frac{\delta}{\omega_{\mathrm{d}}} \sin(\omega_{\mathrm{d}} t) + \cos(\omega_d t) \right) - 1 \right]. \tag{3.50}$$

Setting $\Delta v_{\mathrm{sn}}(t_2)$ equal to $\Delta v_{\mathrm{sn}}(t) = V_{\mathrm{DC}} - V_{\mathrm{sn0}}$, allows the calculation of of the point in time t_2 with negligible damping by rearranging (3.50) to

$$t_2 = \frac{\arccos\left(\frac{R_{\mathrm{main}} I_{\mathrm{Load}}}{R_{\mathrm{main}} I_{\mathrm{Load}} - V_{\mathrm{DC}} + V_{\mathrm{sn0}}} \right)}{\omega_{\mathrm{d}}}. \tag{3.51}$$

As mentioned above, R_{main} is frequency dependent and in case the voltage drop $R_{\mathrm{main}} I_{\mathrm{Load}}$ is negligible as well, this equation simplifies to

$$t_2 = \frac{\pi}{2\omega_{\mathrm{d}}}. \tag{3.52}$$

Interval $t_2 \leq t < t_3$

In the following interval, cf. Fig. 3.3, the drain current slope of the turning off Q_2 is modeled as linear decreasing with a duration of $t_{\mathrm{f23}} = t_3 - t_2$. The resulting snubber current can be calculated with

$$\begin{aligned} i_{\mathrm{sn}}(t) = {} & \frac{A_0}{\omega_{\mathrm{d}}} e^{-\delta t} \sin(\omega_{\mathrm{d}} t) + R_{\mathrm{main}} C_{\mathrm{sn}} \frac{I_{\mathrm{Load}}}{t_{\mathrm{f23}}} \left[1 - e^{-\delta (t - t_2)} \cos(\omega_{\mathrm{d}} (t - t_2)) \right] \\ & + \frac{I_{\mathrm{Load}}}{t_{\mathrm{f23}} \omega_{\mathrm{d}}} \left(\frac{L_{\mathrm{main}}}{L_{\mathrm{res}}} - \delta R_{\mathrm{main}} C_{\mathrm{sn}} \right) e^{-\delta (t - t_2)} \sin(\omega_{\mathrm{d}} (t - t_2)). \end{aligned} \tag{3.53}$$

(3.53) simplifies for negligible damping with $\delta \ll \omega_{\mathrm{d}}$ and for $t_{\mathrm{f12}} \ll T_0$ to

$$i_{\mathrm{snSimpl}}(t) = \frac{V_{\mathrm{DC}} - V_{\mathrm{sn0}}}{L_{\mathrm{res}} \omega_0} \sin(\omega_0 t) + \frac{I_{\mathrm{Load}} T_0}{2\pi t_{\mathrm{f23}}} \frac{L_{\mathrm{main}}}{L_{\mathrm{res}}} \sin(\omega_0 (t - t_2)). \tag{3.54}$$

where $T_0 = 2\pi/\omega_0$ is the period of the undamped oscillation and $\frac{L_{\mathrm{main}}}{L_{\mathrm{res}}}$ considers the capability of the snubber path to provide steep current slopes.
(3.53) results in a snubber voltage change within the first and second interval calculable with

$$\begin{aligned} \Delta v_{\mathrm{sn}}(t_3) = {} & A_0 L_{\mathrm{res}} \left[1 - e^{-\delta t_3} \left(\frac{\delta}{\omega_{\mathrm{d}}} \sin(\omega_{\mathrm{d}} t_3) + \cos(\omega_{\mathrm{d}} t_3) \right) \right] \\ & + \frac{I_{\mathrm{Load}}}{t_{\mathrm{f23}}} \left[\left(L_{\mathrm{main}} - \frac{2\delta}{\omega_0^2} R_{\mathrm{main}} \right) \left(1 - e^{-\delta t_{\mathrm{f23}}} \cos(\omega_{\mathrm{d}} t_{\mathrm{f23}}) \right) \right] \\ & - \frac{I_{\mathrm{Load}}}{t_{\mathrm{f23}}} \left[\left(\frac{R_{\mathrm{main}}}{\omega_0^2} \left(\omega_{\mathrm{d}} - \frac{\delta^2}{\omega_{\mathrm{d}}} \right) + \frac{\delta}{\omega_{\mathrm{d}}} L_{\mathrm{main}} \right) e^{-\delta t_{\mathrm{f23}}} \sin(\omega_{\mathrm{d}} t_{\mathrm{f23}}) \right] + R_{\mathrm{main}} I_{\mathrm{Load}}. \end{aligned} \tag{3.55}$$

It should be mentioned that (3.53) may result in a negative value at t_2 in case the initial snubber voltage and hence the stored energy is comparatively high. This effect is further discussed in Section 4.5.

Interval $t_3 \leq t < t_4$
To calculate the snubber current in the final interval, the following equation can be used.

$$\begin{aligned} i_{\mathrm{sn}}(t) = & \frac{A_0}{\omega_{\mathrm{d}}} e^{-\delta t} \sin(\omega_{\mathrm{d}} t) \\ & + R_{\mathrm{main}} C_{\mathrm{sn}} \frac{I_{\mathrm{Load}}}{t_{\mathrm{f23}}} \left[e^{-\delta(t-t_3)} \cos(\omega_{\mathrm{d}}(t-t_3)) - e^{-\delta(t-t_2)} \cos(\omega_{\mathrm{d}}(t-t_2)) \right] \\ & + \frac{I_{\mathrm{Load}}}{\omega_{\mathrm{d}} t_{\mathrm{f23}}} \left(\frac{L_{\mathrm{main}}}{L_{\mathrm{res}}} - \delta R_{\mathrm{main}} C_{\mathrm{sn}} \right) \\ & \cdot \left[e^{-\delta(t-t_2)} \sin(\omega_{\mathrm{d}}(t-t_2)) - e^{-\delta(t-t_3)} \sin(\omega_{\mathrm{d}}(t-t_3)) \right]. \end{aligned} \tag{3.56}$$

This equation becomes zero at the end of the interval and the turn-off point in time of Q_{aux} which is calculated by

$$\Delta t_4 = \frac{\arctan\left(-\frac{A_{1\mathrm{t4}}}{A_{2\mathrm{t4}}}\right)}{\omega_{\mathrm{d}}} \tag{3.57}$$

or considering the periodic behavior of tangents with

$$t_4 = \frac{\arctan\left(-\frac{A_{1\mathrm{t4}}}{A_{2\mathrm{t4}}}\right)}{\omega_{\mathrm{d}}} + \frac{\pi}{\omega_{\mathrm{d}}} \tag{3.58}$$

respectively. The two constant values are

$$\begin{aligned} A_{1\mathrm{t4}} = & \omega_{\mathrm{d}} R_{\mathrm{main}} C_{\mathrm{sn}} \left(e^{\delta t_3} \cos(\omega_{\mathrm{d}} t_3) - e^{\delta t_2} \cos(\omega_{\mathrm{d}} t_2) \right) \\ & + \left(\frac{L_{\mathrm{main}}}{L_{\mathrm{res}}} - \delta R_{\mathrm{main}} C_{\mathrm{sn}} \right) \left(e^{\delta t_3} \sin(\omega_{\mathrm{d}} t_3) - e^{\delta t_2} \sin(\omega_{\mathrm{d}} t_2) \right) \quad \text{and} \end{aligned} \tag{3.59}$$

$$\begin{aligned} A_{2\mathrm{t4}} = & \omega_{\mathrm{d}} R_{\mathrm{main}} C_{\mathrm{sn}} \left(e^{\delta t_3} \sin(\omega_{\mathrm{d}} t_3) - e^{\delta t_2} \sin(\omega_{\mathrm{d}} t_2) \right) \\ & A_0 \frac{t_{\mathrm{f23}}}{I_{\mathrm{Load}}} + \left(\frac{L_{\mathrm{main}}}{L_{\mathrm{res}}} - \delta R_{\mathrm{main}} C_{\mathrm{sn}} \right) \left(e^{\delta t_2} \cos(\omega_{\mathrm{d}} t_2) - e^{\delta t_3} \cos(\omega_{\mathrm{d}} t_3) \right). \end{aligned} \tag{3.60}$$

However, in case (3.53) is negative at t_2, (3.60) and (3.58) yield in the first zero crossing of the snubber current. In this case, the current is not interrupted by the auxiliary switch channel but continuous flowing through its body diode leading to an interval enlarged by another half of an oscillation as shown in Section 4.5.
Further, (3.58) with (3.60) show that t_4 is a function of the load current as well as the choosen value of t_2 in the controller. The arcus tangens function may cause a pole in the range in which the load current can vary, whose variance is influenced by choosing t_2, cf. Fig. 3.5.

Figure 3.5 shows that there is a point in time t_2 at which the end of the interval becomes approximately independent over a wide range of the load current, see $t_2 = 157\,\mathrm{ns}$ for an exemplary chosen setup as described in Sect. 4.1. A dependence on the load current is very undesirable because a varying t_4 requires continuous adjustments of the gate signal timing of Q_{aux} to achieve zero current turn-off. By knowledge of the optimal $t_2 = t_{2\mathrm{opt}}$, a fixed timing can be used. This strongly reduces the controlling effort for a

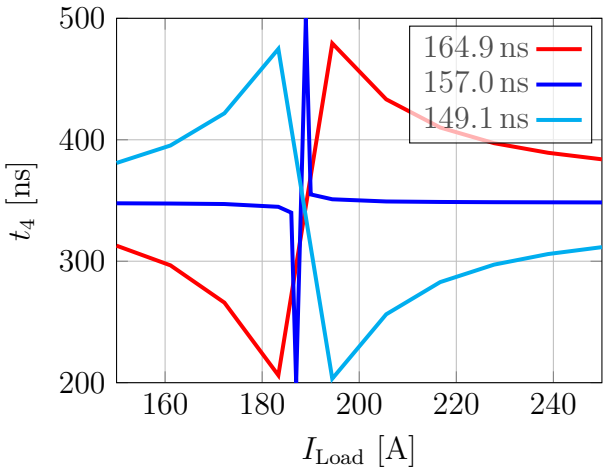


Figure 3.5: t_4 as a function of I_{Load} and t_2

zero current switching of Q_{aux}. However, in Section 4.8 it will be shown that at a load current approximately equal to I_{rrm}, cf. Fig. 4.20, the snubber current $i_{\mathrm{sn}}(t_3)$ is almost zero and thus, the snubber current in the complete interval $t_3 \leq t < t_4$ is also small. Hence, the turn-off losses of Q_{aux} are still very small, even if t_2 is not adjusted according to $t_{2\mathrm{opt}}$.
This optimal t_2, where t_4 becomes current independent occurs in case $A_{2\mathrm{t}4}$ becomes zero. This can be achieved by setting t_2 to

$$\begin{aligned} t_{2\mathrm{opt}} &= \arctan\left(\frac{-e^{\delta t_{\mathrm{f23}}}\left\{K_{\mathrm{t2opt}}\cos(\omega_{\mathrm{d}} t_{\mathrm{f23}}) + \sin(\omega_{\mathrm{d}} t_{\mathrm{f23}})\right\} + K_{\mathrm{t2opt}}}{e^{\delta t_{\mathrm{f23}}}\left\{\cos(\omega_{\mathrm{d}} t_{\mathrm{f23}}) - K_{\mathrm{t2opt}}\sin(\omega_{\mathrm{d}} t_{\mathrm{f23}})\right\} - 1}\right)/\omega_{\mathrm{d}} \\ &\approx \frac{\pi}{2\omega_{\mathrm{d}}} - t_{\mathrm{f23}}, \end{aligned} \tag{3.61}$$

with

$$K_{\mathrm{t2opt}} = \frac{\omega_{\mathrm{d}} R_{\mathrm{main}}}{L_{\mathrm{main}}\omega_0^2 - \delta R_{\mathrm{main}}}. \tag{3.62}$$

To calculate the snubber voltage change over all three intervals, the equation

$$\begin{aligned} \Delta v_{\mathrm{sn}}(t) =& A_0 L_{\mathrm{res}}\left[1 - e^{-\delta t_4}\left(\frac{\delta}{\omega_{\mathrm{d}}}\sin(\omega_{\mathrm{d}} t_4) + \cos(\omega_{\mathrm{d}} t_4)\right)\right] + R_{\mathrm{main}} I_{\mathrm{Load}} \\ &+ \frac{I_{\mathrm{Load}}}{\omega_0^2 t_{\mathrm{f23}}}\left[\left(\omega_{\mathrm{d}} R_{\mathrm{main}} + \frac{\delta}{\omega_{\mathrm{d}}} L_{\mathrm{main}}\omega_0^2 - \frac{\delta^2}{\omega_{\mathrm{d}}} R_{\mathrm{main}}\right)\right. \\ &\cdot \left\{e^{-\delta(t_4 - t_3)}\sin(\omega_{\mathrm{d}}(t_4 - t_3)) - e^{-\delta(t_4 - t_2)}\sin(\omega_{\mathrm{d}}(t_4 - t_2))\right\} \\ &+ (L_{\mathrm{main}}\omega_0^2 - 2\delta R_{\mathrm{main}}) \\ &\left.\cdot \left\{e^{-\delta(t_4 - t_3)}\cos(\omega_{\mathrm{d}}(t_4 - t_3)) - e^{-\delta(t_4 - t_2)}\cos(\omega_{\mathrm{d}}(t_4 - t_2))\right\}\right] \end{aligned} \tag{3.63}$$

can be used. This equation simplifies in case t_2 is chosen according to (3.61) and for current fall times much smaller than half of the oscillation period to

$$\begin{aligned} \Delta v_{\mathrm{sn}}(t) \approx& A_0 L_{\mathrm{res}}\left(1 + e^{-\delta t_4}\right) + R_{\mathrm{main}} I_{\mathrm{Load}} + \frac{I_{\mathrm{Load}}}{\omega_0^2 t_{\mathrm{f23}}}(L_{\mathrm{main}}\omega_0^2 - 2\delta R_{\mathrm{main}}) \\ &\cdot \left(e^{-\delta(t_4 - t_3)}\cos(\omega_{\mathrm{d}}(t_4 - t_3)) - e^{-\delta(t_4 - t_2)}\cos(\omega_{\mathrm{d}}(t_4 - t_2))\right). \end{aligned} \tag{3.64}$$

And with equal conditions, (3.59) and (3.60) can be approximated to

$$A_{1t4} \approx -\omega_d R_{main} C_{sn} e^{\delta t_2} \cos(\omega_d t_2) + \left(\frac{L_{main}}{L_{res}} - \delta R_{main} C_{sn}\right)\left(e^{\delta t_3} - e^{\delta t_2}\sin(\omega_d t_2)\right), \quad (3.65)$$

$$A_{2t4} \approx \omega_d R_{main} C_{sn}\left(e^{\delta t_3} - e^{\delta t_2}\sin(\omega_d t_2)\right) + A_0 \frac{t_{f23}}{I_{Load}} + \left(\frac{L_{main}}{L_{res}} - \delta R_{main} C_{sn}\right) e^{\delta t_2}\cos(\omega_d t_2). \quad (3.66)$$

(3.58) and (3.63) allow the calculation of the snubber voltage at the end of the switching event by knowledge of the system without the need of successive calculation of all intervals. The end value of the snubber voltage can now be calculated with

$$v_{sn}(t_4) = V_{snMaxOff} = V_{sn0} + \Delta v_{sn} \quad (3.67)$$

This eases the estimation of the snubber voltage evolvement in terms of stability together with the turn-on model previously derived as it is done in Chapter 4.

4 Model Validation and Application

As first proposed by [118] for $V_{\mathrm{DC}} = 600\,\mathrm{V}$, in this chapter the model previously derived shall be validated by measurements. First, three similar setups are described, a conventional halfbridge, a halfbridge with DC-snubber as well as a setup with the active snubber. Latter is used for model validation in this Chapter. The halfbridge and DC-snubber module are just introduced but not used until Chapter 5 for system benchmark. The turn-on and turn-off model are compared at higher load currents to the model with a value above the reverse recovery peak as well as with lower load current values.

Further, the presented model is used to predict the behavior of a real application with continuous subsequent switching events. The two single models for turn-on and turn-off, will be alternately calculated to predict a sequence of switching events. In contrast to a real setup, the DC-link voltage is assumed to be time invariant at a value of $V_{\mathrm{DC}} = 750\,\mathrm{V}$. Further, the load current is modeled as a continuous output current. Hence, a ripple voltage and ripple current are not considered. Hence, a varying duty-cycle at constant load current can be neglected as well.
In addition to analyzing the stability of the operation, further goals of these sections are the analysis of damping losses and the comparison with expectable DC-snubber damping losses in a similar operation.

4.1 Module Assembly and Measurement Description

In this section the assembly, components and parameters of the mentioned three very similar power modules are introduced.
As described in detail in Section 2.5, real capacitors are complex components which have to be selected carefully to be the best choice for a given application. In Section 2.4 equivalent circuits for DC-snubber were presented and an exemplary estimation for the damping losses are given, cf. Fig. 2.13. It has been stated that for a minimal stray inductance relevant for turn-off commutation the capacitor must be connected as close as possible to the switching semiconductor. In Section 2.2.1, it is further described that with flat conductors placed in parallel with the wide side in close proximity to each other a minimum inductance can be achieved. Furthermore, the proximity effect on copper substrates lead to an opposite directed current in fully plated copper backside, which equals the previously mentioned bus-bar conductor structure. Hence, the best capacitor placement is directly at the copper substrate in close proximity to the semiconductor.
To ease the comparison, all setups are designed to be equal except the availability of a snubber path on ceramic substrate level to equip the DC and the active snubber. All setups are operated with the same DC-link capacitor and module connection and hence, with equal L_{main}.

4.1.1 Capacitor Selection

Due to the power module manufacturing processes e.g. with soldering at high temperature, polarized electrolytic and metallized polypropylene film capacitors cannot be used.

As a result, ceramic capacitors are the only suitable choice for this application. However, the development of a low inductive connection element to connect a capacitor after the critical assembly processes have taken place may offer other opportunities for capacitor device choice.
According to (2.30), a snubber voltage change below 150 V at a peak load current of 350 A yields in a minimum capacitance of at least

$$C_{\mathrm{sn}} = 37\,\mathrm{nH}\left(\frac{350\,\mathrm{A}}{150\,\mathrm{V}}\right)^2 = 201\,\mathrm{nF}. \tag{4.1}$$

As mentioned in Section 2.5.2 class I dielectrics are linear and temperature independent. Class II materials have higher relative permeability but suffer from highly voltage and temperature dependent parameter change. To find a good fit for this application, a class I capacitance with four parallel C0G ceramic capacitors each $C_{\mathrm{nom}} = 39\,\mathrm{nF}$ forming a 'capacitor assembly' is compared with a class II antiferroelectric capacitor with $C_{\mathrm{nom}} = 250\,\mathrm{nF}$ and $V_{\mathrm{nom}} = 900\,\mathrm{V}$.

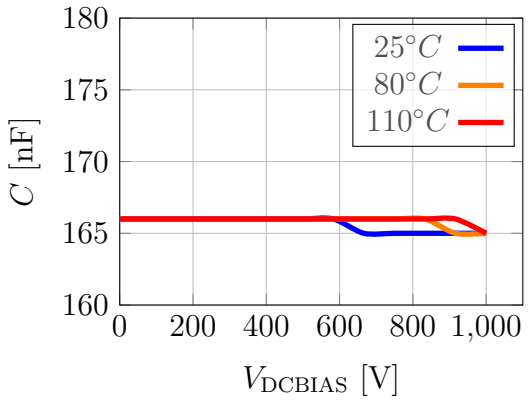


Figure 4.1: Class I: C_{DUT} as a function of V and ϑ at 2 MHz

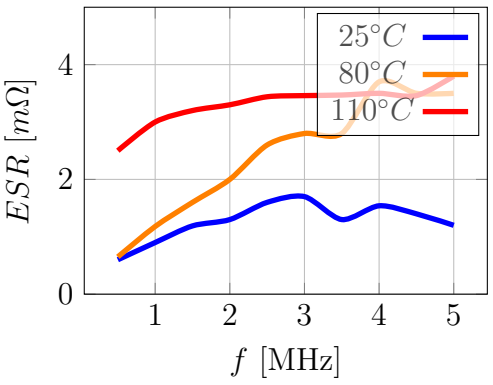


Figure 4.2: Class I: ESR as a function of f and ϑ at 500 VDC

In Figure 4.1 the capacitance value of the class I capacitor assembly as the device under test (DUT) is shown. It can be seen that its capacitance is slightly higher compared to the sum of the four paralleled capacitors of 156 nF. Additionally, the series resistor, cf. Fig. 4.2, is very small within the interesting frequency range.

Contrary to the class I capacitor, the class II capacitor shows a capacitance below the specified value of 250 nF, cf. Fig. 4.3. Additionally, its capacitance indicates a strong dependence on temperature and DC-link voltage. Assuming an application with variable DC-link voltage, e.g. in a battery driven electric car in the range of 400 V to 900 V, its capacitance can vary from 70 nF to 130 nF. Together with the system stray inductance of 37 nH a resonant frequency range of 2.3 MHz to 3.1 MHz occurs.
By analyzing the ESR, cf. Fig. 4.4, its resistance is much higher compared to the class I capacitor. Additionally, its characteristic shows distinct piezo-electric resonances especially in the expected frequency range. According to Sect. 2.5, these results are plausible due to the anti-ferroelectric characteristic of the used capacitor leading to piezo resonances. Further, the lower capacitance might be explained by the measurement principle where a very small AC measurement voltage of 250 mV was used. Therefore, a higher

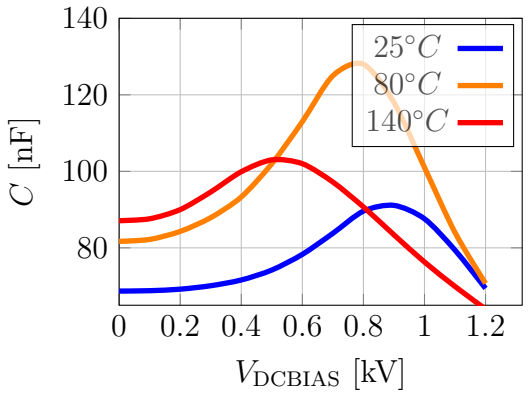


Figure 4.3: Class II: C_{DUT} as a function of V and ϑ at 2 MHz

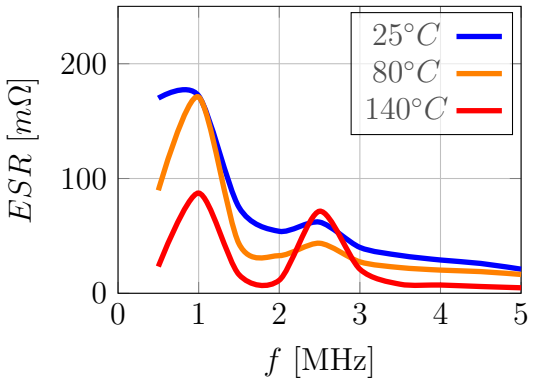


Figure 4.4: Class II: ESR as a function of f and ϑ at 500 VDC

AC-amplitude as it occurs in the target snubber application may lead to a higher number of flipped polarized areas, cf. Fig. 2.15, but also higher hysteresis losses, cf. Fig. 2.16, leading to a higher ESR than measured.
Hence, the class I capacitor is a more reasonable choice in terms of expected capacitor losses, temperature increase and frequency stability.

4.1.2 Conventional Halfbridge

In Figure 4.5, the substrate layout for the conventional halfbridge is shown as also described in [117]. The power terminals, AC and DC+/-, are placed in the middle to ensure a vertical symmetry axis. The distance between the DC+ and DC- terminal is chosen to get a deliberately large stray inductance L_{main}, which is assumed to be beneficial for the active snubber setup and further discussed in Sect. 5.3.3. This results in an effective stray inductance concerning DC-link capacitor and connection similar to $L_{\sigma\mathrm{On}}$ of 37 nH. The high side switch Q_1 and low side switch Q_2 consist of four parallel silicon carbide MOSFETs with an output capacitance in the investigated voltage range of approximately $C_{\mathrm{oss}} \approx 1\,\mathrm{nF}$ and an on-state resistance of $R_{\mathrm{on}} = 4\,\mathrm{m\Omega}$, see also Figs. 4.9 and 5.36. The parallel die connection is designed according to [11] to improve current symmetry during switching events. An important part of this concept is a symmetric design in combination with a common stray inductance in the gate and load current path by using the bond wires exemplary illustrated as a green box, cf. Fig. 4.5. Indeed, this results in enhanced current symmetry, but also limits the achievable switching speed due to the negative feedback loop.
To measure the DC-link current, a coaxial shunt is used with a bandwidth of 400 MHz and is connected to the DC- terminal. The corresponding gate and drain-source voltages are measured directly on substrate beneath and as close to the MOSFET as possible to reduce ringing and interference due to coupling and common parasitics. A detailed description of the measurement setup can be found in Appendix B.

4.1.3 Halfbridge with DC-Snubber

To get a comparable setup equipped with a DC-snubber, the layout is planned with appropriate soldering points. To maintain symmetry, the DC-snubber has been split into

two paralleled capacitor groups leading to a total snubber capacitance with the chosen device of 330 nF.
Because the snubber capacitor will provide a major part of the commutation current, see also [117], the used coaxial shunt in the DC-minus terminal to measure i_{link}, cf. e.g. Fig. 3.4, will not measure the correct value of the drain-source current. Due to the complex parallel connection of the four dies, a direct measurement of i_{D2} is not feasible. Hence, to obtain the drain-source current, the snubber current i_{sn2} within one snubber path is measured with a 30 MHz Rogowski coil in the bond wires, see also Fig. B.2.2. Due to the vertical symmetry, the drain-source current can be calculated with i_{link} and the current within one snubber path to

$$i_{\text{D2}} = i_{\text{link}} - 2 \cdot i_{\text{sn2}}. \tag{4.2}$$

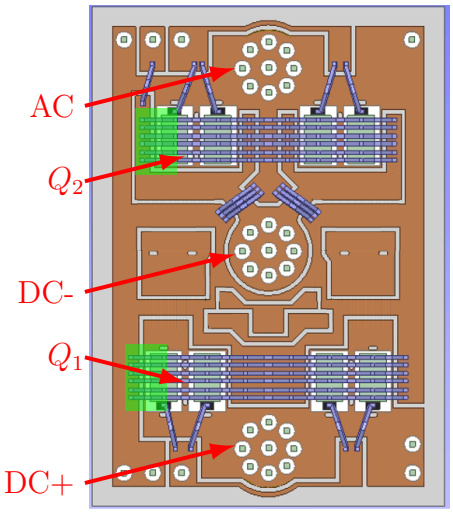


Figure 4.5: Conventional halfbridge

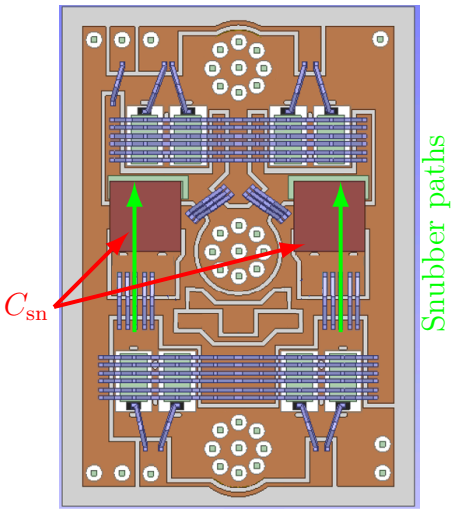


Figure 4.6: Halfbridge with DC-snubber

The inductance of the two coupled snubber paths over the power switches result in the effective stray inductance L_{snhb}, which is equal to the commutation relevant stray inductance $L_{\sigma\text{Off}}$ according to (3.4). This value has been simulated with Ansys Q3D extractor to be 3 nH.
The characteristic parameters relevant for model validation are obtained by analyzing the exponentially damped oscillation after a switching event. The well-known mathematical description

$$i_{\text{sn}}(t) = I_0 \cdot e^{\delta t} \cdot cos(\omega_{\text{d}} t) \tag{4.3}$$

has been fitted to the measured signal. From the fit, the characteristic parameters

$$\delta = \frac{R_{\text{d}}}{2L_{\text{res}}} = 662 \cdot 10^3\,1/\text{s} \quad \text{and} \tag{4.4}$$

$$\omega_{\text{d}} = \sqrt{\omega_0^2 - \delta^2} = 9.03 \cdot 10^6\,1/\text{s}, \tag{4.5}$$

were obtained and allow to calculate the values of the necessary parameters as

$$\omega_0 = \frac{1}{\sqrt{L_{\text{res}} C_{\text{sn}}}} = 9.05 \cdot 10^6\,1/\text{s}, \tag{4.6}$$

$$f_0 = \frac{1}{2\pi\sqrt{L_{\text{res}} C_{\text{sn}}}} = 1.44\,\text{MHz}, \tag{4.7}$$

$$L_{\text{res}} = L_{\text{main}} + L_{\text{sn}} = 37\,\text{nH}, \tag{4.8}$$

$$R_{\text{d}} = R_{\text{main}} + R_{\text{sn}} = 49\,\text{m}\Omega, \tag{4.9}$$

$$L_{\text{main}} \approx L_{\text{res}} - L_{\text{sn}} = 34\,\text{nH} \quad \text{and} \tag{4.10}$$

$$R_{\text{main}} = R_{\text{d}} - R_{\text{sn}} = 45\,\text{m}\Omega. \tag{4.11}$$

This method allows the determination of the effective parameters especially the relevant damping resistance distributed over the total oscillation path including DC-link capacitor and its connection to the power module.

4.1.4 Halfbridge with Active Snubber

The halfbridge with active snubber is very similar to the halfbridge with DC-snubber including the same type and size of used capacitor, similarly presented in [117]. In series to each of the two snubber paths a SiC MOSFET is placed as auxiliary switch Q_{aux} of equal type as the used power switches. These dies are connected without a common stray inductance in the gate and load current path to achieve maximum switching speed. However, as it will be shown on pages 66ff., the losses of Q_{aux} are very small and thus, the size of these two dies can be reduced.

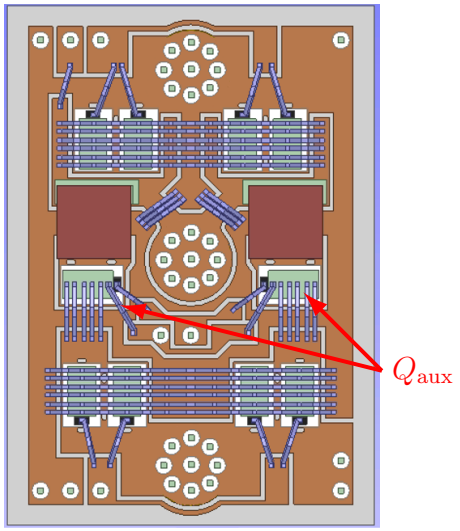


Figure 4.7: Halfbridge with active snubber

The gate and source pin for controlling Q_{aux} are placed in that manner that the magnetic field during commutation and oscillation caused by the DC-link current between the DC+ and DC- pin does not induce voltage in the gate circuit.

Because the geometry differs from the DC-snubber substrate only by the die-thickness, the stray inductance of 3 nH remains valid. It has to be mentioned that the resistance of the snubber path R_{sn}, cf. Fig. 3.4, now includes the resistance of the snubber capacitors of up to $ESR = 4\,\text{m}\Omega$ as well as the on-state resistance of the auxiliary switch of approximately $R_{\text{onAux}} = 10\,\text{m}\Omega$ leading to a higher damping resistance of

$$R_{\text{d}} = 59\,\text{m}\Omega. \tag{4.12}$$

4.2 Turn-On Model Validation for High Operation Currents

The turn-on model derived in Section 2.3.1 is used to calculate the current waveform, see [118]. The calculated values are compared to measurements performed with the setup described in Section 4.1.4 at a DC-link voltage of $V_{\mathrm{DC}} = 750\,\mathrm{V}$ and a constant load current of $I_{\mathrm{Load}} = 350\,\mathrm{A}$. According to (3.18) and (3.2) to (3.3) as well as the measured parameters in Sections 4.1.3ff., the main stray inductance relevant for turn-on is $L_{\sigma\mathrm{On}} = L_{\mathrm{main}} = 34\,\mathrm{nH}$. Further, the resistance relevant for damping R_{d} equals to $59\,\mathrm{m\Omega}$.
The measurement is depicted in Fig. 4.8 with the points in time according to Fig. 3.2.

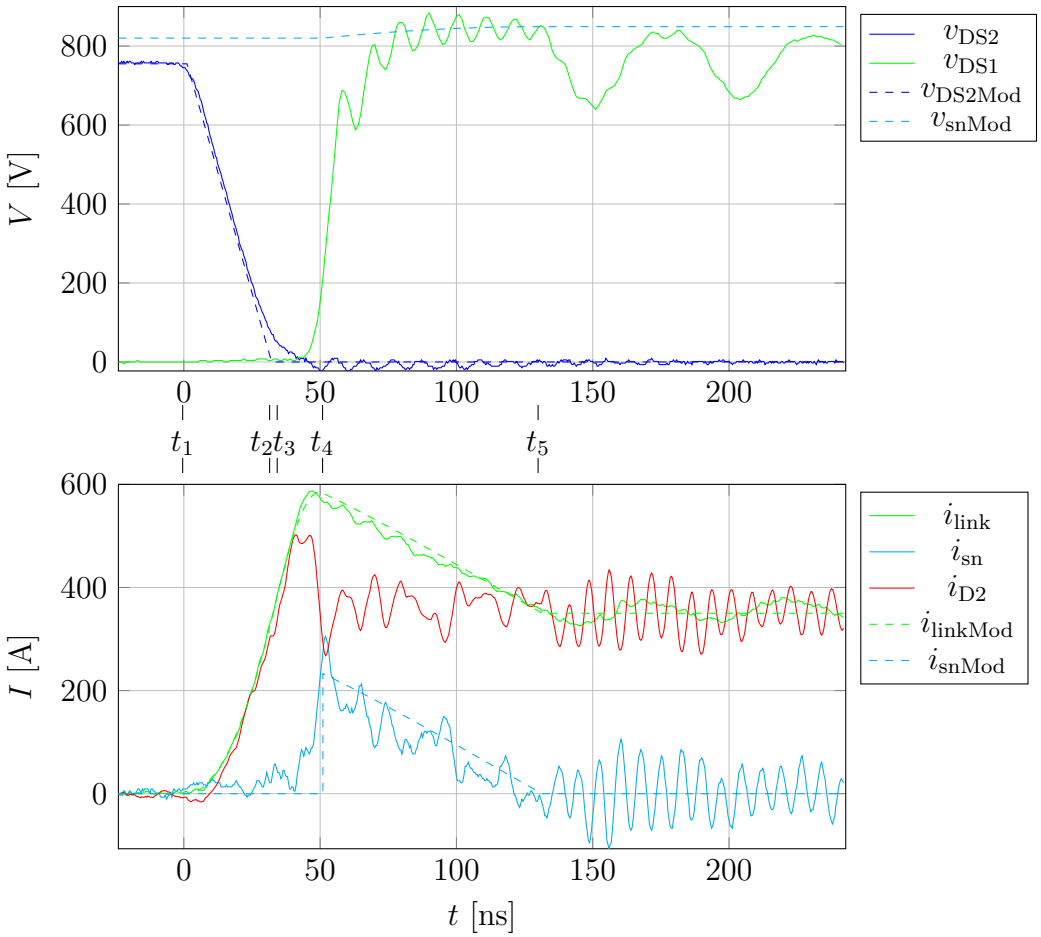


Figure 4.8: Turn-on event for a load current of 350 A at a DC-link voltage of 750 V with measured values (solid) and calculated values (dashed)

Interval $t_1 \leq t < t_2$
At $t = t_1$ the drain-source voltage of Q_2 starts decreasing, cf. Fig. 4.8. As it can be seen, the linear approximation of the voltage slope, cf. v_{DS2Mod}, shows adequate accuracy to model the measured signal. The duration of the modeled voltage slope is adjusted manually to a value of $t_{\mathrm{f12}} = t_2 - t_1 = 31\,\mathrm{ns}$ to fit to the measurements. During this interval, the voltage drop over the main stray inductance v_{Lmain} and the corresponding resistance v_{Rmain} increases, cf. Fig. 3.4. Thus, the drain-source voltage of the blocking

auxiliary switch v_{DSaux} increase, too. According to (3.20), the parameter δ_{14} for the first order differential equation can be calculated to

$$\delta_{14} = \frac{45\,\mathrm{m\Omega}}{2 \cdot 34\,\mathrm{nH}} = 661 \cdot 10^3\,1/\mathrm{s}. \tag{4.13}$$

This parameter allows to calculate the DC-link current at $t = t_2$ with (3.19)

$$i_{\mathrm{link}}(t_2) = \frac{750\,\mathrm{V}}{31\,\mathrm{ns} \cdot 45\,\mathrm{m\Omega}} \left(\frac{1}{2 \cdot 661 \cdot 10^3\,1/\mathrm{s}} (e^{-2 \cdot 661 \cdot 10^3\,1/\mathrm{s} \cdot 31\,\mathrm{ns}} - 1) + 31\,\mathrm{ns} \right) = 337\,\mathrm{A}. \tag{4.14}$$

Interval $t_2 \leq t < t_3$

Because this value according (4.14) is below the load current of 350 A, (3.22) can be used for calculation of t_3 when i_{link} becomes the load current I_{Load}

$$t_3 = \frac{-\ln\left(\frac{(\frac{350\,\mathrm{A} \cdot 45\,\mathrm{m\Omega}}{750\,\mathrm{V}} - 1) 2 \cdot 661 \cdot 10^3\,1/\mathrm{s} \cdot 31\,\mathrm{ns}}{1 - e^{+2 \cdot 661 \cdot 10^3\,1/\mathrm{s} \cdot 31\,\mathrm{ns}}} \right)}{(2 \cdot 661 \cdot 10^3\,1/\mathrm{s})} = 31.6\,\mathrm{ns}. \tag{4.15}$$

Interval $t_3 \leq t < t_4$

In the subsequent interval until $t = t_4$, the main stray inductance L_{main} resonates with the output capacitance of the passive switch Q_1. As mentioned on page 39, the various dependencies of the diode behavior are modeled with a linear capacitance larger than the measured output capacitance of the switch adjusted to be $C_{\mathrm{oss}*} = 3.5\,\mathrm{nF}$ to include the measured reverse recovery charge. This characteristic parameters of the resonant circuit can be calculated to

$$\omega_{034} = \frac{1}{\sqrt{34\,\mathrm{nH} \cdot 3.5\,\mathrm{nF}}} = 91.67 \cdot 10^6\,1/\mathrm{s} \quad \text{and} \tag{4.16}$$

$$\omega_{\mathrm{d34}} = \sqrt{(91.67 \cdot 10^6\,1/\mathrm{s})^2 - 661 \cdot 10^3\,1/\mathrm{s}^2} = 91.67 \cdot 10^6\,1/\mathrm{s}, \tag{4.17}$$

which indicate a high quality oscillation with negligible damping due to $\omega_{034} \approx \omega_{\mathrm{d34}}$.

Comparing the current waveforms in Figure 4.8 with the idealized waveform in Figure 3.2 an increasing snubber current i_{sn} can be noticed at approximately t_3. As it is shown in Figure 3.2, the increasing drain-source voltage of the passive switch v_{DS1} lead to a decreasing voltage at the auxiliary switch v_{DSaux}. While the output capacitance of the auxiliary switch at high drain-source voltages can be neglected for the sake of a manageable model, it becomes larger at lower voltages, cf. Fig. 4.9. The voltage dependency of the output capacitance causes a significant increase of the capacitance at lower voltages. Due to this increase, the output capacitance of Q_{aux} influences the circuit very similar to a small DC-snubber, which is discharged by the commutation current of Q_1. Thus, v_{DS1} rises to this voltage lower than V_{DC} and follows the charging process afterwards. This effect can be noticed in v_{DS1} for $t > 60\,\mathrm{ns}$ in Figure 4.8.

Further, the output capacitance of the auxiliary switch causes a displacement current which is not modeled, cf. i_{snMod}. This displacement current makes the statement that A_{34} is equal to the reverse recovery peak I_{rrm}, p. 41, invalid as it can be noticed in Figure 4.8 by comparing i_{link} and i_{D2} at t_4. Due to the fact that the output capacitance of Q_{aux} is not included in the model and its prediction of i_{link} fits very well to the measurement, it can be concluded that the displacement current of the output capacitance of Q_{aux} measured in the snubber current, actively reduces the reverse recovery current peak under

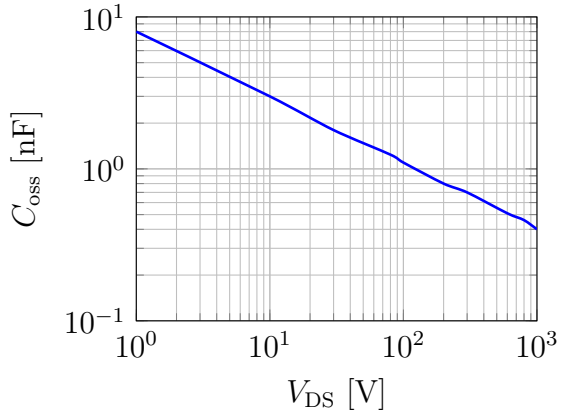


Figure 4.9: C_{oss} of the used SiC-MOSFET dies as a function of v_{DS}

consideration of (4.2). To not violate the rule of charge conservation, this means that the slope of v_{DS1} is reduced. However, the snubber current has been measured using a state-of-the-art Rogowski coil with a bandwidth of 30 MHz. Assuming a first order low-pass characteristic of the Rogowski coil, the resolvable rise-time can be calculated according to [125] p. 30, to be

$$t_{\text{riseMax}} = \frac{0.35}{f_{\text{BW}}} = \frac{0.35}{30\,\text{MHz}} = 11.7\,\text{ns}. \tag{4.18}$$

This is close to the time in which the displacement current in the measured i_{sn} rises. Hence, the measured snubber current slope i_{sn} right before t_4 might be affected by the Rogowski coil and considering (4.2), i_{D2} with the reverse recovery current, too.
With a snubber capacitor, precharged due to previous switching events in the double pulse measurement, the initial snubber voltage V_{sn0} equals 820 V. This enables the calculation of the point in time t_4 at which the auxiliary switch sees a negative drain-source voltage and its body diode becomes conductive. With (3.30) and (3.31), t_4 can be calculated to

$$K = \frac{(750\,\text{V} - 820\,\text{V} - 45\,\text{m}\Omega \cdot 350\,\text{A})\, 2 \cdot 661 \cdot 10^3\,1/\text{s} \cdot 31\,\text{ns}}{750\,\text{V}(e^{-2 \cdot 661 \cdot 10^3\,1/\text{s} \cdot 0.6\,\text{ns}} - e^{-2 \cdot 661 \cdot 10^3\,1/\text{s} \cdot 31.6\,\text{ns}})} = -0.117, \tag{4.19}$$

$$t_4 = \frac{\arccos(K)}{91.67 \cdot 10^6\,1/\text{s}} + 31.6\,\text{ns} = 50\,\text{ns}. \tag{4.20}$$

Now the DC-link current at t_4 can be calculated. This value can be obtained according (3.27) and (3.28) yielding

$$\begin{aligned} A_{34} &= \frac{750\,\text{V}}{31\,\text{ns} \cdot 45\,\text{m}\Omega \cdot 91.67 \cdot 10^6\,1/\text{s}} \left(e^{-2 \cdot 661 \cdot 10^3\,1/\text{s} \cdot 0.6\,\text{ns}} - e^{-2 \cdot 661 \cdot 10^3\,1/\text{s} \cdot 24.6\,\text{ns}}\right) \\ &= 235.6\,\text{A} \quad \text{and} \end{aligned} \tag{4.21}$$

$$\begin{aligned} i_{\text{link}}(t_4) &= A_{34} e^{-661 \cdot 10^3\,1/\text{s} \cdot 18.4\,\text{ns}} \sin(91.67 \cdot 10^6\,1/\text{s} \cdot 18.4\,\text{ns}) + 350\,\text{A} \\ &= 581\,\text{A}. \end{aligned} \tag{4.22}$$

For further calculations, the load current must be subtracted from the DC-link current to obtain the AC-part of

$$i_{\text{linkAC}}(t_4) = 231\,\text{A} \tag{4.23}$$

Interval $t_4 \leq t < t_5$

For $t = t_4$, when the body diode of Q_{aux} becomes conductive, two additional oscillation circuits are formed. One is opened between the output capacitance of the passive switch $C_{\text{oss1}} \approx 1\,\text{nF}$ and the snubber path with an inductance of $L_{\text{snhb}} = 3\,\text{nH}$ leading to a high frequency oscillation of

$$f_{\text{hf}} = \frac{1}{2\pi\sqrt{L_{\text{snhb}} C_{\text{oss1}}}} = 92\,\text{MHz}. \tag{4.24}$$

This can be noticed in v_{DS1}. However, due to the small involved parasitics and the small oscillation amplitude, cf. Fig. 4.8 v_{DS1}, the oscillating energy is also small. Hence, this circuit can be neglected in the model targeting the calculation of damping losses.

A second oscillation circuit is offered through the main stray inductance and the snubber path including the snubber capacitance. Due to the now applicable parasitics according to (4.8) and (4.12) and the measured snubber capacitance of $C_{\text{sn}} = 2 \cdot 165\,\text{nF} = 330\,\text{nF}$ the characteristic parameters of the resonant circuit according (3.34) to (3.36) can now be calculated as

$$\omega_{045} = \frac{1}{\sqrt{37\,\text{nH} \cdot 330\,\text{nF}}} = 9.05 \cdot 10^6\,1/\text{s}, \tag{4.25}$$

$$\delta_{45} = \frac{59\,\text{m}\Omega}{2 \cdot 37\,\text{nH}} = 797 \cdot 10^3\,1/\text{s} \quad \text{and} \tag{4.26}$$

$$\omega_{\text{d45}} = \sqrt{\omega_{045}^2 - \delta_{45}^2} = 9.01 \cdot 10^6\,1/\text{s}. \tag{4.27}$$

This allows to calculate the point in time when the snubber current crosses zero or the DC-link current reaches the load current respectively. According to (3.39) and (3.41), t_5 results in

$$A_{1\text{t5}} = 231\,\text{A} \cdot 9.01 \cdot 10^6\,1/\text{s} \cdot 37\,\text{nH} = 77\,\text{V}, \tag{4.28}$$

$$\begin{aligned} A_{2\text{t5}} =& 750\,\text{V} - 820\,\text{V} + 14\,\text{m}\Omega \cdot 350\,\text{A} \\ & - 37\,\text{nH} \cdot 797 \cdot 10^3\,1/\text{s}(231\,\text{A} + 2 \cdot 350\,\text{A}) = -92.6\,\text{V}, \end{aligned} \tag{4.29}$$

$$t_5 = \frac{\arctan\left(-\frac{77\,\text{V}}{-92.6\,\text{V}}\right)}{9.01 \cdot 10^6\,1/\text{s}} + 50\,\text{ns} = 77\,\text{ns} + 50\,\text{ns} = 127\,\text{ns}, \tag{4.30}$$

which fits very well to the measured curves.

The DC-link current can be calculated with (3.38), (3.37) and the snubber current with (3.42) respectively.

Comparing the modeled DC-link current i_{linkMod} with the measured i_{link}, both currents show a good match in this interval. By comparing the calculated snubber current, the calculated current i_{snMod} also fits to the measured i_{sn} except the neglected higher frequency part according (4.24). This high frequency part does not fit to a clean sinusoidal signal which might be caused by the used Rogowski coil with a bandwidth of approximately one third of the expected frequency of 92 MHz. Additionally, further couplings not included in the model may become relevant at higher frequencies and promote complex coupled oscillators.

As already mentioned, a resistance can be a function of frequency due to proximity and skin effect. The resistor R_{main}, cf. Fig. 3.4, is measured by analyzing its contribution to the oscillation damping, see Section 4.1.3. According to (4.2), the constant load current as well as the oscillation part i_{sn} is flowing through this resistor. Due to the frequency

dependence, the value of R_{main} seen by the constant load current, is very small contrary to its value seen by the alternating part. As a result, only the alternating part results in notable losses due to damping. The total damping power losses are obtained by multiplying the squared calculated snubber current in the interval $t_4 \leq t < t_5$ by the damping resistance leading to an energy of

$$W_{\text{dampOn}} = R_{\text{d}} \cdot \int_{t_4}^{t_5} i_{\text{snMod}}^2 dt = 89\,\mu\text{J}. \tag{4.31}$$

The snubber capacitor is charged by the energy stored in the stray inductance present at $t = t_4$ as well as the energy provided by the DC-link capacitor except the energy damped in the high frequency oscillation. This leads to an increased snubber voltage as it can be calculated according to (3.43) to (3.45) as shown below

$$\begin{aligned} A_{45\text{Vsn1}} =& \frac{231\,\text{A} + 2 \cdot 350\,\text{A}}{9.01 \cdot 10^6\,1/\text{s} \cdot 330\,\text{nF}} - 2 \cdot 9.01 \cdot 10^6\,1/\text{s} \cdot 37\,\text{nH} \cdot 350\,\text{A} \\ & - \frac{797 \cdot 10^3\,1/\text{s}}{9.01 \cdot 10^6\,1/\text{s}} (750\,\text{V} - 820\,\text{V} + 14\,\text{m}\Omega \cdot 350\,\text{A}) = 85.7\,\text{V}, \end{aligned} \tag{4.32}$$

$$A_{45\text{Vsn2}} = 750\,\text{V} - 820\,\text{V} - 45\,\text{m}\Omega \cdot 350\,\text{A} = -85.8\,\text{V} \quad \text{and} \tag{4.33}$$

$$\begin{aligned} \Delta v_{\text{sn}} =& A_{45\text{Vsn1}} \cdot e^{-797 \cdot 10^3\,1/\text{s} \cdot 77\,\text{ns}} \cdot \sin(9.01 \cdot 10^6\,1/\text{s}(t - t_4)) \\ & + A_{45\text{Vsn2}} \cdot \left(1 - e^{-797 \cdot 10^3\,1/\text{s} \cdot 77\,\text{ns}} \cos(9.01 \cdot 10^6\,1/\text{s} \cdot 77\,\text{ns})\right) = 28\,\text{V}. \end{aligned} \tag{4.34}$$

This results in a maximum snubber voltage of $V_{\text{snMaxOn}} = V_{\text{sn0}} + \Delta v_{\text{sn}} = 848\,\text{V}$.
Alternatively, V_{snMaxOn} can be roughly estimated as follows. Approximating the snubber current as linear decreasing, the energy provided by the DC-link can be estimated to

$$W_{\text{link}} = 0.5 \cdot i_{\text{linkAC}}(t_4) \cdot V_{\text{DC}} \cdot (t_5 - t_4) = 0.5 \cdot 231\,\text{A} \cdot 750\,\text{V} \cdot 77\,\text{ns} = 6.67\,\text{mJ}. \tag{4.35}$$

With the initial energy in the snubber capacitor and the energy in the stray inductance, the equation

$$\frac{1}{2} C_{\text{sn}} V_{\text{snMaxOn}}^2 = \frac{1}{2} C_{\text{sn}} V_{\text{sn0}}^2 + \frac{1}{2} L_{\text{main}} i_{\text{linkAC}}(t_4)^2 + W_{\text{link}}, \tag{4.36}$$

$$= \frac{1}{2} 330\,\text{nF} \cdot (820\,\text{V})^2 + \frac{1}{2} 34\,\text{nH} (231\,\text{A})^2 + 6.67\,\text{mJ} = 118.5\,\text{mJ}, \tag{4.37}$$

can be written. This energy stored in the snubber capacitor after the switching event, results in a snubber voltage of

$$V_{\text{snMaxOn}} = \sqrt{\frac{2 \cdot 118.5\,\text{mJ}}{330\,\text{nF}}} = 847.5\,\text{V}, \tag{4.38}$$

which is very similar to the value of $V_{\text{snMaxOn}} = 848\,\text{V}$ calculated with the model.

Interval $t \geq t_5$
At $t = t_5$, v_{DSaux} becomes zero and the body diode of Q_{aux} starts blocking. As a result, the snubber path is disconnected and the effective stray inductance becomes L_{main} as defined in (4.10), see also Fig. 3.4). Because C_{oss} of the high-side switch is charged to a voltage $v_{\text{DS1}} > V_{\text{DC}}$, it starts oscillating with $L_{\sigma\text{On}}$. From Fig. 4.9 the output capacitance of a single chip can be obtained as 480 pF and with four chips in parallel for Q_1, the oscillation period can be calculated to

$$T_{\text{osc}} = 2\pi \sqrt{C_{\text{oss1}} L_{\text{main}}} = 51\,\text{ns}. \tag{4.39}$$

4.3 Turn-On Model Validation for Low Operation Currents

In this section, the application of turn-on model previously validated at high current values is described and discussed at a lower load current. A low load current is defined with $|I_{\mathrm{rrm}}| > |I_{\mathrm{Load}}|$. Except the load current of 50 A and the initial snubber voltage of 760 V, all parameters introduced in Sect. 4.2 are kept unchanged. It will be shown that due to the low load current, some assumptions made for the turn-on model become invalid at the chosen operation conditions, in particular the switching speed. Finally, the consequences for the target application are discussed.

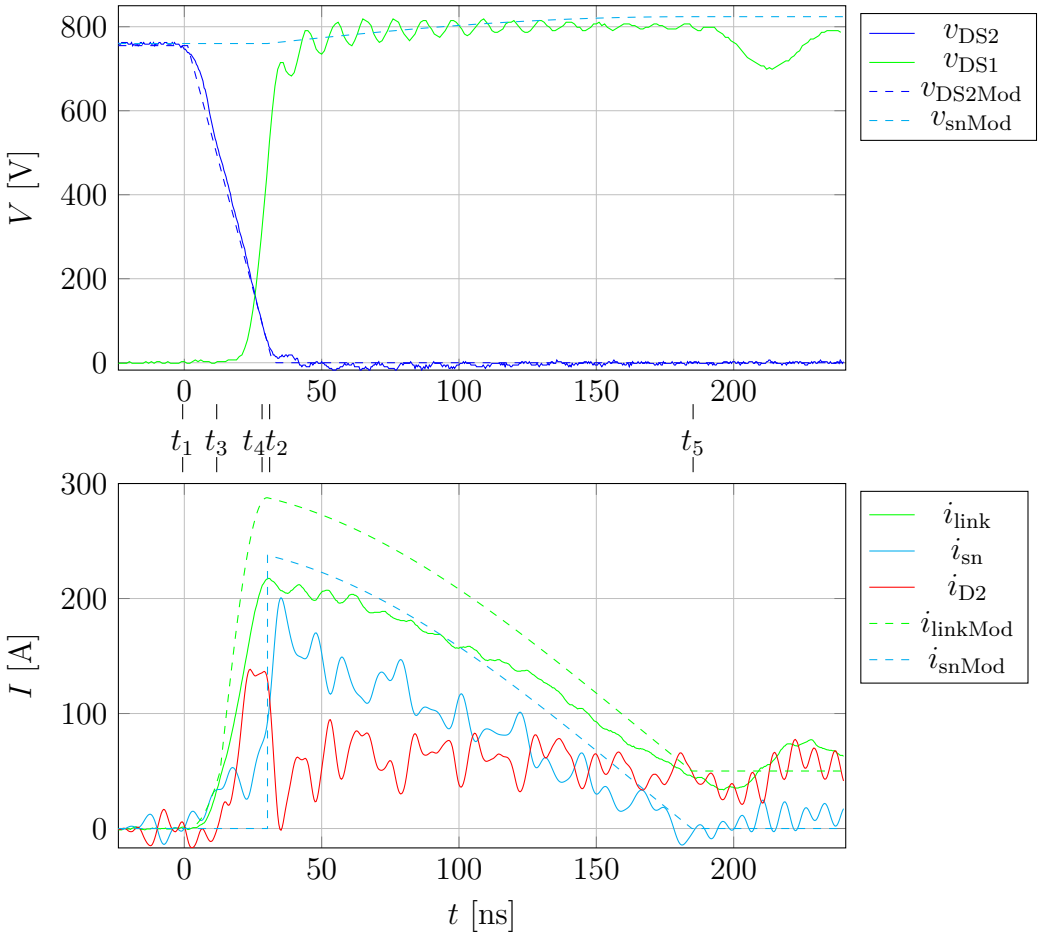


Figure 4.10: Turn-on event for a load current of 50 A at a DC-link voltage of 750 V with measured values (solid) and calculated values (dashed)

In Figure 4.10 the waveforms measured with the calculated values are depicted. Comparing Fig. 4.10 with Fig. 4.8 shows immediately that the calculated signals from high-side show a better fit to the measured as for the low-side signals at $I_{\mathrm{Load}} = 50$ A than for 350 A. The resulting difference is topic of this section.

Interval $t_1 \leq t < t_4$
Similar to Fig. 4.8 the voltage slope with a fall time of $t_{\mathrm{f12}} = t_2 - t_1 = 31$ ns remains unchanged and suits the measured signal. At $t = t_1$ the decreasing voltage v_{DS2} stimulates

the current flow in L_{main} and (3.19) can be applied to calculate the DC-link current. However, due to the low load current, the point in time t_3, where the DC-link current equals the load current, is reached much faster compared to higher load current values. According to the conditions for the time markers, t_3 ($i_{\text{link}} = I_{\text{Load}}$) is now reached before t_2 ($v_{\text{DS2}} = 0\,\text{V}$) which is illustrated with the time markers in Fig. 4.10. This effect has already been predicted on page 40f. and the new point in time t_3 can be calculated according (3.23) and (3.24) to

$$K_* = \frac{50\,\text{A} \cdot 45\,\text{m}\Omega^2}{750\,\text{V} \cdot 34\,\text{nH}} 31\,\text{ns} + 1 = 1.000123 \quad \text{and} \tag{4.40}$$

$$t_3 = \frac{\text{W}\left(-e^{-K_*}\right) + K_*}{2 \cdot 661 \cdot 10^3\,1/\text{s}} = 11.9\,\text{ns}, \tag{4.41}$$

for all $K_* > 1$, where W is the Lambert-W-function. This causes an overlap resulting in an inaccuracy of the turn-on model for all $t > t_3$ except the end of the voltage slope at $t = t_2$. However, it can be discussed, whether the linear approximation of the voltage slope is still sufficient for even slower switching events. So for $t_2 \gg t_3$, further overlap of the voltage slope with later intervals occurs. As a result, various possible changes in mathematical conditions may influence the voltage slope as well. To consider all possible variations of interval overlap at different load currents and switching speeds several sub-models would be necessary which is not reasonable to spend the effort to better estimate damping losses.
To counteract the overlapping effect, the switching speed might be increased, e.g. by further reduction of the gate-resistor. Anyhow, further reduction to fulfill the conditions might be not possible and for very small load currents, e.g. close to the zero crossing at sinusoidal load current operation, this effect cannot be avoided.
However, to avoid the derivation of separate sub-models for each branch of combination of overlapped intervals, and keep the turn-on model manageable, the overall goal to estimate the damping losses and the stability of the snubber voltage can be taken into account.
Considering that at low load current values, the energy stored in $L_{\sigma\text{On}}$ is also small, the damping losses as well as the snubber voltage increase are small as well. Further, in Section 4.8 it will be shown that for operation at low load current values the operation mode as a DC-snubber by permanent activation of the auxiliary switch is more reasonable from a loss perspective. Hence, for DC-snubber operation mode, the turn-on model is not necessary and the equations for the DC-snubber can be applied, see Section 2.4.1.
Finally, the deviation of the model reduces for load currents close to the reverse recovery peak $|I_{\text{rrm}}| \gtrapprox |I_{\text{load}}|$. Therefore, the application of the derived turn-on model would lead to slightly higher predicted values then measured as shown in Figure 4.10 and thus, to an overestimation of losses and snubber voltage change. Hence, the calculated losses and the snubber voltage change in the limited load current range between DC-snubber operation mode and $|I_{\text{rrm}}| = |I_{\text{load}}|$ contribute only modestly to the overall losses and snubber voltage behavior. Therefore, treating the calculated values as a worst case estimation might be sufficient for the sake of a simple manageable turn-on model.

After the DC-current reaches the load current value at $t = t_3$, v_{DS2} is still decreasing. Hence, the voltage across L_{main} is smaller than V_{DC} compared to the behavior at high load currents. This reduces the current slope compared to the calculated values for which it was assumed that the voltage across the inductance is equal to the DC-link voltage, confer i_{linkMod} and i_{link} for $t > t_3$ in Fig. 4.10.

To calculate the point in time t_4, when the body diode becomes conductive, (3.30) and (3.31) are used. It has to be mentioned that (3.31) expects that $t_2 < t_3$. The corresponding exponential term $e^{-2\delta_{14}(t_3-t_2)}$ considers damping influence this interval. Because this interval does not exist, $t_3 - t_2$ is set to zero, cf. (4.43). With

$$\begin{aligned} K &= \frac{(750\,\mathrm{V} - 760\,\mathrm{V} - 45\,\mathrm{m\Omega} \cdot 50\,\mathrm{A})\, 2 \cdot 661 \cdot 10^3\,1/\mathrm{s} \cdot 31\,\mathrm{ns}}{750\,\mathrm{V}(e^{-2\cdot 661 \cdot 10^3\,1/\mathrm{s}\cdot 0\,\mathrm{ns}} - e^{-2\cdot 661 \cdot 10^3\,1/\mathrm{s}\cdot 11.9\,\mathrm{ns}})} \\ &= \frac{(750\,\mathrm{V} - 820\,\mathrm{V} - 45\,\mathrm{m\Omega} \cdot 50\,\mathrm{A})\, 2 \cdot 661 \cdot 10^3\,1/\mathrm{s} \cdot 31\,\mathrm{ns}}{750\,\mathrm{V}(1 - e^{-2\cdot 661 \cdot 10^3\,1/\mathrm{s}\cdot 11.9\,\mathrm{ns}})} = -0.0165 \quad \text{and} \end{aligned} \tag{4.42}$$

$$t_4 = \frac{\arccos(K)}{91.67 \cdot 10^6\,1/\mathrm{s}} + 11.9\,\mathrm{ns} = 29.2\,\mathrm{ns}, \tag{4.43}$$

the DC-link current at $t = t_4$ can be calculated according to (3.27) and (3.29) as

$$\begin{aligned} A_{34} &= \frac{750\,\mathrm{V}}{11.9\,\mathrm{ns} \cdot 45\,\mathrm{m\Omega} \cdot 91.67 \cdot 10^6\,1/\mathrm{s}} \cdot \left(1 - e^{-2\cdot 661 \cdot 10^3\,1/\mathrm{s}\cdot 11.9\,\mathrm{ns}}\right) \\ &= 238.8\,\mathrm{A}, \end{aligned} \tag{4.44}$$

$$\begin{aligned} i_{\mathrm{link}}(t_4) &= A_{34} \cdot e^{-661 \cdot 10^3\,1/\mathrm{s}\cdot(29.2\,\mathrm{ns}-11.9\,\mathrm{ns})} \sin(91.67\,1/\mathrm{s} \cdot (29.2\,\mathrm{ns} - 11.9\,\mathrm{ns})) + 50\,\mathrm{A}. \\ &= 286\,\mathrm{A} \end{aligned} \tag{4.45}$$

Comparing this calculated peak value with the measured, cf. Fig. 4.10, shows that the model predicts a higher value. As explained before, the reason for this is that v_{DS2} is not zero in the measurement but which is expected by the model. Hence, in the measurement, the voltage v_{DS2} influences the current slope by leading to a lower v_{Lmain} and thus, a measurable lower current slope, cf. i_{link} in Fig. 4.10 for $t > t_3$.
For further calculations, the alternating part of the DC-link current must be calculated, cf. (3.27) and (3.33), resulting in

$$i_{\mathrm{linkAC}}(t_4) = 286\,\mathrm{A} - 50\,\mathrm{A} = 236\,\mathrm{A}. \tag{4.46}$$

Similar to the switching event at high current values, the measured snubber current during the rise time of v_{DS1} of the passive switch, shows a displacement current not included in the model, cf. i_{sn} in Fig. 4.10 at $t = 25\,\mathrm{ns}$.

Interval $t_4 \leq t < t_5$
When the body diode of Q_{aux} opens at $t = t_4$, the low inductive snubber path suppresses the voltage overshoot at the diode. The circuit properties are equal to the previous section and hence, the time depending parameters given by (4.24) to (4.27) remain. To obtain the end of the switching event t_5, the Equations (3.39) to (3.41) lead to

$$A_{1\mathrm{t}5} = 236\,\mathrm{A} \cdot 9.01 \cdot 10^6\,1/\mathrm{s} \cdot 37\,\mathrm{nH} = 78.7\,\mathrm{V}, \tag{4.47}$$

$$\begin{aligned} A_{2\mathrm{t}5} =& 750\,\mathrm{V} - 760\,\mathrm{V} + 14\,\mathrm{m\Omega} \cdot 50\,\mathrm{A} \\ & - 37\,\mathrm{nH} \cdot 797 \cdot 10^3\,1/\mathrm{s}(236\,\mathrm{A} + 2 \cdot 50\,\mathrm{A}) = -19.2\,\mathrm{V} \end{aligned} \tag{4.48}$$

and finally to the well suiting

$$t_5 = \frac{\arctan\left(-\frac{78.7\,\mathrm{V}}{-19.2\,\mathrm{V}}\right)}{9.01 \cdot 10^6\,1/\mathrm{s}} + 29.2\,\mathrm{ns} = 147.8\,\mathrm{ns} + 29.2\,\mathrm{ns} = 177\,\mathrm{ns}. \tag{4.49}$$

Due to the higher initial current value $i_{\mathrm{linkAC}}(t_4)$ compared to the measured value, see (4.46) and Fig. 4.10 the modeled currents in this interval are higher. Thus, the estimated damping losses by the model are higher as well and result in

$$W_{\mathrm{dampOn}} = R_{\mathrm{d}} \cdot \int_{t_4}^{t_5} i_{\mathrm{snMod}}^2 dt = 199\,\mu\mathrm{J}. \tag{4.50}$$

Compared to the value according (4.31) this value is higher and can be explained by the higher initial current value $i_{\mathrm{linkAC}}(t_4)$ caused on the model inaccuracy, but also by the longer duration caused by the lower initial snubber voltage of 760 V.
Further, the snubber voltage calculated leads to a higher result as measured. Similarly, to the previous section, the snubber voltage change can be calculated with (3.43) to (3.45) as

$$\begin{aligned} A_{45\mathrm{Vsn1}} =& \frac{236\,\mathrm{A} + 2 \cdot 50\,\mathrm{A}}{9.01 \cdot 10^6\,1/\mathrm{s} \cdot 330\,\mathrm{nF}} - 2 \cdot 9.01 \cdot 10^6\,1/\mathrm{s} \cdot 37\,\mathrm{nH} \cdot 50\,\mathrm{A} \\ & - \frac{797 \cdot 10^3\,1/\mathrm{s}}{9.01 \cdot 10^6\,1/\mathrm{s}} (750\,\mathrm{V} - 760\,\mathrm{V} + 14\,\mathrm{m\Omega} \cdot 50\,\mathrm{A}) = 80.4\,\mathrm{V}, \end{aligned} \tag{4.51}$$

$$A_{45\mathrm{Vsn2}} = 750\,\mathrm{V} - 760\,\mathrm{V} - 45\,\mathrm{m\Omega} \cdot 50\,\mathrm{A} = -12.3\,\mathrm{V} \quad \text{and} \tag{4.52}$$

$$\begin{aligned} \Delta v_{\mathrm{sn}} =& A_{45\mathrm{Vsn1}} \cdot e^{-797 \cdot 10^3\,1/\mathrm{s} \cdot 147.8\,\mathrm{ns}} \cdot \sin(9.01 \cdot 10^6\,1/\mathrm{s} 147.8\,\mathrm{ns}) \\ & + A_{45\mathrm{Vsn2}} \cdot \left(1 - e^{-797 \cdot 10^3\,1/\mathrm{s} \cdot 147.8\,\mathrm{ns}} \cos(9.01 \cdot 10^6\,1/\mathrm{s} \cdot 147.8\,\mathrm{ns})\right) = 59.8\,\mathrm{V}. \end{aligned} \tag{4.53}$$

Thus, the calculated total snubber voltage at $t = t_5$ results in $V_{\mathrm{snMaxOn}} = 760\,\mathrm{V} + 59.8\,\mathrm{V} = 819.8\,\mathrm{V}$ higher than the measured snubber voltage similar to v_{DS1}. However, it has already been mentioned that this deviance relies on the higher current but can be tolerated as a worst case estimation. Thus, the desired damping losses according to (4.50) are overestimated. This overestimation is further evaluated by usage of the measured DC-link peak current, see Fig. 4.10, as $i_{\mathrm{link}}(t_4) = 217\,\mathrm{A}$. Referring to (4.50) and the squared current dependence, an overestimation factor for the lost energy can be calculated as

$$\left(\frac{i_{\mathrm{linkAC}}(t_4)}{i_{\mathrm{link}}(t_4) - I_{\mathrm{Load}}}\right)^2 = \left(\frac{236\,\mathrm{A}}{217\,\mathrm{A} - 50\,\mathrm{A}}\right)^2 = 2. \tag{4.54}$$

Hence, the calculated damping losses according (4.50) deviate by a factor of 2 and thus, the real damping losses are very similar to high load current according (4.31). But it should be kept in mind that this value is only valid for this single measurement and for continuous inverter operation, it might deviate. This is discussed in Sect. 4.6 where it is shown that the initial snubber voltage V_{sn0} is a function of previous switching events. Future work might target to model a corrective factor considering the lower voltage v_{Lmain} leading to a deviance in $i_{\mathrm{link}}(t_4)$.

Interval $t \geq t_5$
Similarly to Sect. 4.2, v_{DSaux} becomes zero at $t = t_5$ and the body diode of Q_{aux} starts blocking. Hence, a similar oscillation can be measured.

4.4 Turn-Off Model Validation for High Operation Currents

In the previous sections, the turn-on model was compared with measurements. In this section, the model for turn-off derived in Section 2.3.2 shall be compared with measurements. Similar to Section 4.2, the turn-off model is validated for a high operation current $I_{\mathrm{Load}} = 350\,\mathrm{A}$ and a DC-link voltage of $V_{\mathrm{DC}} = 765\,\mathrm{V}$ first with the setup described in Section 4.1.4.
Because the auxiliary switch is in on-state during the complete turn-off event, two stray inductances are relevant for description, the effective stray inductance for turn-off responsible for the voltage overshoot $L_{\mathrm{snhb}} = 3\,\mathrm{nH}$ as well as the higher stray inductance $L_{\mathrm{res}} = 37\,\mathrm{nH}$, see Section 4.1.3f.

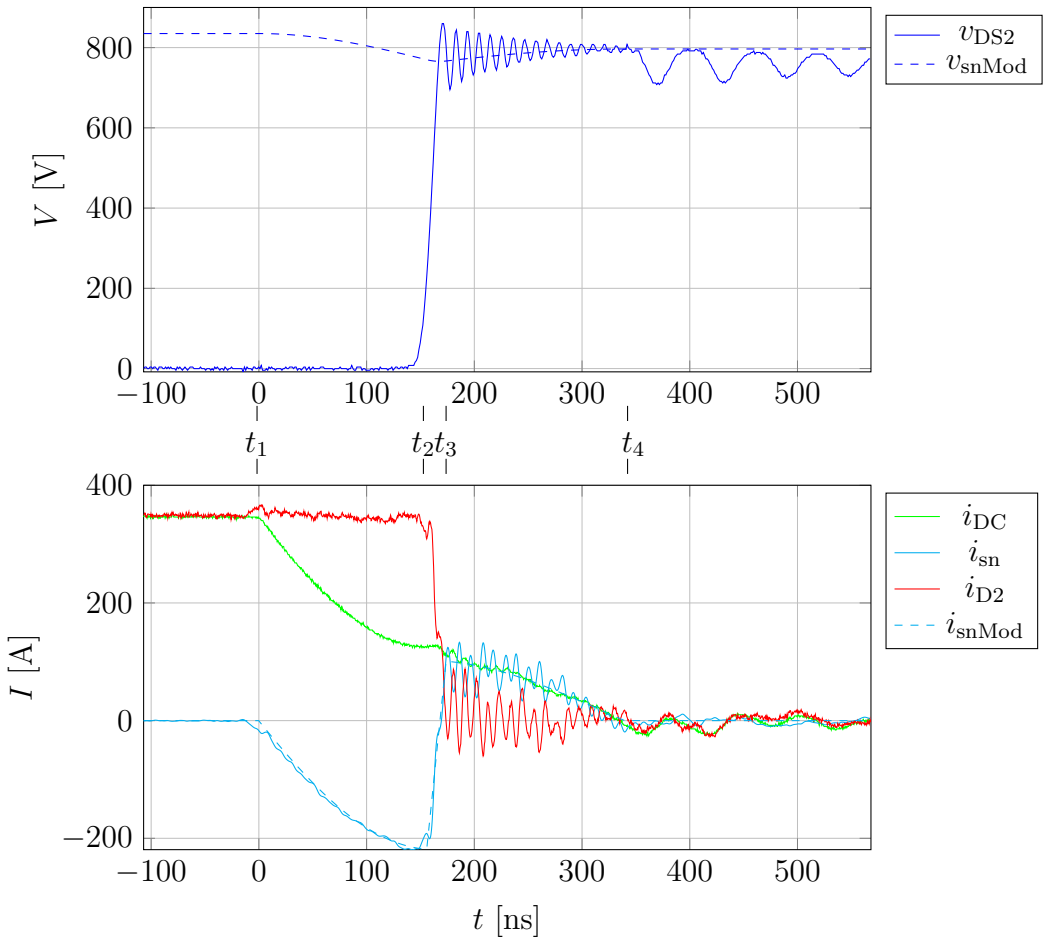


Figure 4.11: Turn-off event for a load current of 350 A at a DC-link voltage of 765 V with measured values (solid) and calculated values (dashed)

Similar to the turn-on event, t_1 is set to zero. Additionally, the linear modeled current slope of i_{D2} is adjusted with a fall time of $t_{\mathrm{f23}} = 18\,\mathrm{ns}$. The corresponding switching curve including the calculated values is shown in Figure 4.11. Further, the naming of the intervals is aligned with the description in Section 3.3. Similar to the turn-on event in Section 4.2, it is assumed that the snubber has been charged to a voltage higher than V_{DC} due to previous switching events resulting in $V_{\mathrm{sn0}} = 835\,\mathrm{V}$. For the measurement performed as a

double pulse, this was ensured by measuring the second turn-off appearing at the end of the second pulse.

Interval $t_1 \leq t < t_2$

The turn-off event starts at t_1 by turning on the auxiliary switch Q_{aux} rapidly. As it can be seen in Fig. 4.11, the snubber current i_{sn}, determined by the resonant circuit L_{res} and C_{sn}, changes slowly and the approximation for an almost zero current turn-on of Q_{aux} is valid. The snubber current can be calculated with (3.48) and (3.49) where the recurrent parameter A_0 results in

$$A_0 = \frac{765\,\mathrm{V} - 835\,\mathrm{V} - 45\,\mathrm{m\Omega} \cdot 350\,\mathrm{A}}{37\,\mathrm{nH}} = -2.318\,\mathrm{kA}/\mu\mathrm{s}. \tag{4.55}$$

In the measurement, the end of this interval has been set to $t_2 = 154\,\mathrm{ns}$, which is close to the optimal point in time according to (3.61) and (3.62) resulting in

$$K_{\mathrm{t2opt}} = \frac{9.01 \cdot 10^6\,1/\mathrm{s} \cdot 45\,\mathrm{m\Omega}}{37\,\mathrm{nH}(9.05 \cdot 10^6\,1/\mathrm{s})^2 - 797 \cdot 10^3\,1/\mathrm{s} \cdot 45\,\mathrm{m\Omega}} = 0.1354, \tag{4.56}$$

$$K_{\mathrm{t2optA}} = \cos(9.01 \cdot 10^6\,1/\mathrm{s} \cdot 18\,\mathrm{ns}) = 0.9869, \tag{4.57}$$

$$K_{\mathrm{t2optB}} = \sin(9.01 \cdot 10^6\,1/\mathrm{s} \cdot 18\,\mathrm{ns}) = 0.1615, \tag{4.58}$$

$$t_{2\mathrm{opt}} = \frac{\arctan\left(\frac{-e^{797 \cdot 10^3\,1/\mathrm{s} \cdot 18\,\mathrm{ns}}\left\{K_{\mathrm{t2opt}}K_{\mathrm{t2optA}} + K_{\mathrm{t2optB}}\right\} + K_{\mathrm{t2opt}}}{e^{797 \cdot 10^3\,1/\mathrm{s} \cdot 18\,\mathrm{ns}}\left\{K_{\mathrm{t2optA}} - K_{\mathrm{t2opt}}K_{\mathrm{t2optB}}\right\} - 1}\right)}{9.01 \cdot 10^6\,1/\mathrm{s}} = 159\,\mathrm{ns}. \tag{4.59}$$

Otherwise, the simplified approximation, see also (3.61), with considering the time offset yields in

$$t_{2\mathrm{opt}} \approx \frac{\pi}{2 \cdot 9.01 \cdot 10^6\,1/\mathrm{s}} - 18\,\mathrm{ns} = 156\,\mathrm{ns}. \tag{4.60}$$

Hence, the snubber current at $t_{2\mathrm{opt}}$ can now be calculated with (3.48) to

$$\begin{aligned} i_{\mathrm{sn}}(159\,\mathrm{ns}) = & \frac{-2.318 \cdot 10^9\,\mathrm{A/s}}{9.01 \cdot 10^6\,1/\mathrm{s}} \cdot e^{-797 \cdot 10^3\,1/\mathrm{s} \cdot 159\,\mathrm{ns}} \\ & \cdot \sin(9.01 \cdot 10^6\,1/\mathrm{s} \cdot 159\,\mathrm{ns}) = -224\,\mathrm{A}, \end{aligned} \tag{4.61}$$

being very similar to the measurement with slightly different adjusted t_2, see Fig. 4.11 $i_{\mathrm{sn}}(153\,\mathrm{ns})$. Additionally, the snubber voltage change can be obtained according to (3.50) to be

$$\begin{aligned} \Delta v_{\mathrm{sn}}(159\,\mathrm{ns}) = & 2.318 \cdot 10^9\,\mathrm{A/s} \cdot 37\,\mathrm{nH}\Big[e^{-797 \cdot 10^3\,1/\mathrm{s} \cdot 159\,\mathrm{ns}} \\ & \left\{\frac{797 \cdot 10^3\,1/\mathrm{s}}{9.01 \cdot 10^6\,1/\mathrm{s}}\sin(9.01 \cdot 10^6\,1/\mathrm{s} \cdot 159\,\mathrm{ns})\right. \\ & \left. + \cos(9.01 \cdot 10^6\,1/\mathrm{s} \cdot 159\,\mathrm{ns})\right\} - 1\Big] = -69\,\mathrm{V}, \end{aligned} \tag{4.62}$$

resulting in a snubber voltage of

$$v_{\mathrm{sn}}(159\,\mathrm{ns}) = 835\,\mathrm{V} - 69\,\mathrm{V} = 766\,\mathrm{V}. \tag{4.63}$$

Interval $t_2 \leq t < t_3$

As mentioned above, the turning off Q_2 is modeled with a linear current slope with a duration of 18 ns. This current is partially provided by the DC-link but mainly by the snubber capacitor due to its much lower inductance L_{snhb}. The snubber current part can be calculated with (3.53) and with the end of the switching process for the adjusted time

$$t_3 = t_2 + t_{\mathrm{f23}} = 159\,\mathrm{ns} + 18\,\mathrm{ns} = 177\,\mathrm{ns}. \tag{4.64}$$

This results in a snubber as well as a DC-link current amplitude at t_3 of

$$\begin{aligned} i_{\mathrm{sn}}(177\,\mathrm{ns}) = {} & \frac{-2.318 \cdot 10^9\,\mathrm{A/s}}{9.01 \cdot 10^6\,1/\mathrm{s}} \cdot e^{-797 \cdot 10^3\,1/\mathrm{s} \cdot 177\,\mathrm{ns}} \quad \sin(9.01 \cdot 10^6\,1/\mathrm{s} \cdot 177\,\mathrm{ns}) \\ & + 45\,\mathrm{m\Omega} \cdot 330 \cdot 10^{-9}\,\mathrm{nF} \cdot \frac{350\,\mathrm{A}}{18\,\mathrm{ns}} \\ & \cdot \left[1 - e^{-797 \cdot 10^3\,1/\mathrm{s} \cdot 18\,\mathrm{ns}} \cos(9.01 \cdot 10^6\,1/\mathrm{s} \cdot 18\,\mathrm{ns})\right] \\ & + \frac{350\,\mathrm{A}}{18\,\mathrm{ns} \cdot 9.01 \cdot 10^6\,1/\mathrm{s}} \left(\frac{34\,\mathrm{nH}}{37\,\mathrm{nH}} - 797 \cdot 10^3\,1/\mathrm{s} \cdot 45\,\mathrm{m\Omega} \cdot 330 \cdot 10^{-9}\,\mathrm{nF}\right) \\ & \cdot e^{-797 \cdot 10^3\,1/\mathrm{s} \cdot 18\,\mathrm{ns}} \sin(9.01 \cdot 10^6\,1/\mathrm{s} \cdot 18\,\mathrm{ns}) \\ = {} & 96\,\mathrm{A}, \end{aligned} \tag{4.65}$$

fitting very well to the measured values, cf. i_{sn} with i_{snMod} in Fig. 4.11.
However, in Section 4.6 it will be shown that this value does not represent a repetitive value appearing in continuous operation. Further, it will be shown, how to obtain representative results for inverter operation.
In the following section, the behavior will be discussed if the value of $i_{\mathrm{sn}}(t_{2\mathrm{opt}})$ becomes negative. This happens in case the energy stored in C_{sn} within previous switching events is higher compared to the energy in L_{main}. Further considerations to this operation are given in Section 4.7.
Due to the low inductive path through the snubber, it mainly provides the commutation current. In Figure 4.11, the snubber current i_{sn} can have a negative and positive part, resulting in a comparatively complex Equation (3.55) for the total snubber voltage change. The three lines of this equation shown on Page 44 are calculated separately and summed up afterwards for the sake of clearness. $Line1$ describes the carrying on part of the main resonance initiated at t_1 resulting in

$$\begin{aligned} Line1 = {} & A_0 L_{\mathrm{res}} \left[1 - e^{-\delta t_3} \left(\frac{\delta}{\omega_{\mathrm{d}}} \sin(\omega_{\mathrm{d}} t_3) + \cos(\omega_{\mathrm{d}} t_3)\right)\right] \\ = {} & -2.318 \cdot 10^9\,\mathrm{A/s} \cdot 37\,\mathrm{nH} \left[1 - e^{-797 \cdot 10^3\,1/\mathrm{s} 177\,\mathrm{ns}}\right. \\ & \left.\left(\frac{797 \cdot 10^3\,1/\mathrm{s}}{9.01 \cdot 10^6\,1/\mathrm{s}} \sin(9.01 \cdot 10^6\,1/\mathrm{s} \cdot 177\,\mathrm{ns}) + \cos(9.01 \cdot 10^6\,1/\mathrm{s} \cdot 177\,\mathrm{ns})\right)\right] \\ = {} & -81\,\mathrm{V}. \end{aligned} \tag{4.66}$$

*Line*2 and *Line*3 include the superimposed stimulus of the circuit caused by the switching Q_2 resulting in

$$\begin{aligned} Line2 &= \frac{I_{\text{Load}}}{t_{\text{f23}}}\left[\left(L_{\text{main}} - \frac{2\delta}{\omega_0^2}R_{\text{main}}\right)\left(1 - e^{-\delta t_{\text{f23}}}\cos(\omega_{\text{d}} t_{\text{f23}})\right)\right] \\ &= \frac{350\,\text{A}}{18\,\text{ns}}\left[\left(34\,\text{nH} - \frac{2\cdot 797\cdot 10^3\,1/\text{s}}{(9.05\cdot 10^6\,1/\text{s})^2}45\,\text{m}\Omega\right)\right. \\ &\quad \left.\left(1 - e^{-797\cdot 10^3\,1/\text{s}\cdot 18\,\text{ns}}\cos(9.01\cdot 10^6\,1/\text{s}\cdot 18\,\text{ns})\right)\right] \\ &= 18\,\text{V} \end{aligned} \tag{4.67}$$

and

$$\begin{aligned} Line3 &= -\frac{I_{\text{Load}}}{t_{\text{f23}}}\left[\left(\frac{R_{\text{main}}}{\omega_0^2}\left(\omega_{\text{d}} - \frac{\delta^2}{\omega_{\text{d}}}\right) + \frac{\delta}{\omega_{\text{d}}}L_{\text{main}}\right)e^{-\delta t_{\text{f23}}}\sin(\omega_{\text{d}} t_{\text{f23}})\right] + R_{\text{main}} I_{\text{Load}} \\ &= -\frac{350\,\text{A}}{18\,\text{ns}}\left[\left(\frac{45\,\text{m}\Omega}{(9.05\cdot 10^6\,1/\text{s})^2}\left(9.01\cdot 10^6\,1/\text{s} - \frac{(797\cdot 10^3\,1/\text{s})^2}{9.01\cdot 10^6\,1/\text{s}}\right)\right.\right. \\ &\quad \left.\left. + \frac{797\cdot 10^3\,1/\text{s}}{9.01\cdot 10^6\,1/\text{s}}34\,\text{nH}\right)e^{-797\cdot 10^3\,1/\text{s}\cdot 18\,\text{ns}}\sin(9.01\cdot 10^6\,1/\text{s}\cdot 18\,\text{ns})\right] \\ &\quad + 45\,\text{m}\Omega\cdot 350\,\text{A} = -25\,\text{V} + 16\,\text{V} = -9\,\text{V}. \end{aligned} \tag{4.68}$$

Here, $R_{\text{main}} I_{\text{Load}}$ describes the voltage drop through the resistance of the DC-link and connection.
Finally, this results in a total change in the snubber voltage from t_1 to t_3 of

$$\Delta v_{\text{sn}}(t_3) = -81\,\text{V} + 18\,\text{V} - 9\,\text{V} = -72\,\text{V}. \tag{4.69}$$

This value is slightly lower compared to (4.62) and indicates further discharge of the snubber capacitor in this interval. A further discharge of C_{sn} is plausible, because the duration between t_2 and t_3 in which i_{sn} is below zero is longer compared to the duration above zero, cf. Fig. 4.11. Now the snubber voltage at t_3 can be calculated to

$$v_{\text{sn}}(177\,\text{ns}) = 835\,\text{V} - 72\,\text{V} = 763\,\text{V}, \tag{4.70}$$

very similar to $V_{\text{DC}} = 760\,\text{V}$.

Interval $t_3 \leq t < t_4$
In this interval, the remaining DC-link current with the corresponding energy in L_{main} commutates into the snubber capacitor. In Figure 4.11, a high frequency oscillation can be recognized. Similar to the interval $t_4 \leq t < t_5$ in the turn-on event, this oscillation is enabled by the output capacitance C_{oss2} of Q_2 and the very low inductance of the snubber path $L_{\text{snhb}} = 3\,\text{nH}$ and has already been estimated with (4.24).
Neglecting the high frequency part, the snubber current is very similar to the DC-link

current in this interval. First, the end of the interval, where the snubber current becomes zero, is calculated with (3.57) to (3.60) resulting in

$$\begin{aligned}
A_{1t4} =& 9.01 \cdot 10^6\,1/\mathrm{s} \cdot 45\,\mathrm{m\Omega} \cdot 330\,\mathrm{nF} \\
& \cdot \left(e^{797 \cdot 10^3\,1/\mathrm{s} \cdot 177\,\mathrm{ns}} \cos(9.01 \cdot 10^6\,1/\mathrm{s} \cdot 177\,\mathrm{ns}) \right. \\
& \left. - e^{797 \cdot 10^3\,1/\mathrm{s} \cdot 159\,\mathrm{ns}} \cos(9.01 \cdot 10^6\,1/\mathrm{s} \cdot 159\,\mathrm{ns})\right) \\
& + \left(\frac{34\,\mathrm{nH}}{37\,\mathrm{nH}} - 797 \cdot 10^3\,1/\mathrm{s} \cdot 45\,\mathrm{m\Omega} \cdot 330\,\mathrm{nF}\right) \\
& \cdot \left(e^{797 \cdot 10^3\,1/\mathrm{s} \cdot 177\,\mathrm{ns}} \sin(9.01 \cdot 10^6\,1/\mathrm{s} \cdot 177\,\mathrm{ns}) \right. \\
& \left. - e^{797 \cdot 10^3\,1/\mathrm{s} \cdot 159\,\mathrm{ns}} \sin(9.01 \cdot 10^6\,1/\mathrm{s} \cdot 159\,\mathrm{ns})\right) \\
=& 370.58e-6, \\
A_{2t4} =& 9.01 \cdot 10^6\,1/\mathrm{s} \cdot 45\,\mathrm{m\Omega} \cdot 330\,\mathrm{nF} \\
& \left(e^{797 \cdot 10^3\,1/\mathrm{s} \cdot 177\,\mathrm{ns}} \sin(9.01 \cdot 10^6\,1/\mathrm{s} \cdot 177\,\mathrm{ns}) \right. \\
& \left. - e^{797 \cdot 10^3\,1/\mathrm{s} \cdot 159\,\mathrm{ns}} \sin(9.01 \cdot 10^6\,1/\mathrm{s} \cdot 159\,\mathrm{ns})\right) \\
& A_0 \frac{18\,\mathrm{ns}}{350\,\mathrm{A}} + \left(\frac{34\,\mathrm{nH}}{37\,\mathrm{nH}} - 797 \cdot 10^3\,1/\mathrm{s} \cdot 45\,\mathrm{m\Omega} \cdot 330\,\mathrm{nF}\right) \\
& \cdot \left(e^{797 \cdot 10^3\,1/\mathrm{s} \cdot 159\,\mathrm{ns}} \cos(9.01 \cdot 10^6\,1/\mathrm{s} \cdot 159\,\mathrm{ns}) \right. \\
& \left. - e^{797 \cdot 10^3\,1/\mathrm{s} \cdot 177\,\mathrm{ns}} \cos(9.01 \cdot 10^6\,1/\mathrm{s} \cdot 177\,\mathrm{ns})\right) \\
=& 0.0583
\end{aligned} \tag{4.71, 4.72}$$

and finally in

$$\Delta t_4 = \frac{\arctan\left(-\frac{370.58e-6}{0.0583}\right)}{9.01 \cdot 10^6\,1/\mathrm{s}} = 705\,\mathrm{ps}. \tag{4.73}$$

However, due to the π-periodic characteristic of tangents, this point in time must be corrected by π/ω_d. Thus, t_4 can be calculated to

$$t_4 = 705\,\mathrm{ps} + \frac{\pi}{9.01 \cdot 10^6\,1/\mathrm{s}} = 349\,\mathrm{ns}. \tag{4.74}$$

By choosing $t_2 = t_{2\mathrm{opt}}$, timing the turn-off of Q_aux at t_4 leads to zero current switching similar as for its turn-on. Further, due to the very short conduction only during the oscillation, the total losses - as a part of the damping losses - are very small and the total size of Q_aux can be reduced compared to Section 4.1.4.

The end of this interval at t_4, allows to calculate the change in the snubber voltage according to (3.63) as

$$\begin{aligned}\Delta v_{\mathrm{sn}}(t_4) =& -2.318\cdot 10^9\,\mathrm{A/s}\cdot 37\,\mathrm{nH}\Big[1-e^{-797\cdot 10^3\,1/\mathrm{s}\cdot 349\,\mathrm{ns}}\\ &\cdot\left(\frac{797\cdot 10^3\,1/\mathrm{s}}{9.01\cdot 10^6\,1/\mathrm{s}}\sin(9.01\cdot 10^6\,1/\mathrm{s}\cdot 349\,\mathrm{ns})+\cos(9.01\cdot 10^6\,1/\mathrm{s}\cdot 349\,\mathrm{ns})\right)\Big]\\ &+45\,\mathrm{m\Omega}\cdot 350\,\mathrm{A}\\ &+\frac{350\,\mathrm{A}}{(9.05\cdot 10^6\,1/\mathrm{s})^2\cdot 18\,\mathrm{ns}}\Big[\Big(9.01\cdot 10^6\,1/\mathrm{s}\cdot 45\,\mathrm{m\Omega}\\ &+\frac{797\cdot 10^3\,1/\mathrm{s}}{9.01\cdot 10^6\,1/\mathrm{s}}\cdot 34\,\mathrm{nH}\cdot(9.05\cdot 10^6\,1/\mathrm{s})^2-\frac{797\cdot 10^3\,1/\mathrm{s}^2}{9.01\cdot 10^6\,1/\mathrm{s}}\cdot 45\,\mathrm{m\Omega}\Big)\\ &\cdot\Big\{e^{-797\cdot 10^3\,1/\mathrm{s}\cdot(349\,\mathrm{ns}-177\,\mathrm{ns})}\sin(9.01\cdot 10^6\,1/\mathrm{s}\cdot(349\,\mathrm{ns}-177\,\mathrm{ns}))\\ &-e^{-797\cdot 10^3\,1/\mathrm{s}\cdot(349\,\mathrm{ns}-159\,\mathrm{ns})}\sin(9.01\cdot 10^6\,1/\mathrm{s}\cdot(349\,\mathrm{ns}-159\,\mathrm{ns}))\Big\}\\ &+(34\,\mathrm{nH}\cdot(9.05\cdot 10^6\,1/\mathrm{s})^2-2\cdot 797\cdot 10^3\,1/\mathrm{s}\cdot 45\,\mathrm{m\Omega})\\ &\cdot\Big\{e^{-797\cdot 10^3\,1/\mathrm{s}\cdot(349\,\mathrm{ns}-177\,\mathrm{ns})}\cos(9.01\cdot 10^6\,1/\mathrm{s}\cdot(349\,\mathrm{ns}-177\,\mathrm{ns}))\\ &-e^{-797\cdot 10^3\,1/\mathrm{s}\cdot(349\,\mathrm{ns}-159\,\mathrm{ns})}\cos(9.01\cdot 10^6\,1/\mathrm{s}\cdot(349\,\mathrm{ns}-159\,\mathrm{ns}))\Big\}\Big]\\ &=-42\,\mathrm{V}.\end{aligned} \tag{4.75}$$

This value is subtracted from the initial snubber voltage to calculate the absolute value at $t = t_4$.

$$v_{\mathrm{sn}}(t_4) = 835\,\mathrm{V}-42\,\mathrm{V} = 793\,\mathrm{V}, \tag{4.76}$$

which fits very well to the measured value, cf. Fig. 4.11 at $t_4 = 349\,\mathrm{ns}$.
However, because the point in time $t_2 = 153\,\mathrm{ns}$ chosen in the measurement is very similar to (4.59), the simplified approach according (3.64) can be used yielding in

$$\begin{aligned}\Delta v_{\mathrm{sn}}(t_4) \approx& -2.318\cdot 10^9\,\mathrm{A/s}\cdot 37\,\mathrm{nH}\left(1+e^{-797\cdot 10^3\,1/\mathrm{s}\cdot 349\,\mathrm{ns}}\right)+45\,\mathrm{m\Omega}\cdot 350\,\mathrm{A}\\ &+\frac{350\,\mathrm{A}}{(9.05\cdot 10^6\,1/\mathrm{s})^2\cdot 18\,\mathrm{ns}}(34\,\mathrm{nH}\cdot(9.05\cdot 10^6\,1/\mathrm{s})^2-2\cdot 797\cdot 10^3\,1/\mathrm{s}\cdot 45\,\mathrm{m\Omega})\\ &\cdot\Big(e^{-797\cdot 10^3\,1/\mathrm{s}(349\,\mathrm{ns}-177\,\mathrm{ns})}\cos(9.01\cdot 10^6\,1/\mathrm{s}\cdot(349\,\mathrm{ns}-177\,\mathrm{ns}))\\ &-e^{-797\cdot 10^3\,1/\mathrm{s}(349\,\mathrm{ns}-159\,\mathrm{ns})}\cos(9.01\cdot 10^6\,1/\mathrm{s}\cdot(349\,\mathrm{ns}-159\,\mathrm{ns}))\Big)\\ &=-45.5\,\mathrm{V},\end{aligned} \tag{4.77}$$

resulting in

$$V_{\mathrm{snMaxOff}} = v_{\mathrm{sn}}(t_4) = 835\,\mathrm{V}-45\,\mathrm{V} = 790\,\mathrm{V}. \tag{4.78}$$

Further, the damping losses can now be calculated by integration of the squared snubber current and multiplication with the damping resistance according (4.12) resulting in

$$W_{\mathrm{dampOff}} = R_{\mathrm{d}}\cdot\int_{t_1}^{t_4} i_{\mathrm{snMod}}^2 dt = 291\,\mu\mathrm{J}. \tag{4.79}$$

Although, it should be noted that these losses also include the conduction losses of the auxiliary switch as considered in (4.12). Therefore, for an exemplary chosen switching

frequency of $f_{\mathrm{sw}} = 10\,\mathrm{kHz}$ and considering zero-voltage-switching and the damping losses during turn-on according (4.31), the losses dissipated in Q_{aux} can be estimated as a negligible value of

$$\begin{aligned} P_{\mathrm{aux}} &= (W_{\mathrm{dampOff}} + W_{\mathrm{dampOn}}) \frac{R_{\mathrm{onAux}}}{R_{\mathrm{d}}} f_{\mathrm{sw}} \\ &= (291\,\mu\mathrm{J} + 89\,\mu\mathrm{J}) \cdot \frac{10\,\mathrm{m\Omega}}{59\,\mathrm{m\Omega}} \cdot 10\,\mathrm{kHz} \\ &= 650\,\mathrm{mW}. \end{aligned} \tag{4.80}$$

Interval $t \geq t_4$

At $t = t_4$, v_{DSaux} becomes zero and similarly to the turn-on events discussed previously, the body diode of Q_{aux} starts blocking. The snubber path is disconnected and an oscillation between L_{main} and C_{oss} of Q_2 can be measured.

4.5 Turn-Off Model Validation for Low Operation Currents

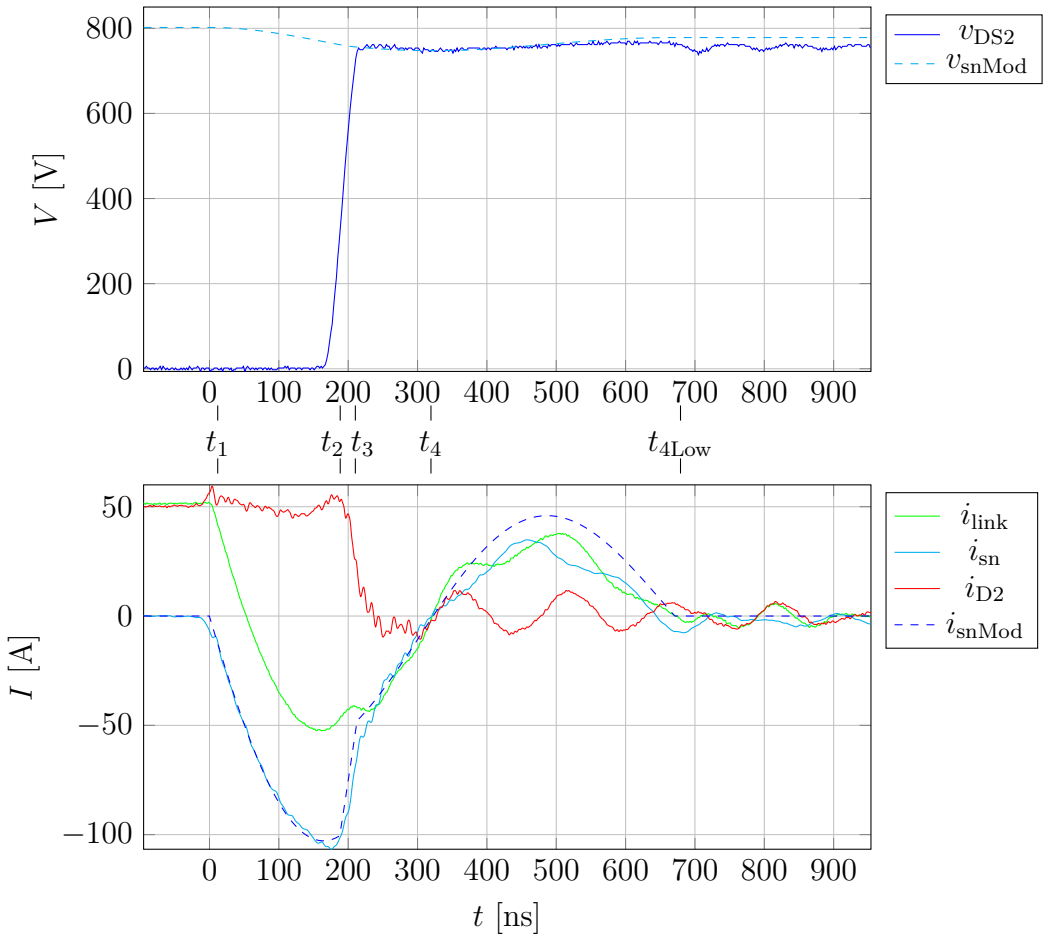


Figure 4.12: Turn-off event for a load current of 50 A at a DC-link voltage of 765 V with measured values (solid) and calculated values (dashed)

The turn-on model has been validated and compared with high as well as low operation currents. While in the previous section the turn-off model was validated for high opera-

tion current, in this section the operation at low operation current is matter of subject. The corresponding measured and calculated waveforms are depicted in Figure 4.12. Similar to the turn-on, see Sect. 4.3, a load current of 50 A was switched. For analysis, the second turn-off event in the double pulse is used and hence, the snubber was charged up to a voltage $V_{\mathrm{sn0}} = 802\,\mathrm{V}$ higher than the DC-Link voltage of $V_{\mathrm{DC}} = 765\,\mathrm{V}$. Additionally the current slope of the drain current of the switching transistor Q_2 is measured to be $t_{\mathrm{f23}} = 25\,\mathrm{ns}$. Otherwise, all other parameters are equal to the turn-off event at high operation current according to Section 4.4.

Interval $t_1 \leq t < t_2$

The turn-off sequence is initiated by turning on the auxiliary switch Q_{aux} as shown in Fig. 4.12. The energy stored in the snubber capacitor C_{sn} during previous switching events is released on the DC-link circuit. With the constant load current, the drain current of Q_2 remains nearly constant except a small spike in i_{D2} at t_1. With Q_{aux} turned on, the current in the DC-link i_{link} decreases according to (4.2). Because the previous turn-on event in the double pulse, similar as described in Sect. 4.3, was also performed at a similar low current, the absolute value of the reverse recovery current peak was higher than the load current. As a result, the energy in the stray inductance at the reverse recovery peak $0.5 \cdot L_{\mathrm{main}} \cdot I_{\mathrm{rrm}}^2$ is higher than the energy at load current $0.5 \cdot L_{\mathrm{main}} \cdot I_{\mathrm{Load}}^2$. Hence, at turn-off, this higher energy reduces the DC-link current below zero, cf. i_{link} in Fig. 4.12 for $50\,\mathrm{ns} \leq t < 160\,\mathrm{ns}$.

The turn-off current slope in the measurement is timed at $t_2 = 188\,\mathrm{ns}$ and manually adjusted in the curve calculated with the model. However, it should be noted that the calculated drain current i_{D2} is not constant. It increases during the rise interval of v_{DS2}, cf. Fig. 4.12 which is not plausible. Considering (4.2), a fraction of the constant load current should flow through the output capacitance of Q_1 leading to a lower i_{D2}, see also Sect. 2.3.2. One explanation might be the two different current probes (Shunt and Rogowski-coil) used for DC-link current and snubber current measurement. Both might not show an identical behavior which might lead to the fluctuating i_{D2} in this interval. Another explanation might be an incomplete model in which a significant effect is not considered. This is further examined on page 92ff. in which the focus is kept on the switching event itself.

The waveforms of the snubber current can be calculated with (3.48) and (3.49). The coefficient A_0 results in

$$A_0 = \frac{765\,\mathrm{V} - 802\,\mathrm{V} - 45\,\mathrm{m\Omega} \cdot 50\,\mathrm{A}}{37\,\mathrm{nH}} = -1.061 \cdot 10^9\,\mathrm{A/s}, \tag{4.81}$$

which leads to a snubber current at $t_2 = 188\,\mathrm{ns}$ of

$$i_{\mathrm{sn}}(t) = \frac{A_0}{9.01 \cdot 10^6\,1/\mathrm{s}} \cdot e^{-797 \cdot 10^3\,1/\mathrm{s} \cdot 188\,\mathrm{ns}} \cdot \sin(9.01 \cdot 10^6\,1/\mathrm{s} \cdot 188\,\mathrm{ns}) = -101\,\mathrm{A}. \tag{4.82}$$

The optimal point for timing the current slope by turning off Q_2 can be calculated similarly to (4.56ff.) with $t_{2\mathrm{opt}} = 159\,\mathrm{ns}$. By considering the enlarged drain current slope, the new optimal timing results in

$$K_{\mathrm{t2opt}} = \frac{9.01 \cdot 10^6\,1/\mathrm{s} \cdot 45\,\mathrm{m\Omega}}{37\,\mathrm{nH}(9.05 \cdot 10^6\,1/\mathrm{s})^2 - 797 \cdot 10^3\,1/\mathrm{s} \cdot 45\,\mathrm{m\Omega}} = 0.1354 \tag{4.83}$$

$$K_{\mathrm{t2optA}} = \cos(9.01 \cdot 10^6\,1/\mathrm{s} \cdot 25\,\mathrm{ns}) = 0.9747 \tag{4.84}$$

$$K_{\mathrm{t2optB}} = \sin(9.01 \cdot 10^6\,1/\mathrm{s} \cdot 25\,\mathrm{ns}) = 0.2234 \tag{4.85}$$

$$t_{2\mathrm{opt}} = \frac{\arctan\left(\frac{-e^{797 \cdot 10^3\,1/\mathrm{s} \cdot 25\,\mathrm{ns}}\left\{K_{\mathrm{t2opt}}K_{\mathrm{t2optA}} + K_{\mathrm{t2optB}}\right\} + K_{\mathrm{t2opt}}}{e^{797 \cdot 10^3\,1/\mathrm{s} \cdot 25\,\mathrm{ns}}\left\{K_{\mathrm{t2optA}} - K_{\mathrm{t2opt}}K_{\mathrm{t2optB}}\right\} - 1}\right)}{9.01 \cdot 10^6\,1/\mathrm{s}} = 154\,\mathrm{ns}, \tag{4.86}$$

or the simplified approximation with considering the time offset

$$t_{2\mathrm{opt}} \approx \frac{\pi}{2 \cdot 9.01 \cdot 10^6\,1/\mathrm{s}} - 25\,\mathrm{ns} = 149\,\mathrm{ns}. \tag{4.87}$$

However, it is suggested that the optimal timing shall be chosen according (4.56)ff. because a deviation at higher load current would cause higher switching losses of the auxiliary switch at $t = t_4$ compared to lower load current.
Further, the calculated value $t_{2\mathrm{opt}} = 154\,\mathrm{ns}$ is below the chosen value in the measurement of $t_2 = 188\,\mathrm{ns}$. Hence, the removed amount of charge will be higher than in optimal timing and thus, the snubber voltage at $t = t_3$ will be below the DC-link voltage. To calculate the change in the snubber voltage, the chosen timing in the measurement $t_2 = 188\,\mathrm{ns}$ is used. The change of the snubber voltage due to the discharge can be obtained according to (3.50) as

$$\begin{aligned}\Delta v_{\mathrm{sn}}(188\,\mathrm{ns}) =& 1.061 \cdot 10^9\,\mathrm{A/s} \cdot 37\,\mathrm{nH}\Big[e^{-797 \cdot 10^3\,1/\mathrm{s} \cdot 188\,\mathrm{ns}} \\ &\left\{\frac{797 \cdot 10^3\,1/\mathrm{s}}{9.01 \cdot 10^6\,1/\mathrm{s}}\sin(9.01 \cdot 10^6\,1/\mathrm{s} \cdot 188\,\mathrm{ns})\right. \\ &\left. + \cos(9.01 \cdot 10^6\,1/\mathrm{s} \cdot 181\,\mathrm{ns})\right\} - 1\Big] = -40.4\,\mathrm{V}.\end{aligned} \tag{4.88}$$

Subtracting this value from the initial snubber voltage leads to a value of

$$v_{\mathrm{sn}}(188\,\mathrm{ns}) = 802\,\mathrm{V} - 38.3\,\mathrm{V} = 761.6\,\mathrm{V}, \tag{4.89}$$

very similar, but below the DC-link voltage of $V_{\mathrm{DC}} = 765\,\mathrm{V}$.

Interval $t_2 \leq t < t_3$
At $t = t_2$, the turn-off of the power switch Q_2 is timed. The linear approximated drain current slope is mainly provided by the snubber due to its small stray inductance. Similar to the end of the previous interval, i_{D2} does not show a plausible behavior due to a noticeable tail-current at $t >= 210\,\mathrm{ns}$ for an unipolar transistor. Further examination of these effects can be found on page 92ff.
In spite of these effects, the linear approximated drain current slope is seen approximately in the snubber current, see i_{snMod} in Fig. 4.12 from $t_2 \leq t < t_3$.
Neglecting a measurement value deviating from the real value, see P. 92ff., the end of this interval can be calculated with the current fall time $t_{\mathrm{f23}} = 25\,\mathrm{ns}$ according to

$$t_3 = t_2 + t_{\mathrm{f23}} = 188\,\mathrm{ns} + 25\,\mathrm{ns} = 213\,\mathrm{ns}. \tag{4.90}$$

The operation at a low load current causes a negative snubber current value at t_3 and can be calculated according to (3.53) yielding in

$$\begin{aligned} i_{\mathrm{sn}}(213\,\mathrm{ns}) = {} & \frac{-1.061\cdot 10^9\,\mathrm{A/s}}{9.01\cdot 10^6\,1/\mathrm{s}}\cdot e^{-797\cdot 10^3\,1/\mathrm{s}\cdot 213\,\mathrm{ns}} \quad \sin(9.01\cdot 10^6\,1/\mathrm{s}\cdot 213\,\mathrm{ns}) \\ & + 45\,\mathrm{m\Omega}\cdot 330\cdot 10^{-9}\,\mathrm{nF}\cdot\frac{50\,\mathrm{A}}{25\,\mathrm{ns}} \\ & \cdot\left[1-e^{-797\cdot 10^3\,1/\mathrm{s}\cdot 25\,\mathrm{ns}}\cos(9.01\cdot 10^6\,1/\mathrm{s}\cdot 25\,\mathrm{ns})\right] \\ & + \frac{50\,\mathrm{A}}{25\,\mathrm{ns}\cdot 9.01\cdot 10^6\,1/\mathrm{s}}\left(\frac{34\,\mathrm{nH}}{37\,\mathrm{nH}} - 797\cdot 10^3\,1/\mathrm{s}\cdot 45\,\mathrm{m\Omega}\cdot 330\cdot 10^{-9}\,\mathrm{nF}\right) \\ & \cdot e^{-797\cdot 10^3\,1/\mathrm{s}\cdot 25\,\mathrm{ns}}\sin(9.01\cdot 10^6\,1/\mathrm{s}\cdot 25\,\mathrm{ns}) \\ = {} & -48\,\mathrm{A}. \end{aligned} \tag{4.91}$$

The removed charge leads to a voltage drop calculated with (3.55), while, equal to the model validation at high current value, the value is successively calculated as follows. Similar with *Line*1 for the main carrying on resonance

$$\begin{aligned} \mathit{Line}1 &= A_0 L_{\mathrm{res}}\left[1-e^{-\delta t_3}\left(\frac{\delta}{\omega_{\mathrm{d}}}\sin(\omega_{\mathrm{d}}t_3)+\cos(\omega_{\mathrm{d}}t_3)\right)\right] \\ &= -1.061\cdot 10^9\,\mathrm{A/s}\cdot 37\,\mathrm{nH}\left[1-e^{-797\cdot 10^3\,1/\mathrm{s}213\,\mathrm{ns}}\right. \\ &\quad \left.\left(\frac{797\cdot 10^3\,1/\mathrm{s}}{9.01\cdot 10^6\,1/\mathrm{s}}\sin(9.01\cdot 10^6\,1/\mathrm{s}\cdot 213\,\mathrm{ns})+\cos(9.01\cdot 10^6\,1/\mathrm{s}\cdot 213\,\mathrm{ns})\right)\right] \\ &= -47.8\,\mathrm{V}, \end{aligned} \tag{4.92}$$

and *Line*2 and *Line*3 for the influence of the stimulus resulting in

$$\begin{aligned} \mathit{Line}2 &= \frac{I_{\mathrm{Load}}}{t_{\mathrm{f23}}}\left[\left(L_{\mathrm{main}}-\frac{2\delta}{\omega_0^2}R_{\mathrm{main}}\right)\left(1-e^{-\delta t_{\mathrm{f23}}}\cos(\omega_{\mathrm{d}}t_{\mathrm{f23}})\right)\right] \\ &= \frac{50\,\mathrm{A}}{25\,\mathrm{ns}}\left[\left(34\,\mathrm{nH}-\frac{2\cdot 797\cdot 10^3\,1/\mathrm{s}}{(9.05\cdot 10^6\,1/\mathrm{s})^2}45\,\mathrm{m\Omega}\right)\right. \\ &\quad \left.\left(1-e^{-797\cdot 10^3\,1/\mathrm{s}\cdot 25\,\mathrm{ns}}\cos(9.01\cdot 10^6\,1/\mathrm{s}\cdot 25\,\mathrm{ns})\right)\right] \\ &= 2.9\,\mathrm{V} \end{aligned} \tag{4.93}$$

and

$$\begin{aligned} \mathit{Line}3 &= -\frac{I_{\mathrm{Load}}}{t_{\mathrm{f23}}}\left[\left(\frac{R_{\mathrm{main}}}{\omega_0^2}\left(\omega_{\mathrm{d}}-\frac{\delta^2}{\omega_{\mathrm{d}}}\right)+\frac{\delta}{\omega_{\mathrm{d}}}L_{\mathrm{main}}\right)e^{-\delta t_{\mathrm{f23}}}\sin(\omega_{\mathrm{d}}t_{\mathrm{f23}})\right]+R_{\mathrm{main}}I_{\mathrm{Load}} \\ &= -\frac{50\,\mathrm{A}}{25\,\mathrm{ns}}\left[\left(\frac{45\,\mathrm{m\Omega}}{(9.05\cdot 10^6\,1/\mathrm{s})^2}\left(9.01\cdot 10^6\,1/\mathrm{s}-\frac{(797\cdot 10^3\,1/\mathrm{s})^2}{9.01\cdot 10^6\,1/\mathrm{s}}\right)\right.\right. \\ &\quad \left.\left.+\frac{797\cdot 10^3\,1/\mathrm{s}}{9.01\cdot 10^6\,1/\mathrm{s}}34\,\mathrm{nH}\right)e^{-797\cdot 10^3\,1/\mathrm{s}\cdot 25\,\mathrm{ns}}\sin(9.01\cdot 10^6\,1/\mathrm{s}\cdot 25\,\mathrm{ns})\right] \\ &\quad + 45\,\mathrm{m\Omega}\cdot 50\,\mathrm{A} = -3.46\,\mathrm{V}+2.25\,\mathrm{V} = -1.22\,\mathrm{V}. \end{aligned} \tag{4.94}$$

The sum of all three lines to calculate the total change in the snubber voltage from t_1 to t_3 leads to

$$\Delta v_{\mathrm{sn}}(t_3) = -47.8\,\mathrm{V}+2.9\,\mathrm{V}-1.22\,\mathrm{V} = -46.1\,\mathrm{V} \tag{4.95}$$

and to obtain the absolute snubber voltage, this value is subtracted from the initial snubber voltage resulting in

$$v_{\mathrm{sn}}(t_3) = 802\,\mathrm{V} - 46.1\,\mathrm{V} = 756\,\mathrm{V} \tag{4.96}$$

This value is below the DC-link voltage of 765 V due to the longer oscillation duration by the chosen timing of t_2.

Interval $t_3 \leq t < t_4$

The last interval in the turn-off sequence begins with a negative snubber and DC-link current. In high current operation, the snubber current and DC-link current at t_3 are positive. Thus, the conductive auxiliary switch can be turned off at a time $t_3 \leq t < t_4$ and the current will proceed through its body diode. Contrary to that, at low current operation, by turning off the auxiliary switch the body diode cannot conduct the negative current and therefore, this would lead to non-negligible turn-off losses of Q_{aux}. Hence, the turn-off of the auxiliary switch according at a fixed timing with $t = t_4$ is most desirable due to the zero crossing of both currents, see P. 68.

After the power switch Q_2 is turned off at $t = t_3$, the main resonance continues until the first zero crossing at which the auxiliary switch is turned off regularly. According to (3.57)ff., this point in time can be calculated with the two parameters

$$\begin{aligned} A_{1\mathrm{t}4} =& 9.01 \cdot 10^6\,1/\mathrm{s} \cdot 45\,\mathrm{m\Omega} \cdot 330\,\mathrm{nF} \\ & \cdot \left(e^{797 \cdot 10^3\,1/\mathrm{s} \cdot 213\,\mathrm{ns}} \cos(9.01 \cdot 10^6\,1/\mathrm{s} \cdot 213\,\mathrm{ns}) \right. \\ & \left. - e^{797 \cdot 10^3\,1/\mathrm{s} \cdot 188\,\mathrm{ns}} \cos(9.01 \cdot 10^6\,1/\mathrm{s} \cdot 188\,\mathrm{ns}) \right) \\ & + \left(\frac{34\,\mathrm{nH}}{37\,\mathrm{nH}} - 797 \cdot 10^3\,1/\mathrm{s} \cdot 45\,\mathrm{m\Omega} \cdot 330\,\mathrm{nF} \right) \\ & \cdot \left(e^{797 \cdot 10^3\,1/\mathrm{s} \cdot 213\,\mathrm{ns}} \sin(9.01 \cdot 10^6\,1/\mathrm{s} \cdot 213\,\mathrm{ns}) \right. \\ & \left. - e^{797 \cdot 10^3\,1/\mathrm{s} \cdot 188\,\mathrm{ns}} \sin(9.01 \cdot 10^6\,1/\mathrm{s} \cdot 188\,\mathrm{ns}) \right) \\ & = -0.0704 \end{aligned} \tag{4.97}$$

(4.98)

and

$$\begin{aligned} A_{2\mathrm{t}4} =& 9.01 \cdot 10^6\,1/\mathrm{s} \cdot 45\,\mathrm{m\Omega} \cdot 330\,\mathrm{nF} \\ & \left(e^{797 \cdot 10^3\,1/\mathrm{s} \cdot 213\,\mathrm{ns}} \sin(9.01 \cdot 10^6\,1/\mathrm{s} \cdot 213\,\mathrm{ns}) \right. \\ & \left. - e^{797 \cdot 10^3\,1/\mathrm{s} \cdot 213\,\mathrm{ns}} \sin(9.01 \cdot 10^6\,1/\mathrm{s} \cdot 213\,\mathrm{ns}) \right) \\ & A_0 \frac{25\,\mathrm{ns}}{50\,\mathrm{A}} + \left(\frac{34\,\mathrm{nH}}{37\,\mathrm{nH}} - 797 \cdot 10^3\,1/\mathrm{s} \cdot 45\,\mathrm{m\Omega} \cdot 330\,\mathrm{nF} \right) \\ & \cdot \left(e^{797 \cdot 10^3\,1/\mathrm{s} \cdot 188\,\mathrm{ns}} \cos(9.01 \cdot 10^6\,1/\mathrm{s} \cdot 188\,\mathrm{ns}) \right. \\ & \left. - e^{797 \cdot 10^3\,1/\mathrm{s} \cdot 213\,\mathrm{ns}} \cos(9.01 \cdot 10^6\,1/\mathrm{s} \cdot 213\,\mathrm{ns}) \right) \\ & = -0.2981, \end{aligned} \tag{4.99}$$

to subsequently calculate the time considering the periodicity of tangents as

$$\Delta t_4 = \frac{\arctan\left(-\frac{70.4e-3}{298.1e-3}\right)}{9.01 \cdot 10^6\,1/\mathrm{s}} = -25.7\,\mathrm{ns}, \tag{4.100}$$

equal to the measurement, see Fig. 4.12. With considering the periodicity of tangents follows

$$t_4 = \frac{\arctan\left(-\frac{70.4e{-}3}{298.1e{-}3}\right)}{9.01 \cdot 10^6\,1/\mathrm{s}} + \frac{\pi}{9.01 \cdot 10^6\,1/\mathrm{s}} = 323\,\mathrm{ns}. \tag{4.101}$$

The negative snubber current until this point t_4 further discharges the snubber and thus, to a value below the DC-link voltage. A snubber voltage below the DC-link voltage causes an increasing current through the body diode of the auxiliary switch and therefore to a continuing main resonance for positive current values. The next zero crossing occurs half of a period later at

$$t_{4\mathrm{Low}} = t_4 + \frac{\pi}{9.01 \cdot 10^6\,1/\mathrm{s}} = 672\,\mathrm{ns}. \tag{4.102}$$

However, the change of the snubber voltage can still be calculated with (3.63) considering the enlarged interval $t_3 \leq t < t_{4\mathrm{Low}}$ to

$$\begin{aligned}
\Delta v_{\mathrm{sn}}(t_{4\mathrm{Low}}) =& A_0 \cdot 37\,\mathrm{nH}\Big[1 - e^{-797 \cdot 10^3\,1/\mathrm{s}\cdot 672\,\mathrm{ns}} \\
&\cdot \left(\frac{797 \cdot 10^3\,1/\mathrm{s}}{9.01 \cdot 10^6\,1/\mathrm{s}} \sin(9.01 \cdot 10^6\,1/\mathrm{s} \cdot 672\,\mathrm{ns}) + \cos(9.01 \cdot 10^6\,1/\mathrm{s} \cdot 672\,\mathrm{ns})\right)\Big] \\
&+ 45\,\mathrm{m\Omega} \cdot 50\,\mathrm{A} \\
&+ \frac{50\,\mathrm{A}}{(9.05 \cdot 10^6\,1/\mathrm{s})^2 \cdot 25\,\mathrm{ns}}\Big[\Big(9.01 \cdot 10^6\,1/\mathrm{s} \cdot 45\,\mathrm{m\Omega} \\
&+ \frac{797 \cdot 10^3\,1/\mathrm{s}}{9.01 \cdot 10^6\,1/\mathrm{s}} \cdot 34\,\mathrm{nH} \cdot (9.05 \cdot 10^6\,1/\mathrm{s})^2 - \frac{797 \cdot 10^3\,1/\mathrm{s}^2}{9.01 \cdot 10^6\,1/\mathrm{s}} \cdot 45\,\mathrm{m\Omega}\Big) \\
&\cdot \Big\{e^{-797 \cdot 10^3\,1/\mathrm{s}\cdot(672\,\mathrm{ns}-213\,\mathrm{ns})} \sin(9.01 \cdot 10^6\,1/\mathrm{s} \cdot (672\,\mathrm{ns} - 213\,\mathrm{ns})) \\
&- e^{-797 \cdot 10^3\,1/\mathrm{s}\cdot(672\,\mathrm{ns}-188\,\mathrm{ns})} \sin(9.01 \cdot 10^6\,1/\mathrm{s} \cdot (672\,\mathrm{ns} - 188\,\mathrm{ns}))\Big\} \\
&+ (34\,\mathrm{nH} \cdot (9.05 \cdot 10^6\,1/\mathrm{s})^2 - 2 \cdot 797 \cdot 10^3\,1/\mathrm{s} \cdot 45\,\mathrm{m\Omega}) \\
&\cdot \Big\{e^{-797 \cdot 10^3\,1/\mathrm{s}\cdot(672\,\mathrm{ns}-213\,\mathrm{ns})} \cos(9.01 \cdot 10^6\,1/\mathrm{s} \cdot (672\,\mathrm{ns} - 213\,\mathrm{ns})) \\
&- e^{-797 \cdot 10^3\,1/\mathrm{s}\cdot(672\,\mathrm{ns}-188\,\mathrm{ns})} \cos(9.01 \cdot 10^6\,1/\mathrm{s} \cdot (672\,\mathrm{ns} - 188\,\mathrm{ns}))\Big\}\Big] \\
&= -23.7\,\mathrm{V}.
\end{aligned} \tag{4.103}$$

This value is subtracted from the initial snubber voltage to calculate the absolute value at $t = t_{4\mathrm{Low}}$ as

$$V_{\mathrm{snMaxOff}} = v_{\mathrm{sn}}(t_{4\mathrm{Low}}) = 802\,\mathrm{V} - 23.7\,\mathrm{V} = 778.3\,\mathrm{V}. \tag{4.104}$$

As it can be noticed, in Figure 4.12, the calculated current waveform from $t_4 \leq t < t_{4\mathrm{Low}}$ is higher than the measured value. This also leads to a higher estimated snubber voltage and is related to the non-ideal body diode characteristic with a comparatively high forward voltage. Further, the measured values, the DC-link current, the snubber current and the drain current show an oscillation of about 6.5 MHz. However, this frequency does not fit to a resonance frequency of any considered combination of inductance and capacitance and is further discussed on page 92ff.

4.6 Continuous Operation at High Load Current

In this section the two models for turn-on and turn-off are used to predict the behavior at a constant load current of $I_{\mathrm{Load}} = 350\,\mathrm{A}$ and thus, at high current mode operation as presented by [118]. Further, a simplified approximation for the simulated snubber voltage is presented. Finally, the damping losses of a DC-snubber setup are calculated as reference. For the calculation, the optimal timing according (4.59) is used. The fall time of the linear voltage slope for turn-on is assumed to be $t_{\mathrm{f12}} = 31\,\mathrm{ns}$ and the fall time of the linear current slope at turn-off is assumed to be $t_{\mathrm{f23}} = 18\,\mathrm{ns}$ respectively according to the measurement. Figure 4.13 shows the end value development of the snubber voltage

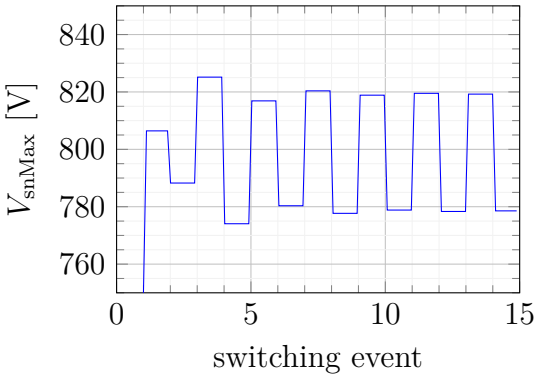


Figure 4.13: Development of snubber voltage over subsequent switching events at 350 A
odd numbers: turn-on, even numbers: turn-off

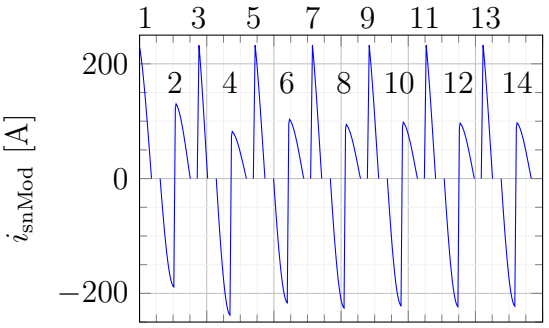


Figure 4.14: Development of snubber current over subsequent switching events at 350 A
odd numbers: turn-on, even numbers: turn-off

after each switching event. Each odd number describes a turn-on event and thus, the voltage V_{snMaxOn} calculated with (3.46). Each even number describes a turn-off event with an end voltage V_{snMaxOff} according (3.67). The corresponding modeled snubber current waveforms are depicted in Figure 4.14. Because the delay between each switching event is kept constant in the calculation with a delay of 25 ns, to separate each event, the abscissa shows a time scale which must not fit to a realistic duty-cycle. However, the time scale for the calculated current within each switching event is correct.
Until the first turn-on occurred, the snubber capacitor C_{sn} is charged through the body diode of Q_{aux} up to the value of the DC-link voltage as indicated in Figure 4.13, No. 0. The first switching event, a turn-on, leads to a positive snubber current as shown in Figure 4.14 caused by the diode recovery, cf. Sect. 4.2. This positive current initially charges the snubber up to a voltage of 806 V. Because the snubber voltage is now above the DC-link voltage, the body diode of Q_{aux} gets in blocking state. Hence, the snubber voltage remains at 806 V.
In a DC-snubber setup according to Figure 4.6, the diode turn-off of the passive switch Q_1 triggers a damped oscillation between L_{main} and C_{sn} with high damping losses, cf. also the measurements on Page 98. Contrary to that, the active snubber allows only current flow for a short duration and stores the energy for the subsequent turn-off event. Thus, the damping losses are much lower compared to a DC-snubber, cf. Figure 4.15.

In the subsequent turn-off event of the active snubber (No. 2), the stored energy is released on the DC-link and reduces the DC-link current. Hence, the snubber current

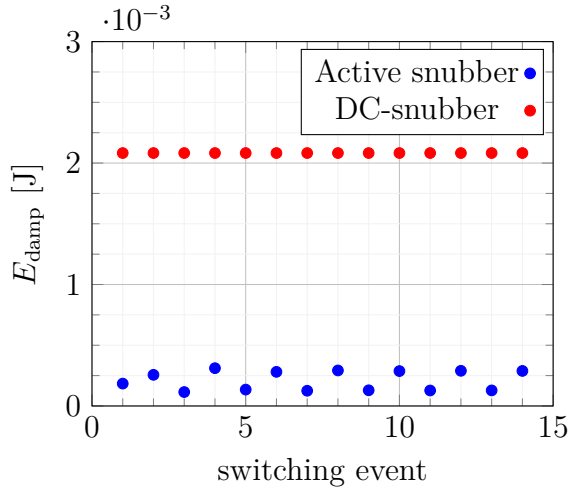


Figure 4.15: Simulated damping losses for subsequent switching events at 350 A

becomes negative. Due to the resistances in this circuit modeled by R_{main} and R_{sn}, a small part of the stored energy is dissipated. Thus, the absolute value of the negative peak current with approximately 190 A is slightly below the peak current at the previous turn-on event with approximately 220 A and indicates losses during oscillation. This allows to draw the conclusion that the quality factor of the resonant circuit

$$Q = (R_{\text{main}} + R_{\text{sn}})\sqrt{\frac{C_{\text{sn}}}{L_{\text{res}}}}, \tag{4.105}$$

is a major performance parameter to rate the efficiency of the active snubber for continuous operation. For the definition of Q, see e.g. [93] P. 255ff. Hence, a DC-link design targeting a low resistance at high frequencies should be a major goal for dimensioning.
At the turn-off of Q_2 the snubber current becomes positive because the remaining current i_{link} flowing through L_{main}, commutates into the snubber capacitor. This charges the snubber capacitor up to a voltage of 788 V which is below its value before the turn-off event. As shown in Figure 4.15, the damping losses are much lower compared to the DC-snubber losses which can be explained similar to the turn-on event due to prohibiting a continuing oscillation and storing the energy.
The subsequent switching event No. 3 shows a very similar current peak compared to the first turn-on event. While the first turn-on event with a snubber voltage of 750 V lead to a duration of current flow of $t_4 - t_3 = 35$ ns the higher snubber voltage of 788 V at event No. 3 reduces this duration to 25 ns and additionally leads to an energy transfer to the load. Considering that the snubber voltage in this interval lies across Q_1 and thus across the load, cf. Fig. 3.4, the dependence on $A_{2\text{t}5}$ on I_{Load} influences t_5 and thus the duration in which v_{sn} is larger than V_{DC}. However, a significant part of this energy commutates into the snubber capacitor, adds up to the already stored energy and charges it up to a voltage of 825 V. This causes a higher negative snubber current peak in the subsequent turn-off event No. 4. The energy exchange from switching event to switching event causes an alternating end value of the snubber voltage as it can be noticed in Figure 4.13. For progressed switching, the end values for each turn-on event as well as the end values for each turn-off event converge to be stable and constant. This also influences the snubber current, and for switching events later than event number 8, this transient exchange evens

out. This allows the conclusion that the small amount of energy damped in each switching event is sufficient to stabilize the snubber voltage and proves stability of the circuit in terms of a snubber voltage not increasing to destructive values. The calculated voltage development indicate an alternating behavior around a mean value of $V_{\mathrm{snMean}} = 798\,\mathrm{V}$.
The alternating current and voltage development allows further investigation and the derivation of a much simpler end value estimation as follows. First, a lossless circuit and a negligible reverse recovery peak current is assumed. Hence, only the energy exchange during turn-off is taken into account first. Analyzing the Figs. 4.13 and 4.14 the conclusion can be made that for continuous switching a maximum snubber energy stored from the previous turn-off, and thus a maximum snubber voltage, is reached which allows to reduce the DC-link current $i_{\mathrm{link}}(t_2)$ during a turn-off event by half. The remaining half of the DC-link current after the turn-off charges the snubber back to a voltage equal to the voltage before the switching event. Based on the simulations from Fig. 4.13 and 4.14 a simplified approach to estimate the snubber voltages for continuous operation at constant load current can be derived with common sense. In case all transitions have been settled, cf. the events No. 8ff., the mean snubber charge about two subsequent switching events must be constant. It is valuable to mention the fact that for $t_{2\mathrm{opt}}$ the last quarter of the snubber current resonance period at turn-off in high current operation mode, see t_3 to t_4 in Fig. 4.11, and $\frac{t_{4\mathrm{Low}}+t_4}{2}$ to $t_{4\mathrm{Low}}$ for low current, charges the snubber capacitor to its end value V_{snMaxOff}. This allows the following approach for a good estimation of V_{snMaxOff}.
The commutation current is provided by the DC-link and snubber capacitors proportionate to a factor

$$\alpha = \frac{L_{\mathrm{main}}}{L_{\mathrm{res}}}, \tag{4.106}$$

which is derived from (3.54).
Focusing on the final turn-on event No. 13, see Fig. 4.14, the $I_{\mathrm{rrm}} = 232\,\mathrm{A}$ starts roughly a quarter of the resonant oscillation period which proceeds during turn-off (event No. 14) resulting in a negative peak current for event No. 14, cf. Fig. 4.14, estimated with good match with

$$i_{\mathrm{snOff}}(t_2) \approx -I_{\mathrm{rrm}}\left(1 - \frac{1}{2}Q\right) = -232\,\mathrm{A}\left(1 - \frac{1}{2}0.176\right) = -211\,\mathrm{A}. \tag{4.107}$$

This value approximates the left term of (3.54) and can be applied in case the damping is very small and the snubber capacitor is large enough that its peak voltage is not much above the DC-link voltage. However, because the turn-on current flow duration is lower than a quarter of the oscillation period due to a higher snubber voltage. Hence, the absolute value is underestimated and indicates that this approximation deviates for smaller snubber capacitors and thus, it can only be a rough estimation.
For a very fast switching event $t_{\mathrm{f23}} = 0$, and considering the left term in (3.54) again, the peak value can be estimated with

$$\begin{aligned} i_{\mathrm{snOff}}(t_3) &\approx -I_{\mathrm{rrm}}\left(1 - \frac{1}{2}Q\right) + I_{\mathrm{Load}} \cdot \alpha \\ &= -232\,\mathrm{A}\left(1 - \frac{1}{2}0.176\right) + 350\,\mathrm{A} \cdot 0.92 = 110\,\mathrm{A}, \end{aligned} \tag{4.108}$$

cf. No. 14 in Fig. 4.14. As mentioned, the remaining quarter of the resonance period until $t = t_4$, the current is further damped and charges the snubber to

$$\begin{aligned} V_{\mathrm{snMaxOff}} &\approx \sqrt{\frac{L_{\mathrm{main}}}{C_{\mathrm{sn}}}} i_{\mathrm{snOff}}(t_3) \left(1 - \frac{1}{4}Q\right) + V_{\mathrm{DC}} \\ &= \sqrt{\frac{34\,\mathrm{nH}}{330\,\mathrm{nF}}} 110\,\mathrm{A} \left(1 - \frac{1}{4}0.176\right) + 750\,\mathrm{V} \\ &= 783\,\mathrm{V}, \end{aligned} \tag{4.109}$$

calculable by modification of (2.29) under consideration of the damping losses for a quarter of a period with Q. This value is higher to Fig. 4.13 No. 14, due to the relation between t_5 and v_{sn} as mentioned above. However, accepting this deviation, the highest voltage V_{snMaxOn}, see Fig. 4.13 No. 13, can be estimated with the help of (2.29) by considering Q yielding in

$$\begin{aligned} V_{\mathrm{snMaxOn}} &\approx \sqrt{\frac{L_{\mathrm{main}}}{C_{\mathrm{sn}}}} \cdot I_{\mathrm{rrm}} \cdot \left(1 - \frac{1}{4}Q\right) + V_{\mathrm{DC}} \\ &= \sqrt{\frac{34\,\mathrm{nH}}{330\,\mathrm{nF}}} \cdot 232\,\mathrm{A} \cdot \left(1 - \frac{1}{4} \cdot 0.176\right) + 750\,\mathrm{V} \\ &= 821\,\mathrm{V}. \end{aligned} \tag{4.110}$$

But it should be noted that this result does not include the energy transferred to the load as well as energy already stored in the snubber capacitor and therefore, it results in a higher value, cf. Fig. 4.13. Both (4.109) and (4.110) allow to estimate the mean snubber voltage to

$$V_{\mathrm{snMean}} \approx \frac{V_{\mathrm{snMaxOn}} + V_{\mathrm{snMaxOff}}}{2} = \frac{783\,\mathrm{V} + 821\,\mathrm{V}}{2} = 802\,\mathrm{V}. \tag{4.111}$$

A further important point to notice is that if this peak voltage is compared to the peak voltage of a DC-snubber according to (2.29) yielding in

$$V_{\mathrm{DCMax}} = \sqrt{\frac{L_{\mathrm{main}}}{C_{\mathrm{sn}}}} \cdot I_{\mathrm{Load}} + V_{\mathrm{DC}} = \sqrt{\frac{34\,\mathrm{nH}}{330\,\mathrm{nF}}} \cdot 350\,\mathrm{A} + 750\,\mathrm{V} = 862\,\mathrm{V}. \tag{4.112}$$

It indicates that the DC-snubber with equal capacitance has to be rated for higher peak voltage or has to be designed larger to lead to similar peak voltages as with the active snubber.

4.7 Continuous Operation at Low Load Current

Similar to Section 4.6 the turn-on and turn-off model are alternately used to calculate the active snubber behavior as presented by [118]. In this section, a low operation current is subject of manner. While the same timing is used for t_{f12} and t_{2opt}, the timing for t_{f23} is adjusted according to the measurement with 25 ns, see Sect. 4.5.

The corresponding snubber voltage and snubber current calculation are shown in Figures 4.16 and 4.17 respectively starting with a DC-link voltage of 750 V. Similarly, each odd switching event represents a turn-on and each even switching event represents a turn-off. During the decreasing current slope at the reverse recovery peak current, the voltage at the passive system rises. Before the very first turn-on event, the snubber capacitor is charged up to the level of the DC-link voltage. Hence, the voltage of the passive switch can rise only

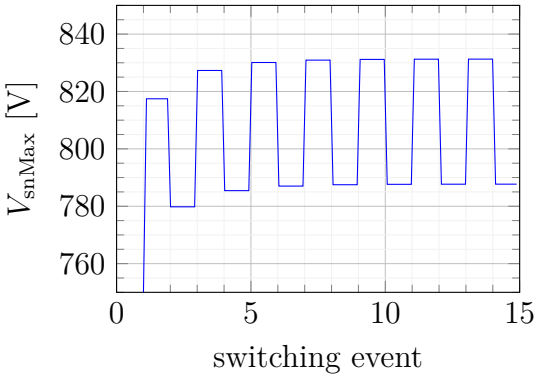


Figure 4.16: Development of snubber voltage over subsequent switching events at 50 A
odd numbers: turn-on, even numbers: turn-off

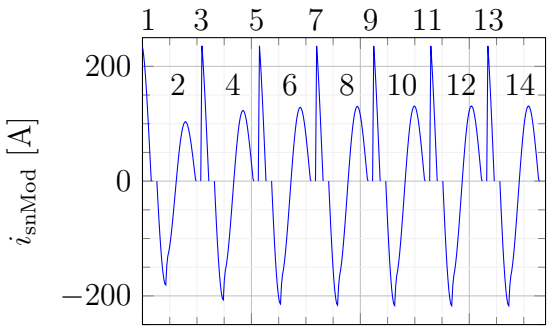


Figure 4.17: Development of snubber current over subsequent switching events at 50 A
odd numbers: turn-on, even numbers: turn-off

slightly above this level until the body diode of the auxiliary switch becomes conductive and allows commutation of the energy stored in L_{main} into the snubber capacitor, cf. Figs. 4.16 and 4.17. Making use of the simplified principle used to derive (4.111), this initial snubber charge increases the snubber voltage to a value of approximately

$$\begin{aligned} V_{\mathrm{snMaxOn}}(1) &\approx \sqrt{\frac{L_{\mathrm{main}}}{C_{\mathrm{sn}}}} \cdot I_{\mathrm{rrm}} \cdot (1 - \frac{1}{4}Q) + V_{\mathrm{sn0}} \\ &= \sqrt{\frac{34\,\mathrm{nH}}{330\,\mathrm{nF}}} \cdot 234\,\mathrm{A} \cdot (1 - \frac{1}{4} \cdot 0.176) + 750\,\mathrm{V} \\ &= 822\,\mathrm{V}, \end{aligned} \tag{4.113}$$

slightly above the complex model simulation, see No. 1 in Fig. 4.16, due to the relation between t_5 and v_{sn}. However, this approximation can be challenged due to the simplifications made to model the effective capacitance of the passive switch $C_{\mathrm{oss*}}$ which does not include a current dependency as well as the points mentioned on Page 76. Thus, a current dependency of I_{rrm} is not considered. Additionally, is was shown in Section 4.3 that the turn-on model overestimates the recovery peak current I_{rrm} and as a consequence, a lower voltage increase can be expected in practice.
However, even at very low current values a reverse recovery peak above zero can be expected due to the voltage slope triggering the oscillation circuit between L_{main} and $C_{\mathrm{oss*}}$ with a characteristic described by (3.25) and (3.26), cf. also the measurements on Page 99. As it can be seen in Figure 4.17 the reverse recovery peak current, much higher than the load current, provides significant energy which cannot be fed to the load in total during the turn-off event due to the low load current. This energy adds up to the already stored energy in C_{sn} and causes a significant negative snubber current peak in the subsequent turn-off events.
To obtain the mean snubber voltage, the approach according to the previous section shall be examined. Although (4.108) stays valid and predicts a plausible value of

$$i_{\mathrm{snOff}}(t_3) \approx -234\,\mathrm{A}\left(1 - \frac{1}{2}0.176\right) + 50\,\mathrm{A} \cdot 0.92 = -167\,\mathrm{A}, \tag{4.114}$$

it must be extended to get the positive peak value at

$$t_{4\mathrm{LowMax}} = \frac{t_{4\mathrm{Low}} + t_4}{2}, \tag{4.115}$$

cf. No. 14 in Fig. 4.17 with Fig. 4.12. The extension must consider the proceeding current oscillation until the maximum occurs which lead to

$$\begin{aligned} i_{\mathrm{snOff}}(t_{4\mathrm{LowMax}}) &\approx -i_{\mathrm{snOff}}(t_3)\left(1 - \frac{1}{2}0.176\right) \\ &= 167\,\mathrm{A}\left(1 - \frac{1}{2}0.176\right) = 152\,\mathrm{A}. \end{aligned} \tag{4.116}$$

Substitution of $i_{\mathrm{snOff}}(t_3)$ in (4.109) lead to the final value of

$$\begin{aligned} V_{\mathrm{snMaxOff}} &\approx \sqrt{\frac{L_{\mathrm{main}}}{C_{\mathrm{sn}}}} i_{\mathrm{snOff}}(t_{4\mathrm{LowMax}})\left(1 - \frac{1}{4}Q\right) + V_{\mathrm{DC}} \\ &= \sqrt{\frac{34\,\mathrm{nH}}{330\,\mathrm{nF}}} 152\,\mathrm{A}\left(1 - \frac{1}{4}0.176\right) + 750\,\mathrm{V} \\ &= 796\,\mathrm{V}. \end{aligned} \tag{4.117}$$

The estimated voltage according to (4.117) predicts a higher value than simulated, cf. Fig. 4.16, due to the already mentioned relation between t_5 and v_{sn}.
The maximum value V_{snMaxOn} is calculated under similar constraints with (4.110) resulting in a value lower than simulated as

$$\begin{aligned} V_{\mathrm{snMaxOn}} &\approx \sqrt{\frac{34\,\mathrm{nH}}{330\,\mathrm{nF}}} \cdot 234\,\mathrm{A} \cdot \left(1 - \frac{1}{4} \cdot 0.176\right) + 750\,\mathrm{V} \\ &= 822\,\mathrm{V}. \end{aligned} \tag{4.118}$$

The higher simulated value is also related to the relation between t_5 and v_{sn} and thus, to the stored energy. The error made due to this relation causes an increased V_{snMaxOn} similar to a decreased V_{snMaxOff}. However, due to this error made in both V_{snMax}-value, the mean snubber voltage is calculated by (4.111) with a good estimation to the value in Fig. 4.16 as

$$V_{\mathrm{snMean}} \approx \frac{796\,\mathrm{V} + 822\,\mathrm{V}}{2} = 809\,\mathrm{V}. \tag{4.119}$$

As already mentioned in Section 4.3 the model accuracy can, indeed, be challenged for lower load currents due to the overlap of the v_{DS2} voltage slope with the subsequent intervals. Therefore, both models, for turn-on and turn-off, can only be used as a hint to estimate the behavior in terms of tendencies for pure low current operation.
Further, the absolute value of the active snubber damping losses depicted in Fig. 4.18 can similarly be challenged. Due to the overestimation of the reverse recovery peak and the squared relation between current and energy stored in the stray inductance, lower damping losses can be expected in practice. Examining the damping losses at each turn-on, a decreasing tendency converging to a value slightly below $150\,\mu\mathrm{J}$ can be noticed, cf. Fig. 4.18. This decreasing tendency is plausible and can be explained as follows. At the very first turn-on, the snubber capacitor is charged to the value of the DC-link voltage. Thus, the current in the stray inductance at t_4 can commutate into the snubber capacitor

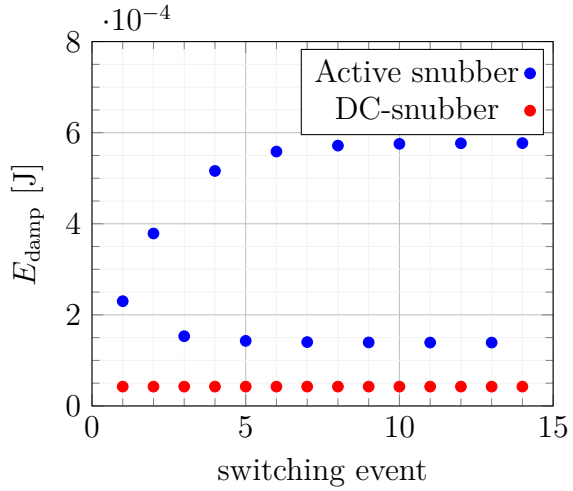


Figure 4.18: Simulated damping losses for subsequent switching events at 50 A

without counteraction. With progressed switching, the snubber voltage increase and thus, the counteraction increase as well and leads to a shorter duration $t_4 \leq t < t_5$. With similar peak current but shorter duration, the damping losses decrease with increasing snubber voltage.
Contrary to the turn-on damping losses, the damping losses for turn-off increase as well for progressed switching. With increasing mean snubber voltage, the energy fed to the load at each turn-off, increase as well. This leads to higher current values and thus to higher damping losses due to the fixed resonance period. Due to the squared dependency of the losses from the current, the damping losses increase much more compared to the decreasing turn-on damping losses. Hence, the total damping losses estimated by the challengeable low current model increase to a constant value for progressed switching.

4.8 Continuous Operation at Sinusoidal Load Current

For practical considerations, especially in main inverter application, a sinusoidal load current is calculated in this section as presented by [118]. To simulate this application, the load current is changed for each switching event to obtain a sinusoidal current shape for a sine half wave. Beginning at zero current, 100 subsequent switching events are calculated with respect to the two operation modes discussed previously. Thus, this calculation is used to predict the behavior for a common operation with a switching frequency of $f_{\text{sw}} = 10\,\text{kHz}$ and a load current frequency of $f_{\text{AC}} = 50\,\text{Hz}$. A current peak value of 350 A is chosen to show the transition from low current operation to high current operation mode. Similar to the previous sections, the duty-cycle is chosen to be constant at 50 % and the timing of descending current and voltage slopes are adapted to the operation mode with respect to the load current.

The calculated snubber voltage and snubber current are shown in Figures 4.20 and 4.19. It can be noticed that for the very first switching event close to the first zero crossing of the load current, the snubber voltage starts at DC-link voltage and need to converge similar as described in the two previous sections. Hence, the predicted values differ to the second zero crossing, at which the circuit has been converged. By comparing the predicted snubber voltage after the switching event shown in Figure 4.19 with the two predictions

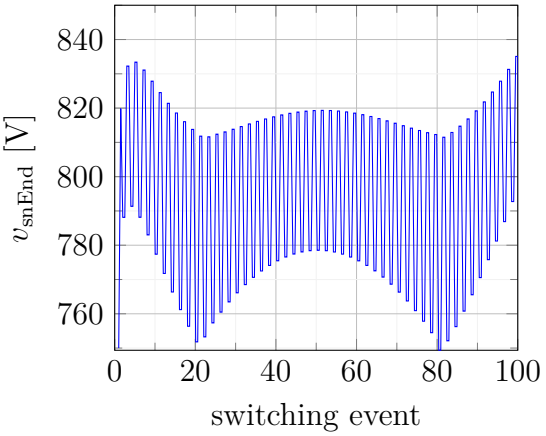


Figure 4.19: Development of snubber voltage over subsequent switching events at sinusoidal load current
odd numbers: turn-on, even numbers: turn-off

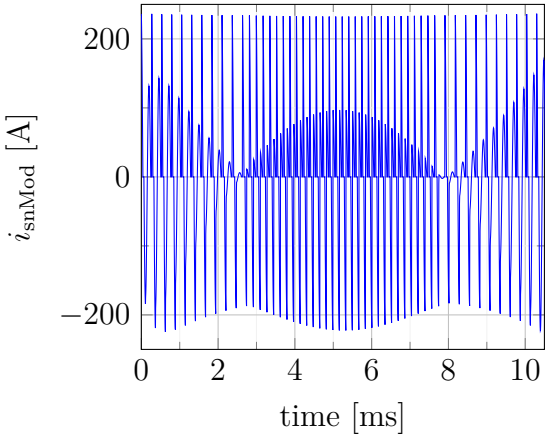


Figure 4.20: Development of snubber current over subsequent switching events at sinusoidal load current
odd numbers: turn-on, even numbers: turn-off

at continuous load current in Figs. 4.16 and 4.13, a similar result with higher end voltage at lower current values is predicted. Around switching event 20 and switching event 80, similar to 2 ms and 8 ms, the load current is close to the reverse recovery peak current. In Section 4.7 it has been mentioned that at this load current, the energy stored in the snubber during turn-on, reduces the DC-link current at turn-off to zero. Comparing both values the snubber current as well as the snubber voltage at this point, the predicted values for low and high current operation mode predict similar values and offer a plausible transition.
Because it has been shown in Section 4.6 that both models show a good prediction for the operation at high load current, the predicted values can be treated as valid from approximately switching event 20 to 80 or 2 ms to 8 ms respectively. The shown prediction out of this interval is at low current operation mode. In Section 4.7 it has already been discussed that the model at low current operation shows a weak prediction of the snubber end voltage and snubber current in this operation mode. However, treating the calculation for low load current as a worst case estimation, the snubber voltage and current increase closer to the zero crossing of the load current but remain in an uncritical range indicating a stable behavior. Of course it should be considered at this point that at the not depicted subsequent negative half wave the switch Q_1 is the turning off switch and the auxiliary switch timing has to be synchronized to Q_1.
In Figure 4.21 the calculation of the damping losses for the active snubber according (4.31) and (4.79) as well as the damping losses for the DC-snubber according (2.28) are depicted. The difference between turn-on and turn-off - leading to a alternating damping loss value - is not depicted separately but is depicted as a sum of the damping loss of a turn-on and the damping loss of the subsequent turn-off event. Hence, each depicted value shows the sum of two subsequent switching events which allows a better comparison.
Figure 4.21 shows that the damping losses are strongly reduced compared to the DC-snubber at load current values above approximately 125 A. Considering the over estimation of both models at low current operation mode, a slightly lower load current value can

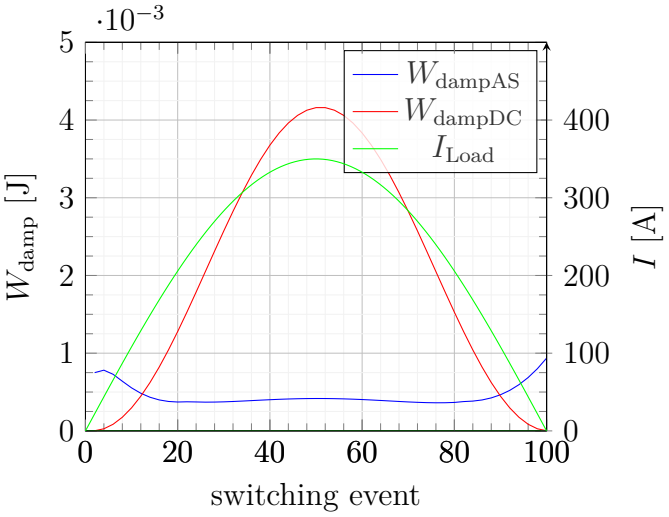


Figure 4.21: Damping losses for sinusoidal load current after [118]

be assumed. In conclusion, the reduced damping losses compared to a DC-snubber allow the application at more harsh conditions. Thus, the active snubber is feasible at much higher load current values or switching frequencies. Further, the cooling conditions for the capacitor can be simplified, e.g. by placing the capacitor not inside the power module on the substrate for good cooling but on driver board.

To estimate the mean expectable damping losses for the DC-snubber $\overline{W_{\mathrm{dampDC}}}$ and for the active snubber $\overline{W_{\mathrm{dampAS}}}$, the shown losses over all 50 switching periods are calculated with

$$\overline{W_{\mathrm{dampDC}}} = \frac{1}{100}\sum_{n=0}^{100} E_{\mathrm{dampDC}} = 2.06\,\mathrm{mJ} \quad \text{and} \tag{4.120}$$

$$\overline{W_{\mathrm{dampAS}}} = \frac{1}{100}\sum_{n=0}^{100} E_{\mathrm{dampAS}} = 456\,\mu\mathrm{J}, \tag{4.121}$$

which results - by considering both switching events - in a dissipated power of

$$P_{\mathrm{dampDC}} = \overline{E_{\mathrm{dampDC}}} \cdot f_{\mathrm{sw}} = 2 \cdot 2.06\,\mathrm{mJ} \cdot 10\,\mathrm{kHz} = 20.6\,\mathrm{W} \quad \text{and} \tag{4.122}$$

$$P_{\mathrm{dampAS}} = \overline{E_{\mathrm{dampAS}}} \cdot f_{\mathrm{sw}} = 2 \cdot 456\,\mu\mathrm{J} \cdot 10\,\mathrm{kHz} = 4.6\,\mathrm{W} \tag{4.123}$$

respectively. Further, the damping loss development allows to deviate a reasonable change in controlling the auxiliary switch or when a DC-snubber is the better choice. By focus on switching events above 80, at which the circuit is converged, the damping losses of the active snubber exceed the damping losses of the DC-snubber at approximately switching event 90 and a load current of 110 A, cf. Fig. 4.21. This marks a tipping point. Neglecting the overestimation of the operation at low current and the additional influence of the on-state-resistance of the auxiliary switch not present for the DC-snubber, it can be concluded that for load current value below this current $I_{\mathrm{LoadTip}} = 110\,\mathrm{A}$ the operation as a DC-snubber gets more beneficial with the chosen setup in terms of damping losses. This can be done by permanently activated auxiliary switch.

Considering the fact that for negative load current values, the turn-off sequence of the active snubber had to be applied for the top-side switch Q_1 and for positive current values for Q_2, a change in the auxiliary switch controlling is necessary. Thus, a proposal for controlling the auxiliary switch can be given as follows. At positive load current values above I_{LoadTip} the auxiliary switch timing is applied as described exemplary in this work for the switch Q_2. For load current values in the range $I_{\mathrm{LoadTip}} > I_{\mathrm{Load}} > -I_{\mathrm{LoadTip}}$ the auxiliary switch is permanently turned on to use the circuit as a DC-snubber. Similarly, for load current values below $-I_{\mathrm{LoadTip}}$, the auxiliary switch timing is applied for the switch Q_1. Further, for this suggested auxiliary switch timing, with an interval of permanent activation, considerations for an optimal transition for a change from Q_2 to Q_1 timing is not necessary.

5 Setup Comparison

While in the previous work the focus was kept on the description and modeling of the optimized commutation circuit, this chapter is about its behavior compared to the similar setups introduced in Section 4.6. At selected operation points, the system stray inductance is varied to outline its influence. Further, key parameters of the setups are compared within an expectable operation range with different DC-link voltages, load currents and switching speeds adjusted by varying the gate resistors and remarkable effects and characteristics are discussed. Subsequently, all setups are dimensioned for a hypothetical inverter operation with respect to maximum allowable switching speed at which the maximum specified breakdown voltage of 1200 V is not exceeded. To enable a proper inverter dimensioning, the static behavior and the thermal resistance are evaluated first. Finally, the maximum achievable output power is estimated at different DC-link voltages for $\vartheta_\mathrm{j} = 25\,$řC to evaluate the efficiency at different operation conditions and estimate a potential application power range for the different setups.

5.1 Finding Appropriate Gate Resistors

At first, a basic characterization was done where DC-link voltage, load current and the gate resistors for turn-on and turn-off are varied with values as shown in Table 5.1. The measurements were performed at a junction temperature of $T_\mathrm{j} = 25\,^\circ$C. However, it should be mentioned that especially the dynamic behavior of the body diode is temperature dependent [122]. Goal of the measurement plan is to find the maximum switching speed which can be allowed at a defined condition.

Table 5.1: Varied parameter for characterization

V_DC [V]	I_Load [A]	R_Gon [Ω]	R_Goff [Ω]	$L_{\sigma\mathrm{On}}$ [nH]
450	50	5	5	37
600	200	2	2	47
750	350	1	1	
		0.5	0.5	

While the lower DC-link voltage and load current values were performed first, each test series begins with the highest gate resistor to ensure that the maximum allowed drain-source peak voltage of 1200 V is not exceeded. Then, keeping DC-link voltage and load current, the gate resistor was reduced until further reduction would lead to a critical overvoltage. Subsequently, the DC-link and load current were successively increased in terms of a full factorial design.

5.1.1 Turn-Off Event

To find the maximum switching speed allowed, the mentioned above experimental design was performed with each setup, the conventional halfbridge (HB), the DC-Snubber setup

(SN) and the active snubber setup (AS). It has been found that the highest drain-source voltage peak at turn-off appears in each setup at a DC-link voltage of 750 V and a load current of 350 A. The overvoltage for each setup at different stray inductances as a function of R_{Goff} is given in Figure 5.1. It should be mentioned that R_{Goff} is meant to be the external gate resistor applied between the power module and the driver and does not include the chip internal gate resistor.

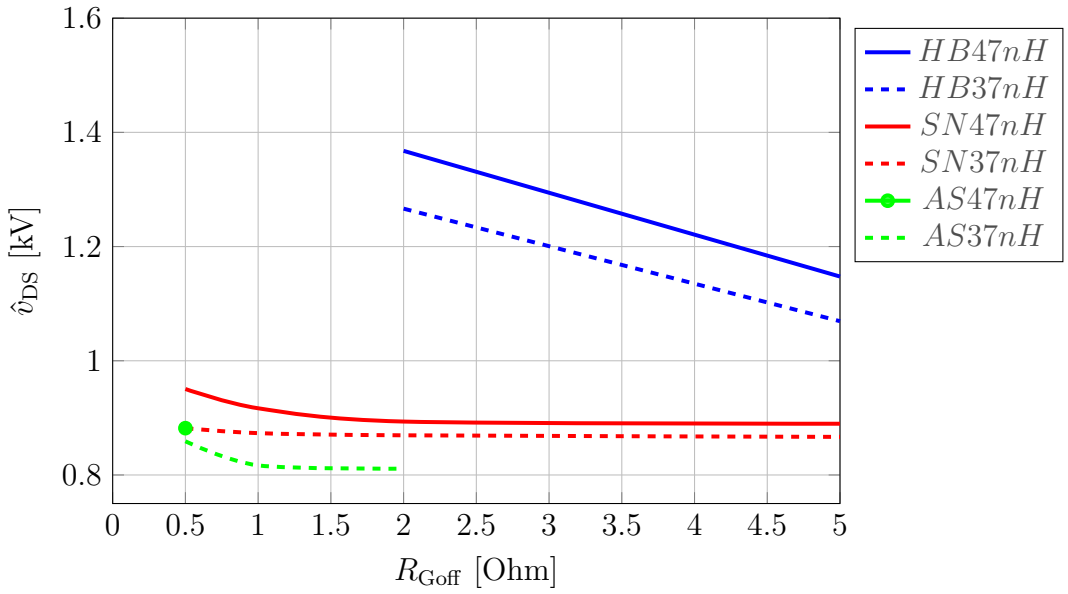


Figure 5.1: Turn-off overvoltage for the three different setups for $V_{\mathrm{DC}} = 750\,\mathrm{V}$ and $I_{\mathrm{Load}} = 350\,\mathrm{A}$

Figure 5.1 shows that the conventional halfbridge suffers strongly from the high main stray inductance and the allowed maximum drain-source voltage is exceeded at gate resistors below $3\,\Omega$ for the 37 nH setup and below $4.25\,\Omega$ for the 47 nH setup respectively. However, it can be discussed whether the chosen setup stray inductance is comparable to practical setups. This is evaluated by comparing the two chosen stray inductance values to the stray inductance given in the data sheet of a similar module commercially available. For example, according to its datasheet [126], the FF6MR12W2M1P-B11 is specified with 35 nH for the setup and 8 nH for the power module. Because the defined main stray inductance is the sum of both, this leads to a value of $L_{\mathrm{mainFF6}} = 43\,\mathrm{nH}$ and therefore, the two chosen values in this work can be kept to lead to a realistic result. Hence, for further comparison, the gate resistor for the turn-off of the conventional halfbridge is selected to be the next characterized value from the measurements as $R_{\mathrm{GoffHB}} = 5\,\Omega$.

For the DC-Snubber setup, it can be noticed that the maximum voltage is constant within a wide range of different gate resistors. This effect is related to the snubber capacitor which stores the energy of the stray inductance. Hence, with respect to (2.29), this voltage can be calculated in good approximation to

$$V_{\mathrm{DSmax}} = 750\,\mathrm{V} + \sqrt{\frac{37\,\mathrm{nH}}{330\,\mathrm{nF}}} \cdot 350\,\mathrm{A} = 870\,\mathrm{V} \tag{5.1}$$

For very low gate resistance values, the stray inductance through the snubber path $L_{\sigma\mathrm{Off}}$ according to (3.1) becomes significant and causes the highest drain-source voltage due to

the fast switching speed. Further, this indicates that a gate resistor could be selected which is even below the smallest chosen value of 0.5 Ω. However, at $R_{\mathrm{Goff}} = 0.5\,\Omega$, the maximum resolvable current fall time with the chosen Rogowski coil is reached, as already described at Page 55. As a result, a lower gate resistance value would not lead to true measurement values which might not be reproducible. Thus, a gate resistor of $R_{\mathrm{GoffSN}} = 0.5\,\Omega$ is the lowest applicable value within the available measurement conditions.
A similar overvoltage characteristic is shown by the active snubber setup. The maximum voltage peak for gate resistors above 1 Ω is constant. As described in Section 4.6 the measurement was performed as a double pulse while the second turn-off event was used to ensure that energy stored in the snubber capacitor. Additionally, it has already been described in Sect. 4.6ff. that this voltage value does not represent the maximum voltage as it can be expected in inverter operation. Because the maximum voltage overshoot occurs in high current operation mode, and the measured peak voltage value of 816 V is below the expectable maximum snubber voltage according Fig. 4.13 with 820 V, the assumption can be made that for gate resistors above 1 Ω, the maximum snubber voltage defines the highest drain-source voltage. This assumption can be validated by analyzing the switching curve, cf. Fig. 5.2. It can be seen that with a gate resistor of 1 Ω, the highest voltage occurs at the switching event and thus, it is caused by $L_{\sigma\mathrm{Off}}$. Contrary to that, for 2 Ω, the highest voltage occurred due to the snubber charging which does not depend on the switching speed but on the load current and the energy management by the manner of operation of the active snubber circuit.
Furthermore, for smaller gate resistors, e.g. 0.5 Ω, the peak voltage of the active snubber setup and for the DC-snubber setup at $L_{\mathrm{main}} = 34\,\mathrm{nH}$ converge to each other. This indicates that for faster switching speeds $L_{\sigma\mathrm{Off}}$ is more relevant in terms of peak voltage reduction as the snubber voltage.
Because for current measurement the same Rogowski coil was used, the selection of the gate-resistor for the active snubber relates to the same limitation of resolvable current slope and thus, a gate-resistor of $R_{\mathrm{GoffAS}} = 0.5\,\Omega$ is used for further investigation.

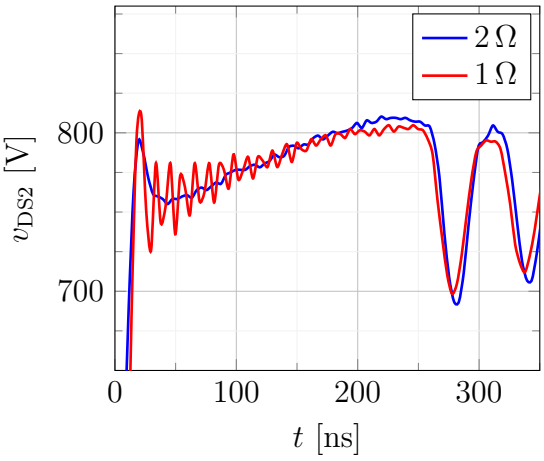


Figure 5.2: Active snubber v_{DS2} for different R_{Goff} at 750 V, 350 A

5.1.2 Turn-On and Diode Recovery

In the previous section, the minimum allowed gate resistor for turn-off at a DC-link voltage of 750 V and a load current of 350 A was selected for each of the three setups to compare. This section focuses on the selection of the gate-resistor for turn-on with respect to the maximum voltage peak at reverse recovery of the device body diode. The characterization has been done according to Table 5.1 and it has been found that for the DC-snubber setup and the active snubber setup the maximum voltage occurs at a load current of 350 A. Contrary to that, the body diode in the conventional halfbridge setup shows the highest voltage at a load current of 200 A, cf. Fig. 5.3. All setups show the

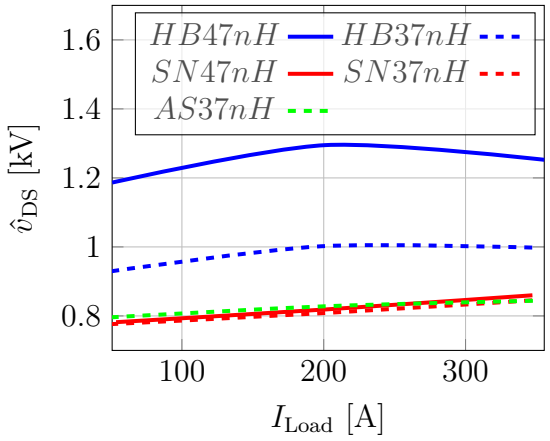


Figure 5.3: $\hat{v}_{DS}$ as a function of I_{Load} at $R_{Gon} = 2\,\Omega$ and 750 V

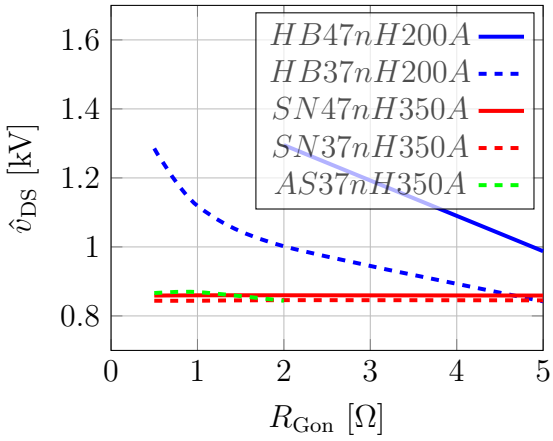


Figure 5.4: $\hat{v}_{DS}$ as a function of R_{gon} at 750 V

highest peak voltage at a DC-link voltage of 750 V. Both Figures, 5.3 and 5.4, indicate that the conventional halfbridge setup suffers strongly from a comparatively high stray inductance and at a load current of 200 A the increase of the inductance from 37 nH to 47 nH causes about 300 V higher peak voltage. Therefore, with respect to Figure 5.4 a gate resistor for the 47 nH setup of $R_{GonHB47} = 5\,\Omega$ and for the 37 nH setup a resistor of $R_{GonHB37} = 1\,\Omega$ must be selected.

The voltage peak of the DC-snubber setup is subject of the same relation as for the turn-off event and can be estimated with (5.1). However, while at the turn-off event, for lower gate resistors the peak voltage is mainly determined by $L_{\sigma Off}$ leading to a higher voltage as estimated with (5.1), this effect cannot be observed for the DC-snubber at diode recovery. Because the DC-snubber is permanently connected, a significant amount of charge is provided by the snubber during the turn-on event. As a result, the snubber is discharged to a lower voltage, which is still present during the voltage peak occurring during diode recovery, see v_{sn} in Fig 5.5. This lower snubber voltage compensates the increased voltage occurring during the negative current slope of the reverse recovery peak. Therefore, for the DC-snubber setup, the lowest gate resistor according Table 5.1 can be selected as $R_{GonSN} = 0.5\,\Omega$.

For the active snubber, the body diode of the turned off Q_{aux} for the active snubber prohibits this discharge of C_{sn} during turn-on. As it can be seen in Figure 5.3 for load current values below 200 A the maximum snubber voltage for the active snubber exceeds the maximum voltage of the DC-snubber. The previously presented model for turn-on predicts that for lower load currents the maximum snubber voltage increases due to the energy stored during turn-on, which cannot be retrieved in total at turn-off, cf. e.g. Section 4.8. On the one hand, due to the performed double pulse measurement, the usage of the measured V_{snMax} value for gate resistor selection might be challenged in terms of transferability to the model prediction. The model indicates that the highest voltage is close to the zero crossing of the load current. On the other hand, as already been discussed on Page 78, the model overestimates the reverse recovery peak current and thus, the stored energy. Therefore, the measured highest voltage value measured at a load current of 350 A was used for selecting a proper gate resistor. As shown in Figure 5.4, the diode recovery in the active snubber setup causes a higher voltage peak for lower gate resistors compared to the DC-snubber. Comparing the characteristics of the DC-snubber

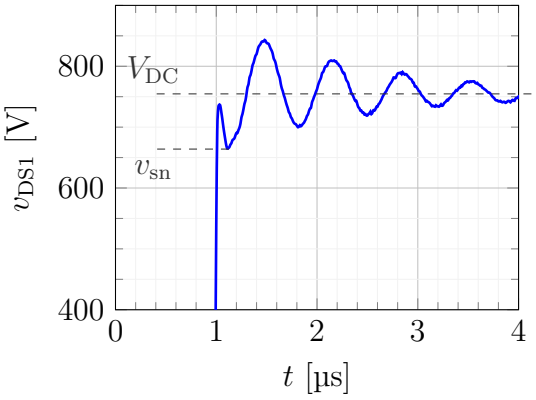


Figure 5.5: DC-snubber v_{DS1} for 750 V, 350 A with $R_{Gon} = 2\,\Omega$

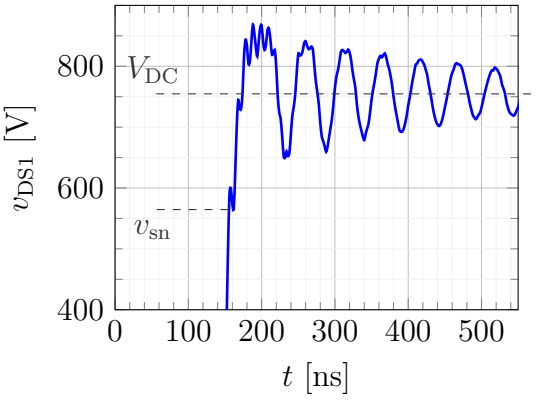


Figure 5.6: AS snubber v_{DS1} for 750 V, 350 A with $R_{Gon} = 1\,\Omega$

in Fig. 5.5 with those of the active snubber in Fig. 5.6, a similar initial voltage drop, cf. v_{sn}, can be recognized but with a stronger reduction for the active snubber. This relation can be explained similar to the DC-snubber. v_{sn} is lower at the active snubber setup due to the non linear voltage dependent output capacitance of Q_{aux} acting as a small DC-snubber capacitance at this point. While at the DC-snubber setup, the large snubber capacitor can provide more charge leading to a lower reduction, the output capacitance of Q_{aux} is lower and thus, v_{sn} is reduced to lower voltage. This lower voltage leads to a reduced initial voltage peak at $t = 159\,\text{ns}$ during the rising v_{DS1} for both snubber setups even below V_{DC}. The increasing output capacitance of Q_{aux} with increasing v_{DS1} and hence decreasing v_{DSaux} causes a smoothing effect until its body diode becomes conductive. Afterwards, the snubber charges and leads to the maximum of v_{DS1}. Nevertheless, the difference between both setups can be neglected for gate resistor selection because all used R_{Gon}-values led to uncritical maximum voltages, see Figs. 5.5 and 5.6. Hence, the same gate resistor for the turn-on event can be chosen for the active snubber setup similarly to the the DC-snubber setup to $R_{GonAS} = 0.5\,\Omega$.
In summary, the gate resistors for driver placement shown in Table 5.2 were chosen according to the above mentioned restrictions. Similarly, the gate resistors for both snubber setups are chosen with respect to resolvable current rise and fall time due to the limitations of available and suitable current probes. Therefore, the hypothesis can be made that faster switching with gate resistors below $0.5\,\Omega$ is feasible and reasonable with respect to further switching loss reduction.

Table 5.2: Chosen gate resistors

Setup	$L_{\sigma On}$ [nH]	R_{Gon} [Ω]	R_{Goff} [Ω]
Halfbridge	47	5	5
Halfbridge	37	1	5
DC-snubber	47	0.5	0.5
DC-snubber	37	0.5	0.5
Active snubber	47	0.5	0.5
Active snubber	37	0.5	0.5

5.2 Comparing Switching Waveforms

In this section, the switching waveforms of each setup are compared with focus on points indicating remarkable differences and effects to be discussed. This is done with focus on practical relevance and also for the active snubber with respect to model predictions to give the reader a better understanding of characteristics shown in later sections. Based on former chapters, a DC-link voltage of 750 V with the gate resistors shown in Table 5.2 is used and the characteristics are compared at load current values of 350 A and 50 A. For comparing the waveforms the setup with $L_{\sigma\mathrm{On}} = 37\,\mathrm{nH}$ is chosen because faster switching is possible and therefore, interesting effects are more pronounced.

5.2.1 Comparison of the Turn-Off Event

The overlay of the turn-off waveforms at a load current of 350 A for all three setups is shown in Figure 5.7. Similarly, the abbreviations 'HB' indicates the conventional halfbridge, 'SN' and 'AS' the DC-snubber and the active snubber setup respectively. The waveforms represent the highest allowed or achieved switching speed for the halfbridge setup in terms of $\hat{v}_{\mathrm{DS}}$ or the highest feasible for both snubber setups in terms of resolvable current slope.

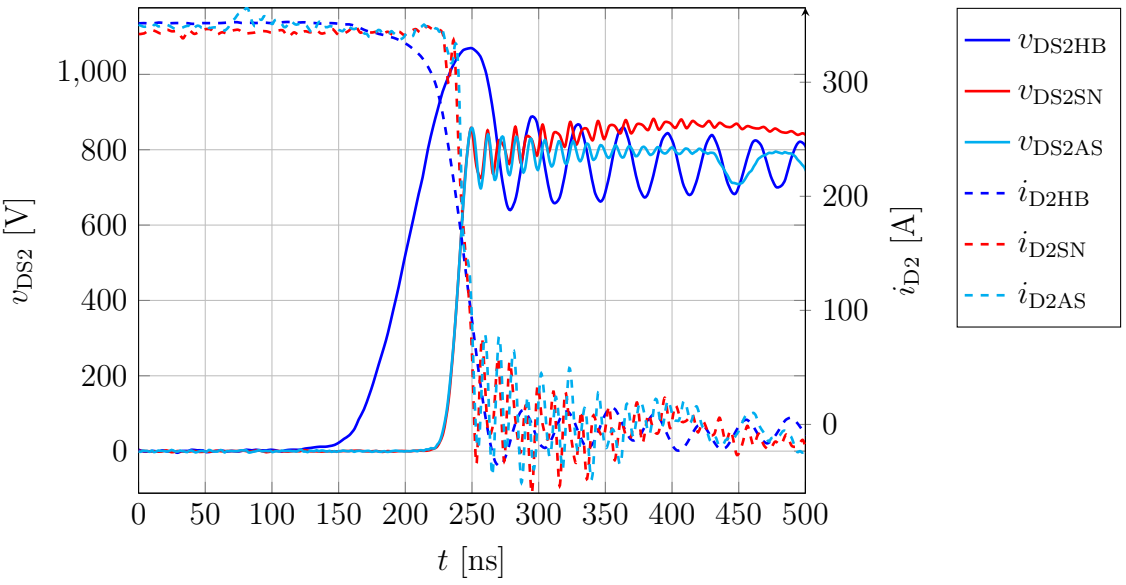


Figure 5.7: Turn-off comparison for $L_{\sigma\mathrm{On}} = 37\,\mathrm{nH}$ at 350 A

By analyzing the current and voltage waveform of the halfbridge, it can be noticed that with increasing drain-source voltage, the drain current i_{D2HB} shows a slightly negative slope, cf. Fig. 5.7 for $100\,\mathrm{ns} < t < 220\,\mathrm{ns}$. The reduction of the drain current can be explained with the displacement current through the output capacitance of Q_1, see Sect. 2.3.1. Separately from the snubber and the DC-link parasitics, according to Figure 3.4, the drain current can be calculated with

$$i_{\mathrm{D2}} \approx I_{\mathrm{Load}} + i_{\mathrm{D1}} = I_{\mathrm{Load}} + C_{\mathrm{oss1}}(v_{\mathrm{D1}})\frac{\mathrm{d}v_{\mathrm{DS1}}}{\mathrm{d}t}. \tag{5.2}$$

With a maximum voltage slope for the halfbridge measured as $16\,\mathrm{kV}/\mu\mathrm{s}$ at this load current and neglecting the parasitics and non-linearities, a displacement current of 32 A can be estimated considering a mean voltage dependent $C_{\mathrm{oss1}} \approx 1\,\mathrm{nF}$, cf. Fig. 4.9 with four dies in parallel. Carefully applying this estimation on both snubber setups, cf. i_{D2SN} and i_{D2AS} in Fig. 5.7, a displacement current related drain current drop can be noticed for both snubber variants at approximately 240 ns but is not appearing despite of a small dip before 240 ns. The theory predicts a current drop of 60 A for the about $60\,\mathrm{kV}/\mu\mathrm{s}$. An additional point to mention is the slight current peak in i_{D2AS} at 75 ns, which is not appearing in i_{D2SN}. This peak is related to the turning on Q_{aux}. As illustrated in Fig. 3.3 at t_1, v_{DSaux} decreases to zero and thus, v_{DS1} increases. Its output capacitance is charged by a current mainly provided by the snubber added to the continuous load current.
Comparing the voltage signals in Fig. 5.7 the halfbridge is turned off much slower and causes a higher voltage overshoot due to the large L_{main}. Contrary to that, both snubber voltages behave identically until the low voltage peak at 250 ns caused by the low $L_{\sigma\mathrm{Off}}$. Then, a high frequency oscillation between the very low stray inductance and the output capacitance occurs, see (4.24). Afterwards, the DC-snubber charges and leads to a further increasing v_{DS2SN} with a maximum at approximately 420 ns. Contrary to that, the active snubber shows also a slight increase with superimposed high frequency signal but much lower as for the DC-snubber. This fits to the already given description in Sect. 4.6 related to the DC-link current reduction. While the DC-snubber oscillation continues for $t > 420\,\mathrm{ns}$, the auxiliary switch of the active snubber goes into blocking state and thus, the remaining energy in the charged up C_{oss2} starts oscillating with $L_{\sigma\mathrm{On}}$ at a frequency of

$$f = \frac{1}{2\pi\sqrt{L_{\sigma\mathrm{On}} C_{\mathrm{oss2}}}} \approx \frac{1}{2\pi\sqrt{37\,\mathrm{nH} \cdot 1\,\mathrm{nF}}} = 26.2\,\mathrm{MHz}. \tag{5.3}$$

Here, an assumed to be linear $C_{\mathrm{oss2}} = 1\,\mathrm{nF}$ for four dies in parallel at $V_{\mathrm{DC}} = 750\,\mathrm{V}$, cf. also Fig. 4.9 is used.

As it can be seen in Fig. 5.8 the snubber setups at $I_{\mathrm{Load}} = 50\,\mathrm{A}$, contrary to the conventional halfbridge, do not show the mentioned displacement current related current drop during the voltage drop either, cf. Fig. 5.8 for $230\,\mathrm{ns} < t < 260\,\mathrm{ns}$. i_{D2AS} even increases at the beginning voltage slope. Comparing the drain-source voltage slope of both snubber setups with Fig. 5.7, the rise time is lower. Questioning the measured current values and considering that only the load current can charge the two output capacitances of $C_{\mathrm{coss1}}(V_{\mathrm{DS1}}) || C_{\mathrm{coss2}}(V_{\mathrm{DS2}}) \approx 2\,\mathrm{nF}$ a voltage slope of approx. $25\,\mathrm{kV}/\mu\mathrm{s}$ can be calculated. This fits very well to the measured voltage slope in Fig. 5.8 and allows to conclude that in this case the quasi-soft turn-off appears mentioned in Sect. 2.3.2. Further, this allows to questionate the rising measured drain current i_{D2AS} during the voltage slope and as a result, the measured switching losses might be much higher than the real turn-off losses. This effect is further investigated at the end of this section.
An additional remarkable fluctuation effect can be noticed in the current waveform of the active snubber setup in both Fig. 5.7 and 5.8 within the time range from 60 ns to 220 ns. At $t = 60\,\mathrm{ns}$ the auxiliary switch is turned on rapidly. As shown in Figure 3.3, this increases the voltage v_{DS1}, which drives a displacement current through C_{oss1}. According (5.2), this displacement current increases the drain-source current i_{D2}. However, the afterwards changing drain current can be challenged. Considering the equivalent circuit in Fig. 3.1, the turned on switches Q_{aux} and Q_2 during this time span, the approximate

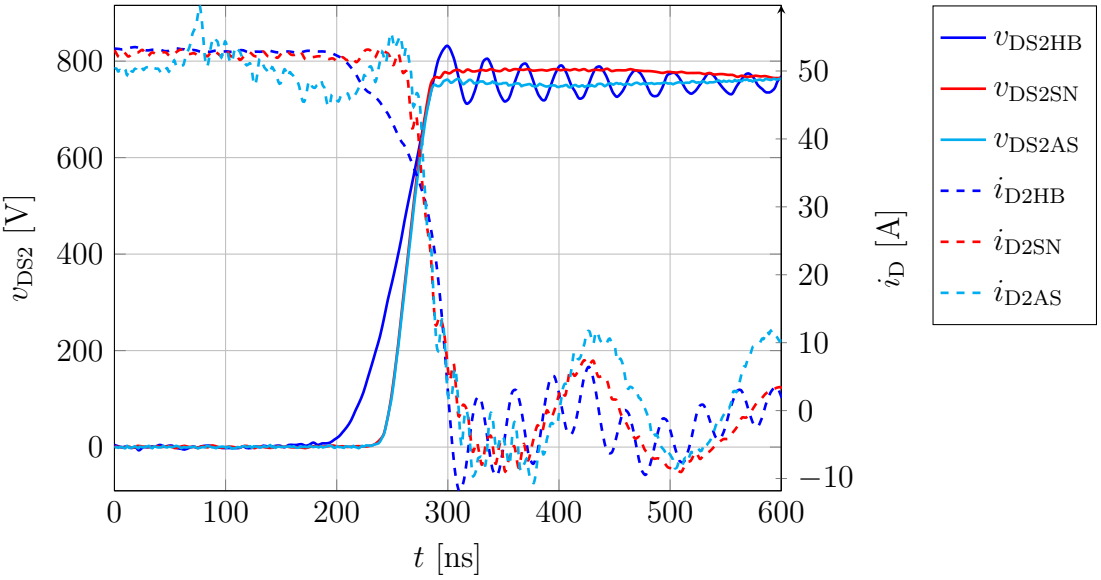


Figure 5.8: Turn-off comparison for $L_{\sigma On} = 37\,\text{nH}$ at 50 A

snubber voltage lies across Q_1. As mentioned in Sect. 4.4 the snubber is charged up to a voltage of 835 V and the DC-link voltage is 765 V. The turned on Q_{aux} results in an oscillation with decreasing snubber voltage and thus, decreasing voltage v_{DS1}. Hence, the assumption can be made, that this voltage change causes a displacement current through C_{oss1} and in conclusion to the observed fluctuation in i_{D2AS}. This hypothesis shall be validated roughly now. The voltage across Q_1 in this interval can be approximated with

$$v_{DS1} = (V_{sn0} - V_{DC}) \cdot \cos(\omega_d t) + V_{DC} \tag{5.4}$$

and leads to its derivative as

$$\begin{aligned} \dot{v_{DS1}} &= -\omega_d \cdot (V_{sn0} - V_{DC}) \cdot \sin(\omega_d t) \\ &= 9.01 \cdot 10^6\,1/\text{s} \cdot (835\,\text{V} - 765\,\text{V}) \cdot \sin(9.01 \cdot 10^6\,1/\text{s} \cdot 140\,\text{ns}) \\ &= -600 \cdot 10^6\,\text{V/s}. \end{aligned} \tag{5.5}$$

With $C_{oss1}(V_{DS1}) \approx 1\,\text{nF}$, this leads to a displacement current of

$$\begin{aligned} i_{D1}(140\,\text{ns}) &= C_{oss1} \cdot \dot{v_{DS1}} \\ &= 1\,\text{nF} \cdot (-600 \cdot 10^6\,\text{V/s}) = 0.6\,\text{A} \end{aligned} \tag{5.6}$$

which is about 10 times lower than the current fluctuation at 200 ns, see Fig. 5.8, which is 140 ns after turning on Q_1. Hence, the change in the snubber voltage does not lead to the measured effect in the drain-source current. Another effect to be mentioned can be noticed as an oscillation of about 6 MHz in the current of both snubber setups after the switching event for $t > 300\,\text{ns}$, see Figs. 5.8 and 4.12. Since various effects are observed, a closer look at these effects is necessary in order to assess how sensitive the measured values react to these effects.

Examination of the measured current effects

In both the 350 A and the 50 A turn-off measurement, effects in the drain current can be observed, which cannot be explained by the expectable circuit behavior based on Fig. 3.4. Hence, other influences not considered yet might have a significant influence.
First, all observations are collected below.

1. The absolute value of the unexplained noticed or expected disturbances seems to be constant. This follows from a comparison of Figs. 5.7 and 5.8, showing that the amplitudes noticed do not scale with the load current. Immediately, this allows to focus on the low load current operation where the effects are more pronounced.

2. A drain current peak occurs with the active snubber not shown with the DC-snubber at the point in time at which Q_{aux} is turned on, see $t = 60\,\text{ns}$ in Fig. 5.8.

3. The drain current fluctuates with the active snubber and not with the DC-snubber between the turning on of Q_{aux} and turning off Q_2, see $60\,\text{ns} < t < 210\,\text{ns}$ in Fig. 5.8.

4. While the conventional halfbridge shows a significant current drop during the whole voltage slope, cf. i_{D2HB} in Fig. 5.8, the current drop at the DC-snubber is less pronounced in spite of a steeper voltage slope. The drain current i_{D2SN} even seams to increase, see $210\,\text{ns} < t < 280\,\text{ns}$ in Fig. 5.8. Further, the active snubber current i_{D2AS} shows a clear increase during the voltage slope.

5. While at the conventional halfbridge i_{D2} goes straight through its zero crossing, both the DC- and active snubber current starts flattening at approximately 290 ns, cf. Fig. 5.8. Both drain currents are shaped similar as a tail current or a beginning oscillation. However, assuming an oscillation, it can be noticed that both currents are very similar until $t = 400\,\text{ns}$ and then start deviating. Further, neglecting the higher superimposed frequency, the drain current at the conventional halfbridge also fluctuates after its zero crossing.

6. By analyzing Fig. 4.12 between $160\,\text{ns} < t < 210\,\text{ns}$, the sinusoidal shape of i_{link} and i_{sn} starts deviating during the voltage slope. After the drain-source voltage has risen to the snubber voltage, i_{link} and i_{sn} equalize again until 230 ns when the calculated i_{D2} crosses zero.

7. Further, analyzing Fig. 4.12 focusing on $320\,\text{ns} < t < 670\,\text{ns}$, the drain current oscillates at approximately 6 MHz. This is related to the measured currents i_{link} and i_{sn} showing an antiphase oscillation in the measured currents considering (4.2).

Initially two basic assumptions can be made leading to different approaches for further investigation. Firstly, it can be assumed that the measured drain current is true and the measurement can be trusted. Hence, the resulting loss estimation for the switching event would be correct. The effects seen might be caused through external components or parasitics not included in the equivalent circuit according Fig. 3.4 or due to the non-linearities of the MOSFETs.
Secondly, the measurement itself can be questioned. As already mentioned on Page 55, the used Rogowski coil cannot resolve the high current slopes. Further, described in

Sect. B.2, the voltage probes and the used coaxial shunt are connected to a common potential at the oscilloscope. While the voltage probes are equipped with common-mode chokes implemented as ferrites to suppress circular currents through the probe wires, this might be not sufficient to suppress circular currents in total. An overview of all evaluated hypotheses is given below:

1. Measured current values are assumed to be true. Thus, the effects might be related to
   - a difference in the two parallel snubber paths, cf. Fig. 4.6. Tolerances between the two capacitors might result in an oscillation between both. Because the current of only one snubber path is measured, cf. Sect. B.2, this oscillation would result in a misinterpretation of the calculated drain current.
   - a non-ideal load inductor showing a more complex frequency behavior as it can be assumed for an ideal infinite inductance. The load inductor might have parasitic capacitances leading to oscillations or displacement currents due to the high voltage slope.
   - the connection between the analyzed power module and the load inductor. The connection is implemented as laboratory wires connected to a 3 m two-wire cable going to the load inductor. This manner of connection might result in propagation effects, reflection at the load inductor or cable charge currents.
2. Measured current values are assumed to be false. Thus, the effects might be related to
   - wrong measurement of the Rogowski coil related to
     - its low bandwidth of 30 MHz.
     - a propagation delay caused by the device integrator circuit.
     - inductive couplings into the coil placed in close proximity to the bond wires, see Fig. B.2.2, directly influencing the measured signal.
     - capacitive couplings into the coil placed in close proximity to the bond wires, see Fig. B.2.2, indirectly influencing the measured signal by causing a circular current flowing through the cable shield to the oscilloscope.
   - wrong measurement of the coaxial shunt related to
     - circular currents through the coaxial cable connected to the common oscilloscope potential.
     - non-optimal 50 Ω signal termination.
   - a misalignment in the corrected deskew of both measured current probe signals.
   - a small deviance in the amplitudes of both used current probes.

Because the used current probes are already the best suitable choice available on the market for this purpose and the measurements have been carried out carefully to suppress unwanted effects in a best-can-do manner, further evaluation is done by simulation. To achieve most trustworthy results, a complex simulation using a complex parasitic model of the module and a non-linear MOSFET model has been used for investigation. The comparison of the simulation with ideal signal probes is shown in Figure 5.9. The com-

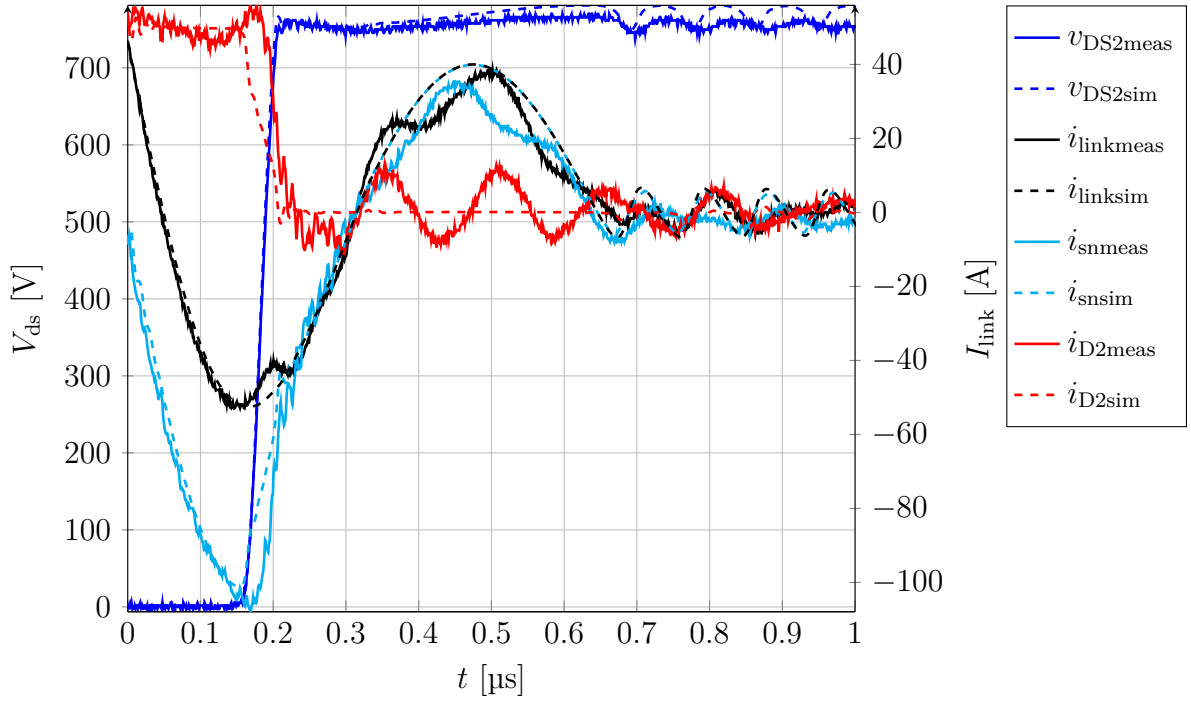


Figure 5.9: Comparison between real measurement and ideal simulation for alignment at 50 A

parison indicates that the assumption of a true drain current being less than the measured value seems to be correct, cf. i_{D2meas} and i_{D2sim}. Hence, a much smaller switching loss than measured in Sect. 5.3.3 can be expected. Additionally, the simulated drain current does not show a fluctuation before the switching event as well as no oscillation afterwards. A further remarkable point can be noticed in the snubber and DC-link current between $320\,\text{ns} < t < 650\,\text{ns}$. Neglecting the 6 MHz oscillation, the simulated DC-link current is above the measured signal and thus, it is more close to the model, cf. Fig. 4.12. However, comprehensive variations of the simulation considering different load connections, parasitic load capacitances, circular currents through non-ideal probe cable shields were performed. None of the investigated parameter variations have shown a plausible cause for either the higher DC-link current nor the 6 MHz oscillation.
It was found that the hypotheses based on the assumption of true measurement values have shown that a difference in the two parallel snubber paths within a reasonable range of capacitance tolerances does not reproduce the effects neither quantitatively nor qualitatively. A non-ideal load modeled as an inductor with a parallel capacitance in the range of 100 pF to 1 nF and a non-ideal 3 m transmission line connection to it resulting in an oscillating drain current after the turn-off event with a similar shape and frequency. However, both i_{link} and i_{sn} are in phase and not in anti-phase as shown in Fig. 4.12. Hence, the hypotheses assuming a true measurement did not explain the effects.
Contrary to that, the hypotheses assuming false measurement values have led to more promising results, although only the drain current fluctuation before the switching event could be reproduced qualitatively. To evaluate the influence of the Rogowski coil, the current measurement was simulated with a 1 mΩ shunt decoupled with a voltage controlled voltage source and a transmission factor of 1000. The resulting signal was filtered with

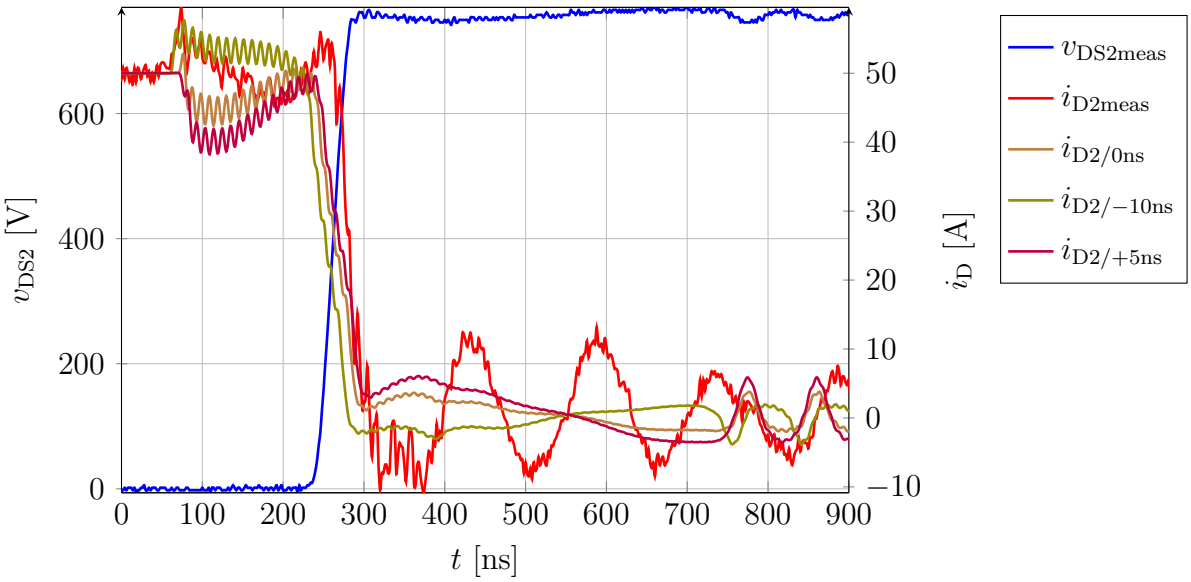


Figure 5.10: Comparison between real measurement and simulation with a 30 MHz low-pass filtered Rogowski coil and signal deskew at 50 A

a first order low-pass filter designed with a corner frequency of 30 MHz. The resulting phase delay of i_{sn} was compensated during post processing to values between −10 ns and 5 ns leading to the results shown in Fig. 5.10. It can be seen that the first initial peak, cf. Fig. 5.8 at $t = 60$ ns as well as the fluctuation until 200 ns could be reproduced. However, the fluctuation is significantly influenced by the deskew of the measured snubber current, the shape of the measured signal still differs. Further, the higher measured drain current and the 6 MHz oscillation could not be reproduced by various circuit variations. Because no parameter variation could finally clarify the difference it should be discussed in future work. Therefore, only the measured value can be taken as valid, which is used in subsequent chapters.

5.2.2 Comparison of the Turn-On Event

Comparing the turn-on event for the three setups is subject of this section. The overlay for the 350 A operation point is shown in Figure 5.11 and for 50 A in Fig. 5.12 respectively. As investigated in Section 5.1.2, the conventional halfbridge was turned on with a gate resistor of $R_{Gon} = 1\,\Omega$ limited by the overvoltage during diode recovery. Both snubber circuits were switched with a gate resistor of 0.5 Ω.

The first remarkable point in both 350 A and 50 A load current operation is a current fluctuation in i_{D2AS} right before the turn-on occurs and the drain current starts increasing. It can be noticed that this fluctuation only occurs in the active snubber setup for $t < 30$ ns but not in the DC-snubber and conventional halfbridge setup. Because the auxiliary switch in the active snubber setup is in off-state during turn-on, its output capacitance is in series to the snubber capacitor. Because it is much smaller than the snubber capacitor it dominates the effective capacitance of the snubber path. Considering its voltage dependence, cf. Fig. 4.9 for a single die, its capacitance can be modeled

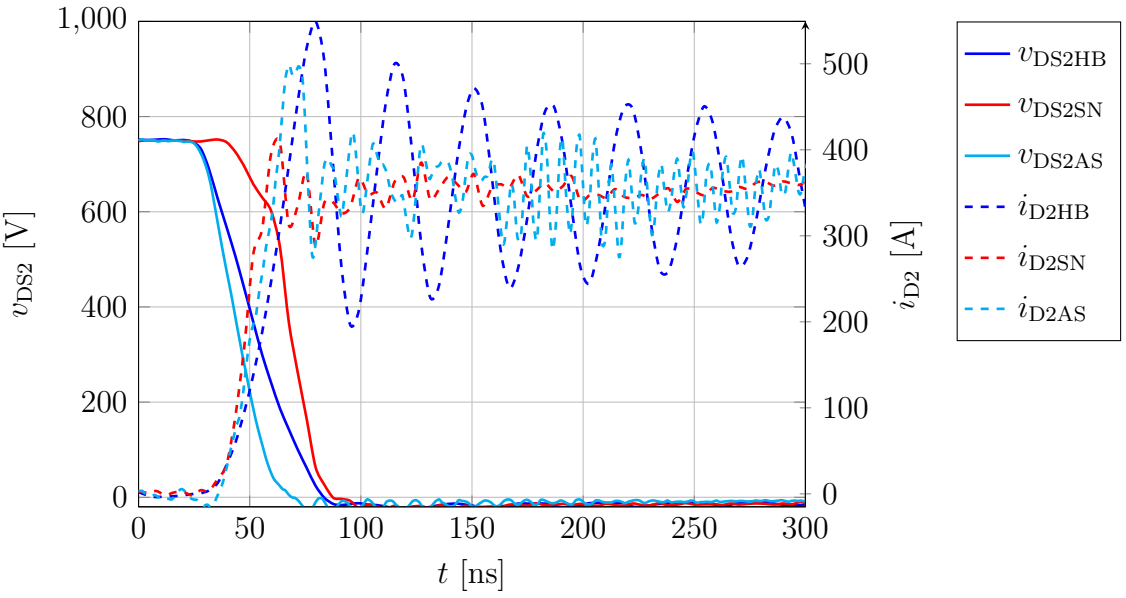


Figure 5.11: Turn-on comparison for $L_{\sigma On} = 37\,\text{nH}$ at 350 A

with a capacitance approximately in the range of 600 pF to 6 nF. Thus, turning on the power switch Q_2 leads to a voltage drop across the main stray inductance similar to the halfbridge. However, this voltage drop occurs also at the auxiliary switch, cf. Fig. 3.2 for $t_1 < t < t_4$ and thus at its output capacitance. This causes a displacement current subtracted from the load current and thus, decreases the drain current of Q_2. The DC-snubber setup is not affected due to the buffering effect of the large snubber capacitor. This can be noticed in the drain-source voltage in both Figures, 5.11 and 5.12. The voltage drop in v_{DS2SN}, noticeable around 50 ns, is caused by a depletion of the snubber capacitance due to the commutation current.

By analyzing the current slope, it can be seen that the DC-snubber has the highest current gradient. The active snubber setup and the conventional halfbridge show a lower gradient. This can be explained with the lower voltage gradient also. As described in Section 2.3.1, the miller capacitance causes a displacement current during the voltage gradient which counteracts the driver influence. If the voltage gradient is less, the driver can turn-on the channel faster. However, the higher i_{D2SN} current slope does not affect the turn-on losses in a positive way compared to the two comparative setups. The voltage drop over the main stray inductance is a more effective way of turn-on loss reduction as it can be seen also in Fig. 5.25, especially if it is considered that the switching speed cannot be increased much more.

It can also be seen that the conventional halfbridge shows the highest peak current while the DC-snubber setup shows the lowest. However, by comparing this value with the measured values in Section 5.2.3, a significant difference can be noticed related to the different used active switch as explained on Page 98.

For both operation conditions shown in Figures 5.11 and 5.12, all setups show an oscillation in the drain current after the current peak. While the oscillation in the conventional halfbridge setup has the highest amplitude but lowest frequency, both snubber setups shown only a minor amplitude but higher frequency. The oscillation of the conventional

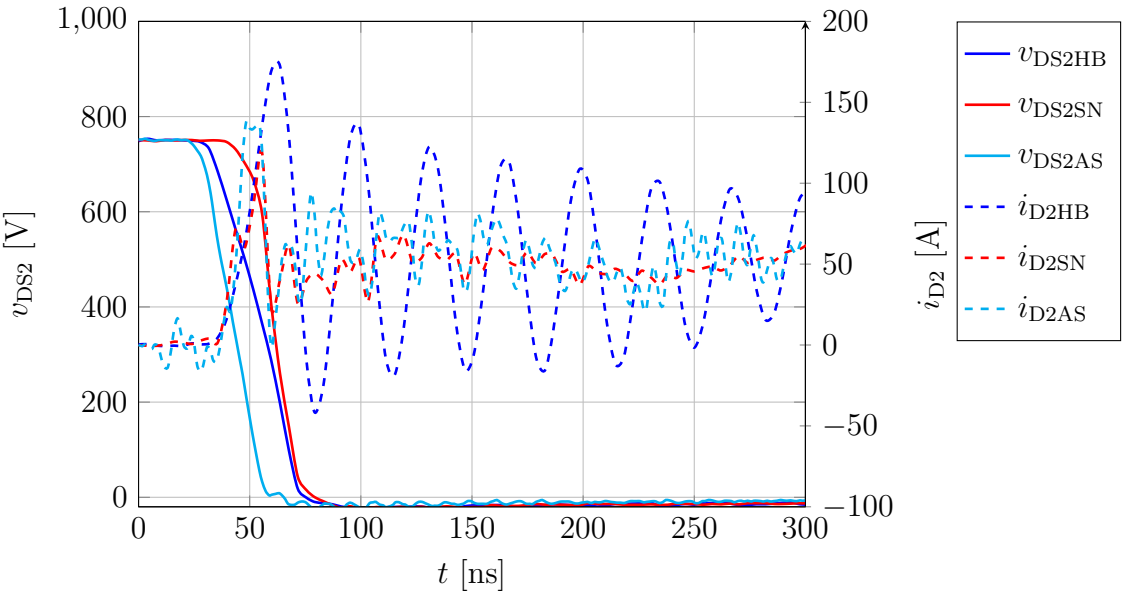


Figure 5.12: Turn-on comparison for $L_{\sigma On} = 37\,\text{nH}$ at 50 A

halfbridge is caused by the well-known oscillation circuit formed by the stray inductance and the output capacitance of the switch and results in

$$f_{HB} = \frac{1}{2\pi\sqrt{L_{\sigma On}C_{oss1}}} = \frac{1}{2\pi\sqrt{37\,\text{nH}\cdot 1\,\text{nF}}} = 26.2\,\text{MHz}. \tag{5.7}$$

Similarly, the oscillation of the snubber circuits can be calculated by considering the much smaller effective stray inductance L_{snhb} according (3.18)

$$f_{SN} = f_{AS} = \frac{1}{2\pi\sqrt{L_{snhb}C_{oss1}}} = \frac{1}{2\pi\sqrt{3\,\text{nH}\cdot 1\,\text{nF}}} = 92\,\text{MHz}. \tag{5.8}$$

However, the signal is not pure sinusoidal and the oscillation is interfered by other fluctuations.

Further, another high frequency oscillation can be seen in the current of the active snubber setup. The oscillation to be analyzed can be noticed for a time above $t_5 = 160\,\text{ns}$ in Fig. 5.11 and for $t_5 = 220\,\text{ns}$ in Fig. 5.12. As predicted by the model and shown in the Sections 4.2 and 4.3, the main stray inductance is charged by the reverse recovery peak current. Its energy commutates into the snubber after the switching event. The voltage difference between the snubber and the DC-link capacitor counteracts this commutation. Because the snubber capacitor is not charged up to a significant voltage in the shown switching event shown in Figure 5.12, the duration until v_{sn} reaches its maximum is longer. After the commutation is finished, the body diode of the auxiliary switch goes into blocking state and thus its output capacitance is charged to the voltage difference between the snubber and DC-link capacitor. Hence, an oscillation circuit is formed by the stray inductance L_{snhb} and the output capacitances of Q_1 and Q_{aux} connected in series. Outgoing from a voltage difference of $C_{ossAux} \approx 50\,\text{V}$ and considering the voltage dependent capacitance of each of the two auxiliary switch MOSFETs according to Fig.

4.9 an effective capacitance of $C_{\text{eff}} \approx 550\,\text{pF}$ for the series connection of C_{oss1} and C_{ossAux} can be approximated. This leads to an oscillation frequency of

$$f_{\text{AS}}(t > t_5) = \frac{1}{2\pi\sqrt{L_{\text{snhb}} C_{\text{eff}}}} = \frac{1}{2\pi\sqrt{3\,\text{nH} \cdot 550\,\text{pF}}} = 124\,\text{MHz} \tag{5.9}$$

fitting very well to the frequency measured.

5.2.3 Comparison of the Diode-Recovery Event

Finally, the overlay of the diode recovery events are depicted in the Figures 5.13 and 5.14. It should be mentioned that the switched semiconductor was chosen to be Q_1. This was done to keep the analyzed switch Q_2. Further, for this configuration the shunt used for measuring i_{link} does not have to be changed because of the reference potential of the passive voltage probes, see Appendix B.2.
Focusing on the current waveform of the reverse recovery, the curves show basically a similar shape despite of higher frequency oscillations superimposed to the drain current of the different setups. Analyzing the time span and the frequency of the superposition, similar frequencies can be found pointing to the same oscillation circuits as root cause.

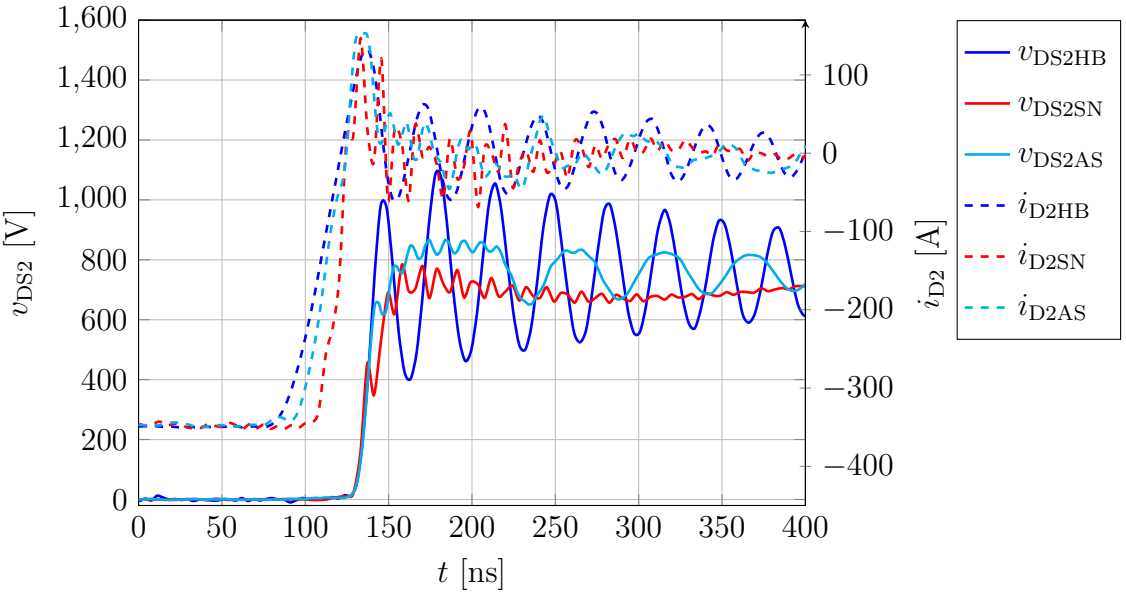


Figure 5.13: Diode recovery comparison for $L_{\sigma\text{On}} = 37\,\text{nH}$ at 350 A

In both operation points, for a load current of 350 A and 50 A, the voltage waveforms are identical for all setups up to a drain-source voltage of 400 V, cf. Figs. 5.13 and 5.14. For voltages above this value, the setups differ. In Section 5.2.2 the difference in the voltage drop during the turn-on has been elucidated. The drain-source voltage waveform in e.g. Figure 5.11 indicates, that for the active snubber setup and the conventional halfbridge approximately the total DC-link voltage is across the main stray inductance. Thus, for the conventional halfbridge the voltage waveform during diode recovery follows from the interaction between the stray inductance, its voltage and the diode behavior. Assuming a

similar behavior of the body diode in all setups due to the equal semiconductor technology, the following hypothesis can be made. As described in Section 2.1.2, see Figure 2.3, the carriers are extracted and allow an electric field in already depleted regions. The field accelerates the charge carriers in the depicted directions and thus, the electric field has a direct influence on the speed and the depletion current. With the conventional halfbridge, the comparatively large effective stray inductance L_{main} causes a larger voltage and thus a larger current in the diode. The diode depletion speed increases due to higher carrier acceleration and the resulting higher current change causes a higher voltage at the stray inductance. This positive feedback loop causes the highest voltage overshoot with the conventional halfbridge setup.
At the active snubber setup, the auxiliary switch sees the large voltage drop across the main stray inductance also as described in the previous section. After the reverse recovery peak occurred, the current decreases. The high voltage across the auxiliary switch has to decrease rapidly and with the output capacitance of the auxiliary switch, a slight buffering effect can be noticed in the drain-source voltage of the active snubber setup until it diverges from the voltage waveform of the halfbridge setup. This occurs approximately at a drain-source voltage of 600 V. The negative current slope of the drain current causes a voltage increase across the main stray inductance. Due to the body diode of the auxiliary switch, this voltage is limited to the voltage of the snubber capacitor.

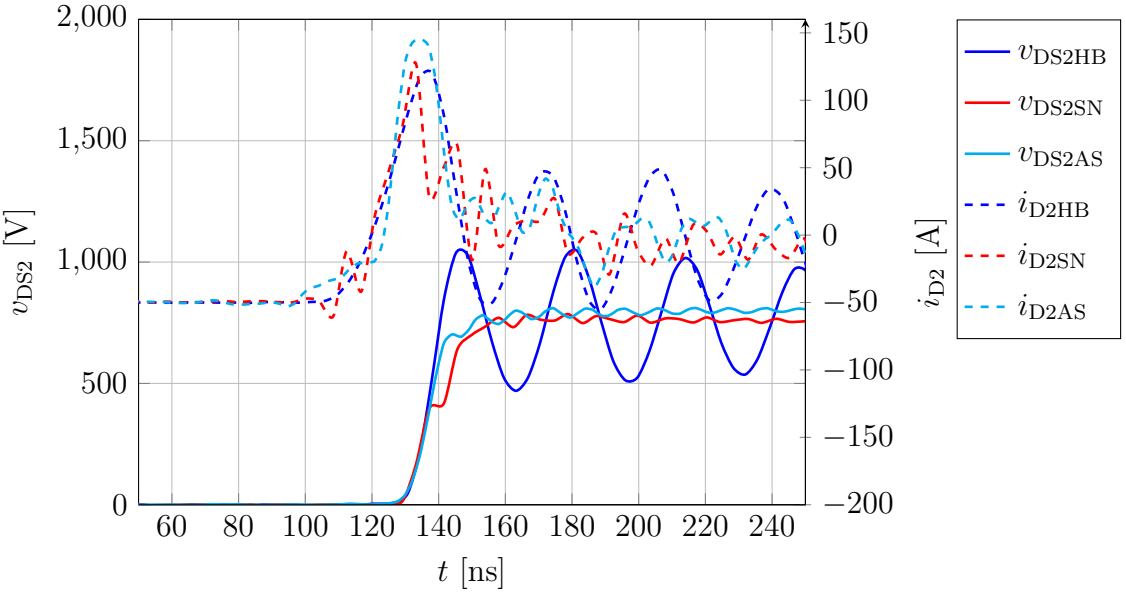


Figure 5.14: Diode recovery comparison for $L_{\sigma\text{On}} = 37\,\text{nH}$ at 50 A

Hence, the voltage at the body diode of Q_2, determining the waveform, is strongly reduced compared to the conventional halfbridge. With the above mentioned hypothesis, the electric field accelerating the charge carriers within the drift region is lower and thus, the charge carriers are accelerated weakly leading to a much smoother, less harsh, recovery behavior.
Additionally to the lower voltage reducing the losses, the reverse recovery of the DC-snubber setup benefits from a more depleted snubber capacitor, which has provided the commutation current. The reduces snubber voltage further decreases the initial voltage peak.

5.3 Behavior within Operation Range

Goal of this chapter is to evaluate and compare the behavior of the three introduced setups over a wide range of DC-link voltages and load currents. If not specified otherwise, each diagram is plotted at a DC-link voltage of 750 V, at a load current of 350 A and with the gate resistors shown in Table 5.2. All dynamic values are depicted for a main stray inductance of 37 nH and 47 nH to evaluate the influence according to the research questions.

5.3.1 Voltage Gradients

First, the maximum voltage gradients during the voltage slope of the switching event are discussed. To determine the maximum gradient considering noise, a window of 10 % of the nominal voltage was slided over the slope and the maximum value was taken as measurement value. Due to various oscillations, the commonly used value from 10 % to 90 % suffers from non-static measurement curves. The corresponding measurement values are shown in Figure 5.15 and Figure 5.16. Due to the restricted switching speed of the conventional halfbridge, the achievable voltage gradient is limited to values below 20 GV/s. In Figure 5.15, only a small dependence on the load current can be noticed for the conventional halfbridge. Contrary, both snubber setups show a significant dependence at load current values below 200 A which flattens for higher current values. In Section 2.3.2, quasi soft switching was explained with a high voltage gradient that causes significant current through the output capacitance. While this displacement current is also provided by the constant load current, a limited voltage gradient is consequence. Thus, at lower load current values, the transition is controlled by both the channel as well as the displacement current limited by the load current. At higher load currents, the quotient of current and output capacitance allows higher gradients.

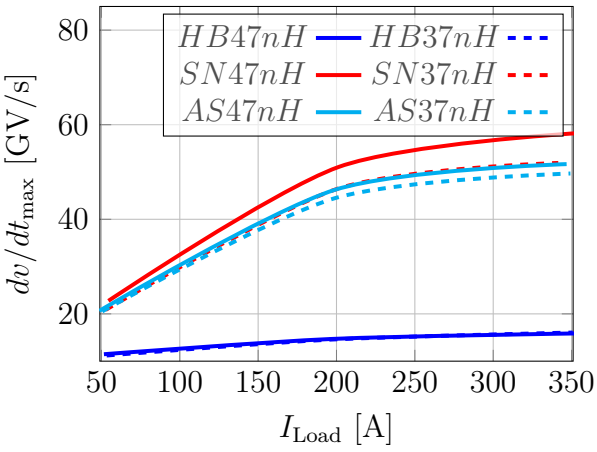


Figure 5.15: dv/dt_{max} over I_{Load} for turn-off

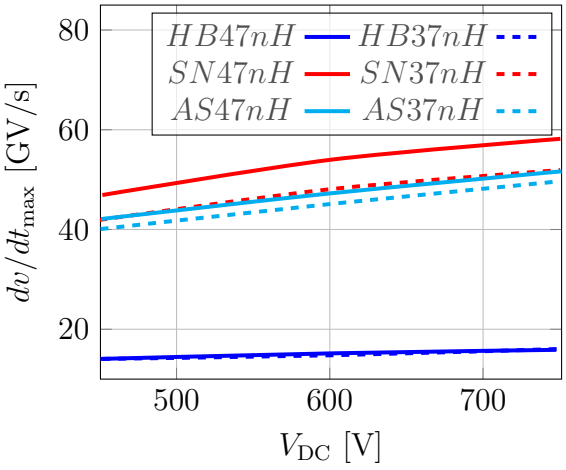


Figure 5.16: dv/dt_{max} over V_{DC} for turn-off

Further, it can be seen that due to the equal gate resistor, the stray inductance for the conventional halfbridge has only minor influence. At both snubber setups, with equal gate resistors, the voltage gradients are very similar. However, both setups show a slightly higher gradient at 47 nH as for 37 nH especially at the DC-Snubber setup. By comparing the waveforms of the (not depicted) 47 nH DC-Snubber setup with the 37 nH DC-Snubber

setup no difference in the DC-link current value was found. Additionally, the current gradient is close to zero during the voltage slope so the displacement current through the output capacitance can be neglected as well. Hence, no immediate influence from the stray inductance can be observed. However, the snubber current at 37 nH suffers from higher oscillations in the 90 MHz range, which do not appear at the 47 nH setup. This allows to draw the conclusion that the difference in the voltage gradient shown in the corresponding figure is related to device specific tolerances.

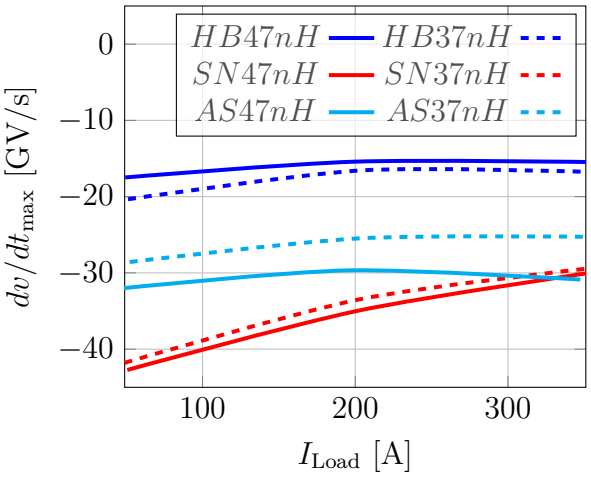


Figure 5.17: $dv/dt_{\max}$ over I_{Load} for turn-on

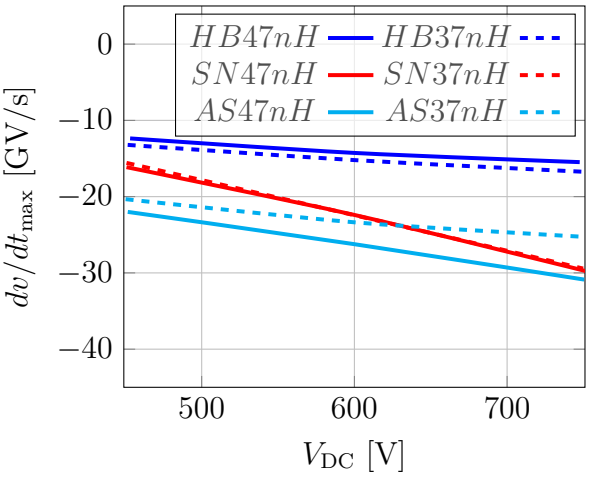


Figure 5.18: $dv/dt_{\max}$ over V_{dc} for turn-on

Due to the voltage drop over the stray inductance, the absolute value of the voltage gradients at the turn-on event is not similar to the corresponding gradient at diode reverse recovery. Hence, both gradients have to be analyzed separately. The gradients for the turn-on event are shown in Figures 5.17 and 5.18. As noted in Section 2.3.1 a larger stray inductance is beneficial at turn-on due to a higher voltage drop. As it can be seen in both figures, besides the halfbridge setup using different R_{Gon}, the setup with higher stray inductance causes a more negative voltage gradient. Due to the higher voltage overshoot at diode recovery, cf. Figs. 5.3 and 5.4, a higher gate resistor has to be used for the halfbridge with 47 nH to keep the voltage overshoot below the maximum specification of the semiconductor. As a result, a larger stray inductance cannot be utilized for a quasi soft turn-on and higher turn-on losses can be expected, see Sect. 5.3.3. Contrary to that, the active snubber setup provides a large stray inductance during the positive current slope but a small stray inductance for diode recovery. Thus, for both evaluated stray inductances the same gate resistance value can be used and thus, the influence of the stray inductance can also be utilized.
Further, it can be noticed that for both - the conventional halfbridge as well as the active snubber setup - the dependence on the load current is negligible, while a higher DC-link voltage causes a higher absolute value of the voltage gradient. Focusing on the DC-snubber setup, a significant influence of the load current can be noticed as well as a more distinct influence of the DC-link voltage. To evaluate the effect, the DC-snubber values in Figures 5.11 and 5.12 are compared with Figures 5.13 and 5.14. It can be noticed that the voltage buffering effect of the DC-snubber with the small effective stray inductance L_{snhb} is significant. Thus, both switches, Q_1 and Q_2 share a significant voltage at the

same point in time during the switching event. Contrary to that, for an ideal quasi soft turn-on where the negative voltage slope of the turning on Q_2 and the positive voltage slope of the turning off Q_1 appear consecutively. As a result, the voltage slope of the turning on switch for the DC-snubber setup is significantly influenced by the behavior of the body diode.

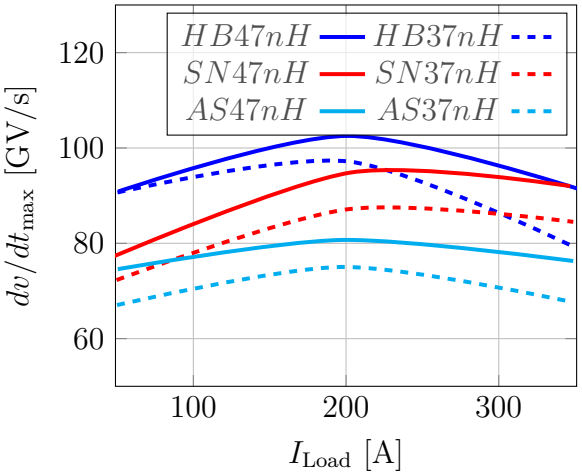


Figure 5.19: $dv/dt_{\max}$ over I_{Load} for diode recovery

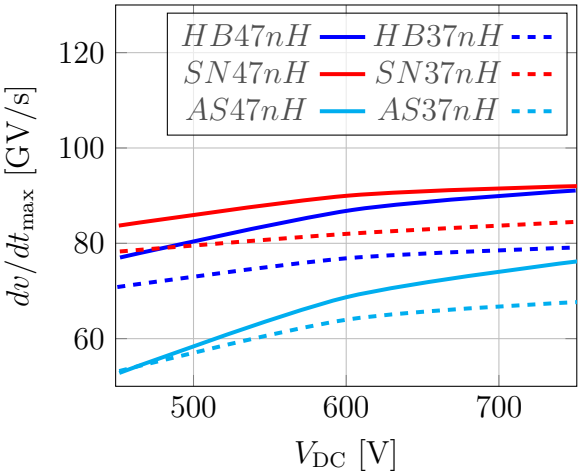


Figure 5.20: $dv/dt_{\max}$ over V_{DC} for diode recovery

Finally, the voltage gradients for the diode recovery are discussed. The corresponding values measured are shown in Figures 5.19 and 5.20. It can be noticed that for all setups a maximum value can be measured at a load current of 200 A. Additionally in all setups a higher stray inductance leads to a higher voltage gradient. By analyzing the switching curves, it could be found that similar to the halfbridge and the DC-snubber setups the highest voltage gradient occurs also at the active snubber setup at a point in time very close to the appearance of the maximum recovery peak current. According to [124], the body diode builds up voltage once the bipolar plasma is extracted. Hence, the increasing voltage is directly caused by charging the capacitive part of the body diode, see also Section 2.1.2. However, this effect may differ if another semiconductor is used, see [127]. The dependence on the stray inductance can be derived with (3.25) to (3.28), which model the transition at the point in time where the zero crossing of the body diode current occurred as an oscillation. Neglecting the more complex behavior due to the charge carrier extraction behavior and the voltage dependent capacitance, the model predicts a longer oscillation period at a higher stray inductance values. Thus, assuming a similar amount of charge to be recovered, a longer oscillation period causes a lower reverse recovery peak current to not infringe the rule of charge conservation.
A further remarkable point is the more significant influence on the voltage gradient of higher DC-link voltages for the active snubber setup. By analyzing the corresponding switching curves, a significant difference in the reverse recovery peak current can be noticed, which is explained in the following Section 5.3.2.

5.3.2 Reverse Recovery Peak Current

It has been stated that the reverse recovery peak current is a significant parameter to the turn-on model of the active snubber, see P. 41. While the influence of the stray inductance value for the conventional halfbridge is comparatively small as shown in Figures 5.21 and 5.22, its influence at both snubber circuits is significant. However, while the DC-snubber shows a significant decrease of I_{rrm} with increased stray inductance, the active snubber circuit shows an opposite behavior. By analyzing the switching curves, it can be found

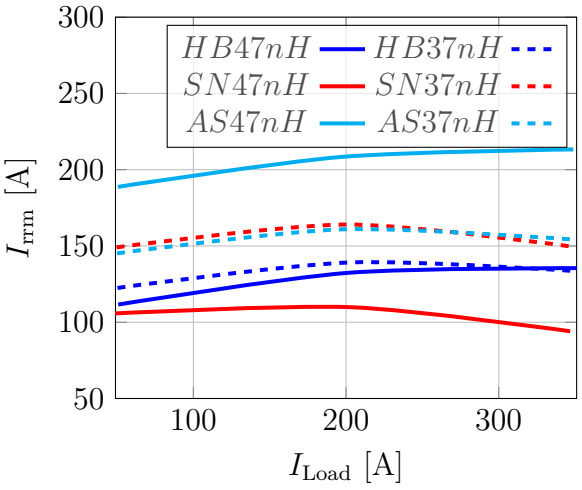


Figure 5.21: I_{rrm} over I_{Load}

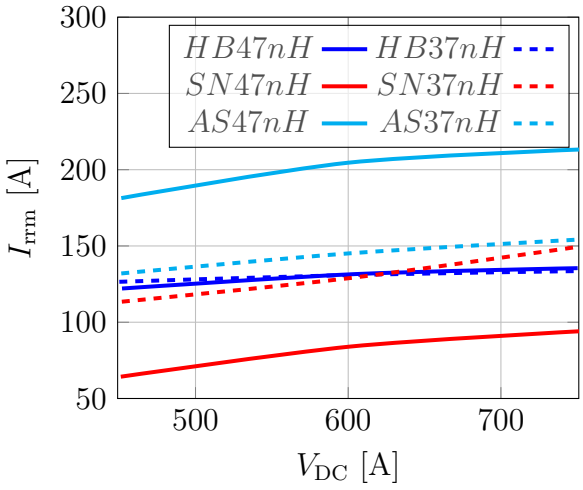


Figure 5.22: I_{rrm} over V_{DC}

that at the setup with $L_{\mathrm{res}} = 37\,\mathrm{nH}$ a higher frequency oscillation with significant amplitude is superimposed especially to the current waveform of the DC-snubber setup, cf. also Fig. 5.13. This oscillation causes a difference in the measured value of I_{rrm} while an averaged current waveform is very similar to the 47 nH setup. However, comparing the peak current of both snubber setups with a stray inductance of 47 nH, which is less affected by the oscillation, a difference can be noticed. The DC-snubber setup shows significantly less peak current compared to the active snubber setup. The analysis for the 47 nH setup at a load current of 350 A and a DC-link voltage of 750 V shows a reverse recovery charge of $Q_{\mathrm{rrAS}} = 3.5\,\mu\mathrm{C}$ for the active snubber and $Q_{\mathrm{rrSN}} = 0.8\,\mu\mathrm{C}$ for the DC-snubber setup. A possible explanation might be derived from (3.25) to (3.28). While for the active snubber approximately the total DC-link voltage is across the main stray inductance L_{main}, the buffering effect of the DC-snubber and a lower effective stray inductance L_{snhb} cause the already mentioned voltage drop across the turning on Q_2. In conclusion, the stray inductance L_{snhb} sees a lower voltage. Hence, the active snubber setup can be modeled as an LC-circuit with a large stimulus from the DC-link voltage V_{DC} across the stray inductance modeled by (3.28) leading to a higher A_{34}. Differently, the DC-snubber setup modeled similarly with an LC-circuit sees a much lower stimulus due to the buffering effect. As a result, the oscillation triggered in the DC-snubber circuit has a lower amplitude.

Additionally, the DC-snubber setup shows no or even a slightly negative dependence on the load current while the dependence of the active snubber setup is slightly positive, see Fig. 5.21. As mentioned in Section 4.3 the assumption that the total DC-link voltage is across the main stray inductance is not true for lower current values due to an overlap

in the defined intervals, see Sect. 4.3. As a result, with the previously stated LC-circuit approximation, the stimulus is less for lower currents and increases with higher load currents.
The DC-snubber setup shows no (37 nH) or a slightly negative (47 nH) load current dependence of I_{rrm}. This can be explained together with the positive dependence on the DC-link voltage of I_{rrm} as shown in Fig. 5.22. Because the inductance L_{snhb} is much smaller than L_{main}, the commutation current is provided by the snubber capacitor, which is discharged to a lower voltage. Because of a higher stray inductance L_{main} to the DC-link capacitor the snubber has to provide more charge as with lower L_{main} where the DC-link capacitor can provide more. As a result, the effective voltage across the halfbridge approximately equal to the snubber voltage v_{sn} during diode recovery is also lower and thus, the dependence of I_{rrm} according to Fig. 5.22 determines this effect.

5.3.3 Switching Losses

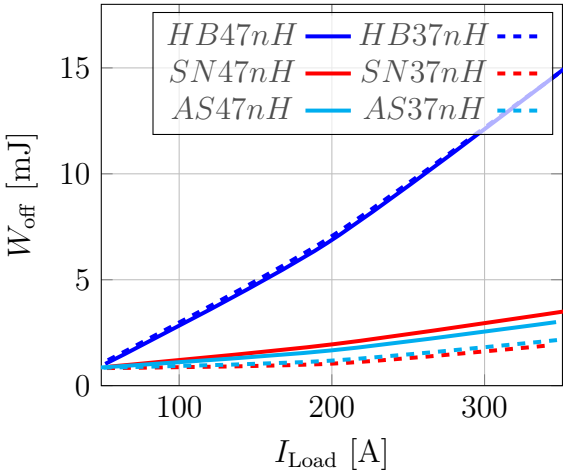


Figure 5.23: W_{off} over I_{Load}

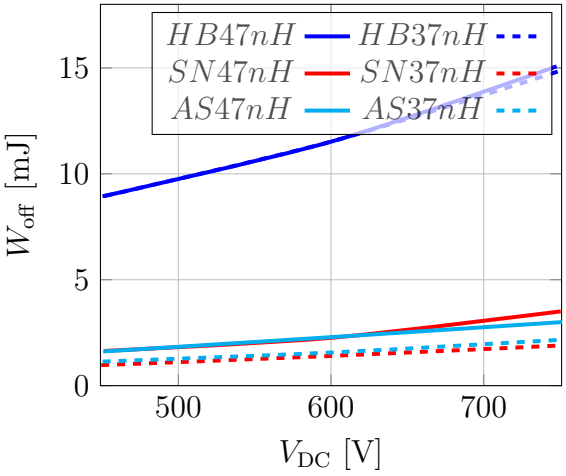


Figure 5.24: W_{off} over V_{DC}

The switching losses for turn-off are shown in Figures 5.23 and 5.24. It can be seen that all turn-off loss curves increase approximately linear with the load current and DC-link voltage. Further, the conventional halfbridge shows similar losses at both stray inductances, which relates to the equal gate resistors of 5 Ω. Additionally, the losses at both snubber circuits show approximately the same losses at each stray inductance, which fits to the very symmetric overlay according Figures 5.7 and 5.8. This also indicates that the active snubber shows very similar behavior as a DC-snubber with similar capacitance C_{sn}. Both Figures indicate also that especially at high current values the conventional halfbridge suffers from excessive losses, which can be explained by the non-optimal product of stray inductance and load current, see Sect. 2.2.2. Contrary to that, both snubber circuits are less affected, due to the comparatively low effective stray inductance L_{snhb} provided by the snubbers.

The turn-on losses are compared in Figures 5.25 and 5.26. Both show that the active snubber setup strongly benefits from the asymmetric stray inductance, which is much higher at turn-on and the losses are close to zero. Further, it can be seen that the conventional halfbridge cannot utilize this benefit due to the switching speed limitation

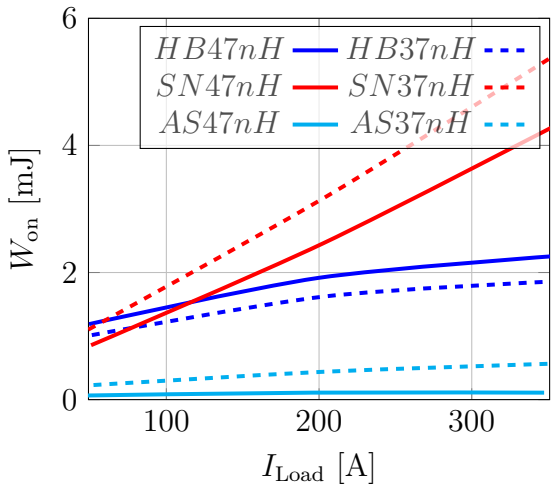


Figure 5.25: W_{on} over I_{Load}

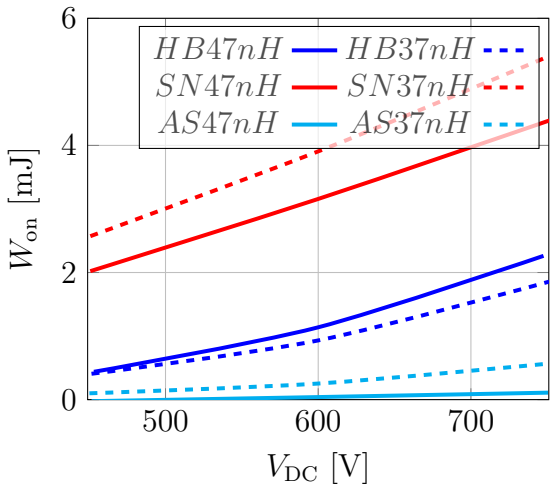


Figure 5.26: W_{on} over V_{DC}

with respect to the overvoltage during diode recovery. The two stray inductance values have to be switched with different turn-on gate resistors and thus, the setup shows higher losses at a higher stray inductance while the active snubber does not suffer from a limited switching speed. Focusing on the DC-snubber setup, it can be noticed that the small effective stray inductance L_{snhb} strongly increases the losses even with a low gate resistance value. The change from 47 nH to 37 nH also increases the losses significantly.

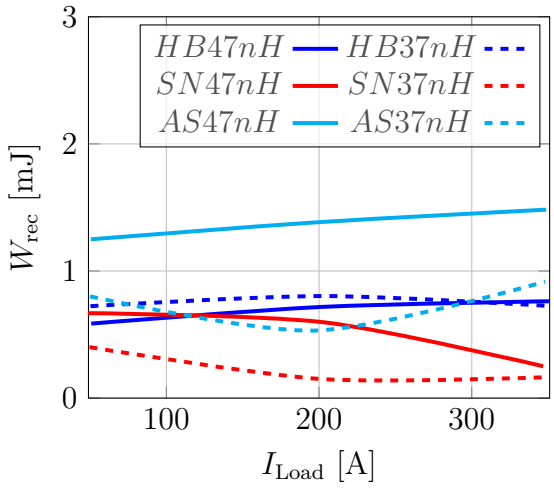


Figure 5.27: W_{rec} over I_{Load}

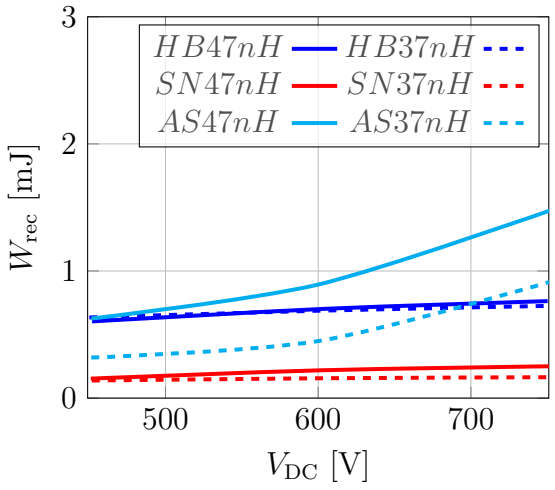


Figure 5.28: W_{rec} over V_{DC}

The losses during diode recovery are shown in Figures 5.27 and 5.28. The conventional halfbridge does not show a significant dependence on the load current as well as on the DC-link voltage. Only a weak dependence on the stray inductance in spite of different gate resistors can be noticed. For both snubber setups, a lower stray inductance is beneficial for the recovery losses. This is related to the lower stimulus of the LC-circuit as described in Section 5.3.2. Additionally, the lower voltage increase at the DC-snubber, cf. e.g. Fig. 5.13 for $t > 140$ ns leads to lower losses compared to the active snubber. However, the losses of all setups are comparatively low compared to the turn-off losses, see Figs. 5.23 and 5.24. A further effect that should be discussed is the significant posi-

tive dependence of the active snubber losses on the DC-link voltage while the DC-snubber and the conventional halfbridge does not seem to be affected. Analyzing all corresponding switching curves indicate that this effect is related to the method of analysis based on [128]. The energy is calculated by integrating the power from the zero crossing to the point in time after the reverse recovery peak where the current is equal to 2 % of I_{rrm}. The current of the conventional halfbridge suffers from high amplitude oscillations and thus, the 2 % value is reached approximately simultaneously for both stray inductances. Hence, the loss-integral shows also a similar value. The DC-snubber setup shows an identical overlay to the halfbridge of the drain voltages until I_{rrm} occurred. After the occurrence of the current peak, the current waveform shows a tail also superimposed by an oscillation but with less amplitude compared to the halfbridge. Nevertheless, the 2 % I_{rrm} value is reached also simultaneously.
The independence on the DC-link voltage of the DC-snubber setup as well as its low value compared to the other setup is related to the voltage waveform. A similar load current causes also a similar depletion of the snubber capacitor. By comparing Figure 5.13 with 5.14, it can be noticed that at both load current values the drain voltage value rises rapidly to approximately 400 V. Additionally, this value is independent of the DC-link voltage. However, after reaching the 400 V, at higher DC-link voltages a much slower voltage increase is shown. This much slower voltage increase relies on the DC-link voltage and causes a similar energy loss for each DC-link voltage.
Analyzing the active snubber shows that the voltage rises rapidly to a much higher value of about 650 V, see e.g. Fig. 5.13 at $t \approx 140$ ns. Afterwards, the body diode shows a tail-current similar to the DC-snubber but the energy from the stray inductance commutates into the snubber capacitor. The increasing snubber capacitor voltage is very similar to the voltage across Q_1 due to the small L_{snhb}. Hence, the charging process of the snubber capacitor in the active snubber circuit causes a higher voltage v_{DS1} and thus higher recovery losses at the body diode.

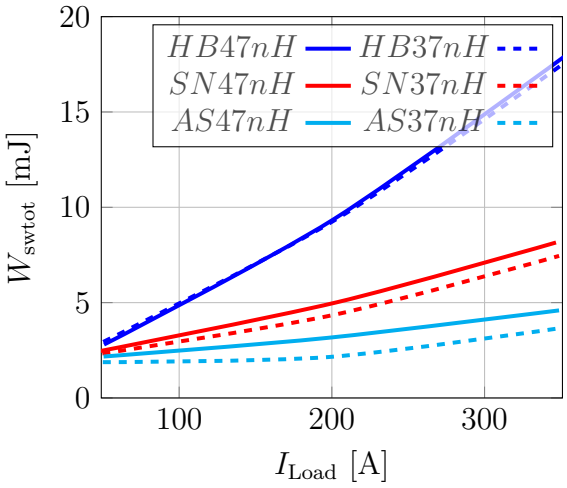


Figure 5.29: W_{swtot} over I_{Load}

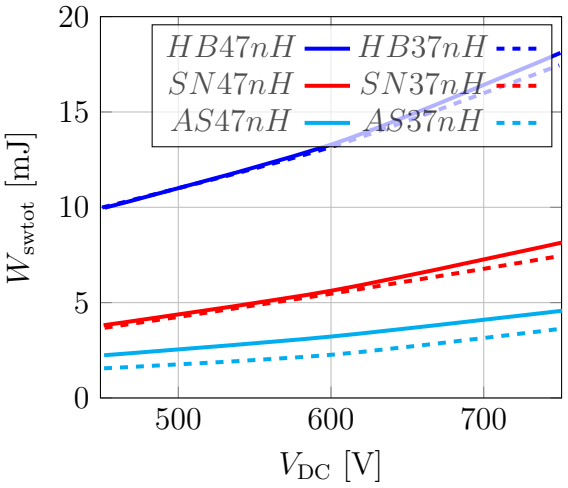


Figure 5.30: W_{swtot} over V_{DC}

To answer the research question whether a larger stray inductance might be positive for the total switching losses, the total losses are shown in Figs. 5.29 and 5.30. First, it can be noticed that the change in the stray inductance has no significant influence on the conventional halfbridge which confirms the finding in [22]. Both snubber setups show

lower total losses with lower stray inductance. Thus, a higher main stray inductance L_{main} is not reasonable. However, considering the DC-snubber as a DC-link capacitor with an effective stray inductance of $L_{\text{snhb}} = 3\,\text{nH}$ and considering Fig. 5.25, showing that with $L_{\text{main}} = 47\,\text{nH}$ the turn-on losses are already close to zero, there must be an optimal value between 37 nH and 3 nH leading to the lowest total losses. Finding this optimal value should be part of future investigations.
Another remarkable point can be observed by extrapolating the total losses to lower load current values. The extrapolation indicates that at very low load currents both snubber setups have higher total switching losses, which is mainly related to the turn-off losses, cf. Fig. 5.23. However, as discussed in Sect. 5.2.1, there is an unexplained effect, which might lead to higher current values during the turn-off voltage slope. Hence, it is unclear whether the switching losses at lower current values can be trusted.

5.3.4 Damping Losses

In this section, the measured values of the damping losses are discussed. To evaluate the damping losses, the oscillation with the highest amplitude has been analyzed by fitting the mathematical expression for a damped oscillation to the signal as explained on Page 51. From this fit, the effective damping resistor has been calculated and is used to obtain the damping losses. However, this method cannot be applied to the active snubber current because the duration of the exponentially damped signal is interrupted by the switching event and thus, the fit cannot be done with reproducible accuracy. Therefore, the following method has been used for the active snubber. Because the frequency of the active snubber oscillation is very similar to the oscillation of the DC-snubber setup it is assumed that a very similar effective damping resistance results due to skin and proximity effect. Hence, as explained in Sect. 4.1.4, the effective damping resistor derived from the otherwise identical DC-snubber setup is modified by the on-state resistance of Q_{aux} to obtain the damping resistance of the active snubber setup. The results for the

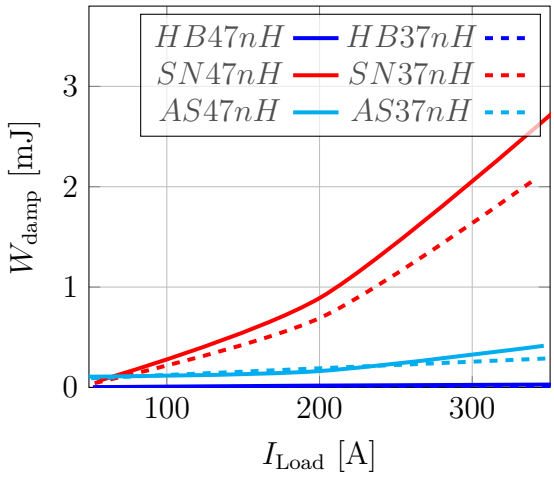


Figure 5.31: W_{dampOff} over I_{Load}

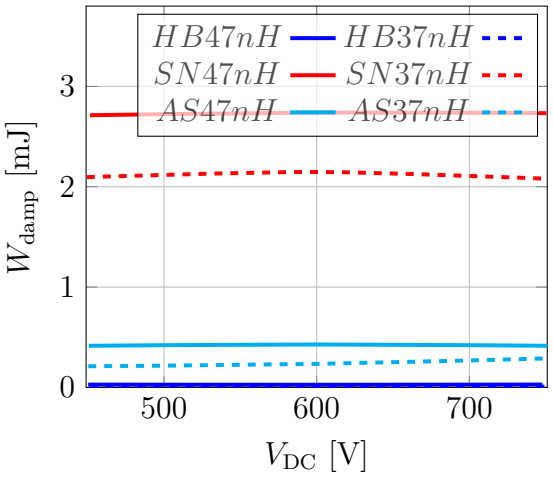


Figure 5.32: W_{dampOff} over V_{DC}

turn-off event for all setups are shown in Figures 5.31 and 5.32. It can be seen that the energy damped in the conventional halfbridge setup is negligible is spite of the high voltage amplitude. The high voltage amplitude is related to the small output capacitance C_{oss} compared to the snubber capacitance C_{sn}. The two snubber setups don't show a

dependency on the DC-link voltage, which is related to the use of a very linear class I snubber capacitor, see Section 4.1.1. The DC-snubber shows an expected quadratic dependency on the load current, see (2.28). This results in damping losses within a range very similar to the corresponding turn-on and turn-off losses. Contrary to that, the active snubber shows only a weak dependence on the load current. This was also predicted by the model, cf. Fig. 4.21. However, the validity of this absolute measurement value for continuous operation can be challenged as already explained in Chapter 4. However, the measured damping losses for the double pulse measurement, cf. Fig. 5.31 at $I_{\mathrm{Load}} = 350\,\mathrm{A}$ are very similar to the model prediction shown in Fig. 4.15. Nevertheless, the losses are significantly reduced compared to the DC-snubber and fits also very well to the prediction in Fig. 4.15. Additionally, they also show only a small or even negligible dependence in the used stray inductance.

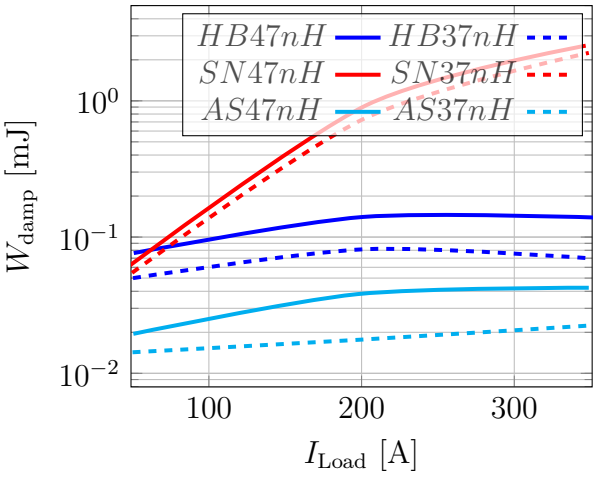


Figure 5.33: W_{dampRec} over I_{Load}

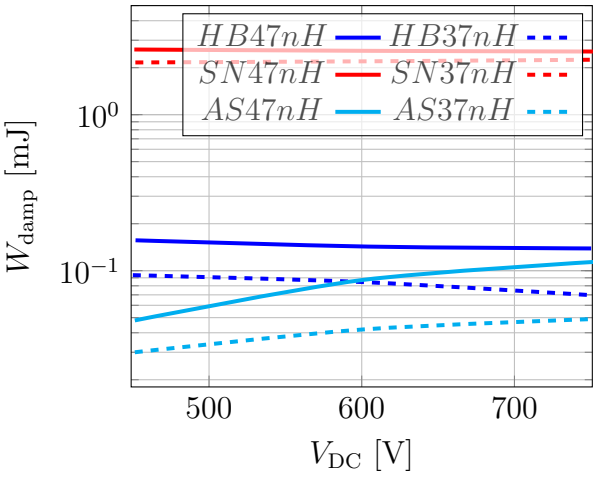


Figure 5.34: W_{dampRec} over V_{DC}

A similar result can be seen for the turn-on or diode reverse recovery shown in Figures 5.33 and 5.34. Similarly, the losses show only a negligible dependency on the DC-link voltage. Further, especially for higher load current values, the damping losses for the conventional halfbridge as well as the active snubber setup are negligible which stays in contrast to the damping losses of the DC-snubber setup (note the log-scaled y-axis). While at the conventional halfbridge setup, the energy in the stray inductance commutates into the output capacitance and causes a significant voltage overshoot, this overvoltage is clamped to the snubber voltage by the body diode of the auxiliary switch becoming conductive. Hence, a significant amount of energy is prevented from contributing to an oscillation and thus is not dissipated. Therefore, the damping losses of the active snubber setup are less compared to the halfbridge setup.
Most significant is the much lower damping loss of the active snubber compared to the DC-snubber, cf. Fig. 5.33. Comparing this result to the model prediction in Fig. 4.18 indicates that the model predicts much higher losses. An overestimation of the losses has already been explained on Page 61. Additionally, the measurements were performed as double pulse and thus, the snubber voltage has not been converged to a steady state. Hence, the damping losses might differ during continuous operation. Contrary to the active snubber deviation between measurement and model, the DC-snubber measurement

fits very well to the model prediction, cf. Figs. 4.15 and 4.18 to Fig. 5.33. As a result, this proves the active snubber capability of being used at higher load current applications.

5.3.5 On-State Resistance

To be able to calculate an inverter operation as described in Section 5.4.1ff., this section is about the static behavior of the used MOSFET devices. In Figure 5.35 the channel characteristic of the used semiconductor setup is shown. The measurements with turned on channel in both directions (blue) are done with a gate-source voltage of $V_{\mathrm{GS}} = 18\,\mathrm{V}$ and the body diode with a $V_{\mathrm{GS}} = -5\,\mathrm{V}$ (red). The forward conducting channel from drain to source (DS) shows a slight non-linear measurement V_{DS}, which might be related to short channel effects, see Section 2.1.3. As a result, the on-state resistance becomes a function of the drain-source voltage. Contrary to that, the inverse direction with V_{SD} considering the

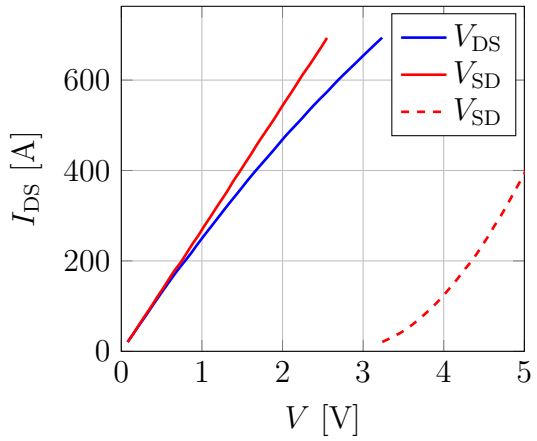


Figure 5.35: Channel characteristic of the drain-source (DS) and source-drain (SD) path over I_{Load}, solid $V_{\mathrm{GS}} = 18\,\mathrm{V}$, dashed $V_{\mathrm{GS}} = -5\,\mathrm{V}$, $\vartheta_{\mathrm{J}} = 25\,^{\circ}$

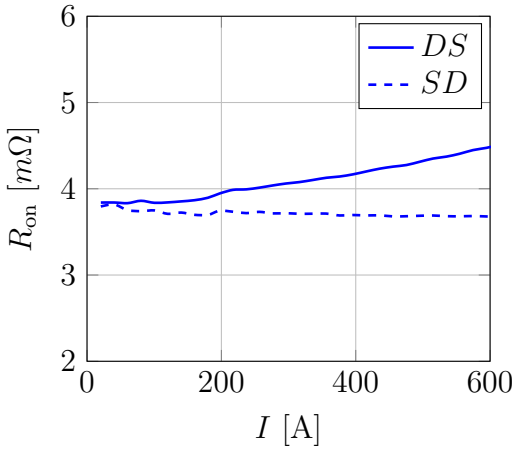


Figure 5.36: On-resistance of the drain-source (DS) and source-drain (SD) path over I_{Load}, $\vartheta_{\mathrm{J}} = 25\,^{\circ}$

source-drain path, shows a more independent behavior of the drain-source voltage. The comparatively high voltage across the source-drain path by turned-off channel is caused by the body diode. To reduce conduction losses in inverter operation this necessitates the use of the channel during free wheeling by turning on the device. It should be noted that the on-state resistance is also a function of temperature [129, 130]. However, because in Sect. 5.4, an achievable inverter output power is estimated also for an optimized semiconductor with less breakdown voltage for which a temperature dependency cannot be predicted yet, this dependency is neglected for the sake of simplicity.

5.4 Achievable Output Power for Inverter Operation

As shown in Section 5.3.3, the active snubber setup allows a significant reduction of switching losses. In Section 4.6, it has been stated that the damping losses during the snubber oscillation can be significantly reduced at continuous operation compared to a DC-snubber, which is supported by the measurements shown in Section 5.3.4.

With respect to the research question, see Page 5, the influence of the active snubber on the system performance still needs to be quantified. The setups build for model validation introduced in Sect. 4.1, are used in this chapter to dimension a hypothetical drive inverter application. The goal is estimating the achievable output power at a constant DC-link voltage of $V_{\mathrm{DC}} = 750\,\mathrm{V}$.
As introduced on Page 11, the specific on-resistance strongly depends on the desired breakdown voltage of the MOSFET device. Thus, the significant effect on voltage overshoot for both snubber circuits may allow the usage of an optimized device with smaller R_{DSon}. This is considered by dimensioning a hypothetical inverter with optimized MOSFET devices according to the relative change in specific on-resistance with reduced breakdown voltage estimated with a reduction factor γ given by (A.197). The resulting parameters for this optimized inverter shall give an extrapolation to potential enhancements achievable with the active snubber.
The inverter setups shown in Table 5.3 were dimensioned and compared to each other.

Table 5.3: Calculated setups for comparison

Setup Name	**Abbreviation**	R_{DSon} **according to**
Conventional Halfbridge	HB	Sect. 5.3.5
DC-Snubber	SN	Sect. 5.3.5
Active Snubber	AS	Sect. 5.3.5
DC-Snubber opt.	SNo	(A.197)
Active Snubber opt.	ASo	(A.197)

As shown in Section 5.3.5, the on-state resistance deviates with the direction of current flow and whether the channel is opened or closed. For the inverter operation the following operation mode is assumed. In forward conduction mode, the current dependent resistance for the drain-source path according 'DS' in Fig. 5.36 is used. Due to the higher forward voltage with turned off channel, see 5.35, active free wheeling with turned on channel with $V_{\mathrm{GS}} = 18\,\mathrm{V}$ during reverse conduction is assumed.
Because the snubber setups show significantly reduced switching losses, it might be reasonable to increase the switching frequency. According to [131], a higher switching frequency might be positive for magnetic losses in the electric motor. Therefore, the inverter setups are calculated for a commonly used switching frequency of $f_{\mathrm{sw10}} = 10\,\mathrm{kHz}$ as well as an increased switching frequency of $f_{\mathrm{sw30}} = 30\,\mathrm{kHz}$.
However, some parameters for inverter dimensioning have to be estimated. The thermal resistance of both two power switches Q_1 and Q_2 as well as of the snubber capacitor rely on the module assembly, thickness of thermal grease and the kind of external cooling, see Sect. A.5. Further, besides the estimation of the optimized on-state resistance, its potential temperature dependence relies on the device dimensioning and thus, cannot be determined. Therefore, a temperature independent on-state resistance for the optimized as well as for the regular MOSFETs using Fig. 5.34 is assumed to reduce uncertainties.

5.4.1 Evaluation of Losses

The achievable inverter output power is limited by the allowed semiconductor or snubber capacitor temperature $\vartheta_{\mathrm{Jmax}} = \vartheta_{\mathrm{Cmax}} = 150\,^{\circ}\mathrm{C}$. The corresponding losses are calculated

in this chapter according the calculation scheme documented in Sect. A.6. This is done up to a load current at which the devices reach their maximum temperature. Additionally, the inverter operation is calculated for a common switching frequency of 10 kHz and a switching frequency of 30 kHz to consider motor loss reduction, see [131] and thus, potentially optimized overall system losses.
The total inverter conduction losses for a three phase setup with sinusoidal output currents are depicted in Figure 5.37. The diagram shows the losses of a MOSFET with a conduction characteristic according Sect. 5.3.5 and a MOSFET optimized for lower breakdown voltage and lower on-state resistance, see (A.197), as it can be used with both snubber types. Both losses are calculated up to the highest current achievable with one of the mentioned setups due to the overvoltage suppression. It can be seen that the optimized semiconductor allows about 22 % higher current. However, the potential reduction of the on-state resistance according to (A.197) cannot be achieved, which is related to the switching losses as a part of the total semiconductor losses. (2.7) indicates that the on-state resistance is a function of the critical electric field E_C as a function of doping, [43]p.97ff. Further, the saturation current is also a function of doping as indicated by (2.10). Hence, a change in the switching behavior can be expected for the optimized MOSFET compared to the non-optimized MOSFET. Because a lower on-state resistance may result in a higher transconductance, the load current is reached faster and the switching losses might decrease. However, this dependence cannot be quantified and thus, is neglected for the switching loss estimation. Hence, the losses of the non-optimized MOSFET according Sect. 5.3.3 are used.

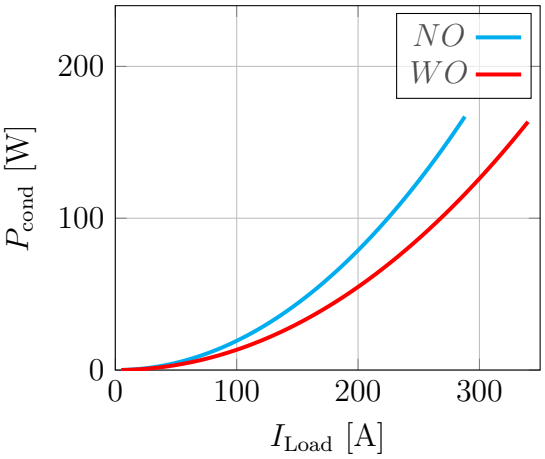


Figure 5.37: Inverter conduction losses over I_{Load} for non-optimized (NO) and with optimized (WO) semiconductors

The switching losses for a frequency of $f_{\text{sw}} = 10\,\text{kHz}$ are depicted in Fig. 5.38 and for $f_{\text{sw}} = 30\,\text{kHz}$ in Fig. 5.39 respectively. The conventional halfbridge shows stronger dependence on the load current compared to both snubber setups. With respect to the measured switching losses according Sect. 5.3.3, where recovery losses for the conventional halfbridge are approximately constant, this dependence is dominated by the turn-off and turn-on losses. Further, the DC-snubber is more affected by a higher load current than the active snubber. This is mainly related to the much higher turn-on losses, cf. Sect. 5.3.3 and further underlines the beneficial influence from the main stray inductance on active snubber setup during turn-on. A further remarkable relation is that both snubber setups show higher switching losses compared to the conventional halfbridge at very low current values below approximately 30 A. By comparing the losses measured, especially Fig. 5.23, it can be seen that the decrease in switching losses for lower current values is less compared to the conventional halfbridge. This effect has been discussed at the end of Section 5.2.1, and may be related to the used measurement setup. The finally not

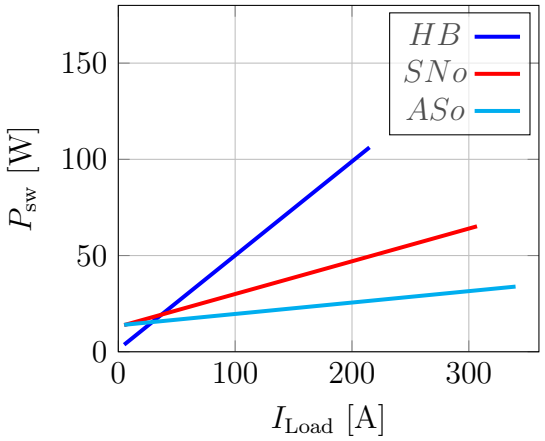


Figure 5.38: Switching losses at $f_{sw} = 10\,kHz$

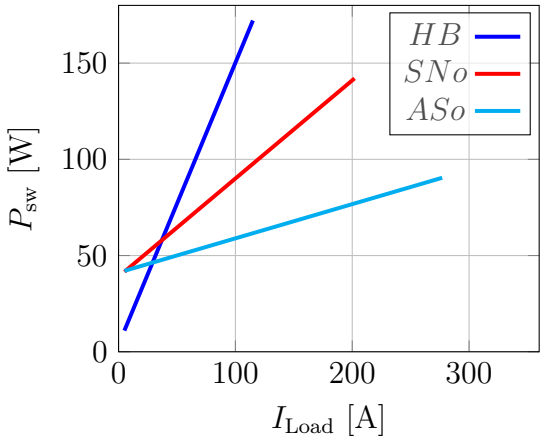


Figure 5.39: Switching losses at $f_{sw} = 30\,kHz$

clarified higher measured drain current for both snubber setups might be lower resulting in lower losses at lower load currents. However, it has been chosen to use the measured values and in conclusion, the conventional halfbridge can utilize the voltage drop at L_{main} more effective for very low currents. Hence, both snubber setups might not be reasonable for an application where the power module has to be dimensioned for a high peak load, while the majority of operation time is only at a power slightly above zero.
Another potentially limiting factor is the snubber temperature related to the losses caused by the capacitor ESR. As shown with (A.208) and (A.209), the losses of the chosen capacitor with low loss class I ceramic are only a small part of the total damping losses. As a result, the snubber temperature remains below $\vartheta_{Cmax} = 150\,°C$ as shown in Figs. 5.40 and 5.41. Hence, for both switching frequencies the snubber is not the limiting device. However, while the used capacitor has a very small ESR of $<4\,m\Omega$, see Fig. 4.2, the losses of a class II capacitor with much higher ESR, see Fig. 4.4, might lead to critical temperature increase especially for the DC-snubber. Alternatively, a non-optimal thermal dissipation, e.g. with a capacitor on driver board leading to a higher thermal resistance from capacitor to heat-sink, might not be possible even with a class I capacitor. However, it should also be considered, the thermal resistance R_{thSn} was estimated making various assumptions. Therefore, only a real inverter setup can finally show the feasibility of the calculated setups.

For the chosen parameters, both figures show that the temperature of both snubber setups remain uncritical. The increase of the temperature - and therefore the losses - is much lower for the active snubber setup. Hence, the active snubber setup is suitable for much higher output currents as already indicated in Section 4.8. Furthermore, in contrast to the model prediction in Fig. 4.21, the damping loss at very low load currents is not higher than the damping loss at the peak current value. Indeed, while this is also a result of the measured damping losses, see Sect. 5.3.4, this result might need further investigation because the measurement was only done at three different current values limiting the accuracy for very low current values.
With respect to the switching frequency, it can be noticed that the DC-snubber setup becomes critical at much lower current values. Extrapolating the DC-snubber temperature with the model parameters from Table C.1 and the given calculation scheme, see Sect. A.6, results in a critical current value of $I_{rms} = 505\,A$ for $10\,kHz$ and $I_{rms} = 293\,A$ for

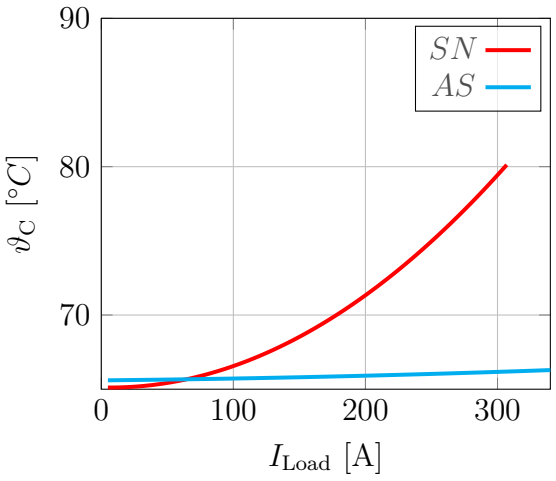


Figure 5.40: Snubber temperature at $f_{sw} = 10\,kHz$

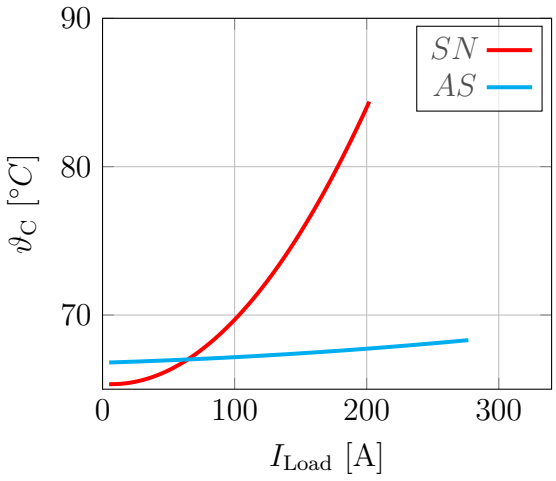


Figure 5.41: Snubber temperature at $f_{sw} = 30\,kHz$

30 kHz respectively. Contrary to that, the active snubber shows a limitation for currents above $I_{rms} > 2500\,A$ at 30 kHz and even higher for 10 kHz. Indeed, this value is only hypothetical because the power module is not suitable for currents in this range and a capacitor being effective for voltage reduction has to be designed much larger, which also reduces the ESR and R_{thSn}.

5.4.2 Achievable Inverter Output Power

In this section, the output power, achievable with a three phase setup build up with the power modules introduced in Section 4.1 and the thermal assembly described in Section A.5, is estimated according to Section A.6. Furthermore, an outlook is given for a DC- and active snubber setup with an optimized MOSFET to evaluate the potential semiconductor improvement, see Tab. 5.1.
The achievable output power for different configurations is depicted in Figure 5.42. The conventional halfbridge is always used as reference.

First, the focus is kept on the operation at $f_{sw} = 10\,kHz$. The achievable output power of the conventional halfbridge with considered to be temperature independent on-state resistance was calculated to be 170 kW. Due to lower switching losses, the DC-snubber setup reaches 23 % higher output power and the active snubber setup 43 % respectively. While these are the expectable improvements using the same MOSFET technology, the capability of optimizing the MOSFET allows further improvements. With respect to the conventional halfbridge - which cannot be further optimized - the DC-snubber (SNo) offers an improvement of 35 % more output power for $f_{sw} = 10\,kHz$. The active snubber (ASo) shows an increased output power of 59 % to the conventional halfbridge, which answers the research question to the influence on the system performance.
Changing the switching frequency from 10 kHz to 30 kHz significantly reduces the achievable output power of the conventional halfbridge by 46 % to 91 kW. However, both snubber setups with non-optimized MOSFETs are less affected with about 31 % reduction for the DC-snubber and 17 % for the active snubber due to lower switching losses. Admittedly, the active snubber setup at $f_{sw} = 30\,kHz$ achieves a slightly lower output power of 160 kW compared to the conventional halfbridge at $f_{sw} = 10\,kHz$ with 170 kW.

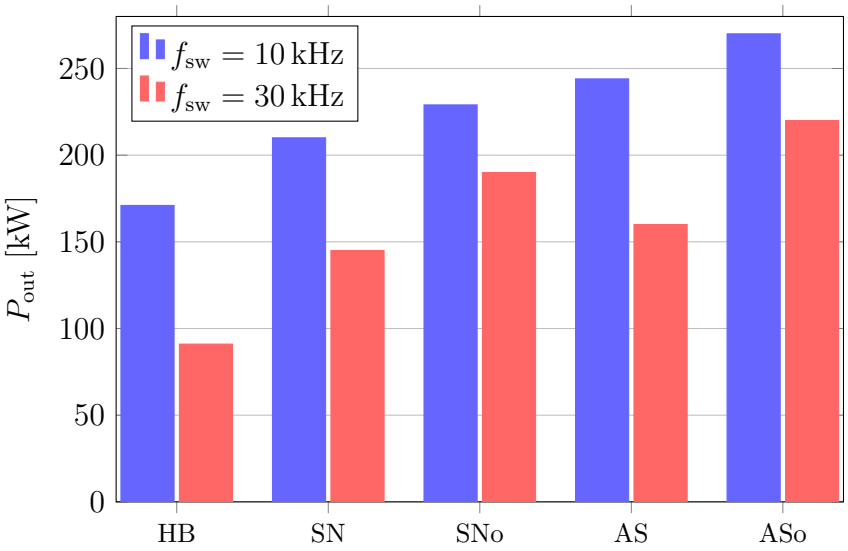


Figure 5.42: Achievable output power with $\vartheta_{HS} = 65\,°C$ assumed to be constant

With optimized MOSFET devices, the DC-snubber (SNo) achieves 190 kW output power, which is a reduction of 17 % compared to $f_{sw} = 10\,kHz$ and still lower than the conventional halfbridge. Contrary to that, the active snubber (ASo) reaches 220 kW, which is a reduction of 19 % compared to $f_{sw} = 10\,kHz$ and also 29 % above the conventional halfbridge.
It should be kept in mind that the thermal dependency of the MOSFET's on-state resistance was not considered. An increasing on-state resistance with increasing temperature would lead to higher conduction losses. Hence, the absolute estimated output power as well as the relation between the setups would result in lower values.
Considering the lower damping losses of the active snubber compared to the DC-snubber and its higher achievable output power, the active snubber may be a reasonable replacement for conventional state-of-the-art halfbridge power modules within this power range. This conclusion is also supported by achieving higher output power even at $f_{sw} = 30\,kHz$ and its potential of further motor loss reduction. However, latter has to be still quantified by measurements. Because the damping losses and thus, the losses in the snubber capacitor, are not affecting the results in Fig. 5.42 due to uncritical ϑ_C, see Figs 5.40 and 5.41. However, they contribute to the total inverter losses and thus, have influence on the module efficiency, which is part of the next section.

5.4.3 Inverter Efficiency

With the losses according Section 5.4.1 and the output power according Sect. 5.4.2, the inverter efficiency characteristic can be estimated with

$$\eta = \frac{P_{out}}{P_{out} + 6 \cdot (P_{sw} + P_{cond}) + 3 \cdot P_{damp}}, \tag{5.10}$$

by considering the losses of the six switches and the damping caused by the three snubber capacitors, one for each halfbridge.

At an inverter switching frequency of 10 kHz, see Fig. 5.43 it can be seen that the halfbridge has the highest efficiency for currents around approximately 30 A also compared with the snubber setups, see the discussion on Page 92ff. In case the true drain

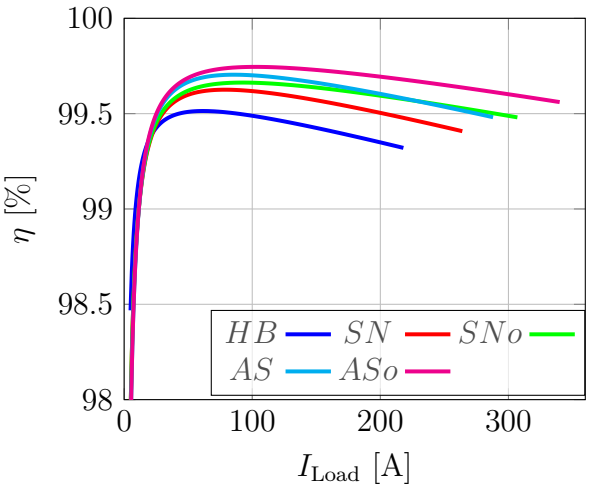


Figure 5.43: Inverter efficiency at $f_{\text{sw}} = 10\,\text{kHz}$

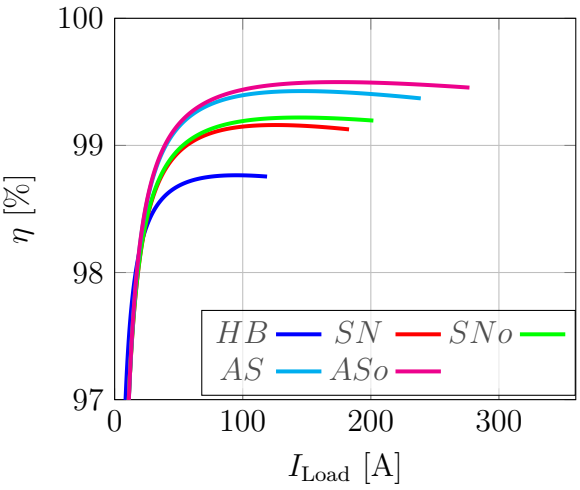


Figure 5.44: Inverter efficiency at $f_{\text{sw}} = 30\,\text{kHz}$

current for the turn-off event of the snubber setups is lower than measured, this would immediately change the efficiency at lower load currents to higher values than shown in Figs. 5.43 and 5.44. Nevertheless, for current values above 30 A both snubber setups are much more efficient with an efficiency >99 % up to the highest output current achieved with the particular setup. The halfbridge has a peak efficiency of $\eta_{\text{max10HB}} = 99.24\,\%$ at 13 % of the highest output current of $I_{\text{maxHB}} = 215\,\text{A}$.
Comparing the non-optimized snubber setups, it can be seen that the DC-snubber shows its highest efficiency of 99.33 % at an output current of 80 A, which is 30 % of the highest current achieved with $I_{\text{maxSN}} = 264\,\text{A}$. Contrary to that, the active snubber setup reaches $\eta_{\text{max10AS}} = 99.49\,\%$ at a similar current value. However, the active snubber setup allows a maximum inverter output current of $I_{\text{max10AS}} = 288\,\text{A}$.
A further improvement can be noticed for the optimized setups where the DC-snubber shows a peak efficiency of $\eta_{\text{max10SNo}} = 99.41\,\%$ also at $0.3 \cdot I_{\text{max10SNo}}$. The highest overall efficiency is achieved by the optimized active snubber with $\eta_{\text{max10ASo}} = 99.56\,\%$ as well as the highest output current with $I_{\text{maxASo}} = 340\,\text{A}$.

For an inverter switching frequency of 30 kHz shown in Fig. 5.44, the achievable efficiency is lower, which is plausible due to the three times higher switching and damping losses. Similarly to $f_{\text{sw}} = 10\,\text{kHz}$, the conventional halfbridge has a higher efficiency for output currents below approximately 30 A, while all snubber setups are better for current values above. However, by comparing the efficiencies in Fig. 5.43 and Fig. 5.44 it can be seen that the conventional halfbridge suffers strongly from a higher switching frequency by a peak efficiency decreased below 98 %. Further, it can be seen that the efficiency curves at 10 kHz show its maximum at lower values compared to 30 kHz and the efficiency decreases more significant at 10 kHz than for 30 kHz. Both can be explained by the current dependency of the conduction and switching losses, see Figs. 5.37 to 5.39. At 10 kHz the linear load current dependency of the switching losses has lower contribution to the total losses compared to the squared dependency of the conduction losses. Contrary to that, the contribution of higher switching losses at 30 kHz causes a more homogeneous efficiency

over a wide output current range. Additionally it can be seen that the active snubber setup for both optimized and non-optimized semiconductor shows superior efficiency to the DC-snubber setups as well as the conventional halfbridge.

The efficiency analysis supports the result from Section 5.4.2 that the active snubber is the more reasonable choice in terms of utilizing the semiconductor material especially for high desired output currents and switching frequencies. However, as mentioned above, if the application requires a peak output current much higher than the continuous current, both a DC-snubber or an active snubber might not be the reasonable setup in terms of losses. But by considering the not validated yet higher measurement losses at lower current values, see P. 92ff, this restriction might be challenged. Additionally, both snubber setups benefit from fast switching causing high voltage slopes. Nevertheless, high voltage slopes might be undesired depending on the application, which is subject of the next chapter.

6 Operation with Pulsed LC filter

In the previous sections it has been shown that the active snubber concept allows faster switching compared to a conventional halfbridge setup and the damping losses as well as the switching losses are significantly reduced. While this is beneficial for higher load currents and thus, for higher inverter output power this is at the expense of higher voltage slopes up to 80 GV/s, cf. Fig. 5.19. This might not be tolerated by every application. Typical cases where a comparatively slow voltage slope is mandatory are for example applications in which the length of the connection cable between inverter and electric motor is long in terms of rise-time to propagation delay ratio, see [132], or applications where the motor windings suffer from high voltage slopes [24]. Additionally higher slopes cause higher frequency harmonics and may cause EMI problems. Possible countermeasures are the use of large filters to suppress the harmonics, see e.g [26, 133, 134] or slowing down the semiconductor switching speed for the sake of higher switching losses. Due to higher switching losses it might be necessary to reduce the switching frequency to keep the semiconductor losses in a manageable range. As described by [131], a lower switching frequency has also influence on the motor losses in terms of higher magnetic losses due to higher amplitude harmonics. An optimal inverter has a sinusoidal output voltage at the desired frequency, typically in the range from 0 Hz up to a few hundred Hertz depending on the target application. However, due to this low frequency range, fast switching semiconductors with low switching losses necessitate huge and expensive filter components.
To allow fast switching without the need of a huge and expensive filter, in [27] a controlling scheme for a smaller LC output filter actively driven by the power switches has been proposed. The active controlling allows a much smaller filter dimension compared to a typical sinusoidal filter and thus reduced cost. However, the active controlling causes more switching events and thus higher losses. Hence, it depends strongly on the achievable switching loss reduction whether this technology is applicable [135]. Thus, the combination of the active snubber concept with the actively controlled filter might be a desired combination in applications with a need for increased efficiency combined with the requirement of slow voltage slopes.
To investigate the compatibility and possible design limitations, this chapter presents the findings from [136] about the combination of the active snubber setup with the actively driven filter. Additionally, the findings are set in this work's context and further relations are shown. Additionally, equal to [136], the setup is compared to a state-of-the-art IGBT setup as a reference for a mentioned slow switching application and shall allow a better interpretation of the results. First, the filter controlling scheme is introduced. Afterwards, the filter component is designed for double-pulse measurements. Further, the setup is used to perform a turn-on event in terms of decreasing output voltage slope and a turn-off event in terms of an increasing output voltage slope.

6.1 Active Filter Introduction

To offer the reader an insight to the basic principal of the actively driven filter a brief introduction shall be given in this section.
As proposed by [137] an LC-low-pass-filter is connected between the AC-terminal and

the DC-minus potential. Figure 6.1 shows the active snubber setup with the mentioned low-pass filter. It is assumed that initially the power semiconductor Q_2 is in on-state and the filter capacitor C_f is discharged.

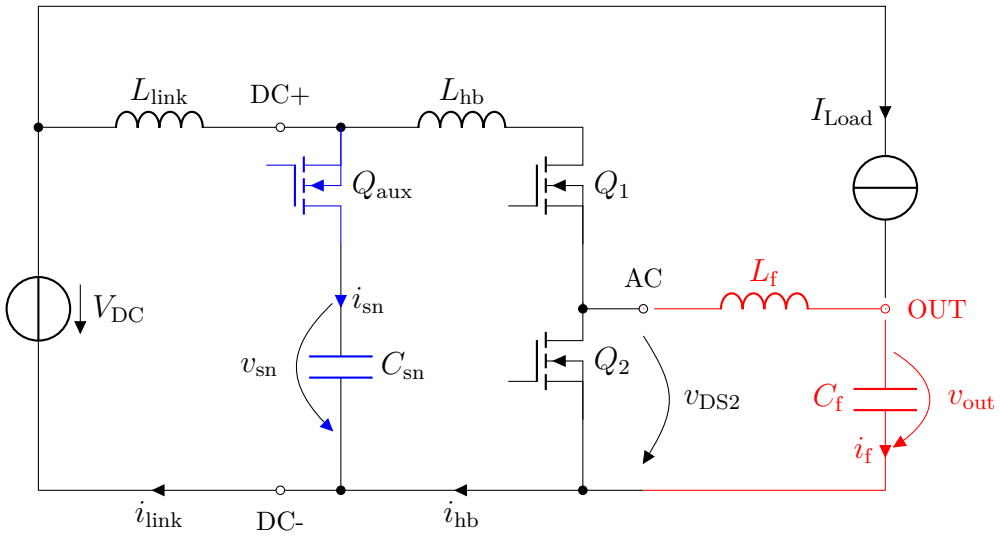


Figure 6.1: Basic active filter circuit, based on [136]

After the first turn-off of Q_2 the voltage at the AC-terminal increases with respect to the DC-minus potential. As a result, a current starts flowing through the filter inductance L_f and the filter capacitor C_f starts charging as illustrated in Figure 6.2. After the filter capacitor is charged up to $v_\mathrm{out} = V_\mathrm{DC}/2$, the power switch Q_2 is turned on again. Due to the current flow through the filter inductivity, the filter capacitor is further charged with decreasing voltage slope. By proper dimension and timing, the output voltage v_out reaches the level of V_DC with a filter current of $i_\mathrm{f} = 0\,\mathrm{A}$. At this point in time, the power semiconductor is turned off again and the output voltage remains at V_DC.

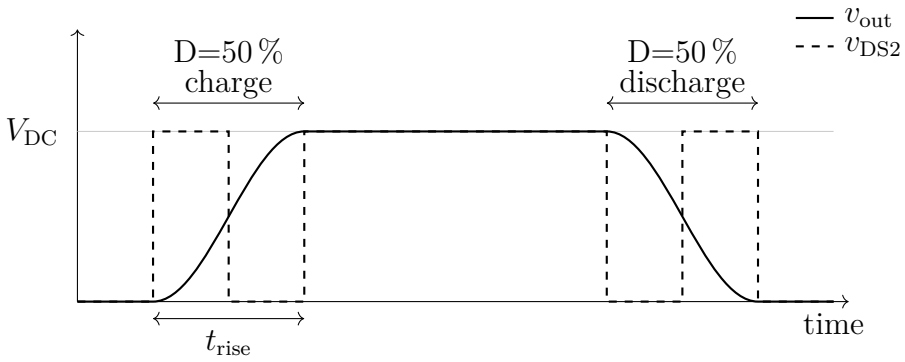


Figure 6.2: Active filter principle of operation after [137]

The resulting duty-cycle results in $D = 50\,\%$. The load connected to the OUT-Terminal is stressed with the less steep voltage slope of v_out compared to a load connected to the AC-terminal. For the discharge pulse, the switching scheme is repeated in inverse manner. Further, the setup allows slower voltage slopes of v_out generated by more switching events with a more complex timing as published in [138].

6.2 Filter Dimensioning

For the investigation a filter is dimensioned according to [137] for a peak charge current of 25 % of the desired maximum load current of 350 A and a rise time of $t_{\text{rise}} = 1\,\mu\text{s}$.
As presented by [137], the peak charge pulse current and the rise time can be calculated with

$$\hat{i}_{\text{f}} = \frac{V_{\text{DC}}}{\sqrt{L_{\text{f}}/C_{\text{f}}}} \sin(\frac{\pi}{3}) \quad \text{and} \tag{6.1}$$

$$t_{\text{rise}} = \frac{2\pi}{3}\sqrt{L_{\text{f}}C_{\text{f}}}. \tag{6.2}$$

With the selected constrains and by rearranging (6.1) and (6.2), the capacitor can be calculated to

$$C_{\text{f}} = \frac{\sqrt{3}t_{\text{rise}}\hat{i}_{\text{f}}}{\pi V_{\text{DC}}} = \frac{\sqrt{3}\cdot 1\,\mu\text{s}\cdot 0.25\cdot 350\,\text{A}}{\pi\cdot 600\,\text{V}} = 80\,\text{nF}. \tag{6.3}$$

Due to the availability, a polypropylene capacitor with 68 nF has been selected, which allows to calculate the inductivity yielding

$$L_{\text{f}} = \frac{9t_{\text{rise}}\hat{i}_{\text{f}}}{4\pi^2 C_{\text{f}}} = \frac{9\cdot 1\,\mu\text{s}\cdot 87.5\,\text{A}}{4\pi^2\cdot 68\,\text{nF}} = 3.3\,\mu\text{H}. \tag{6.4}$$

This inductivity was implemented as a manually winded air coil.
The chosen components result in a resonant frequency of

$$f_{\text{resf}} = \frac{1}{2\pi\sqrt{3.3\,\mu\text{H}\cdot 68\,\text{nF}}} = 336\,\text{kHz}, \tag{6.5}$$

and bode plot of the designed LC-filter shown in Figure 6.3 proofs the calculation of f_{resf}. Further, the filter shows an increased gain at its resonant frequency as well as a strong decreased negative gain peak at 3 MHz, which points to a further resonance peak with a parasitic element. The shape of the curve with a plateau at −40 dB at 10 MHz and the phase respond, points to a parasitic inductance of the capacitor of

$$L_{\text{Cf}} \approx 3.3\,\mu\text{H}\cdot 10^{\frac{-40\,\text{dB}}{20}} = 33\,\text{nH} \tag{6.6}$$

verified by spice simulation. This is plausible due to the axial capacitor design.

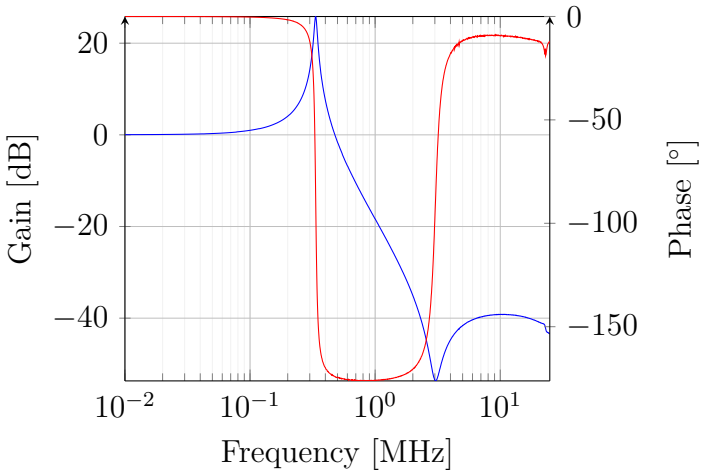


Figure 6.3: LC-filter bode plot, based on [136]

Further, a decreasing gain for frequencies above 10 MHz points to further parasitics, e.g. a parasitic capacitance of the inductivity, which may reduce the filter efficiency for high frequencies. A spice based simulation of the filter points to a parasitic capacitance of the filter inductivity in the lower pF-range, which cannot be determined further.

6.3 Discharge Pulse

In this section, the discharge pulse is performed with the active snubber setup leading to a negative voltage slope of v_{out} and shall simulate a turn-on event from the load point of view. The pulse is performed within a double pulse setup. The gate control signal for each switching event is modified by a dedicated timing circuit, which derives the timing sequence needed for the active filter. The timing and the duty-cycle of the sequence is adjusted manually with the goal that the output voltage does not oscillate after the sequence is finished for $t > 1\,\mu$s, cf. Fig. 6.4. Because the duration of the switching sequence for the discharge pulse is much longer compared to a single switching event, a high load inductance is chosen. This causes only a negligible rise in load current between the switching events. The gate resistors are chosen according Table 5.2.
The corresponding switching curve is shown in Figure 6.4. Initially, the power switch Q_2 is in blocking state and according Figure 6.1, the load current of 350 A is flowing through the body diode of Q_1.

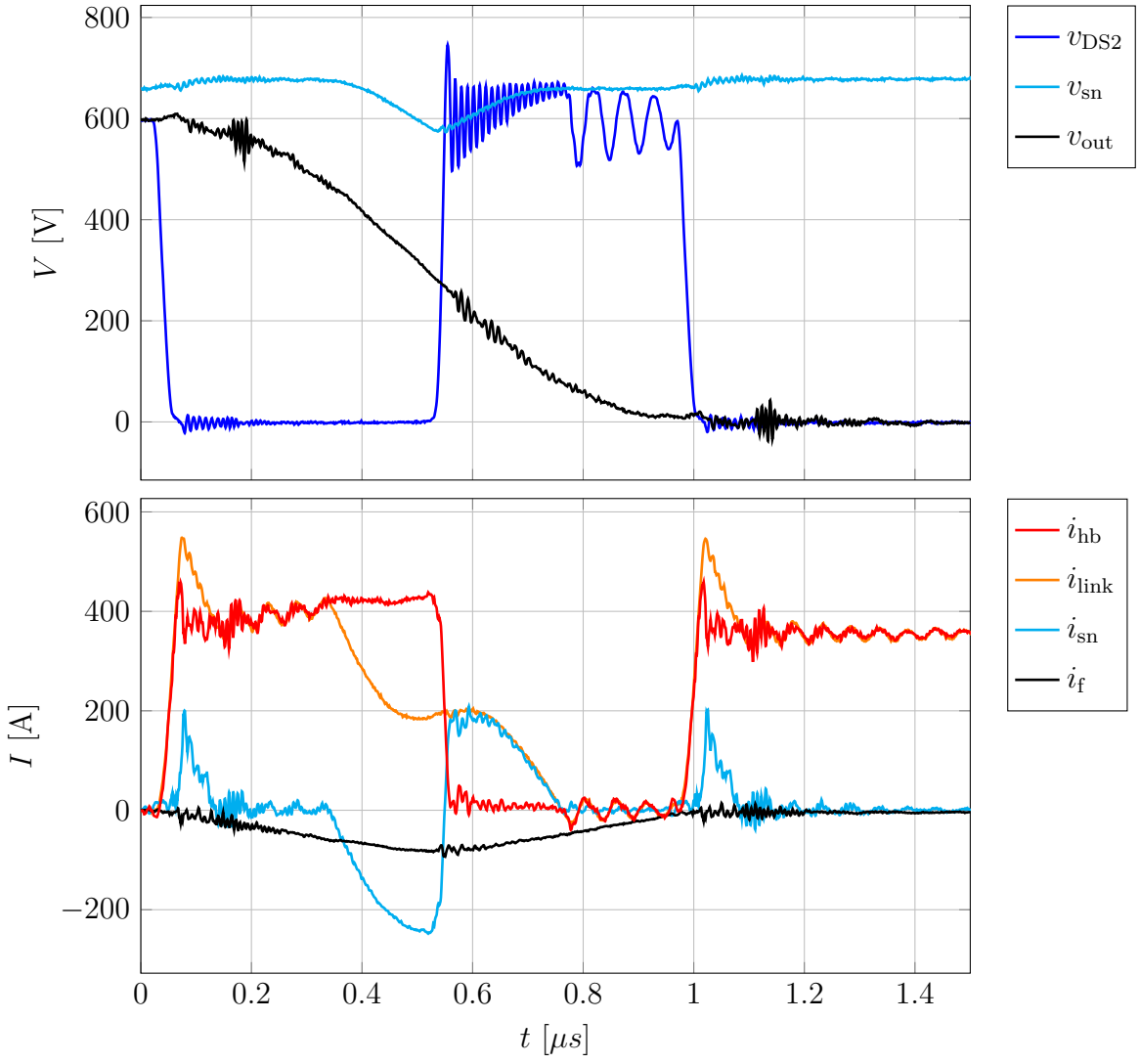


Figure 6.4: Discharge pulse, based on [136]

As it can be seen in Figure 6.4, the initial snubber voltage, cf. v_{sn}, is above the DC-link voltage $V_{\mathrm{DC}} = 600\,\mathrm{V}$ due to previous switching events within the double pulse sequence. The turn-on event of Q_2, beginning at approximately $t = 20\,\mathrm{ns}$, is very similar to the turn-on event analyzed in Section 5.2.2 and shows similar effects in terms of occurring frequencies. Furthermore, the voltage and current waveform of the filter signals, cf. v_{out} and i_{f} in the interval $100\,\mathrm{ns} < t < 200\,\mathrm{ns}$, show a high-frequency signal according (5.9) passing through the LC-filter. This high-frequency path-through was already assumed after analyzing the bode plot on Page 119. Further, the filter current increases the DC-link i_{link} current and halfbridge current i_{hb} in the interval $20\,\mathrm{ns} < t < 530\,\mathrm{ns}$.
Before the second switching event is timed, the auxiliary switch is turned-on with a lead time according to (3.51). As it can be seen in the output voltage as well in the filter current, the initiated oscillation process starting at $t = 330\,\mathrm{ns}$ has no influence on the filter signals. This is plausible due to turned on Q_2 which shortens the output filter.
Contrary to the theory given by [137] the manually adjusted timing does not result in a duty-cycle of $D = 50\,\%$ to achieve a non-oscillating output voltage after the pulse sequence. With respect to the $50\,\%$ values of v_{DS2} equal to $300\,\mathrm{V}$, the first pulse-time $20\,\mathrm{ns} < t < 530\,\mathrm{ns}$ is slightly longer compared to the second from $530\,\mathrm{ns} < t < 1\,\mu\mathrm{s}$. This results in a duty-cycle of

$$D = \frac{530\,\mathrm{ns} - 20\,\mathrm{ns}}{1\,\mu\mathrm{s} - 20\,\mathrm{ns}} = 52\,\%. \tag{6.7}$$

As a result, the output voltage at the second switching event at $t = 530\,\mathrm{ns}$ is below $V_{\mathrm{DC}}/2$. This effect is further explained below.
After the second switching event, in the interval $540\,\mathrm{ns} < t < 700\,\mathrm{ns}$, the output voltage shows a beat with a mean frequency of about $f_{\mathrm{R}} = 82\,\mathrm{MHz}$ and a frequency of the hull curve of about $f_{\mathrm{B}} = 11\,\mathrm{MHz}$. According to the well known theory of coupled oscillators based on trigonometric identities the two fundamental frequencies can be calculated to

$$f_1 = f_{\mathrm{R}} + f_{\mathrm{B}} = 93\,\mathrm{MHz} \quad \text{and} \tag{6.8}$$

$$f_2 = f_{\mathrm{R}} - f_{\mathrm{B}} = 71\,\mathrm{MHz}. \tag{6.9}$$

Because the beat is missing in the filter current signal i_{f} and f_1 is very close to the oscillation according (5.8), the conclusion can be made that, considering Fig. 6.1, the second frequency f_2 results from an interaction with the load inductance. Otherwise, a possible interaction might be caused by the parasitic capacitance of L_{f} interacting with the load connection and inductivity or an interaction of the filter inductance with a parasitic load capacitance and needs further investigation.
In the interval $530\,\mathrm{ns} < t < 1\,\mu\mathrm{s}$ the power switch Q_2 is in blocking state. The increasing snubber voltage with a value above the DC-link voltage counteracts the filter current more effective compared to a voltage equal to V_{DC}. Hence, the duration until the filter current and the derivative of the output voltage become zero is shortened compared to the theory given by [137]. This causes the already mentioned deviance in the duty-cycle of $2\,\%$.

6.4 Charge Pulse

Similar to the previous section, the charge pulse is performed within a double pulse sequence under similar conditions. Hence, the snubber capacitor is charged up to a voltage of $715\,\mathrm{V}$ higher than the DC-link voltage shown in the corresponding switching curve depicted in Figure 6.5. With a lead time according to (3.51), the auxiliary switch Q_{aux} of

the active snubber path is turned on and the discharging snubber capacitor decreases the DC-link current i_{link}. At $t = 300\,\text{ns}$, the power switch Q_2 is turned off and initiates the filter charging process by increasing the filter current. As it can be seen in the interval

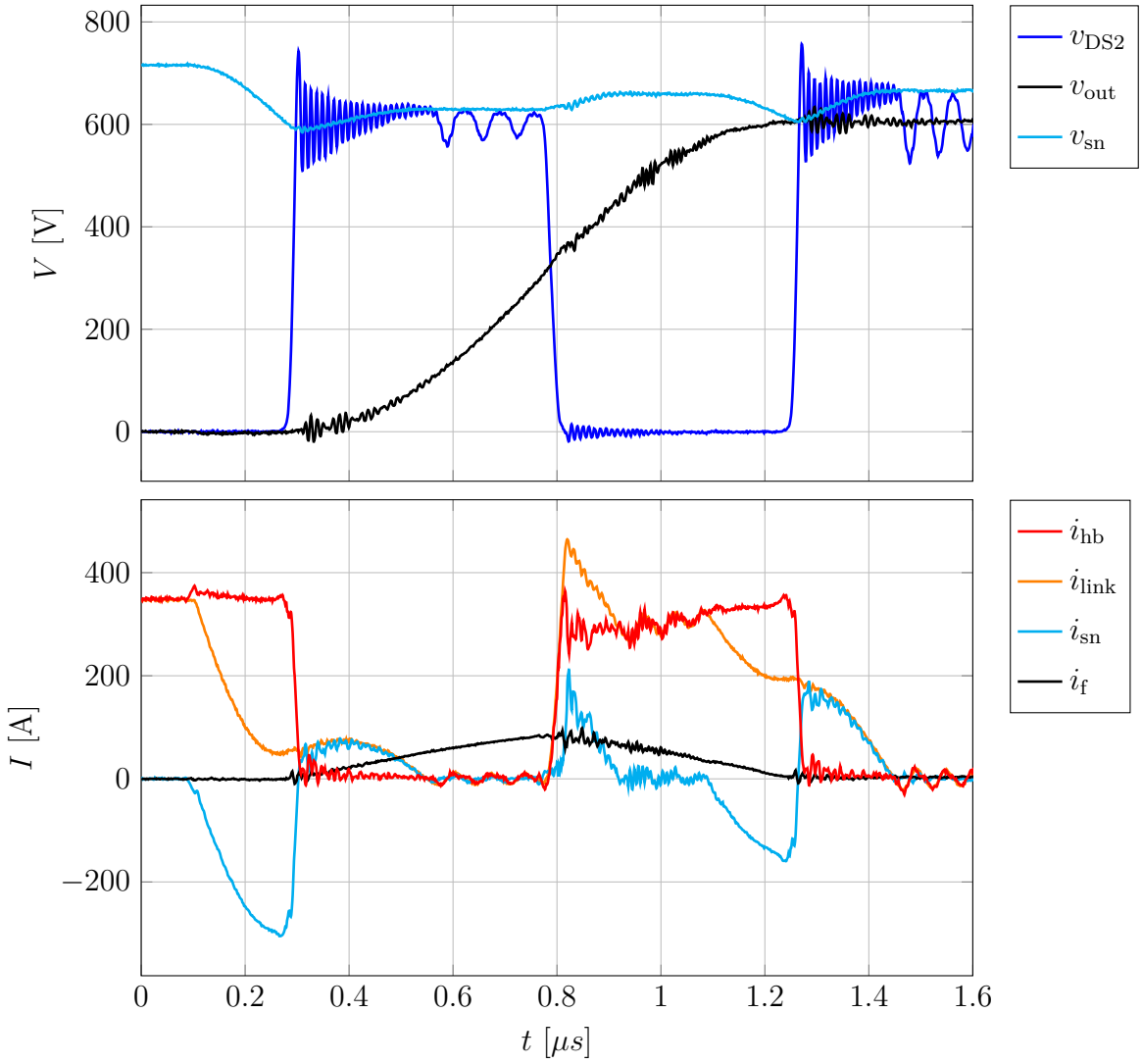


Figure 6.5: Charge pulse, based on [136]

$300\,\text{ns} < t < 500\,\text{ns}$ the output voltage v_{out} shows the beat frequency already found in the discharge pulse, cf. page 121.
Similar to the discharge pulse, the manually adjusted duty-cycle, as a relation of on-time to cycle-time for Q_1, does not fit to the theory with respect to the 10 % values of i_{hb} and v_{DS2}. A duty-cycle of $D = 48.7\,\%$ had to be adjusted to prohibit an oscillation of the output voltage for $t > 1.25\,\mu\text{s}$, cf. Fig. 6.5. This can be explained similarly with the increasing snubber voltage and the resulting stronger filter current increase. After the first turn-off event of Q_2, the snubber current increases and accelerates the filter charging. However, the remaining energy in the stray inductance is less compared to the turn-off event in Figure 6.4. This reduction is related to the double pulse measurement leading to a different snubber voltage at the beginning of the sequence compared to the discharge pulse. As a result, the relative deviance of D compared to the theory is also

less compared to the discharge event. Considering Sect. 4.8, this predicts a load current dependent duty-cycle.

6.5 Comparison to IGBT-Setup

As mentioned in the introduction, a possible measure to deal with the disadvantages of high voltage slopes is decelerated switching speed. Further, silicon IGBTs are still the common power semiconductor. Similar as published by [136], in this section a state-of-the-art IGBT module [139] with dedicated DC-link capacitor [140] is used as reference setup. It is compared to the setup shown in Figure 6.1.
Goal of the comparison is to investigate the benefits for a system replacement in a quantitative manner especially focusing the efficiency. To investigate this, the gate resistors were varied to evaluate the losses at different switching speeds. Firstly, the gate resistor was adjusted to achieve a voltage slope similar to the maximum slope achieved with the active filter of $dv/dt_{\mathrm{max}} = 1\,\mathrm{kV}/\mu\mathrm{s}$. Secondly, the gate resistor was adjusted to the nominal operation point according the device datasheet [139]. Finally, the gate resistor was chosen very small to evaluate the maximum achievable switching speed, which allows to derive whether the active snubber module is a reasonable replacement for the IGBT module setup in terms of losses.

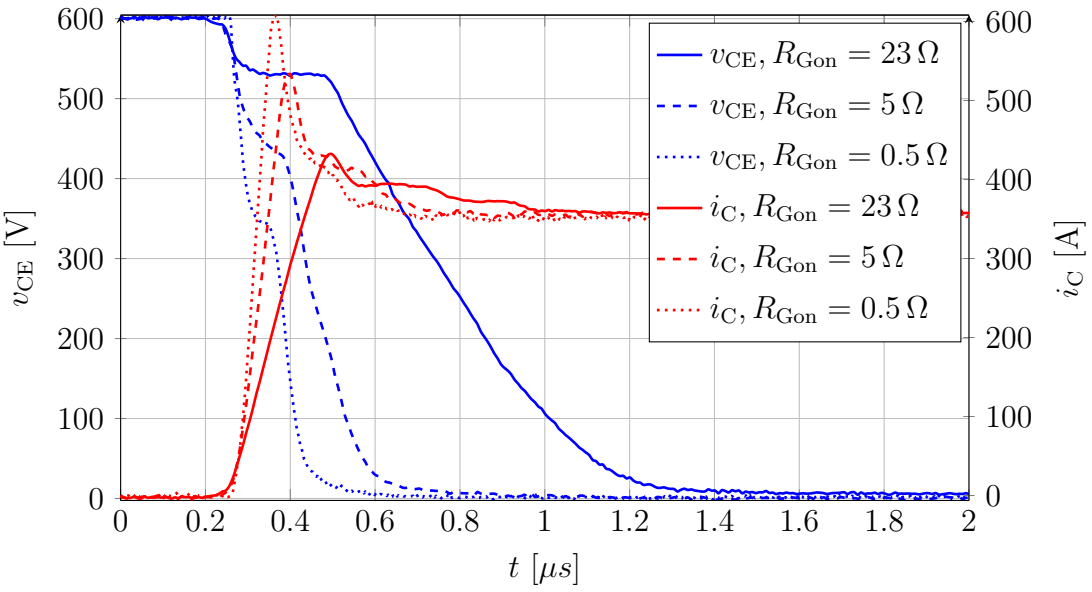


Figure 6.6: IGBT turn-on reference, based on [136]

The switching curves for the turn-on event with different R_{Gon} values are shown in Figure 6.6. First, it can be noticed that for all switching speeds the waveforms show no oscillation. By analyzing the collector current, a significant tail-current from the freewheeling diode can be noticed. The resulting parameters for turn-on and diode reverse recovery are shown in Tables 6.1 and 6.2.

Table 6.1 indicates that for a slow switching event with $R_{\mathrm{Gon}} = 23\,\Omega$, causing similar voltage gradient compared to the LC-filter setup, excessive switching losses of 93 mJ have to be accepted. Additionally, even at accelerated conditions with an $R_{\mathrm{Gon}} = 0.5\,\Omega$, the turn-on losses decrease only by a factor of approximately 5. This non-proportional

Table 6.1: Turn-on parameters

R_{Gon} $[\Omega]$	E_{on} $[mJ]$	dv/dt_{max} $[kV/\mu s]$
23	92.7	-0.96
5	33.2	-2.15
0.5	17.4	-5.3

Table 6.2: Diode recovery parameters

R_{Gon} $[\Omega]$	E_{rec} $[mJ]$	dv/dt_{max} $[kV/\mu s]$
23	4	1.09
5	7.9	10.8
0.5	11.5	23.2

scaling is maybe related to an effective negative feedback loop caused by a common stray inductance in control and power path or a collector-gate capacitance, cf. e.g. L_{S} and C_{DG} in Fig. 2.7. These may counteract the gate driver slowing down the switching speed. Another possible limitation might be influenced by the charge density and carrier life time as mentioned in [4] P. 220.
Contrary to the turn-on losses, the recovery losses increase with accelerated switching speed. However, the absolute value of the recovery losses, especially for a gate resistor of $0.5\,\Omega$, are less compared to the turn-on losses. A further important deviance is the significant difference in the maximum voltage slope especially for faster switching. Because the used passive voltage probes connect the measured system to the oscilloscope reference potential, only the bottom system could be measured. Therefore, the top system is used as switch for the diode reverse recovery measurement. In case both systems, top and bottom, differ in their negative feedback loop, the switching speed also differ. Hence, the resulting reverse recovery parameters according Table 6.2, may not be equal to the parameters for the free wheeling diode of the bottom switch.
In Figure 6.7 the switching curves for the turn-off event of the bottom-side IGBT are depicted for different gate resistors. By analyzing the collector current, the current-tail is less compared to the diode-tail shown in Figure 6.6.

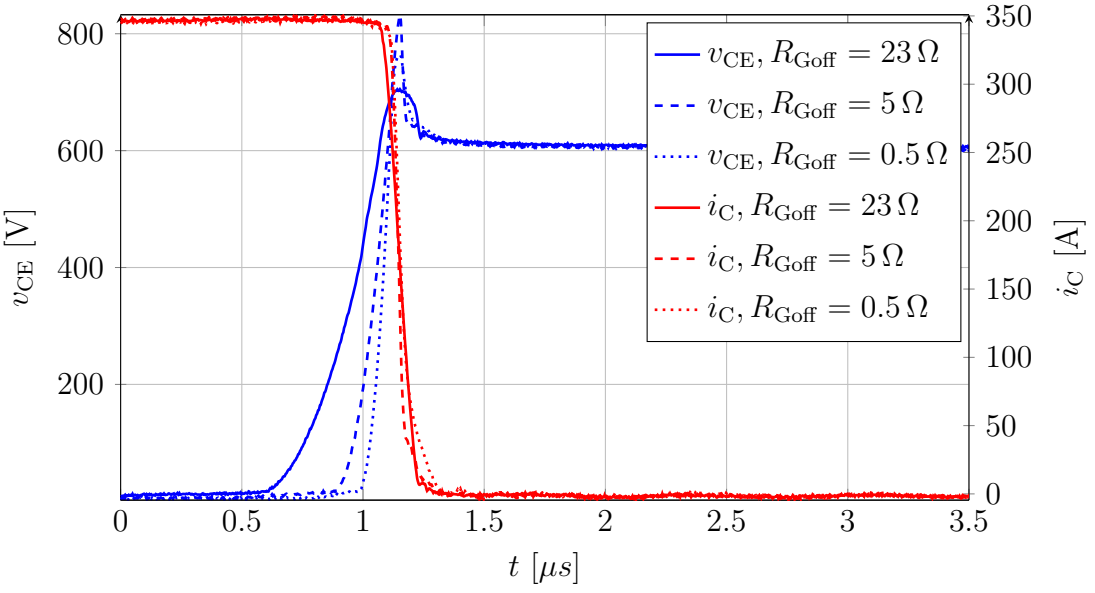


Figure 6.7: IGBT turn-off reference

However, no oscillation occurs independent of the used gate resistor. The resulting parameters are shown in Table 6.3 First it can be noticed for the IGBT that the maximum

Table 6.3: Turn-off parameters

R_{Goff} $[\Omega]$	E_{off} $[mJ]$	dv/dt_{max} $[kV/\mu s]$
23	61	1.9
5	31	4.5
0.5	24.3	7.3

voltage slopes are higher compared to Table 6.1. Further, the IGBT turn-off losses at $R_{\text{Goff}} = 23\,\Omega$ are approximately 30 % lower compared to the corresponding IGBT turn-on losses, while the losses at nominal gate resistor of $5\,\Omega$ are very similar.
However, the IGBT turn-off losses for $R_{\text{Goff}} = 0.5\,\Omega$ are about 40 % higher compared to the corresponding turn-on losses. Hence, the turn-off losses decrease less with lower gate resistor compared to turn-on. This effect can be explained by comparing both figures, 6.6 and 6.7. Analyzing the voltage waveform points to a significant influence of the system stray inductance. While faster switching at turn-on causes a higher voltage drop, the switching event becomes more soft. On the other hand, a faster switching at turn-off cause a higher voltage overshoot reducing the effect of loss reduction for faster switching.

With the measurement results from the IGBT and the active snubber a quantitative comparison can be done. In Figure 6.8, the switching energies for the IGBT setup with the adjusted switching speeds as well as for the active snubber setup with the LC-filter are depicted. However, it is important to mention that the depicted losses for the active

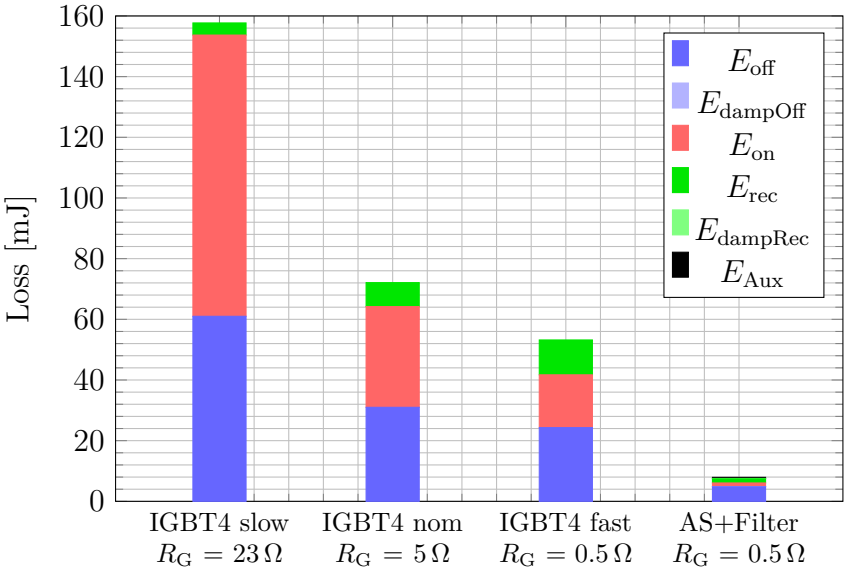


Figure 6.8: Energy comparison, based on [136]

snubber setup combined with the LC-filter are the summarized switching losses over all six single switching events shown in Figs. 6.4 and 6.4. This shall give a better expression to compare the losses for an event with a positive and a negative output voltage slope as a load would be stressed with.

Knowing about the switching losses allows judging the comparability of the IGBT setup and the active snubber setup in terms of current capability. From Fig. 6.8 it can be derived that the IGBT-setup within an application needing a rather slow voltage slope, e.g. due to long motor wires, would cause significant semiconductor switching losses. The comparative active snubber setup designed for a similarly slow voltage slope would cause about 20 times less losses. It should be noted that the losses of the used LC-filter are not considered because a filter not optimized for losses was used. The losses of a filter would reduce the efficiency of the active filter setup compared to the IGBT setup without additional filter.
Applications with no need for such very slow slopes are represented by the nominal IGBT operation point. Regardless faster switching speed with $R_{\mathrm{Gon}} = 0.5\,\Omega$, the IGBT shows still significantly higher switching losses. Finally, the IGBT with lowest gate resistors, representing a setup with maximized switching speed, suffers from an intrinsic speed limitation most likely limited by the charge carrier extraction. Hence, it is also not reasonable to operate the active filter with an IGBT due to the higher count of necessary switching events.
The active snubber setup used to drive an LC-filter combines both, slow current slopes as well as low switching losses. Further work may target a proper LC-filter dimensioning with improved HF-blocking and designed for continuous inverter operation. With such a filter, a better estimation of conductive filter losses can be made, which would add up to the above mentioned losses.
In Figures 6.4 and 6.5, it can be noticed that the oscillating snubber current i_{sn} has a period duration in the range of the total switching cycle. While the LC-filter was designed for a voltage slope of $1\,\mathrm{kV}/\mu\mathrm{s}$, this snubber current oscillation period limits the minimum time between the switching events an thus, the maximum achievable voltage slope.
A possible limitation might be the influence of a higher snubber voltage on the necessary duty-cycle to achieve an output voltage after the slope without oscillation. This may necessitate a continuous duty-cycle adjustment during sinusoidal output current operation depending on the load current dependent snubber voltage level, cf. e.g. Fig. 4.21.

7 Summary and Outlook

7.1 Summary

This work is about an active snubber circuit with an unsymmetrical system stray inductance build into a power module. The setup is based on a DC-snubber and an additional auxiliary series switch in the DC-snubber path. The manner of active operation shown in this work allows a large stray inductance during turn-on as well as a small stray inductance during turn-off and diode recovery without the disadvantages of a conventional DC-snubber. This allows the switching speed to be maximized, leading to a significant voltage drop during turn-on, making use of the large stray inductance to the main DC-link capacitor. For turn-off, a very low stray inductance allows fastest switching. It could be shown that the proposed manner of operation of the active snubber allows storing the energy from the system stray inductance before the turn-on and makes use of it in subsequent switching events by temporary unburdening the main DC-link capacitor. Hence, by cost of slightly increased controlling effort the switching losses are significantly reduced. The presented manner of operation further allows to use this stored energy to reduce ringing duration and shifts this otherwise lost damping energy to the load. Additionally, the buffering effect of the snubber capacitor reduces the turn-off voltage overshoot and thus, may further allow the reduction of the specific on-resistance of the used SiC MOSFET.
To find potential points to consider and allow proper dimensioning, the turn-off as well as the turn-on sequence was mathematically modeled. The calculations were validated by measurements afterwards. Furthermore, the model makes some assumptions, which allow to describe a fast switching event at high currents with very good accuracy. However, these assumptions lead to an inaccuracy especially for low and very low load currents. Nevertheless, the mathematical description was applied alternately for turn-on and turn-off showing that the mean snubber capacitor voltage converges to a stable voltage. Further, it could be shown that the effective usage of the snubber energy reduces the maximum expectable capacitor voltage to lower values than to be expected for a similar DC-snubber setup. This allows to use a capacitor with lower capacitance as it would be necessary for DC-snubber designed for similar turn-off overvoltage suppression. With the mathematical description a dependency between the zero crossings of the snubber current and the used timing was predicted. While the auxiliary switch in series to the snubber capacitor is meant to be switched at zero current, this dependency would increase its losses or necessitate continuous timing adjustments. The model was used to derive an optimal timing, which makes the zero crossings of the snubber current independent of the load current over a wide range.
The active snubber setup used for validation was compared in its switching behavior to two very similar other setups, a conventional halfbridge and a halfbridge with DC-snubber. After dimensioning the three setups to achieve maximum switching speeds at two different stray inductance values to the main DC-link capacitor, the measurements were compared to outline remarkable differences. The measurements indicated that both snubber setups the DC-snubber and the active snubber, are identical in their current and voltage behavior during turn-on until the voltage overshoot occurs. As expected, due to its much higher system stray inductance, the conventional halfbridge had to be deceler-

ated by higher gate resistors, while both snubber setups were able to switch at highest switching speed. However, it was also found that the used state-of-the-art Rogowski coil is a major limitation for proper judgment of the switching behavior and shows the need for development of better measurement devices. Additionally, a lower drain current during turn-off is expected and was also simulated in a complex simulation. However, because the cause of the higher measured drain current could not be found, further investigation is necessary.
For turn-on, the active snubber can utilize the larger system stray inductance and the resulting large voltage drop during the positive current slope. Contrary to that, the conventional halfbridge cannot utilize this benefit of a large stray inductance and had to be switched with much higher gate resistor to not exceed the overvoltage during diode recovery. Additionally, the DC-snubber buffers the voltage drop leading to the highest turn-on losses over all three setups. Similarly, the DC-snubber showed the highest damping losses and confirms the literature. Contrary to that, the active snubber, making use of the energy, shows much lower damping losses and is also less affected by the load current, which makes it applicable for higher current applications than a DC-snubber. In addition, while the conventional halfbridge showed the lowest damping losses, the ringing voltage amplitude is the highest compared to the active snubber showing the lowest voltage ringing amplitude. However, different stray inductances located in different circuit parts being relevant at different time spans showing the most complex ringing scheme with different frequencies and ringing sequences. Hence, the active snubber combines both benefits a low oscillation amplitude as well as low oscillation losses.
To quantize the active snubber appropriateness for inverter operation, it is compared with the two other mentioned setups within a theoretical inverter design. The total system losses, the achievable inverter output power as well as the inverter efficiency was calculated for the conventional halfbridge, the DC-snubber and the active snubber. Further, for the two snubber setups an optimized MOSFET designed for lower voltage overshoot is estimated to give a range which can be expected if the active snubber benefits are utilized. It was found that for a common switching frequency of 10 kHz the active snubber allows about 40 % higher output power compared to a conventional halfbridge as well as a maximum inverter efficiency of about 99.5 %. Additionally, for the hypothetical optimized MOSFET the expected system efficiency exceeds 99.5 %. Further, it could be shown that for the active snubber a lower dependency on the switching frequency can be expected. However, while a temperature independent on-state resistance was assumed, a temperature dependency would reduce the efficiency of all setups.
While the active snubber is beneficial in terms of lowest switching losses it might not be suitable for applications where steep voltage slopes are undesired. Therefore, finally, the active snubber is used to drive an actively pulsed LC-filter, resulting in much lower output voltage gradients. It was found that the timing of the pulse sequence shows a dependency on the state of charge of the snubber capacitor resulting in either a ringing in the output voltage or a need for snubber voltage-dependent timing adjustments. Further, while the LC-filter was exemplary designed for a voltage rise time of about 1 μs, the timing and the oscillation duration of the active snubber limits much smaller rise times.
The setup is compared with a state-of-the-art IGBT setup commonly used for applications with restricted high voltage slopes. It was shown that the active snubber setup combined with the LC-filter allows less steep voltage slopes as well as a reduction of the switching losses. Compared to the IGBT setup slowed down to similar rise time a loss reduction by

a factor of 20 could be found. However, while the losses of the active snubber together with the filter are only dependent on the number of switching events, the highest achieved voltage slope of the IGBT setup, resulting in up to 23 kV/μs results in about 6.7 times higher switching losses than the active snubber.

7.2 Outlook

Mathematical model:
The derived mathematical model is helpful to determine the expectable damping losses and to calculate the appropriate timing of the auxiliary switch. This allows to predict the device stress in critical high load conditions. While the setup is meant to be switched at highest switching speeds also covered by the model, there might be use cases, where the assumption might not be applicable. This would lead to inaccuracies of the model. Further work might target the improvement of the mathematical model for a wider range of applications covering also the operation at low and very low load currents.
A specific load current is defined as high or low and is mainly dependent on the reverse recovery current of the body diode. This might be critical for the model reliability in case a super junction MOSFET is used, which usually has a higher reverse recovery peak current, cf. e.g. [127].

Model validation and measurement:
In Section 5.2.1, an unexpected high drain current during the turn-off voltage slope was discussed and investigated by simulation. However, it was not able to clarify beyond doubt whether this higher drain current is true, leading to higher device losses. It is mandatory to clarify whether the measurement can be trusted or if there are effects may be related to the indirect drain current measurement done by measuring the DC-link current and subtracting the snubber current or if there are setup influences. Therefore, further investigation may target a direct drain current measurement or vary the setup to uncover dependencies not considered during the simulations. The measurement of the drain current has a direct effect on the findings of the inverter design. However, it is expected that the improved drain current measurement would lead to a reduced current during the voltage slope. Hence, while the presented findings are based on the measurements, a reduced drain current would indicate better results for output power and efficiency than presented.
In case it is not possible to improve the direct drain current measurement, an indirect measurement targeting the determination of the losses might be applicable. For this, a calorimetric inverter test might be reasonable to determining the efficiency.

Further developments:
In this work, a prototype module with the active snubber setup was designed. The design was also related to be comparable to a similar DC-snubber setup and a conventional halfbridge setup. While the active snubber module was designed to obtain a deliberately large stray inductance to the main DC-link capacitor, it was shown in Sect. 5.3.3 that reducing this conductivity is still beneficial for the total switching losses. However, a lower stray inductance to the DC-link would also increase the turn-on losses. For a very low main stray inductance, e.g. in the range of the stray inductance provided by the DC-snubber path, the total losses further increase to higher values, cf. e.g. Fig. 5.29.

This allows to draw the conclusion that a more optimal main stray inductance value lies between the used $L_{\mathrm{main}} = 34\,\mathrm{nH}$ and the inductance provided by the DC-snubber $L_{\mathrm{snhb}} = 3\,\mathrm{nH}$.

For the used snubber assemblies, the capacitors were soldered to the aluminum oxide ceramic substrate. Dependent on the capacitor dielectric ceramics used, a mismatch in the coefficient of thermal expansion can be expected may having a significant impact on the reliability. The literature shows a lack in research in this type of material combination for this application. Future work may target determining the reliability of alternative assembly techniques.
Further, the capacitors used are usually designed for PCB mounting in a less harsh environment with lower temperature and stress. Future research may find new failure modes and methods to improve reliability.

For ease of use and to prove the concept of the active snubber presented, a linear low loss class I ceramic capacitor type was used. However, a class II capacitor with antiferroelectric dielectric might be a more interesting choice in terms of device size and cost. It was mentioned that such a capacitor would show a capacitance and loss dependency on the DC-link voltage and temperature. Future work may target finding a proper design strategies for using and dimensioning such a capacitor.

In Section 5.4, the expectable inverter efficiency was estimated by calculation. The validation of the presented findings by measurements is still necessary and needs further investigation. Also the dimensioning of an inverter using an optimized MOSFET with respect to lower voltage overshoot necessitates further research.

A Mathematical derivations

A.1 Calculation of Density of States

A derivation of the calculation of density of states can be found in e.g. [30]. As the energy gap shows a temperature dependency, the gap can be calculated with

$$W_{\mathrm{g}}(\vartheta) = W_{\mathrm{g0}} - \frac{\alpha\vartheta^2}{\vartheta + \beta}, \tag{A.1}$$

where ϑ is the absolute temperature and α and β are fitting parameters.
According to [141] P. 17, for 4H-SiC the parameters are given $\alpha_{\mathrm{SiC}} = 8.2 \cdot 10^{-4}\,\mathrm{eV/K}$, $\beta_{\mathrm{SiC}} = 1.8 \cdot 10^{3}\,\mathrm{K}$ valid up to a doping concentration of $1 \cdot 10^{19}\,\mathrm{cm}^{-3}$, see [142]. For Silicon the parameters can be found in [30] with $\alpha_{\mathrm{Si}} = 4.9 \cdot 10^{-4}\,\mathrm{eV/K}$, $\beta_{\mathrm{Si}} = 665\,\mathrm{K}$.
The energy gap can be calculated with the initial energy at 0 K with $W_{\mathrm{g0Si}} = 1.17\,\mathrm{eV}$ and $W_{\mathrm{g0SiC}} = 3.29\,\mathrm{eV}$, cf. [142, 143].

The effective masses for density of states can be calculated with the values given in Table A.1 using the formulas below, cf. [30, 144], where m_0 is the electron mass.

$$\begin{aligned} m_{\mathrm{de}} &= \sqrt[3]{m_{\mathrm{e}\parallel} \cdot m_{\mathrm{e}\perp}^2} \\ m_{\mathrm{dh}} &= \sqrt[3]{m_{\mathrm{h}\parallel} \cdot m_{\mathrm{h}\perp}^2} \quad = \sqrt[2/3]{m_{\mathrm{lh}}^{3/2} + m_{\mathrm{hh}}^{3/2}} \end{aligned} \tag{A.2}$$

The results are $m_{\mathrm{de,Si}} = 0,32m_0$ and $m_{\mathrm{dh,Si}} = 0,55m_0$ for silicon and $m_{\mathrm{de,SiC}} = 0,37m_0$ and $m_{\mathrm{dh,SiC}} = 0,79m_0$ for 4H-SiC respectively.
This allows to calculate the density-of-states to

$$N_{\mathrm{C}} \equiv 2M_{\mathrm{C}} \left(\frac{2\pi m_{\mathrm{de}} k\vartheta}{h^2}\right)^{3/2}, \quad \text{and} \quad N_{\mathrm{V}} \equiv 2 \left(\frac{2\pi m_{\mathrm{dh}} k\vartheta}{h^2}\right)^{3/2}, \tag{A.3}$$

for the conduction band and for the valence band with the Boltzmann constant k.

Table A.1: Effective masses of electrons and holes

	Si	4H-SiC
M_{C}[142][141]	6	3
$m_{\mathrm{e}\parallel}$ $[1/m_0]$	0.92[144]	0.29[145]
$m_{\mathrm{e}\perp}$ $[1/m_0]$	0.19[144]	0.42[145]
$m_{\mathrm{h}\parallel}$ $[1/m_0]$		1.56[146]
$m_{\mathrm{h}\perp}$ $[1/m_0]$		0.56[146]
m_{lh} $[1/m_0]$	0.16[30]	
m_{hh} $[1/m_0]$	0.49[30]	

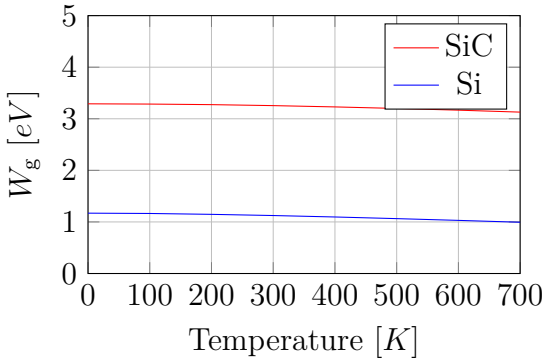


Figure A.1.1: Energy gap

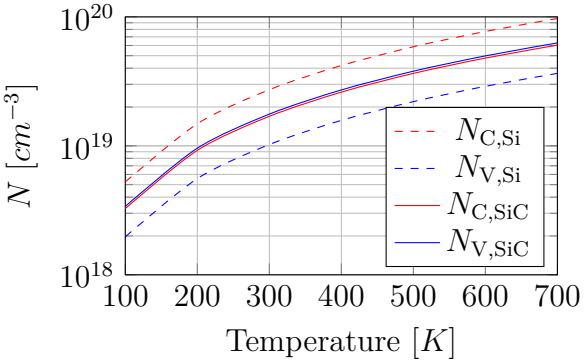


Figure A.1.2: Density of states

A.2 Equations of an RLC Circuit

In this section the well-known basic equations for the series oscillation circuit are derived to give a standard parameter definition and as a reference in subsequent sections. With the

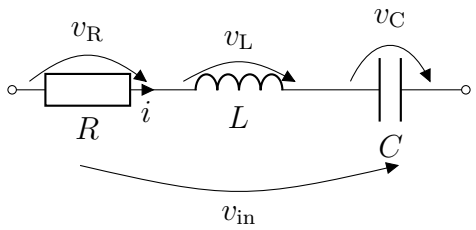


Figure A.2.1: Basic RLC circuit

general linear differential equations for L and C and the dot notation for time derivatives the complete mesh equation for a series resonant circuit according Fig. A.2.1 can be written as

$$v_{in} = v_R + v_L + v_C = R \cdot i + L \cdot \dot{i} + \frac{1}{C} \int i \, dt + V_{C0}, \tag{A.4}$$

where V_{C0} is the initial capacitor voltage.
With the simplification $v_{in0} = v_{in} - V_{C0}$ follows

$$v_{in0} = R \cdot i + L \cdot \dot{i} + \frac{1}{C} \int i \, dt. \tag{A.5}$$

After derivation of (A.5) assuming a time invariant v_{in} the homogeneous differential equation results as

$$0 = L \cdot \ddot{i} + R \cdot \dot{i} + \frac{1}{C} \cdot i. \tag{A.6}$$

With the two characteristic values of a resonant circuit

$$\delta = \frac{R}{2L} \quad \text{and} \quad \omega_0^2 = \frac{1}{LC} \tag{A.7}$$

(A.6) can be rearranged to

$$0 = \ddot{i} + 2\delta \cdot \dot{i} + \omega_0^2 \cdot i. \tag{A.8}$$

The general solution of the linear homogeneous differential equation can be obtained with the exponential approach $i = Ke^{\lambda t}$. Applying on (A.8) lead to

$$\begin{aligned} 0 &= K\lambda^2 e^{\lambda t} + 2\delta \cdot K\lambda e^{\lambda t} + \omega_0^2 \cdot Ke^{\lambda t} \\ &= \lambda^2 + 2\delta \cdot \lambda + \omega_0^2, \end{aligned} \tag{A.9}$$

where λ can be calculated with

$$\lambda_{1,2} = -\delta \pm \sqrt{\omega_\mathrm{d}^2}, \tag{A.10}$$

while

$$\omega_\mathrm{d}^2 = \delta^2 - \omega_0^2. \tag{A.11}$$

Considering (A.11), the solution of (A.9) depends on the relation between δ and ω.

For $\delta \geq \omega$: The damping dominates the circuit behavior. From (A.7) the resistor value can be derived to

$$R_{dDominant} \geq 2\sqrt{\frac{L}{C}}. \tag{A.12}$$

In case both sides of (A.12) are equal, aperiodic behavior is achieved.

For $\delta < \omega$: The behavior is a damped oscillation. With

$$R_d < 2\sqrt{\frac{L}{C}}, \tag{A.13}$$

the damping relevant resistor can be calculated.
With the circular frequency $\omega_\mathrm{d} = j\sqrt{\omega_0^2 - \delta^2}$, (A.10) results in

$$\lambda_{1,2} = -\delta \pm j\omega_\mathrm{d}. \tag{A.14}$$

Inserting (A.14) into the exponential approach $i = Ke^{\lambda t}$ leads to the general solution

$$\begin{aligned} i &= \underline{K} \cdot e^{(-\delta \pm j\omega_\mathrm{d})t} \\ &= \underline{K} \cdot e^{-\delta t} e^{\pm j\omega_\mathrm{d} t} \\ &= K_1 \cdot e^{-\delta t}\cos(\omega_\mathrm{d} t) + K_2 \cdot e^{-\delta t}\sin(\omega_\mathrm{d} t) \end{aligned} \tag{A.15}$$

with a generic complex constant $\underline{K}$ or the real constants K_1 and K_2 respectively.

For further calculations the integral is given as

$$\int i \,\mathrm{d}t = \frac{e^{-\delta t}}{\omega_0^2}\left(\sin(\omega_\mathrm{d} t)(K_1\omega_\mathrm{d} - \delta K_2) - \cos(\omega_\mathrm{d} t)(K_1\delta + \omega_\mathrm{d} K_2)\right), \tag{A.16}$$

with $\omega_0^2 = \delta^2 + \omega_d^2$ and the derivatives

$$\dot{i} = e^{-\delta t}\left(\cos(\omega_\mathrm{d} t)(K_2\omega_\mathrm{d} - \delta K_1) - \sin(\omega_\mathrm{d} t)(K_2\delta + \omega_\mathrm{d} K_1)\right) \quad \text{and} \tag{A.17}$$

$$\ddot{i} = e^{-\delta t}\left(\cos(\omega_\mathrm{d} t)(K_1(\delta^2 - \omega_\mathrm{d}^2) + 2\delta\omega_\mathrm{d} K_2) + \sin(\omega_\mathrm{d} t)(K_2(\delta^2 - \omega_\mathrm{d}^2) + 2\delta\omega_\mathrm{d} K_1)\right). \tag{A.18}$$

A.3 Analytical Derivation of Active Snubber Turn-On

This section gives a comprehensive derivation including important considerations and steps in between for the active snubber turn-on event.

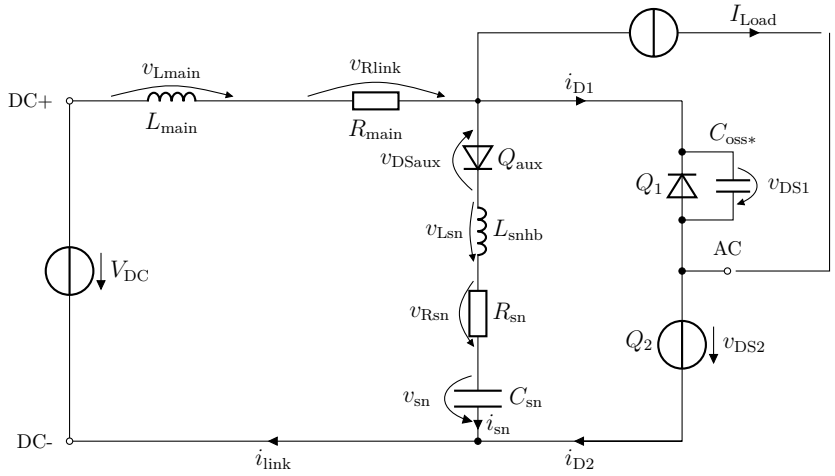


Figure A.3.1: Active snubber turn-on equivalent circuit

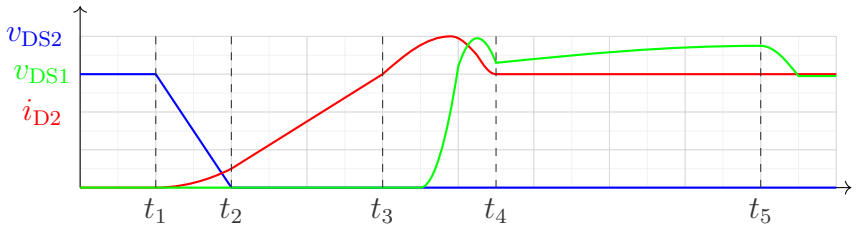


Figure A.3.2: Active snubber turn-on current and time intervals

A.3.1 Fundamental Equations

Definition of non-continuous equations:

$$R_{\text{main}} = \begin{cases} R_{\text{mainSkin}} & : t_1 \leq t \leq t_4 \\ 0 & : otherwise \end{cases} \tag{A.19}$$

$$v_{\text{DS2}} = \begin{cases} V_{\text{DC}} & : -\infty < t \leq t_1 \\ V_{\text{DC}} - \frac{V_{\text{DC}}}{t_2 - t_1} \cdot (t - t_1) & : t_1 < t \leq t_2 \\ 0 & : otherwise \end{cases} \tag{A.20}$$

Basic node-equations:

$$i_{\text{link}} = i_{\text{sn}} + i_{\text{D2}} \tag{A.21}$$

$$i_{\text{D2}} = i_{\text{D1}} + I_{\text{Load}} \tag{A.22}$$

Initial state for $t < t_1$

$$i_{\text{link}}(0) = i_{\text{D2}} = 0\,\text{A} \tag{A.23}$$

$$i_{\text{D1}}(0) = -I_{\text{Load}} \tag{A.24}$$

A.3.2 Solution for the First Interval

Interval: $t_1 \leq t < t_2$
Due to the high voltage slope of the turning on Q_2, the body diode of the turned off Q_{aux} gets into blocking state. Thus, the snubber path can be neglected and the equations for the first interval can be written as follows. By considering that the DC value of R_{main} for $t < t_1$ is neglected, see (A.19), the basic equation of the voltage loop is given with

$$V_{\text{DC}} = L_{\text{main}} \dot{i}_{\text{link}} + i_{\text{link}} R_{\text{main}} + v_{\text{DS2}}(t). \tag{A.25}$$

With (A.20), (A.25) can be rearranged to the inhomogeneous linear differential equation and its derivation as

$$\frac{V_{\text{DC}}}{L_{\text{main}} t_{\text{f12}}} t = \dot{i}_{\text{link}} + \frac{R_{\text{main}}}{L_{\text{main}}} i_{\text{link}}, \tag{A.26}$$

$$\frac{V_{\text{DC}}}{L_{\text{main}} t_{\text{f12}}} = \ddot{i}_{\text{link}} + \frac{R_{\text{main}}}{L_{\text{main}}} \dot{i}_{\text{link}}, \tag{A.27}$$

where $t_{\text{f12}} = t_2 - t_1$ is the fall time of the drain-source voltage of Q_2.

Approach:
The general solution of the homogeneous part in (A.26) as

$$0 = \dot{i}_{\text{link}} + \frac{R_{\text{main}}}{L_{\text{main}}} i_{\text{link}} \tag{A.28}$$

can be obtained using the exponential approach as

$$i_{\text{link}} = K_{\text{1I1}} e^{-\frac{R_{\text{main}}}{L_{\text{main}}} t}. \tag{A.29}$$

This allows to write the initial value problem of the inhomogeneous equation and its derivations as

$$i_{\text{link}} = K_{\text{1I1}} e^{-2\delta t} + K_{\text{p2I1}} t + K_{\text{p1I1}}, \tag{A.30}$$

$$\dot{i}_{\text{link}} = -2\delta K_{\text{1I1}} e^{-2\delta t} + K_{\text{p2I1}}, \tag{A.31}$$

$$\ddot{i}_{\text{link}} = 4\delta^2 K_{\text{1I1}} e^{-2\delta t} \tag{A.32}$$

where

$$2\delta = \frac{R_{\text{main}}}{L_{\text{main}}}. \tag{A.33}$$

At $t_1 = 0$ and the initial condition according (A.23) this leads with (A.27) to

$$i_{\text{link}}(0) = K_{\text{1I1}} + K_{\text{p1I1}} = 0, \tag{A.34}$$

$$\dot{i}_{\text{link}}(0) = -2\delta K_{\text{1I1}} + K_{\text{p2I1}} = 0 \quad \text{and} \tag{A.35}$$

$$\ddot{i}_{\text{link}}(0) = 4\delta^2 K_{\text{1I1}} = \frac{V_{\text{DC}}}{t_{\text{f12}} L_{\text{main}}}. \tag{A.36}$$

Solving the system of equation leads to the results

$$K_{\text{1I1}} = \frac{V_{\text{DC}} L_{\text{main}}}{R_{\text{main}}^2 t_{\text{f12}}}, \tag{A.37}$$

$$K_{\text{p1I1}} = -\frac{V_{\text{DC}} L_{\text{main}}}{R_{\text{main}}^2 t_{\text{f12}}} \quad \text{and} \tag{A.38}$$

$$K_{\text{p2I1}} = \frac{V_{\text{DC}}}{R_{\text{main}} t_{\text{f12}}}. \tag{A.39}$$

This allows to write the final solution for the DC-link current in the first interval by inserting K_{1I1}, K_{p1I1} and K_{p2I1} into (A.30) leading to

$$i_{\mathrm{link}}(t) = \frac{V_{\mathrm{DC}}}{R_{\mathrm{main}} t_{\mathrm{f12}}} \left[\frac{1}{2\delta} \left(e^{-2\delta t} - 1 \right) + t \right], \tag{A.40}$$

and its derivation

$$\dot{i}_{\mathrm{link}}(t) = \frac{V_{\mathrm{DC}}}{R_{\mathrm{main}} t_{\mathrm{f12}}} \left(1 - e^{-2\delta t} \right). \tag{A.41}$$

A.3.3 Solution for the Second Interval

Interval: $t_2 \leq t < t_3$
With the constraint that v_{DS2} is zero before i_{D2} reaches the load current value

$$v_{\mathrm{DS2}}(t_2) = 0\,\mathrm{V}, \tag{A.42}$$

there is a second interval in which the total DC-link voltage is across the main stray inductance. Thus, the perturbation is decayed and (A.25) can be rewritten as

$$V_{\mathrm{DC}} = L_{\mathrm{main}} \frac{\mathrm{d}i_{\mathrm{link}}}{\mathrm{d}t} + R_{\mathrm{main}} i_{\mathrm{link}}. \tag{A.43}$$

Approach:
With the identical homogeneous part according (A.28), the initial value problem of the approach to solve the inhomogeneous equation can be written as

$$i_{\mathrm{link}} = K_{1I2} e^{-2\delta t} + K_{p1I2}, \tag{A.44}$$

$$\dot{i}_{\mathrm{link}} = -2\delta K_{1I2} e^{-2\delta t}, \tag{A.45}$$

with the initial values for $t = t_2$ according to (A.40) and (A.41) as

$$i_{\mathrm{link}}(t_2) = \frac{V_{\mathrm{DC}}}{R_{\mathrm{main}} t_{\mathrm{f12}}} \left[\frac{1}{2\delta} \left(e^{-2\delta t_2} - 1 \right) + t_2 \right], \tag{A.46}$$

$$\dot{i}_{\mathrm{link}}(t_2) = \frac{V_{\mathrm{DC}}}{R_{\mathrm{main}} t_{\mathrm{f12}}} \left(1 - e^{-2\delta t_2} \right). \tag{A.47}$$

Solving the system of equations according (A.44)ff. leads to the coefficients

$$K_{1I2} = -\frac{V_{\mathrm{DC}} L_{\mathrm{main}}}{R_{\mathrm{main}}^2 t_{\mathrm{f12}}} \left(1 - e^{-2\delta t_{\mathrm{f12}}} \right) \quad \text{and} \tag{A.48}$$

$$K_{p1I2} = \frac{V_{\mathrm{DC}}}{R_{\mathrm{main}}}. \tag{A.49}$$

And finally by insertion into (A.44) and rearranging to the solution

$$i_{\mathrm{link}} = \frac{V_{\mathrm{DC}}}{R_{\mathrm{main}} t_{\mathrm{f12}}} \left[\frac{1}{2\delta} \left(e^{-2\delta t} - e^{-2\delta (t - t_{\mathrm{f12}})} \right) + t_{\mathrm{f12}} \right] \tag{A.50}$$

and its derivations

$$\dot{i}_{\mathrm{link}} = \frac{V_{\mathrm{DC}}}{R_{\mathrm{main}} t_{\mathrm{f12}}} \left(e^{-2\delta (t - t_{\mathrm{f12}})} - e^{-2\delta t} \right) = \frac{V_{\mathrm{DC}}}{R_{\mathrm{main}} t_{\mathrm{f12}}} \left(1 - e^{-2\delta t_{\mathrm{f12}}} \right) e^{-2\delta (t - t_{\mathrm{f12}})} \quad \text{and} \tag{A.51}$$

$$\ddot{i}_{\mathrm{link}} = -\frac{V_{\mathrm{DC}}}{L_{\mathrm{main}} t_{\mathrm{f12}}} \left(e^{-2\delta (t - t_{\mathrm{f12}})} - e^{-2\delta t} \right). \tag{A.52}$$

Calculation of $t = t_3$
At t_3, the condition $i_{\mathrm{D2}} = i_{\mathrm{link}} = I_{\mathrm{Load}}$ occurs. Inserting $i_{\mathrm{link}} = I_{\mathrm{Load}}$ into (A.50) allows to calculate t_3 with the rearranged form

$$t_3 = -\frac{1}{2\delta} Ln\left(\frac{2\delta \frac{I_{\mathrm{Load}} R_{\mathrm{main}} t_{\mathrm{f12}}}{V_{\mathrm{DC}}} - 2\delta t_{\mathrm{f12}}}{1 - e^{+2\delta t_{\mathrm{f12}}}}\right). \tag{A.53}$$

A.3.4 Solution for the Third Interval

Interval: $t_3 \leq t < t_4$
At $t = t_3$ the current $i_{\mathrm{D2}} = i_{\mathrm{link}}$ is equal to the load current and the body diode Q_1, see Fig. A.3.1 gets into blocking-state. Thus, the capacitance $C_{\mathrm{oss}*}$ starts charging and causes a reverse recovery peak current.
The contribution of $C_{\mathrm{oss}*}$ allows to write the loop equation as

$$V_{\mathrm{DC}} = L_{\mathrm{main}} \dot{i}_{\mathrm{link}} + R_{\mathrm{main}} i_{\mathrm{link}} + \frac{1}{C_{\mathrm{oss}*}} \int i_{\mathrm{D1}}\, \mathrm{d}t \tag{A.54}$$

and afterwards by considering (A.22) and $i_{\mathrm{D2}} = i_{\mathrm{link}}$ the rearranged equation as

$$V_{\mathrm{DC}} + \frac{I_{\mathrm{Load}}}{C_{\mathrm{oss}*}} t = L_{\mathrm{main}} \dot{i}_{\mathrm{link}} + R_{\mathrm{main}} i_{\mathrm{link}} + \frac{1}{C_{\mathrm{oss}*}} \int i_{\mathrm{link}}\, \mathrm{d}t. \tag{A.55}$$

Derivation and rearranging leads to the inhomogeneous differential equation as

$$\frac{I_{\mathrm{Load}}}{L_{\mathrm{main}} C_{\mathrm{oss}*}} = \ddot{i}_{\mathrm{link}} + 2\delta \dot{i}_{\mathrm{link}} + \omega_0^2 i_{\mathrm{link}}, \tag{A.56}$$

with the two values 2δ and ω_0^2 according to Section A.2 as

$$2\delta = \frac{R_{\mathrm{main}}}{L_{\mathrm{main}}} \quad \text{and} \tag{A.57}$$

$$\omega_0^2 = \frac{1}{L_{\mathrm{main}} C_{\mathrm{oss}*}}. \tag{A.58}$$

Approach:
With the homogeneous solution and its derivations according to (A.15)ff. the approach and its derivations can be written as

$$i_{\mathrm{link}} = e^{-\delta t}\left[K_{1\mathrm{I3}} \cos(\omega_{\mathrm{d}} t) + K_{2\mathrm{I3}} \sin(\omega_{\mathrm{d}} t)\right] + K_{\mathrm{p1I3}}, \tag{A.59}$$

$$\dot{i}_{\mathrm{link}} = e^{-\delta t}\left[\cos(\omega_d t)(K_{2\mathrm{I3}}\omega_d - \delta K_{1\mathrm{I3}}) - \sin(\omega_d t)(K_{2\mathrm{I3}}\delta + \omega_d K_{1\mathrm{I3}})\right] \quad \text{and} \tag{A.60}$$

$$\ddot{i}_{\mathrm{link}} = e^{-\delta t}\left[\cos(\omega_d t)(K_{1\mathrm{I3}}(\delta^2 - \omega_d^2) + 2\delta\omega_d K_{2\mathrm{I3}}) + \sin(\omega_d t)(K_{2\mathrm{I3}}(\delta^2 - \omega_d^2) + 2\delta\omega_d K_{1\mathrm{I3}})\right]. \tag{A.61}$$

Here ω_{d} can be obtained with (A.57) and (A.58) considering (A.11).

The initial condition $i_{\mathrm{D2}} = i_{\mathrm{link}} = I_{\mathrm{Load}}$ may occur with various preconditions e.g. by slow switching speed or by adequately low load currents. With the intention to switch fast, meaning that in the second interval the total DC-link voltage is across the main

stray inductance, the initial state is given with (A.53) inserted into (A.50)ff. leading to the set of equations as follows

$$i_{\text{link}}(t_3) = K_{1\text{I}3} + K_{\text{p1I}3} = I_{\text{Load}}, \tag{A.62}$$

$$\dot{i_{\text{link}}}(t_3) = K_{2\text{I}3}\omega_d - \delta K_{1\text{I}3} = \frac{V_{\text{DC}}}{R_{\text{main}} t_{\text{f12}}} \left(e^{-2\delta(t_3 - t_{\text{f12}})} - e^{-2\delta t_3}\right), \tag{A.63}$$

$$\ddot{i_{\text{link}}}(t_3) = K_{1\text{I}3}(\delta^2 - \omega_d^2) + 2\delta\omega_d K_{2\text{I}3} = -\frac{V_{\text{DC}}}{L_{\text{main}} t_{\text{f12}}} \left(e^{-2\delta(t_3 - t_{\text{f12}})} - e^{-2\delta t_3}\right). \tag{A.64}$$

Solving this set results in the coefficients

$$K_{1\text{I}3} = 0, \tag{A.65}$$

$$K_{2\text{I}3} = \frac{V_{\text{DC}}}{\omega_{\text{d}} R_{\text{main}} t_{\text{f12}}} \left(e^{-2\delta(t_3 - t_{\text{f12}})} - e^{-2\delta t_3}\right) \quad \text{and} \tag{A.66}$$

$$K_{\text{p1I}3} = I_{\text{Load}}. \tag{A.67}$$

Thus, the final solution for the current in this interval can be obtained as

$$i_{\text{link}} = \frac{V_{\text{DC}}}{\omega_{\text{d}} R_{\text{main}} t_{\text{f12}}} \left(e^{-2\delta(t_3 - t_{\text{f12}})} - e^{-2\delta t_3}\right) e^{-\delta(t - t_3)} \sin(\omega_{\text{d}}(t - t_3)) + I_{\text{Load}} \tag{A.68}$$

and its derivation as

$$\dot{i_{\text{link}}} = \frac{V_{\text{DC}}}{\omega_{\text{d}} R_{\text{main}} t_{\text{f12}}} \left(e^{-2\delta(t_3 - t_{\text{f12}})} - e^{-2\delta t_3}\right) e^{-\delta(t - t_3)} \left(-\delta \sin(\omega_{\text{d}}(t - t_3)) + \omega_{\text{d}} \cos(\omega_{\text{d}}(t - t_3))\right). \tag{A.69}$$

Until the end of this interval $t = t_4$, the body diode of Q_{aux} - assumed to be ideal - was in blocking state and no current was flowing through the snubber path and therefore, the initial condition for this interval is

$$i_{\text{sn}}(t_4) = 0\,\text{A} \quad \text{and} \quad \dot{i_{\text{sn}}}(t_4) = 0\,\text{A/s}^2. \tag{A.70}$$

Thus, the voltages v_{Lsn} and v_{Rsn}, cf. Fig. A.3.1 are zero also. This allows to write the condition at which the body diode of Q_{aux} becomes conductive during the negative current slope of the reverse recovery current as

$$V_{\text{DC}} - L_{\text{main}} \dot{i_{\text{link}}}(t_4) - R_{\text{main}} i_{\text{link}} = v_{\text{sn}}. \tag{A.71}$$

Rearranging and insertion of (A.68) and (A.69) into (A.71) and considering (A.57) leads to

$$\dot{i_{\text{link}}}(t_4) = \frac{V_{\text{DC}} - V_{\text{sn0}}}{L_{\text{main}}} - \frac{R_{\text{main}}}{L_{\text{main}}} i_{\text{link}} \tag{A.72}$$

and finally to

$$\begin{aligned} &A e^{-\delta(t_4 - t_3)} \left(-\delta \sin(\omega_{\text{d}}(t_4 - t_3)) + \omega_{\text{d}} \cos(\omega_{\text{d}}(t_4 - t_3))\right) \\ &= \frac{V_{\text{DC}} - V_{\text{sn0}}}{L_{\text{main}}} - 2\delta A e^{-\delta(t_4 - t_3)} \sin(\omega_{\text{d}}(t_4 - t_3)) - 2\delta I_{\text{Load}}, \end{aligned} \tag{A.73}$$

where A is the constant coefficient

$$A = \frac{V_{\text{DC}}}{\omega_{\text{d}} R_{\text{main}} t_{\text{f12}}} \left(e^{-2\delta(t_3 - t_{\text{f12}})} - e^{-2\delta t_3}\right). \tag{A.74}$$

With a snubber capacitor C_{sn} designed to be large, $\omega_{\mathrm{d}} \cdot (t_4 - t_3) \approx 0$ resulting in negligible sinus-therms leading to

$$\frac{V_{\mathrm{DC}} - V_{\mathrm{sn0}}}{L_{\mathrm{main}}} - 2\delta I_{\mathrm{Load}} \approx \omega_{\mathrm{d}} A e^{-\delta(t_4 - t_3)} \cos(\omega_{\mathrm{d}}(t_4 - t_3)). \tag{A.75}$$

Finally, this equation can be rearranged to t_4 to obtain the point in time at which the body diode becomes conductive and this intervals ends to

$$t_4 \approx \frac{1}{\omega_{\mathrm{d}}} \arccos\left(\frac{2\delta t_{\mathrm{f12}} \left(V_{\mathrm{DC}} - V_{\mathrm{sn0}} - R_{\mathrm{main}} I_{\mathrm{Load}}\right)}{V_{\mathrm{DC}} \left(e^{-2\delta(t_3 - t_{\mathrm{f12}})} - e^{-2\delta t_3}\right)}\right) + t_3. \tag{A.76}$$

A.3.5 Solution for the Fourth Interval

Interval: $t_4 \leq t < t_5$
In this interval, the switching of the semiconductors Q_1 and Q_2 is finished and the body diode of Q_{aux} is conductive. As a result, the equivalent circuit according Figure A.3.1 can be simplified to Fig. A.3.3 with the following fundamental mesh and knot equations

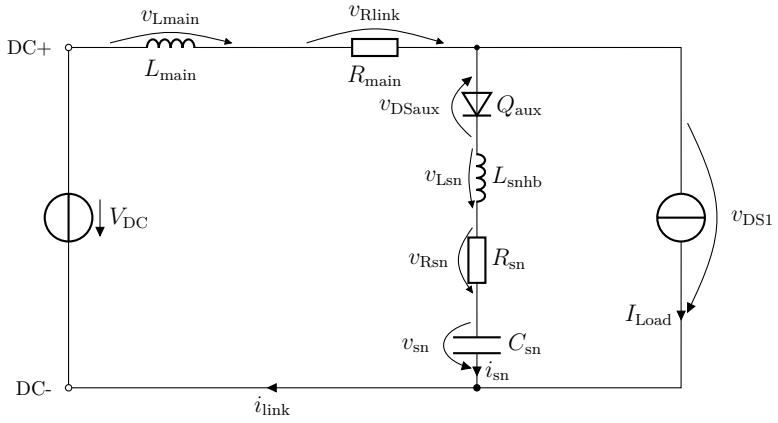


Figure A.3.3: Active snubber turn-on equivalent circuit for the last interval

$$i_{\mathrm{link}} = i_{\mathrm{sn}} + I_{\mathrm{Load}} \tag{A.77}$$

and

$$V_{\mathrm{DC}} = L_{\mathrm{main}} \cdot \dot{i}_{\mathrm{link}} + R_{\mathrm{main}} \cdot i_{\mathrm{link}} + R_{\mathrm{sn}} \cdot i_{\mathrm{sn}} + L_{\mathrm{snhb}} \cdot \dot{i}_{\mathrm{sn}} + \frac{1}{C_{\mathrm{sn}}} \int i_{\mathrm{sn}} \,\mathrm{d}t + V_{\mathrm{sn0}}. \tag{A.78}$$

Inserting (A.77) into (A.78) and rearranging leads to the equation

$$V_{\mathrm{DC}} - V_{\mathrm{sn0}} + R_{\mathrm{sn}} I_{\mathrm{Load}} + \frac{1}{C_{\mathrm{sn}}} I_{\mathrm{Load}} t = L \dot{i}_{\mathrm{link}} + R i_{\mathrm{link}} + \frac{1}{C_{\mathrm{sn}}} \int i_{\mathrm{link}} \,\mathrm{d}t, \tag{A.79}$$

where $L = L_{\mathrm{main}} + L_{\mathrm{snhb}}$ and $R = R_{\mathrm{main}} + R_{\mathrm{sn}}$. The inhomogeneous differential equation can be obtained by dividing through L and derivation resulting in

$$\omega_{045}^2 I_{\mathrm{Load}} = \ddot{i}_{\mathrm{link}} + 2\delta_{45} \dot{i}_{\mathrm{link}} + \omega_{045}^2 i_{\mathrm{link}} \tag{A.80}$$

where

$$2\delta_{45} = \frac{R}{L} \quad \text{and} \quad \omega_{045}^2 = \frac{1}{L C_{\mathrm{sn}}}. \tag{A.81}$$

The homogeneous solution according (A.15) and the constant perturbation function in (A.80) leads to the special solution for the DC-link current as

$$i_{\text{link}} = e^{-\delta(t-t_4)} \left[K_{1\text{I}4} \cos(\omega_{\text{d}}(t-t_4)) + K_{2\text{I}4} \sin(\omega_{\text{d}}(t-t_4))\right] + K_{\text{pI}4}. \tag{A.82}$$

The unknown constants $K_{1\text{I}4}, K_{2\text{I}4}$ and $K_{\text{pI}4}$ can be obtained for $t = t_4$ with the following equations. With (A.68) and (A.76) as well as (A.82) follows

$$i_{\text{link}}(t_4) = K_{1\text{I}4} + K_{\text{pI}4}. \tag{A.83}$$

(A.79) rearranged to $\dot{i_{\text{link}}}$ leads to

$$\dot{i_{\text{link}}} = \frac{V_{\text{DC}} - V_{\text{sn0}}}{L} - \frac{R_{\text{sn}}}{L} I_{\text{Load}} + \omega_0^2 I_{\text{Load}}(t-t_4) - 2\delta i_{\text{link}}(t_4) - \omega_0^2 \int i_{\text{link}} \,\mathrm{d}t. \tag{A.84}$$

Subsequently, with (A.82) and considering that the capacitor has still the same amount of charge for $t = t_4$ (A.84) can be simplified to

$$\begin{aligned} \dot{i_{\text{link}}} &= \frac{V_{\text{DC}} - V_{\text{sn0}}}{L} - \frac{R_{\text{sn}}}{L} I_{\text{Load}} - 2\delta i_{\text{link}}(t_4) \\ &= \omega_0^2 K_{2\text{I}4} - \delta K_{1\text{I}4}. \end{aligned} \tag{A.85}$$

The second derivation can be obtained from (A.80), (A.85) and (A.79) resulting in

$$\begin{aligned} \ddot{i_{\text{link}}} &= \omega_{045}^2 I_{\text{Load}} - 2\delta_{45} \dot{i_{\text{link}}} - \omega_{045}^2 i_{\text{link}} \\ &= K_{1\text{I}4}(\delta^2 - \omega_{\text{d}}^2) - 2\delta\omega_{\text{d}} K_{2\text{I}4}. \end{aligned} \tag{A.86}$$

Solving (A.83), (A.85) and (A.86) results in the coefficients

$$K_{\text{pI}4} = I_{\text{Load}}, \tag{A.87}$$

$$K_{1\text{I}4} = i_{\text{link}}(t_3) - I_{\text{Load}} \quad \text{and} \tag{A.88}$$

$$K_{2\text{I}4} = \frac{V_{\text{DC}} - V_{\text{sn0}}}{L\omega_{\text{d}}} + \frac{R_{\text{sn}}}{L\omega_{\text{d}}} I_{\text{Load}} - \frac{\delta}{\omega_{\text{d}}}(I_{\text{Load}} + i_{\text{link}}(t_4)). \tag{A.89}$$

Finally, this allows to write the solution of the DC-link current in the last interval as

$$\begin{aligned} i_{\text{link}} = e^{-\delta(t-t_4)} &\left[(i_{\text{link}}(t_3) - I_{\text{Load}}) \cos(\omega_{\text{d}}(t-t_4)) \right. \\ &\left. + \left(\frac{V_{\text{DC}} - V_{\text{sn0}} + R_{\text{sn}} I_{\text{Load}}}{L\omega_{\text{d}}} - \frac{\delta}{\omega_{\text{d}}}(I_{\text{Load}} + i_{\text{link}}(t_4))\right) \sin(\omega_{\text{d}}(t-t_4))\right] \\ &+ I_{\text{Load}}. \end{aligned} \tag{A.90}$$

According to the definition, cf. Fig. 3.2, the end of this interval occurs when the snubber current crosses zero and hence, the snubber voltage reaches its maximum. Considering (A.77) with (A.90) the end at $t = t_5$ can be calculated for negligible damping with the alternating part as

$$\begin{aligned} 0 &= i_{\text{link}} - I_{\text{Load}} \\ &= (i_{\text{link}}(t_4) - I_{\text{Load}}) \cos(\omega_{\text{d}}(t_5 - t_4)) \\ &\quad + \left(\frac{V_{\text{DC}} - V_{\text{sn0}} + R_{\text{sn}} I_{\text{Load}}}{L\omega_{\text{d}}} - \frac{\delta}{\omega_{\text{d}}}(I_{\text{Load}} + i_{\text{link}}(t_4))\right) \sin(\omega_{\text{d}}(t_5 - t_4)). \end{aligned} \tag{A.91}$$

Rearranging to t_5 lead to

$$t_5 = \frac{1}{\omega_\mathrm{d}} \arctan\left(-\frac{(i_\mathrm{link}(t_4) - I_\mathrm{Load})\omega_\mathrm{d} L}{V_\mathrm{DC} - V_\mathrm{sn0} + R_\mathrm{sn} I_\mathrm{Load} - L\delta(i_\mathrm{link}(t_4) + I_\mathrm{Load})}\right) + t_4. \tag{A.92}$$

Finally, the change in the snubber voltage can be calculated by solving the integral

$$\begin{aligned}\Delta v_\mathrm{sn} &= \frac{1}{C_\mathrm{sn}} \int_{t_4}^{t_5} i_\mathrm{sn}\,\mathrm{d}t \\ &= L e^{-\delta(t-t_4)} \left[(i_\mathrm{link}(t_3) - I_\mathrm{Load}) \cos(\omega_\mathrm{d}(t-t_4)) \right. \\ &\quad \left. + \left(\frac{V_\mathrm{DC} - V_\mathrm{sn0} + R_\mathrm{sn} I_\mathrm{Load}}{L\omega_\mathrm{d}} - \frac{\delta}{\omega_\mathrm{d}}(I_\mathrm{Load} + i_\mathrm{link}(t_4))\right) \sin(\omega_\mathrm{d}(t-t_4))\right],\end{aligned} \tag{A.93}$$

which leads to

$$\begin{aligned}\Delta v_\mathrm{sn} =& A_1 e^{-\delta(t-t_4)} \sin(\omega_\mathrm{d}(t-t_4)) \\ &+ A_2(1 - e^{-\delta(t-t_4)} \cos(\omega_\mathrm{d}(t-t_4)))\end{aligned} \tag{A.94}$$

with the two constant parameters

$$A_1 = \frac{I_\mathrm{Load} + i_\mathrm{link}(t_3)}{\omega_\mathrm{d} C_\mathrm{sn}} - \frac{\delta}{\omega_\mathrm{d}}(V_\mathrm{DC} - V_\mathrm{sn0} + R_\mathrm{sn} I_\mathrm{Load}) - 2\omega_\mathrm{d} L I_\mathrm{Load} \quad \text{and} \tag{A.95}$$

$$A_2 = V_\mathrm{DC} - V_\mathrm{sn0} - R_\mathrm{main} I_\mathrm{Load}. \tag{A.96}$$

A.4 Analytical Derivation of Active Snubber Turn-Off

Similar to Section A.3 this section shows the derivation including important considerations and steps for the active snubber turn-off event.

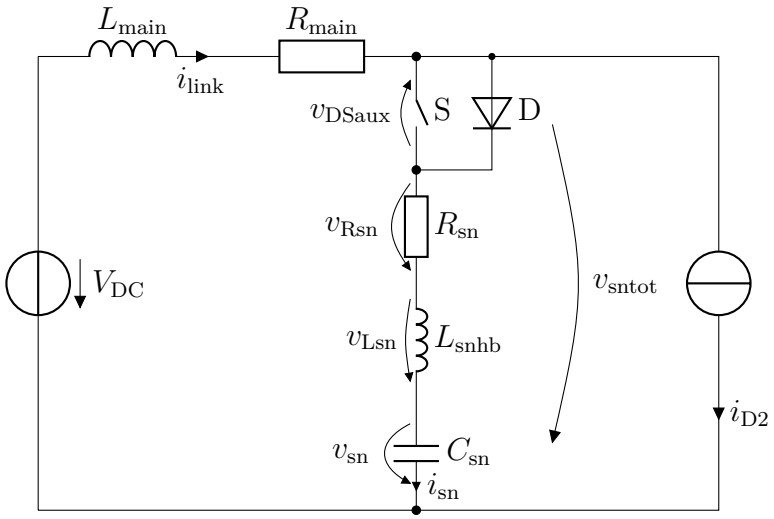


Figure A.4.1: Active snubber turn-off equivalent circuit

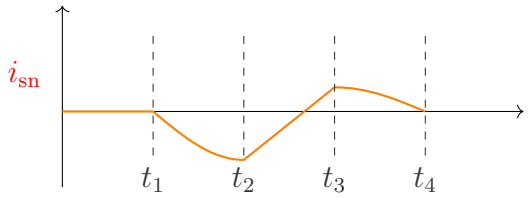


Figure A.4.2: Active snubber turn-off current and time intervals

A.4.1 Fundamental Equations

Definition of non-continuous equations:

$$R_{\text{main}} = \begin{cases} R_{\text{mainSkin}} & : t_1 \leq t \leq t_4 \\ 0 & : otherwise \end{cases} \tag{A.97}$$

$$i_{\text{D2}} = \begin{cases} I_{\text{Load}} & : -\infty < t \leq t_2 \\ I_{\text{Load}} - \frac{I_{\text{Load}}}{t_3 - t_2} \cdot (t - t_2) & : t_2 < t \leq t_3 \\ 0 & : otherwise \end{cases} \tag{A.98}$$

Basic loop and node-equations:

$$i_{\text{link}} = i_{\text{sn}} + i_{\text{D2}} \tag{A.99}$$

$$V_{\text{DC}} = L_{\text{main}} \cdot \dot{i}_{\text{link}} + R_{\text{main}} \cdot i_{\text{link}} + R_{\text{sn}} \cdot i_{\text{sn}} + L_{\text{snhb}} \cdot \dot{i}_{\text{sn}} + \frac{1}{C_{\text{sn}}} \int i_{\text{sn}} \, \mathrm{d}t + V_{\text{sn0}} \tag{A.100}$$

and rearranged for simplification to

$$\begin{aligned}\Delta v_{\mathrm{sntot}} &= V_{\mathrm{DC}} - V_{\mathrm{sn0}} \\ &= L_{\mathrm{main}} \cdot \dot{i}_{\mathrm{link}} + R_{\mathrm{main}} \cdot i_{\mathrm{link}} + R_{\mathrm{sn}} \cdot i_{\mathrm{sn}} + L_{\mathrm{sn}} \cdot \dot{i}_{\mathrm{sn}} + \frac{1}{C_{\mathrm{sn}}} \int i_{\mathrm{sn}} \,\mathrm{d}t.\end{aligned} \tag{A.101}$$

With (A.99) inserted into (A.101) follows

$$\begin{aligned}\Delta v_{\mathrm{sntot}} =& L_{\mathrm{main}} \cdot \dot{i}_{\mathrm{sn}} + L_{\mathrm{main}} \cdot \dot{i}_{\mathrm{D2}} \\ &+ R_{\mathrm{main}} \cdot i_{\mathrm{sn}} + R_{\mathrm{main}} \cdot \dot{i}_{\mathrm{D2}} \\ &+ R_{\mathrm{sn}} \cdot i_{\mathrm{sn}} + L_{\mathrm{sn}} \cdot \dot{i}_{\mathrm{sn}} + \frac{1}{C_{\mathrm{sn}}} \int i_{\mathrm{sn}} \,\mathrm{d}t.\end{aligned} \tag{A.102}$$

Further simplification with the definitions

$$L = L_{\mathrm{main}} + L_{\mathrm{sn}} \quad \text{and} \quad R = R_{\mathrm{main}} + R_{\mathrm{sn}} \tag{A.103}$$

results in

$$\Delta v_{\mathrm{sntot}} = L \cdot \dot{i}_{\mathrm{sn}} + L_{\mathrm{main}} \cdot \dot{i}_{\mathrm{D2}} + R \cdot i_{\mathrm{sn}} + R_{\mathrm{main}} \cdot i_{\mathrm{D2}} + \frac{1}{C_{\mathrm{sn}}} \int i_{\mathrm{sn}} \,\mathrm{d}t. \tag{A.104}$$

The derivative leads to the in-homogeneous differential equation

$$\begin{aligned}0 =& L \cdot \ddot{i}_{\mathrm{sn}} + L_{\mathrm{main}} \cdot \ddot{i}_{\mathrm{D2}} + R \cdot \dot{i}_{\mathrm{sn}} + R_{\mathrm{main}} \cdot \dot{i}_{\mathrm{D2}} + \frac{i_{\mathrm{sn}}}{C_{\mathrm{sn}}} \\ 0 =& \ddot{i}_{\mathrm{sn}} + \frac{R}{L} \cdot \dot{i}_{\mathrm{sn}} + \frac{i_{\mathrm{sn}}}{LC_{\mathrm{sn}}} \qquad \text{homogeneous} \\ &+ \frac{L_{\mathrm{main}}}{L} \cdot \ddot{i}_{\mathrm{D2}} + \frac{R_{\mathrm{main}}}{L} \cdot \dot{i}_{\mathrm{D2}} \qquad \text{perturbation.}\end{aligned} \tag{A.105}$$

With the definitions of (A.7), the homogeneous equation can be solved similarly to (A.8) as described in Section A.2. With the corresponding definitions

$$\delta = \frac{R}{2L}, \tag{A.106}$$

$$\omega_0^2 = \frac{1}{LC_{\mathrm{sn}}} \quad \text{and} \tag{A.107}$$

$$\omega_{\mathrm{d}}^2 = \delta^2 - \omega_0^2, \tag{A.108}$$

(A.15) can be written as the general solution with its derivatives and integral:

$$i_{\mathrm{sn}} = K_1 \cdot e^{-\delta t} \cos(\omega_{\mathrm{d}} t) + K_2 \cdot e^{-\delta t} \sin(\omega_{\mathrm{d}} t) \tag{A.109}$$

$$\dot{i}_{\mathrm{sn}} = -e^{-\delta t}(\cos(\omega_{\mathrm{d}} t)(\delta K_1 - K_2 \omega_{\mathrm{d}}) + \sin(\omega_{\mathrm{d}} t)(K_2 \delta + \omega_{\mathrm{d}} K_1)) \tag{A.110}$$

$$\begin{aligned}\ddot{i}_{\mathrm{sn}} =& e^{-\delta t}(\cos(\omega_{\mathrm{d}} t)(K_1(\delta^2 - \omega_{\mathrm{d}}^2) - 2\delta\omega_{\mathrm{d}} K_2) \\ &+ \sin(\omega_{\mathrm{d}} t)(K_2(\delta^2 - \omega_{\mathrm{d}}^2) + 2\delta\omega_{\mathrm{d}} K_1))\end{aligned} \tag{A.111}$$

$$\int i_{\mathrm{sn}} \,\mathrm{d}t = \frac{e^{-\delta t}}{\omega_0^2}(\sin(\omega_{\mathrm{d}} t)(K_1 \omega_{\mathrm{d}} - \delta K_2) - \cos(\omega_{\mathrm{d}} t)(K_1 \delta + \omega_{\mathrm{d}} K_2)). \tag{A.112}$$

A.4.2 Solution for the First Interval

Interval: $t_1 \leq t < t_2$
Due to $\dot{i_{\mathrm{D2}}}(t_1) = \ddot{i_{\mathrm{D2}}}(t_1) = 0$ only the homogeneous part of (A.105) remains and the special solution of (A.109) as the solution for this interval can be obtained with the following initial conditions:

$$i_{\mathrm{D2}}(t_1) = I_{\mathrm{Load}}, \tag{A.113}$$

$$i_{\mathrm{sn}}(t_1) = 0 \quad \text{and} \tag{A.114}$$

$$\int i_{\mathrm{sn}}(t_1)\,\mathrm{d}t = 0. \tag{A.115}$$

Approach:
With $t = t_1 = 0$ the constant K_1 for the first interval defined as $K_{1\mathrm{I}1}$ can be obtained from (A.109)

$$K_{1\mathrm{I}1} = 0 \tag{A.116}$$

Furthermore, with the given initial conditions above, (A.104) simplifies to

$$\Delta V_{\mathrm{Csn0}} = L \cdot \dot{i_{\mathrm{sn}}} + R \cdot i_{\mathrm{sn}} + R_{\mathrm{main}} \cdot I_{\mathrm{Load}}, \tag{A.117}$$

which can be further simplified considering (A.106) to

$$\frac{\Delta V_{\mathrm{Csn0}} - R_{\mathrm{main}} I_{\mathrm{Load}}}{L} = \dot{i_{\mathrm{sn}}} + 2\delta i_{\mathrm{sn}} \tag{A.118}$$

By inserting (A.109) and (A.110) the following relation can be obtained

$$\begin{aligned}\frac{\Delta V_{\mathrm{Csn0}} - R_{\mathrm{main}} I_{\mathrm{Load}}}{L} = &- e^{-\delta t}(\cos(\omega_{\mathrm{d}} t)(\delta K_{1\mathrm{I}1} - K_{2\mathrm{I}1}\omega_{\mathrm{d}}) + \sin(\omega_{\mathrm{d}} t)(K_{2\mathrm{I}1}\delta + \omega_{\mathrm{d}} K_{1\mathrm{I}1})) \\ &+ 2\delta K_{1\mathrm{I}1} \cdot e^{-\delta t}\cos(\omega_{\mathrm{d}} t) + 2\delta K_{2\mathrm{I}1} \cdot e^{-\delta t}\sin(\omega_{\mathrm{d}} t).\end{aligned} \tag{A.119}$$

With $t = t_1 = 0$ this simplifies to

$$\frac{\Delta V_{\mathrm{Csn0}} - R_{\mathrm{main}} I_{\mathrm{Load}}}{L} = K_{2\mathrm{I}1}\omega_{\mathrm{d}} - \delta K_{1\mathrm{I}1} + 2\delta K_{1\mathrm{I}1} = \delta K_{1\mathrm{I}1} + K_{2\mathrm{I}1}\omega_{\mathrm{d}}. \tag{A.120}$$

And finally, with respect to (A.116) the constant $K_{2\mathrm{I}1}$ can be calculated as

$$K_{2\mathrm{I}1}\omega_{\mathrm{d}} = \frac{\Delta V_{\mathrm{Csn0}} - R_{\mathrm{main}} I_{\mathrm{Load}}}{L} \quad \text{or} \tag{A.121}$$

$$K_{2\mathrm{I}1} = \frac{A_0}{\omega_{\mathrm{d}}}. \tag{A.122}$$

With the definition

$$A_0 = \frac{\Delta V_{\mathrm{Csn0}} - R_{\mathrm{main}} I_{\mathrm{Load}}}{L} \tag{A.123}$$

the final solution for the first interval can be written

$$i_{\mathrm{sn}}(0 \leqq t < t_2) = \frac{A_0}{\omega_{\mathrm{d}}} \cdot e^{-\delta t} \cdot \sin(\omega_{\mathrm{d}} t) \tag{A.124}$$

Capacitor voltage change
With the snubber current i_{sn} known from (A.124) the change in capacitor charge can be calculated

$$\begin{aligned}\Delta Q_{\mathrm{Csn}} &= \int i_{\mathrm{sn}}\,\mathrm{d}t \\ &= -\frac{A_0}{\omega_{\mathrm{d}}\omega_0^2}e^{-\delta t}(\delta\sin(\omega_{\mathrm{d}}t)+\omega_{\mathrm{d}}\cos(\omega_{\mathrm{d}}t)),\end{aligned} \tag{A.125}$$

resulting with the definite integral as a function of time in

$$\begin{aligned}\Delta Q_{\mathrm{CsnI1}} = \int_0^{t_2} i_{\mathrm{sn}}\,\mathrm{d}t &= \left[-\frac{A_0}{\omega_{\mathrm{d}}\omega_0^2}e^{-\delta t}(\delta\sin(\omega_{\mathrm{d}}t)+\omega_{\mathrm{d}}\cos(\omega_{\mathrm{d}}t))\right]_0^{t_2} \\ &= -\frac{A_0}{\omega_{\mathrm{d}}\omega_0^2}\left[e^{-\delta t_2}(\delta\sin(\omega_{\mathrm{d}}t_2)+\omega_{\mathrm{d}}\cos(\omega_{\mathrm{d}}t_2))-\omega_{\mathrm{d}}\right].\end{aligned} \tag{A.126}$$

From (A.126) the voltage change can be calculated by dividing through C_{sn} and considering (A.107) follows

$$\Delta v_{\mathrm{Csn}}(t) = -\frac{A_0\cdot L}{\omega_{\mathrm{d}}}\left[e^{-\delta t_2}(\delta\sin(\omega_{\mathrm{d}}t_2)+\omega_{\mathrm{d}}\cos(\omega_{\mathrm{d}}t_2))-\omega_{\mathrm{d}}\right]. \tag{A.127}$$

A.4.3 Solution for the Second Interval

Interval: $t_2 \le t < t_3$
First the initial conditions are calculated. From (A.98) the conditions for the drain current are given with

$$i_{\mathrm{D2}} = I_{\mathrm{Load}} - \frac{I_{\mathrm{Load}}}{t_{\mathrm{f23}}}\cdot(t-t_2), \tag{A.128}$$

$$\dot{i_{\mathrm{D2}}} = -\frac{I_{\mathrm{Load}}}{t_{\mathrm{f23}}} \quad \text{and} \tag{A.129}$$

$$\ddot{i_{\mathrm{D2}}} = 0 \tag{A.130}$$

under consideration of the drain current fall-time of $t_{\mathrm{f23}} = t_3 - t_2$. Contrary to the first interval, the perturbation function does not disappear and with the given initial conditions, (A.105) becomes

$$\frac{R_{\mathrm{main}}}{L}\frac{I_{\mathrm{Load}}}{t_{\mathrm{f23}}} = \ddot{i_{\mathrm{sn}}} + 2\delta\cdot\dot{i_{\mathrm{sn}}} + \omega_0^2 i_{\mathrm{sn}}. \tag{A.131}$$

Here, the constant perturbation is $\frac{R_{\mathrm{main}}}{L}\frac{I_{\mathrm{Load}}}{t_{\mathrm{f23}}}$.

Inserting (A.124), (A.129) and (A.126) into (A.104) and division by L leads to the derivative

$$\begin{aligned}\dot{i_{\mathrm{sn}}}(t_2) =& A_0 + \frac{L_{\mathrm{main}}I_{\mathrm{Load}}}{Lt_{\mathrm{f23}}} - 2\frac{\delta}{\omega_{\mathrm{d}}}A_0e^{-\delta t_2}\sin(\omega_{\mathrm{d}}t_2) \\ &+ \frac{A_0\omega_0^2}{\omega_{\mathrm{d}}\omega_0^2}\left[e^{-\delta t}(\delta\sin(\omega_{\mathrm{d}}t_2)+\omega_{\mathrm{d}}\cos(\omega_{\mathrm{d}}t_2))-\omega_{\mathrm{d}}\right].\end{aligned} \tag{A.132}$$

This simplifies to

$$\dot{i_{\mathrm{sn}}}(t_2) = \frac{L_{\mathrm{main}}I_{\mathrm{Load}}}{Lt_{\mathrm{f23}}} - A_0e^{-\delta t_2}\left(\frac{\delta}{\omega_{\mathrm{d}}}\sin(\omega_{\mathrm{d}}t_2)-\cos(\omega_{\mathrm{d}}t_2)\right). \tag{A.133}$$

By inserting (A.124) and (A.133) into (A.131) the second derivative of the snubber current can be calculated

$$\begin{aligned} \ddot{i}_{\mathrm{sn}} =& \frac{R_{\mathrm{main}}}{L}\frac{I_{\mathrm{Load}}}{t_{\mathrm{f23}}} - 2\delta\frac{L_{\mathrm{main}}I_{\mathrm{Load}}}{Lt_{\mathrm{f23}}} + \frac{2\delta^2}{\omega_{\mathrm{d}}}A_0 e^{-\delta t_2}\sin(\omega_{\mathrm{d}}t_2) \\ & - 2\delta A_0 e^{-\delta t_2}\cos(\omega_{\mathrm{d}}t_2) - \frac{\omega_0^2}{\omega_{\mathrm{d}}}A_0 e^{-\delta t_2}\sin(\omega_{\mathrm{d}}t_2), \end{aligned} \tag{A.134}$$

and with the simplified solution

$$\begin{aligned} \ddot{i}_{\mathrm{sn}} =& \frac{I_{\mathrm{Load}}}{Lt_{\mathrm{f23}}}(R_{\mathrm{main}} - 2\delta L_{\mathrm{main}}) - 2\delta A_0 e^{-\delta t_2}\cos(\omega_{\mathrm{d}}t_2) \\ & + \frac{A_0}{\omega_{\mathrm{d}}}(2\delta^2 - \omega_0^2)e^{-\delta t_2}\sin(\omega_{\mathrm{d}}t_2), \end{aligned} \tag{A.135}$$

the initial conditions are complete.

Approach:
The in-homogeneous differential equation with constant perturbation and its derivatives are

$$i_{\mathrm{sn}} = K_{1\mathrm{I}2}\cdot e^{-\delta(t-t_2)}\cos(\omega_{\mathrm{d}}(t-t_2)) + K_{2\mathrm{I}2}\cdot e^{-\delta(t-t_2)}\sin(\omega_{\mathrm{d}}(t-t_2)) + K_{\mathrm{p1I}2}, \tag{A.136}$$

$$\dot{i}_{\mathrm{sn}} = -e^{-\delta(t-t_2)}(\cos(\omega_{\mathrm{d}}(t-t_2))(\delta K_{1\mathrm{I}2} - K_{2\mathrm{I}2}\omega_{\mathrm{d}}) + \sin(\omega_{\mathrm{d}}(t-t_2))(K_{2\mathrm{I}2}\delta + \omega_{\mathrm{d}}K_{1\mathrm{I}2})), \tag{A.137}$$

$$\begin{aligned} \ddot{i}_{\mathrm{sn}} =& e^{-\delta(t-t_2)}(\cos(\omega_{\mathrm{d}}(t-t_2))(K_{1\mathrm{I}2}(\delta^2 - \omega_{\mathrm{d}}^2) - 2\delta\omega_{\mathrm{d}}K_{2\mathrm{I}2}) \\ & + \sin(\omega_{\mathrm{d}}(t-t_2))(K_{2\mathrm{I}2}(\delta^2 - \omega_{\mathrm{d}}^2) + 2\delta\omega_{\mathrm{d}}K_{1\mathrm{I}2})). \end{aligned} \tag{A.138}$$

(A.136) results with $t = t_2$ in

$$i_{\mathrm{sn}}(t = t_2) = K_{1\mathrm{I}2} + K_{\mathrm{p1I}2}. \tag{A.139}$$

By inserting (A.124) into the previous equation, $K_{1\mathrm{I}2}$ is given with

$$K_{1\mathrm{I}2} = \frac{A_0}{\omega_{\mathrm{d}}}\cdot e^{-\delta t_2}\cdot\sin(\omega_{\mathrm{d}}t_2) - K_{\mathrm{p1I}2}. \tag{A.140}$$

Similarly (A.137) results with $t = t_2$ in

$$\dot{i}_{\mathrm{sn}}(t = t_2) = -\delta K_{1\mathrm{I}2} + K_{2\mathrm{I}2}\omega_{\mathrm{d}}. \tag{A.141}$$

Combination of (A.141), (A.133) and (A.140) leads to

$$\begin{aligned} K_{2\mathrm{I}2}\omega_{\mathrm{d}} =& \frac{L_{\mathrm{main}}I_{\mathrm{Load}}}{Lt_{\mathrm{f23}}} - A_0 e^{-\delta t_2}\frac{\delta}{\omega_{\mathrm{d}}}\sin(\omega_{\mathrm{d}}t_2) + A_0 e^{-\delta t_2}\cos(\omega_{\mathrm{d}}t_2) \\ & - A_0 e^{-\delta t_2}\frac{\delta}{\omega_{\mathrm{d}}}\sin(\omega_{\mathrm{d}}t_2) - \delta K_{\mathrm{p1I}2} \\ =& \frac{L_{\mathrm{main}}I_{\mathrm{Load}}}{Lt_{\mathrm{f23}}} + A_0 e^{-\delta t_2}\cos(\omega_{\mathrm{d}}t_2) - \delta K_{\mathrm{p1I}2}. \end{aligned} \tag{A.142}$$

Division by ω_{d} gives

$$K_{2\mathrm{I}2} = \frac{L_{\mathrm{main}}I_{\mathrm{Load}}}{\omega_{\mathrm{d}}Lt_{\mathrm{f23}}} + \frac{A_0}{\omega_{\mathrm{d}}}e^{-\delta t_2}\cos(\omega_{\mathrm{d}}t_2) - \frac{\delta}{\omega_{\mathrm{d}}}K_{\mathrm{p1I}2}. \tag{A.143}$$

With $t = t_2$ (A.138) simplifies to

$$\ddot{i}_{\mathrm{sn}} = K_{1\mathrm{I}2}(\delta^2 - \omega_{\mathrm{d}}^2) - 2\delta\omega_{\mathrm{d}}K_{2\mathrm{I}2}. \tag{A.144}$$

And with the results from (A.140) and (A.143) the following relation can be written

$$\begin{aligned}\ddot{i}_{\mathrm{sn}} =& \frac{\delta^2}{\omega_{\mathrm{d}}}A_0 \cdot e^{-\delta t_2} \cdot \sin(\omega_{\mathrm{d}}t_2) - \delta^2 K_{\mathrm{p1I2}} \\ &- \omega_{\mathrm{d}}A_0 \cdot e^{-\delta t_2} \cdot \sin(\omega_{\mathrm{d}}t_2) + \omega_{\mathrm{d}}^2 K_{\mathrm{p1I2}} \\ &- 2\delta\frac{L_{\mathrm{main}}I_{\mathrm{Load}}}{Lt_{\mathrm{f23}}} - 2\delta A_0 e^{-\delta t_2}\cos(\omega_{\mathrm{d}}t_2) + 2\delta^2 K_{\mathrm{p1I2}}.\end{aligned} \tag{A.145}$$

Comparing (A.134) with (A.145) and eliminating equal therms leads to

$$\begin{aligned}\frac{R_{\mathrm{main}}}{L}\frac{I_{\mathrm{Load}}}{t_{\mathrm{f23}}} + \frac{\delta^2}{\omega_{\mathrm{d}}}A_0 e^{-\delta t_2}\sin(\omega_{\mathrm{d}}t_2) - \frac{\omega_0^2}{\omega_{\mathrm{d}}}A_0 e^{-\delta t_2}\sin(\omega_{\mathrm{d}}t_2) \\ = -\omega_{\mathrm{d}}A_0 \cdot e^{-\delta t_2} \cdot \sin(\omega_{\mathrm{d}}t_2) + K_{\mathrm{p1I2}}(\delta^2 + \omega_{\mathrm{d}}^2)\end{aligned} \tag{A.146}$$

and further reduced with respect to (A.108)

$$\frac{R_{\mathrm{main}}}{L}\frac{I_{\mathrm{Load}}}{t_{\mathrm{f23}}} - \omega_{\mathrm{d}}A_0 e^{-\delta t_2}\sin(\omega_{\mathrm{d}}t_2) = -\omega_{\mathrm{d}}A_0 \cdot e^{-\delta t_2} \cdot \sin(\omega_{\mathrm{d}}t_2) + K_{\mathrm{p1I2}}\omega_0^2. \tag{A.147}$$

Subsequently, K_{p1I2} can be calculated with (A.107) by

$$K_{\mathrm{p1I2}} = \frac{R_{\mathrm{main}}}{L\omega_0^2}\frac{I_{\mathrm{Load}}}{t_{\mathrm{f23}}} = R_{\mathrm{main}}C_{\mathrm{sn}}\frac{I_{\mathrm{Load}}}{t_{\mathrm{f23}}}. \tag{A.148}$$

To get the constants $K_{1\mathrm{I}2}$ and $K_{2\mathrm{I}2}$ the previous equation is inserted into (A.140) and (A.143):

$$K_{1\mathrm{I}2} = \frac{A_0}{\omega_{\mathrm{d}}} \cdot e^{-\delta t_2} \cdot \sin(\omega_{\mathrm{d}}t_2) - R_{\mathrm{main}}C_{\mathrm{sn}}\frac{I_{\mathrm{Load}}}{t_{\mathrm{f23}}}, \tag{A.149}$$

$$K_{2\mathrm{I}2} = \frac{L_{\mathrm{main}}I_{\mathrm{Load}}}{\omega_{\mathrm{d}}Lt_{\mathrm{f23}}} + \frac{A_0}{\omega_{\mathrm{d}}}e^{-\delta t_2}\cos(\omega_{\mathrm{d}}t_2) - \frac{\delta}{\omega_{\mathrm{d}}}R_{\mathrm{main}}C_{\mathrm{sn}}\frac{I_{\mathrm{Load}}}{t_{\mathrm{f23}}}. \tag{A.150}$$

The snubber current can now be obtained by inserting (A.148)-(A.150) into the general Equation (A.136) resulting in the complex equation

$$\begin{aligned}i_{\mathrm{sn}} =& \left[\frac{A_0}{\omega_{\mathrm{d}}} \cdot e^{-\delta t_2} \cdot \sin(\omega_{\mathrm{d}}t_2) - R_{\mathrm{main}}C_{\mathrm{sn}}\frac{I_{\mathrm{Load}}}{t_{\mathrm{f23}}}\right] \cdot e^{-\delta(t-t_2)}\cos(\omega_{\mathrm{d}}(t-t_2)) \\ &+ \left[\frac{L_{\mathrm{main}}I_{\mathrm{Load}}}{\omega_{\mathrm{d}}Lt_{\mathrm{f23}}} + \frac{A_0}{\omega_{\mathrm{d}}}e^{-\delta t_2}\cos(\omega_{\mathrm{d}}t_2) - \frac{\delta}{\omega_{\mathrm{d}}}R_{\mathrm{main}}C_{\mathrm{sn}}\frac{I_{\mathrm{Load}}}{t_{\mathrm{f23}}}\right] \cdot e^{-\delta(t-t_2)}\sin(\omega_{\mathrm{d}}(t-t_2)) \\ &+ R_{\mathrm{main}}C_{\mathrm{sn}}\frac{I_{\mathrm{Load}}}{t_{\mathrm{f23}}} \\ =& \frac{A_0}{\omega_{\mathrm{d}}}e^{-\delta t}\sin(\omega_{\mathrm{d}}t_2)\cos(\omega_{\mathrm{d}}(t-t_2)) - R_{\mathrm{main}}C_{\mathrm{sn}}\frac{I_{\mathrm{Load}}}{t_{\mathrm{f23}}}e^{-\delta(t-t_2)}\cos(\omega_{\mathrm{d}}(t-t_2)) \\ &+ \frac{I_{\mathrm{Load}}}{t_{\mathrm{f23}}\omega_{\mathrm{d}}}\left(\frac{L_{\mathrm{main}}}{L} - \delta R_{\mathrm{main}}C_{\mathrm{sn}}\right) \cdot e^{-\delta(t-t_2)}\sin(\omega_{\mathrm{d}}(t-t_2)) \\ &+ \frac{A_0}{\omega_{\mathrm{d}}}e^{-\delta t}\cos(\omega_{\mathrm{d}}t_2)\sin(\omega_{\mathrm{d}}(t-t_2)) + R_{\mathrm{main}}C_{\mathrm{sn}}\frac{I_{\mathrm{Load}}}{t_{\mathrm{f23}}}.\end{aligned} \tag{A.151}$$

Using the auxiliary calculations

$$\begin{aligned}\sin(\omega_\mathrm{d}t_2)\cos(\omega_\mathrm{d}(t-t_2)) &= \sin(\omega_\mathrm{d}t_2)\left[\cos(\omega_\mathrm{d}t)\cos(\omega_\mathrm{d}t_2)+\sin(\omega_\mathrm{d}t)\sin(\omega_\mathrm{d}t_2)\right], \\ &= \sin(\omega_\mathrm{d}t_2)\cos(\omega_\mathrm{d}t)\cos(\omega_\mathrm{d}t_2)+\sin(\omega_\mathrm{d}t)\sin(\omega_\mathrm{d}t_2)^2 \\ \cos(\omega_\mathrm{d}t_2)\sin(\omega_\mathrm{d}(t-t_2)) &= \cos(\omega_\mathrm{d}t_2)\left[\sin(\omega_\mathrm{d}t)\cos(\omega_\mathrm{d}t_2)-\cos(\omega_\mathrm{d}t)\sin(\omega_\mathrm{d}t_2)\right], \\ &= \sin(\omega_\mathrm{d}t)\cos(\omega_\mathrm{d}t_2)^2-\cos(\omega_\mathrm{d}t_2)\cos(\omega_\mathrm{d}t)\sin(\omega_\mathrm{d}t_2)\end{aligned} \tag{A.152}$$

and

$$\begin{aligned}&\sin(\omega_\mathrm{d}t_2)\cos(\omega_\mathrm{d}(t-t_2))+\cos(\omega_\mathrm{d}t_2)\sin(\omega_\mathrm{d}(t-t_2)) \\ &=\sin(\omega_\mathrm{d}t)\sin(\omega_\mathrm{d}t_2)^2+\sin(\omega_\mathrm{d}t)\cos(\omega_\mathrm{d}t_2)^2 \\ &=\sin(\omega_\mathrm{d}t),\end{aligned} \tag{A.153}$$

the snubber current Equation (A.151) can be simplified to

$$\begin{aligned}i_\mathrm{sn}(t_2 \leqq t < t_3) = \frac{A_0}{\omega_\mathrm{d}}e^{-\delta t}\sin(\omega_\mathrm{d}t) + R_\mathrm{main}C_\mathrm{sn}\frac{I_\mathrm{Load}}{t_\mathrm{f23}}\left[1-e^{-\delta(t-t_2)}\cos(\omega_\mathrm{d}(t-t_2))\right] \\ + \frac{I_\mathrm{Load}}{t_\mathrm{f23}\omega_\mathrm{d}}\left(\frac{L_\mathrm{main}}{L}-\delta R_\mathrm{main}C_\mathrm{sn}\right)\cdot e^{-\delta(t-t_2)}\sin(\omega_\mathrm{d}(t-t_2)).\end{aligned} \tag{A.154}$$

Capacitor voltage change

To obtain the change of capacitor charge, (A.154) was integrated leading to

$$\begin{aligned}
\Delta Q_{\mathrm{CsnI2}} &= \int_{t_2}^{t_3} i_{\mathrm{sn}}\,\mathrm{d}t \\
&= \frac{A_0}{\omega_{\mathrm{d}}}\int_{t_2}^{t_3} e^{-\delta t}\sin(\omega_{\mathrm{d}}t)\,\mathrm{d}t + R_{\mathrm{main}}C_{\mathrm{sn}}\frac{I_{\mathrm{Load}}}{t_{\mathrm{f23}}}(t_3-t_2) \\
&\quad - R_{\mathrm{main}}C_{\mathrm{sn}}\frac{I_{\mathrm{Load}}}{t_{\mathrm{f23}}}\int_{t_2}^{t_3} e^{-\delta(t-t_2))}\cos(\omega_{\mathrm{d}}(t-t_2))\,\mathrm{d}t \\
&\quad + \frac{I_{\mathrm{Load}}}{t_{\mathrm{f23}}\omega_{\mathrm{d}}}\left(\frac{L_{\mathrm{main}}}{L} - \delta R_{\mathrm{main}}C_{\mathrm{sn}}\right)\int_{t_2}^{t_3} e^{-\delta(t-t_2))}\sin(\omega_{\mathrm{d}}(t-t_2))\,\mathrm{d}t \\
&= \frac{A_0}{\omega_{\mathrm{d}}\omega_0^2}\left[e^{-\delta t_2}(\delta\sin(\omega_{\mathrm{d}}t_2)+\omega_{\mathrm{d}}\cos(\omega_{\mathrm{d}}t_2)) - e^{-\delta t_3}(\delta\sin(\omega_{\mathrm{d}}t_3)+\omega_{\mathrm{d}}\cos(\omega_{\mathrm{d}}t_3))\right] \\
&\quad + \frac{R_{\mathrm{main}}C_{\mathrm{sn}}}{\omega_0^2}\frac{I_{\mathrm{Load}}}{t_{\mathrm{f23}}}e^{-\delta(t_3-t_2)}\left(\delta\cos(\omega_{\mathrm{d}}(t_3-t_2)) - \omega_{\mathrm{d}}\sin(\omega_{\mathrm{d}}(t_3-t_2))\right) \\
&\quad - \frac{I_{\mathrm{Load}}}{t_{\mathrm{f23}}\omega_{\mathrm{d}}\omega_0^2}\left(\frac{L_{\mathrm{main}}}{L} - \delta R_{\mathrm{main}}C_{\mathrm{sn}}\right)e^{-\delta(t_3-t_2)}\left[\delta\sin(\omega_{\mathrm{d}}(t_3-t_2)) + \omega_{\mathrm{d}}\cos(\omega_{\mathrm{d}}(t_3-t_2))\right] \\
&\quad + \frac{I_{\mathrm{Load}}}{t_{\mathrm{f23}}}\left[-\frac{\delta}{\omega_0^2}R_{\mathrm{main}}C_{\mathrm{sn}} + \frac{1}{\omega_{\mathrm{d}}\omega_0^2}\left(\frac{L_{\mathrm{main}}}{L} - \delta R_{\mathrm{main}}C_{\mathrm{sn}}\right) + R_{\mathrm{main}}C_{\mathrm{sn}}(t_3-t_2)\right].
\end{aligned} \tag{A.155}$$

The previous (A.155) is then added to (A.126) to get the change of charge at $t = t_3$ with respect to t_1 following

$$\begin{aligned}
\Delta Q_{\mathrm{CsnI1I2}} &= \Delta Q_{\mathrm{Csn}}(t=t_3) = \int_{t_1}^{t_2} i_{\mathrm{sn}}\,\mathrm{d}t + \int_{t_2}^{t_3} i_{\mathrm{sn}}\,\mathrm{d}t = \int_{t_1}^{t_3} i_{\mathrm{sn}}\,\mathrm{d}t \\
&= -\frac{A_0}{\omega_{\mathrm{d}}\omega_0^2}\left[e^{-\delta t_2}(\delta\sin(\omega_{\mathrm{d}}t_2)+\omega_{\mathrm{d}}\cos(\omega_{\mathrm{d}}t_2)) - \omega_{\mathrm{d}}\right] \\
&\quad + \frac{A_0}{\omega_{\mathrm{d}}\omega_0^2}\left[e^{-\delta t_2}(\delta\sin(\omega_{\mathrm{d}}t_2)+\omega_{\mathrm{d}}\cos(\omega_{\mathrm{d}}t_2)) - e^{-\delta t_3}(\delta\sin(\omega_{\mathrm{d}}t_3)+\omega_{\mathrm{d}}\cos(\omega_{\mathrm{d}}t_3))\right] \\
&\quad + \frac{R_{\mathrm{main}}C_{\mathrm{sn}}}{\omega_0^2}\frac{I_{\mathrm{Load}}}{t_{\mathrm{f23}}}e^{-\delta(t_3-t_2)}\left(\delta\cos(\omega_{\mathrm{d}}(t_3-t_2)) - \omega_{\mathrm{d}}\sin(\omega_{\mathrm{d}}(t_3-t_2))\right) \\
&\quad - \frac{I_{\mathrm{Load}}}{t_{\mathrm{f23}}\omega_{\mathrm{d}}\omega_0^2}\left(\frac{L_{\mathrm{main}}}{L} - \delta R_{\mathrm{main}}C_{\mathrm{sn}}\right)e^{-\delta(t_3-t_2)}\left[\delta\sin(\omega_{\mathrm{d}}(t_3-t_2)) + \omega_{\mathrm{d}}\cos(\omega_{\mathrm{d}}(t_3-t_2))\right] \\
&\quad + \frac{I_{\mathrm{Load}}}{t_{\mathrm{f23}}}\left[-\frac{\delta}{\omega_0^2}R_{\mathrm{main}}C_{\mathrm{sn}} + \frac{1}{\omega_{\mathrm{d}}\omega_0^2}\left(\frac{L_{\mathrm{main}}}{L} - \delta R_{\mathrm{main}}C_{\mathrm{sn}}\right) + R_{\mathrm{main}}C_{\mathrm{sn}}(t_3-t_2)\right],
\end{aligned} \tag{A.156}$$

which can be simplified under additional consideration of $t_{\mathrm{f23}} = t_3 - t_2$ to

$$\begin{aligned}
\Delta Q_{\mathrm{CsnI1I2}} &= \frac{A_0}{\omega_0^2}\left[1 - e^{-\delta t_3}\left(\frac{\delta}{\omega_{\mathrm{d}}}\sin(\omega_{\mathrm{d}}t_3) + \cos(\omega_{\mathrm{d}}t_3)\right)\right] + R_{\mathrm{main}}C_{\mathrm{sn}}I_{\mathrm{Load}} \\
&\quad + \frac{I_{\mathrm{Load}}}{t_{\mathrm{f23}}\omega_0^2}\left[\left(\frac{L_{\mathrm{main}}}{L} - 2\delta R_{\mathrm{main}}C_{\mathrm{sn}}\right)\left(1 - e^{-\delta t_{\mathrm{f23}}}\cos(\omega_{\mathrm{d}}t_{\mathrm{f23}})\right)\right] \\
&\quad - \frac{I_{\mathrm{Load}}}{t_{\mathrm{f23}}\omega_0^2}\left[\left(R_{\mathrm{main}}C_{\mathrm{sn}}\left(\omega_{\mathrm{d}} - \frac{\delta^2}{\omega_{\mathrm{d}}}\right) + \frac{\delta L_{\mathrm{main}}}{\omega_{\mathrm{d}}L}\right)e^{-\delta t_{\mathrm{f23}}}\sin(\omega_{\mathrm{d}}t_{\mathrm{f23}})\right].
\end{aligned} \tag{A.157}$$

By division through the snubber capacitance and with respect to (A.107), the total snubber voltage change at $t = t_3$ can be calculated with

$$\begin{aligned}\Delta V_{\mathrm{Csn}}(t = t_3) = A_0 L \left[1 - e^{-\delta t_3}\left(\frac{\delta}{\omega_\mathrm{d}}\sin(\omega_\mathrm{d} t_3) + \cos(\omega_\mathrm{d} t_3)\right)\right] + R_\mathrm{main} I_\mathrm{Load} \\ + \frac{I_\mathrm{Load}}{t_\mathrm{f23}}\left[\left(L_\mathrm{main} - \frac{2\delta}{\omega_0^2} R_\mathrm{main}\right)\left(1 - e^{-\delta t_\mathrm{f23}}\cos(\omega_\mathrm{d} t_\mathrm{f23})\right)\right] \\ - \frac{I_\mathrm{Load}}{t_\mathrm{f23}}\left[\left(\frac{R_\mathrm{main}}{\omega_0^2}\left(\omega_\mathrm{d} - \frac{\delta^2}{\omega_\mathrm{d}}\right) + \frac{\delta}{\omega_\mathrm{d}} L_\mathrm{main}\right) e^{-\delta t_\mathrm{f23}}\sin(\omega_\mathrm{d} t_\mathrm{f23})\right].\end{aligned} \tag{A.158}$$

A.4.4 Solution for the Third Interval

Interval: $t_3 \leq t < t_4$
First the already defined initial conditions for $t = t_3$ are given

$$i_\mathrm{D2}(t_3) = 0 = \dot{i_\mathrm{D2}}(t_3) = \ddot{i_\mathrm{D2}}(t_3) \tag{A.159}$$

Hence, (A.104) divided by L can be written as

$$\frac{\Delta V_\mathrm{sn0}}{L} = \dot{i_\mathrm{sn}}(t_3) + 2\delta \cdot i_\mathrm{sn}(t_3) + \omega_0^2 \int_{t_1}^{t_3} i_\mathrm{sn}\,\mathrm{d}t. \tag{A.160}$$

Further, the derivative of the snubber current can be calculated respectively

$$\dot{i_\mathrm{sn}}(t_3) = \frac{\Delta V_\mathrm{sn0}}{L} - 2\delta \cdot i_\mathrm{sn}(t_3) - \omega_0^2 \int_{t_1}^{t_3} i_\mathrm{sn}\,\mathrm{d}t. \tag{A.161}$$

Considering (A.154) and (A.157) the snubber current gradient can be calculated at $t = t_3$ to

$$\begin{aligned}\dot{i_\mathrm{sn}}(t_3) = \frac{\Delta V_\mathrm{sn0}}{L} \\ - \frac{2\delta}{\omega_\mathrm{d}} A_0 e^{-\delta t_3}\sin(\omega_\mathrm{d} t_3) - 2\delta R_\mathrm{main} C_\mathrm{sn}\frac{I_\mathrm{Load}}{t_\mathrm{f23}}\left[1 - e^{-\delta t_\mathrm{f23}}\cos(\omega_\mathrm{d} t_\mathrm{f23})\right] \\ - 2\delta\frac{I_\mathrm{Load}}{t_\mathrm{f23}\omega_\mathrm{d}}\left(\frac{L_\mathrm{main}}{L} - \delta R_\mathrm{main} C_\mathrm{sn}\right)\cdot e^{-\delta t_\mathrm{f23}}\sin(\omega_\mathrm{d} t_\mathrm{f23}) \\ - A_0\left[1 - e^{-\delta t_3}\left(\frac{\delta}{\omega_\mathrm{d}}\sin(\omega_\mathrm{d} t_3) + \cos(\omega_\mathrm{d} t_3)\right)\right] - \frac{R_\mathrm{main}}{L} I_\mathrm{Load} \\ - \frac{I_\mathrm{Load}}{t_\mathrm{f23}}\left[\left(\frac{L_\mathrm{main}}{L} - 2\delta R_\mathrm{main} C_\mathrm{sn}\right)\left(1 - e^{-\delta t_\mathrm{f23}}\cos(\omega_\mathrm{d} t_\mathrm{f23})\right)\right] \\ + \frac{I_\mathrm{Load}}{t_\mathrm{f23}}\left[\left(R_\mathrm{main} C_\mathrm{sn}\left(\omega_\mathrm{d} - \frac{\delta^2}{\omega_\mathrm{d}}\right) + \frac{\delta L_\mathrm{main}}{\omega_\mathrm{d} L}\right) e^{-\delta t_\mathrm{f23}}\sin(\omega_\mathrm{d} t_\mathrm{f23})\right].\end{aligned} \tag{A.162}$$

And simplified by eliminating double therms

$$\begin{aligned}\dot{i_\mathrm{sn}}(t_3) = A_0 e^{-\delta t_3}\left(\cos(\omega_\mathrm{d} t_3) - \frac{\delta}{\omega_\mathrm{d}}\sin(\omega_\mathrm{d} t_3)\right) - \frac{L_\mathrm{main} I_\mathrm{Load}}{L t_\mathrm{f23}} \\ + \frac{I_\mathrm{Load}}{t_\mathrm{f23}} e^{-\delta t_\mathrm{f23}}\left[\frac{L_\mathrm{main}}{L}\cos(\omega_\mathrm{d} t_\mathrm{f23}) + \left(R_\mathrm{main} C_\mathrm{sn}\left(\omega_\mathrm{d} + \frac{\delta^2}{\omega_\mathrm{d}}\right) - \frac{\delta L_\mathrm{main}}{\omega_\mathrm{d} L}\right)\sin(\omega_\mathrm{d} t_\mathrm{f23})\right],\end{aligned} \tag{A.163}$$

the approach can be made.

Approach:

$$i_{\mathrm{sn}} = K_{1\mathrm{I}3} \cdot e^{-\delta(t-t_3)} \cos(\omega_{\mathrm{d}}(t-t_3)) + K_{2\mathrm{I}3} \cdot e^{-\delta(t-t_3)} \sin(\omega_{\mathrm{d}}(t-t_3)), \tag{A.164}$$

$$\dot{i_{\mathrm{sn}}} = -e^{-\delta(t-t_3)}(\cos(\omega_{\mathrm{d}}(t-t_3))(\delta K_{1\mathrm{I}3} - K_{2\mathrm{I}3}\omega_{\mathrm{d}}) + \sin(\omega_{\mathrm{d}}(t-t_3))(K_{2\mathrm{I}3}\delta + \omega_{\mathrm{d}}K_{1\mathrm{I}3})), \tag{A.165}$$

which simplifies for the initial value problem with $t = t_3$ to

$$i_{\mathrm{sn}}(t_3) = K_{1\mathrm{I}3}, \tag{A.166}$$

$$\dot{i_{\mathrm{sn}}}(t_3) = K_{2\mathrm{I}3}\omega_{\mathrm{d}} - \delta K_{1\mathrm{I}3}. \tag{A.167}$$

$K_{1\mathrm{I}3}$ can be immediately calculated with (A.154) to

$$\begin{aligned} K_{1\mathrm{I}3} &= i_{\mathrm{sn}}(t_3) \\ &= \frac{A_0}{\omega_{\mathrm{d}}} e^{-\delta t_3} \sin(\omega_{\mathrm{d}} t_3) + R_{\mathrm{main}} C_{\mathrm{sn}} \frac{I_{\mathrm{Load}}}{t_{\mathrm{f}23}} \left[1 - e^{-\delta t_{\mathrm{f}23}} \cos(\omega_{\mathrm{d}} t_{\mathrm{f}23})\right] \\ &\quad + \frac{I_{\mathrm{Load}}}{t_{\mathrm{f}23}\omega_{\mathrm{d}}} \left(\frac{L_{\mathrm{main}}}{L} - \delta R_{\mathrm{main}} C_{\mathrm{sn}}\right) \cdot e^{-\delta t_{\mathrm{f}23}} \sin(\omega_{\mathrm{d}} t_{\mathrm{f}23}) \end{aligned} \tag{A.168}$$

and $K_{2\mathrm{I}3}$ using (A.168) and (A.163) resulting in

$$\begin{aligned} K_{2\mathrm{I}3} &= \frac{\dot{i_{\mathrm{sn}}}(t_3)}{\omega_{\mathrm{d}}} + \frac{\delta}{\omega_{\mathrm{d}}} K_{1\mathrm{I}3} \\ &= \frac{A_0}{\omega_{\mathrm{d}}} e^{-\delta t_3} \left(\cos(\omega_{\mathrm{d}} t_3) - \frac{\delta}{\omega_{\mathrm{d}}} \sin(\omega_{\mathrm{d}} t_3)\right) - \frac{L_{\mathrm{main}} I_{\mathrm{Load}}}{\omega_{\mathrm{d}} L t_{\mathrm{f}23}} \\ &\quad + \frac{I_{\mathrm{Load}}}{\omega_{\mathrm{d}} t_{\mathrm{f}23}} e^{-\delta t_{\mathrm{f}23}} \left[\frac{L_{\mathrm{main}}}{L} \cos(\omega_{\mathrm{d}} t_{\mathrm{f}23}) + \left(R_{\mathrm{main}} C_{\mathrm{sn}} \left(\omega_{\mathrm{d}} + \frac{\delta^2}{\omega_{\mathrm{d}}}\right) - \frac{\delta L_{\mathrm{main}}}{\omega_{\mathrm{d}} L}\right) \sin(\omega_{\mathrm{d}} t_{\mathrm{f}23})\right] \\ &\quad + \frac{\delta A_0}{\omega_{\mathrm{d}}^2} e^{-\delta t_3} \sin(\omega_{\mathrm{d}} t_3) + \frac{\delta R_{\mathrm{main}} C_{\mathrm{sn}}}{\omega_{\mathrm{d}}} \frac{I_{\mathrm{Load}}}{t_{\mathrm{f}23}} \left[1 - e^{-\delta t_{\mathrm{f}23}} \cos(\omega_{\mathrm{d}} t_{\mathrm{f}23})\right] \\ &\quad + \frac{\delta I_{\mathrm{Load}}}{\omega_{\mathrm{d}} t_{\mathrm{f}23}} \left(\frac{L_{\mathrm{main}}}{L} - \delta R_{\mathrm{main}} C_{\mathrm{sn}}\right) \cdot e^{-\delta t_{\mathrm{f}23}} \sin(\omega_{\mathrm{d}} t_{\mathrm{f}23}). \end{aligned} \tag{A.169}$$

With simplification this yields in

$$\begin{aligned} K_{2\mathrm{I}3} &= \frac{A_0}{\omega_{\mathrm{d}}} e^{-\delta t_3} \cos(\omega_{\mathrm{d}} t_3) - \frac{I_{\mathrm{Load}}}{\omega_{\mathrm{d}} t_{\mathrm{f}23}} \left(\frac{L_{\mathrm{main}}}{L} - \delta R_{\mathrm{main}} C_{\mathrm{sn}}\right) \\ &\quad + \frac{I_{\mathrm{Load}}}{\omega_{\mathrm{d}} t_{\mathrm{f}23}} e^{-\delta t_{\mathrm{f}23}} \left[\left(\frac{L_{\mathrm{main}}}{L} - \delta R_{\mathrm{main}} C_{\mathrm{sn}}\right) \cdot \cos(\omega_{\mathrm{d}} t_{\mathrm{f}23}) + R_{\mathrm{main}} C_{\mathrm{sn}} \omega_{\mathrm{d}} \sin(\omega_{\mathrm{d}} t_{\mathrm{f}23})\right]. \end{aligned} \tag{A.170}$$

Subsequently, the snubber current can be calculated by inserting (A.168) and (A.170) into (A.164) as

$$
\begin{aligned}
i_{\mathrm{sn}}(t_3 \leqq t < t_4) = \Bigg\{ & \frac{A_0}{\omega_\mathrm{d}} e^{-\delta t_3} \sin(\omega_\mathrm{d} t_3). \\
& + R_{\mathrm{main}} C_{\mathrm{sn}} \frac{I_{\mathrm{Load}}}{t_{\mathrm{f23}}} \left[1 - e^{-\delta(t_3 - t_2)} \cos(\omega_\mathrm{d}(t_3 - t_2))\right] \\
& + \frac{I_{\mathrm{Load}}}{t_{\mathrm{f23}} \omega_\mathrm{d}} \left(\frac{L_{\mathrm{main}}}{L} - \delta R_{\mathrm{main}} C_{\mathrm{sn}}\right) \cdot e^{-\delta(t_3 - t_2)} \sin(\omega_\mathrm{d}(t_3 - t_2))\Bigg\} \\
& \cdot e^{-\delta(t - t_3)} \cos(\omega_\mathrm{d}(t - t_3)) \\
& + \Bigg\{ \frac{A_0}{\omega_\mathrm{d}} e^{-\delta t_3} \cos(\omega_\mathrm{d} t_3) - \frac{I_{\mathrm{Load}}}{\omega_\mathrm{d} t_{\mathrm{f23}}} \left(\frac{L_{\mathrm{main}}}{L} - \delta R_{\mathrm{main}} C_{\mathrm{sn}}\right) \\
& + \frac{I_{\mathrm{Load}}}{\omega_\mathrm{d} t_{\mathrm{f23}}} e^{-\delta(t_3 - t_2)} \Bigg[\left(\frac{L_{\mathrm{main}}}{L} - \delta R_{\mathrm{main}} C_{\mathrm{sn}}\right) \cdot \cos(\omega_\mathrm{d}(t_3 - t_2)) \\
& + R_{\mathrm{main}} C_{\mathrm{sn}} \omega_\mathrm{d} \sin(\omega_\mathrm{d}(t_3 - t_2))\Bigg]\Bigg\} \\
& \cdot e^{-\delta(t - t_3)} \sin(\omega_\mathrm{d}(t - t_3)).
\end{aligned}
\tag{A.171}
$$

And with addition theorems

$$
\begin{aligned}
i_{\mathrm{sn}}(t_3 \leqq t < t_4) = \Bigg[& -\frac{A_0}{2\omega_\mathrm{d}} e^{-\delta t} \sin(\omega_\mathrm{d}(t - 2t_3)) + \frac{A_0}{2\omega_\mathrm{d}} e^{-\delta t} \sin(\omega_\mathrm{d} t) \\
& + R_{\mathrm{main}} C_{\mathrm{sn}} \frac{I_{\mathrm{Load}}}{t_{\mathrm{f23}}} e^{-\delta(t - t_3)} \cos(\omega_\mathrm{d}(t - t_3)) \\
& - R_{\mathrm{main}} C_{\mathrm{sn}} \frac{I_{\mathrm{Load}}}{2t_{\mathrm{f23}}} e^{-\delta(t - t_2)} \cos(\omega_\mathrm{d}(t - 2t_3 + t_2)) \\
& - R_{\mathrm{main}} C_{\mathrm{sn}} \frac{I_{\mathrm{Load}}}{2t_{\mathrm{f23}}} e^{-\delta(t - t_2)} \cos(\omega_\mathrm{d}(t - t_2)) \\
& - \frac{I_{\mathrm{Load}}}{2\omega_\mathrm{d} t_{\mathrm{f23}}} \left(\frac{L_{\mathrm{main}}}{L} - \delta R_{\mathrm{main}} C_{\mathrm{sn}}\right) e^{-\delta(t - t_2)} \sin(\omega_\mathrm{d}(t - 2t_3 + t_2)) \\
& + \frac{I_{\mathrm{Load}}}{2\omega_\mathrm{d} t_{\mathrm{f23}}} \left(\frac{L_{\mathrm{main}}}{L} - \delta R_{\mathrm{main}} C_{\mathrm{sn}}\right) e^{-\delta(t - t_2)} \sin(\omega_\mathrm{d}(t - t_2))\Bigg] \\
& + \Bigg[\frac{A_0}{2\omega_\mathrm{d}} e^{-\delta t} \sin(\omega_\mathrm{d} t) + \frac{A_0}{2\omega_\mathrm{d}} e^{-\delta t} \sin(\omega_\mathrm{d}(t - 2t_3)) \\
& - \frac{I_{\mathrm{Load}}}{\omega_\mathrm{d} t_{\mathrm{f23}}} \left(\frac{L_{\mathrm{main}}}{L} - \delta R_{\mathrm{main}} C_{\mathrm{sn}}\right) e^{-\delta(t - t_3)} \sin(\omega_\mathrm{d}(t - t_3)) \\
& + \frac{I_{\mathrm{Load}}}{2\omega_\mathrm{d} t_{\mathrm{f23}}} \left(\frac{L_{\mathrm{main}}}{L} - \delta R_{\mathrm{main}} C_{\mathrm{sn}}\right) e^{-\delta(t - t_2)} \sin(\omega_\mathrm{d}(t - 2t_3 + t_2)) \\
& + \frac{I_{\mathrm{Load}}}{2\omega_\mathrm{d} t_{\mathrm{f23}}} \left(\frac{L_{\mathrm{main}}}{L} - \delta R_{\mathrm{main}} C_{\mathrm{sn}}\right) e^{-\delta(t - t_2)} \sin(\omega_\mathrm{d}(t - t_2)) \\
& + R_{\mathrm{main}} C_{\mathrm{sn}} \frac{I_{\mathrm{Load}}}{2t_{\mathrm{f23}}} e^{-\delta(t - t_2)} \cos(\omega_\mathrm{d}(t - 2t_3 + t_2)) \\
& - R_{\mathrm{main}} C_{\mathrm{sn}} \frac{I_{\mathrm{Load}}}{2t_{\mathrm{f23}}} e^{-\delta(t - t_2)} \cos(\omega_\mathrm{d}(t - t_2))\Bigg]
\end{aligned}
\tag{A.172}
$$

can be simplified to

$$\begin{aligned} i_{\mathrm{sn}}(t_3 \leqq t < t_4) = \frac{A_0}{\omega_\mathrm{d}} e^{-\delta t} \sin(\omega_\mathrm{d} t) + R_{\mathrm{main}} C_{\mathrm{sn}} \frac{I_{\mathrm{Load}}}{t_{\mathrm{f23}}} \Big[e^{-\delta(t-t_3)} \cos(\omega_\mathrm{d}(t-t_3)) \\ - e^{-\delta(t-t_2)} \cos(\omega_\mathrm{d}(t-t_2)) \Big] + \frac{I_{\mathrm{Load}}}{\omega_\mathrm{d} t_{\mathrm{f23}}} \left(\frac{L_{\mathrm{main}}}{L} - \delta R_{\mathrm{main}} C_{\mathrm{sn}} \right) \\ \cdot \Big[e^{-\delta(t-t_2)} \sin(\omega_\mathrm{d}(t-t_2)) - e^{-\delta(t-t_3)} \sin(\omega_\mathrm{d}(t-t_3)) \Big] . \end{aligned} \tag{A.173}$$

Capacitor voltage change

Similar to the two previous intervals, the snubber capacitor change in charge is calculated first. Later, the result is summed to (A.157) to obtain the total change in charge over all intervals. The charge deviation within this interval can be calculated according to

$$\begin{aligned} \Delta Q_{\mathrm{CsnI3}} &= \int_{t_3}^{t_4} i_{\mathrm{sn}} \, \mathrm{d}t \\ &= \frac{A_0}{\omega_\mathrm{d}} \int_{t_3}^{t_4} e^{-\delta t} \sin(\omega_\mathrm{d} t) \, \mathrm{d}t + R_{\mathrm{main}} C_{\mathrm{sn}} \frac{I_{\mathrm{Load}}}{t_{\mathrm{f23}}} \\ &\quad \cdot \int_{t_3}^{t_4} e^{-\delta(t-t_3)} \cos(\omega_\mathrm{d}(t-t_3)) - e^{-\delta(t-t_2)} \cos(\omega_\mathrm{d}(t-t_2)) \, \mathrm{d}t \\ &\quad + \frac{I_{\mathrm{Load}}}{\omega_\mathrm{d} t_{\mathrm{f23}}} \left(\frac{L_{\mathrm{main}}}{L} - \delta R_{\mathrm{main}} C_{\mathrm{sn}} \right) \\ &\quad \cdot \int_{t_3}^{t_4} e^{-\delta(t-t_2)} \sin(\omega_\mathrm{d}(t-t_2)) - e^{-\delta(t-t_3)} \sin(\omega_\mathrm{d}(t-t_3)) \, \mathrm{d}t \\ &= \left(\omega_\mathrm{d} R_{\mathrm{main}} C_{\mathrm{sn}} + \frac{\delta L_{\mathrm{main}}}{\omega_\mathrm{d} L} - \frac{\delta^2 R_{\mathrm{main}} C_{\mathrm{sn}}}{\omega_\mathrm{d}} \right) \frac{I_{\mathrm{Load}}}{\omega_0^2 t_{\mathrm{f23}}} \Big[e^{-\delta(t_4-t_3)} \sin(\omega_\mathrm{d}(t_4-t_3)) \\ &\quad + e^{-\delta(t_3-t_2)} \sin(\omega_\mathrm{d}(t_3-t_2)) - e^{-\delta(t_4-t_2)} \sin(\omega_\mathrm{d}(t_4-t_2)) \Big] \\ &\quad + \left(\frac{L_{\mathrm{main}}}{L} - 2\delta R_{\mathrm{main}} C_{\mathrm{sn}} \right) \frac{I_{\mathrm{Load}}}{\omega_0^2 t_{\mathrm{f23}}} \Big[e^{-\delta(t_3-t_2)} \cos(\omega_\mathrm{d}(t_3-t_2)) \\ &\quad - e^{-\delta(t_4-t_2)} \cos(\omega_\mathrm{d}(t_4-t_2)) + e^{-\delta(t_4-t_3)} \cos(\omega_\mathrm{d}(t_4-t_3)) - 1 \Big] \\ &\quad + \frac{A_0 \delta}{\omega_\mathrm{d} \omega_0^2} \Big[e^{-\delta t_3} \sin(\omega_\mathrm{d} t_3) - e^{-\delta t_4} \sin(\omega_\mathrm{d} t_4) \Big] \\ &\quad + \frac{A_0}{\omega_0^2} \Big[e^{-\delta t_3} \cos(\omega_\mathrm{d} t_3) - e^{-\delta t_4} \cos(\omega_\mathrm{d} t_4) \Big] - \frac{I_{\mathrm{Load}}}{\omega_0^2 t_{\mathrm{f23}}} \left(\frac{L_{\mathrm{main}}}{L} - 2\delta R_{\mathrm{main}} C_{\mathrm{sn}} \right) , \end{aligned} \tag{A.174}$$

which is added to the charge deviation of all previous intervals according to (A.157) leading to

$$\begin{aligned}\Delta Q_{\mathrm{CsnI1I2I3}} &= \int_{t_1}^{t_3} i_{\mathrm{sn}}\,\mathrm{d}t + \int_{t_3}^{t_4} i_{\mathrm{sn}}\,\mathrm{d}t \\ &= R_{\mathrm{main}} C_{\mathrm{sn}} I_{\mathrm{Load}} + \frac{A_0}{\omega_0^2}\left[1 - e^{-\delta t_4}\left(\frac{\delta}{\omega_{\mathrm{d}}}\sin(\omega_{\mathrm{d}} t_4) + \cos(\omega_{\mathrm{d}} t_4)\right)\right] \\ &\quad + \left(\omega_{\mathrm{d}} R_{\mathrm{main}} C_{\mathrm{sn}} + \frac{\delta L_{\mathrm{main}}}{\omega_{\mathrm{d}} L} - \frac{\delta^2 R_{\mathrm{main}} C_{\mathrm{sn}}}{\omega_{\mathrm{d}}}\right)\frac{I_{\mathrm{Load}}}{\omega_0^2 t_{\mathrm{f23}}} \\ &\quad \cdot \left[e^{-\delta(t_4-t_3)}\sin(\omega_{\mathrm{d}}(t_4-t_3)) - e^{-\delta(t_4-t_2)}\sin(\omega_{\mathrm{d}}(t_4-t_2))\right] \\ &\quad + \left(\frac{L_{\mathrm{main}}}{L} - 2\delta R_{\mathrm{main}} C_{\mathrm{sn}}\right)\frac{I_{\mathrm{Load}}}{\omega_0^2 t_{\mathrm{f23}}} \\ &\quad \cdot \left[e^{-\delta(t_4-t_3)}\cos(\omega_{\mathrm{d}}(t_4-t_3)) - e^{-\delta(t_4-t_2)}\cos(\omega_{\mathrm{d}}(t_4-t_2))\right].\end{aligned} \tag{A.175}$$

(A.175) allows to calculate the snubber voltage change from t_2 to t_4 by dividing it through C_{sn}.

$$\begin{aligned}\Delta v_{\mathrm{CsnI1I2I3}} &= R_{\mathrm{main}} I_{\mathrm{Load}} + A_0 L\left[1 - e^{-\delta t_4}\left(\frac{\delta}{\omega_{\mathrm{d}}}\sin(\omega_{\mathrm{d}} t_4) + \cos(\omega_{\mathrm{d}} t_4)\right)\right] \\ &\quad + \left(\frac{\omega_{\mathrm{d}}}{\omega_0^2} R_{\mathrm{main}} + \frac{\delta L_{\mathrm{main}}}{\omega_{\mathrm{d}}} - \frac{\delta^2 R_{\mathrm{main}}}{\omega_{\mathrm{d}}\omega_0^2}\right)\frac{I_{\mathrm{Load}}}{t_{\mathrm{f23}}} \\ &\quad \cdot \left[e^{-\delta(t_4-t_3)}\sin(\omega_{\mathrm{d}}(t_4-t_3)) - e^{-\delta(t_4-t_2)}\sin(\omega_{\mathrm{d}}(t_4-t_2))\right] \\ &\quad + \left(L_{\mathrm{main}} - \frac{2\delta}{\omega_0^2} R_{\mathrm{main}}\right)\frac{I_{\mathrm{Load}}}{t_{\mathrm{f23}}} \\ &\quad \cdot \left[e^{-\delta(t_4-t_3)}\cos(\omega_{\mathrm{d}}(t_4-t_3)) - e^{-\delta(t_4-t_2)}\cos(\omega_{\mathrm{d}}(t_4-t_2))\right].\end{aligned} \tag{A.176}$$

Deriving optimal timing

The end of the switching event which is defined by $I_{\mathrm{sn}} = 0\,\mathrm{A}$, can be calculated by setting (A.173) to zero at $t = t_4$ yielding

$$\begin{aligned}i_{\mathrm{sn}}(t_4) &= \frac{A_0}{\omega_{\mathrm{d}}} e^{-\delta t_4}\sin(\omega_{\mathrm{d}} t_4) + R_{\mathrm{main}} C_{\mathrm{sn}}\frac{I_{\mathrm{Load}}}{t_{\mathrm{f23}}}\left[e^{-\delta(t_4-t_3)}\cos(\omega_{\mathrm{d}}(t_4-t_3))\right. \\ &\quad \left. - e^{-\delta(t_4-t_2)}\cos(\omega_{\mathrm{d}}(t_4-t_2))\right] + \frac{I_{\mathrm{Load}}}{\omega_{\mathrm{d}} t_{\mathrm{f23}}}\left(\frac{L_{\mathrm{main}}}{L} - \delta R_{\mathrm{main}} C_{\mathrm{sn}}\right) \\ &\quad \cdot \left[e^{-\delta(t_4-t_2)}\sin(\omega_{\mathrm{d}}(t_4-t_2)) - e^{-\delta(t_4-t_3)}\sin(\omega_{\mathrm{d}}(t_4-t_3))\right] \\ &= 0\,\mathrm{A}.\end{aligned} \tag{A.177}$$

Rearranging the equation and by using the two constant values

$$\begin{aligned}K_{1\mathrm{t}3} =& \omega_{\mathrm{d}} R_{\mathrm{main}} C_{\mathrm{sn}}\left(e^{\delta t_3}\cos(\omega_{\mathrm{d}} t_3) - e^{\delta t_2}\cos(\omega_{\mathrm{d}} t_2)\right) \\ &+ \left(\frac{L}{L_{\mathrm{res}}} - \delta R_{\mathrm{main}} C_{\mathrm{sn}}\right)\left(e^{\delta t_3}\sin(\omega_{\mathrm{d}} t_3) - e^{\delta t_2}\sin(\omega_{\mathrm{d}} t_2)\right)\end{aligned} \quad \text{and} \tag{A.178}$$

$$\begin{aligned}K_{2\mathrm{t}3} =& \omega_{\mathrm{d}} R_{\mathrm{main}} C_{\mathrm{sn}}\left(e^{\delta t_3}\sin(\omega_{\mathrm{d}} t_3) - e^{\delta t_2}\sin(\omega_{\mathrm{d}} t_2)\right) \\ & A_0\frac{t_{\mathrm{f23}}}{I_{\mathrm{Load}}} + \left(\frac{L}{L_{\mathrm{res}}} - \delta R_{\mathrm{main}} C_{\mathrm{sn}}\right)\left(e^{\delta t_2}\cos(\omega_{\mathrm{d}} t_2) - e^{\delta t_3}\cos(\omega_{\mathrm{d}} t_3)\right),\end{aligned} \tag{A.179}$$

to obtain t_4 results in

$$t_4 = \frac{\arctan\left(-\frac{K_{1t3}}{K_{2t3}}\right)}{\omega_d} + n\frac{\pi}{\omega_d} + t_3. \tag{A.180}$$

Here, $n \in \mathbb{N}_0$.
To eliminate the load current dependency of t_4, see K_{2t3}, K_{1t3} can be set to zero which can be achieved by proper selection of t_3 as follows

$$\begin{aligned} 0 =& \omega_d R_{main} C_{sn} \left(e^{\delta t_3}\cos(\omega_d t_3) - e^{\delta t_2}\cos(\omega_d t_2)\right) \\ &+ \left(\frac{L}{L_{res}} - \delta R_{main} C_{sn}\right)\left(e^{\delta t_3}\sin(\omega_d t_3) - e^{\delta t_2}\sin(\omega_d t_3)\right). \end{aligned} \tag{A.181}$$

Rearranging and setting $t_3 = t_2 + t_{f23}$ results in

$$\begin{aligned} -\frac{\omega_d R_{main} C_{sn}}{\left(\frac{L}{L_{res}} - \delta R_{main} C_{sn}\right)} &= K_{3t3} \\ &= \frac{e^{\delta(t_2+t_{f23})}\cos(\omega_d(t_2+t_{f23})) - e^{\delta t_2}\cos(\omega_d t_2)}{e^{\delta(t_2+t_{f23})}\sin(\omega_d(t_2+t_{f23})) - e^{\delta t_2}\sin(\omega_d t_2)}. \end{aligned} \tag{A.182}$$

Eliminating the term $e^{\delta t_2}$ and using addition theorems lead to

$$K_{3t3} = \frac{e^{\delta t_{f23}}\left[\tan(\omega_d t_2)\cos(\omega_d t_{f23}) + \sin(\omega_d t_{f23})\right] - \tan(\omega_d t_2)}{e^{\delta t_{f23}}\left[\cos(\omega_d t_{f23}) - \tan(\omega_d t_2)\sin(\omega_d t_{f23})\right] - 1}. \tag{A.183}$$

And rearranging previous equation to t_2 results in the optimal point in time t_{2opt} for current independent t_4

$$t_{2opt} = \frac{\arctan\left(\frac{e^{\delta t_{f23}}\{-K_{3t3}\cos(\omega_d t_{f23}) - \sin(\omega_d t_{f23})\} + K_{3t3}}{e^{\delta t_{f23}}\{-K_{3t3}\sin(\omega_d t_{f23}) + \cos(\omega_d t_{f23})\} - 1}\right)}{\omega_d}. \tag{A.184}$$

A.5 Determining the Thermal Resistance

Heat dissipation is a key factor for achieving maximum output power [147, 148]. Hence, the thermal resistance must be determined first. Figure A.5.1 shows the module heat sink assembly with the corresponding layer thicknesses.

For calculation, the following assumptions and agreements are made:

- The semiconductor losses occur at the top-side of the chip close to the channel
- Heat dissipation through the bond wires can be neglected
- Thermal spreading as described in e.g. [149] is neglected
- The sum of the heat dissipation related area of all four paralleled dies is $A_{\text{heat}} = 100\,\text{mm}^2$
- The heat sink has a constant temperature of $\vartheta_{\text{HS}} = 65\,°\text{C}$
- Thermal conductivity is temperature independent

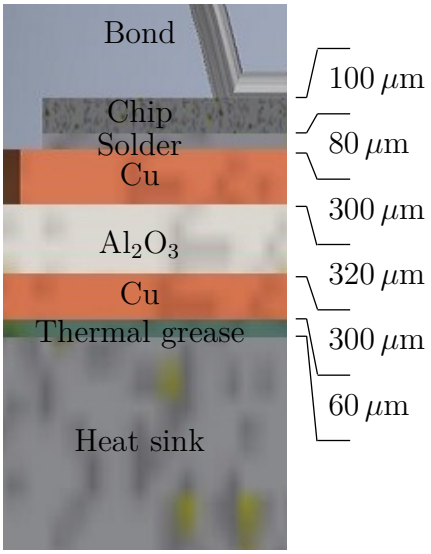


Figure A.5.1: Vertical layer arrangement from bond wire to heat sink

With the agreements above and the given measurements of the thermal layer arrangement in Fig. A.5.1, the thermal resistance of the total structure can be calculated. Table A.2 shows the results with the two most significant contributors, the ceramic and the thermal grease.

Table A.2: Thermal stack

Layer	**Material**	λ $[W/cmK]$	d $[\mu m]$	R_{th} $[mK/W]$
Chip	SiC	3.7[a]	100	27
Solder	Sn96.5/Ag3.0/Cu0.5	≈6.7	80	15
Substrate top	Cu	38.5[b]	300	7.8
Ceramic	Al_2O_3	2.4[c]	320	133.3
Substrate bottom	Cu	38.5[b]	300	7.8
Th. grease	HTCP	0.25[d]	60	240
Total				431

References: a:[4, 44], b:[150] , c:[151] , d:[152]

Another important thermal resistance considers the heat dissipation from the snubber capacitors. However, due to missing supplier information, the thermal resistance of the ceramic class I capacitor can only be estimated. In Section 2.5, it has been stated that class I capacitors consist of calcium zircon oxides and in Section 4.1.1, a class I capacitor

has been selected due to its low ESR. The specific thermal conductivity for this ceramics in the desired temperature range can be found in [153] within the range of 0.2 W/cmK to 0.35 W/cmK. For calculation, a value of $\lambda_{\mathrm{CaZr}} = 0.25\,\mathrm{W/cmK}$ shall be used.

First, the thermal resistance for one of the two capacitor assemblies for each snubber

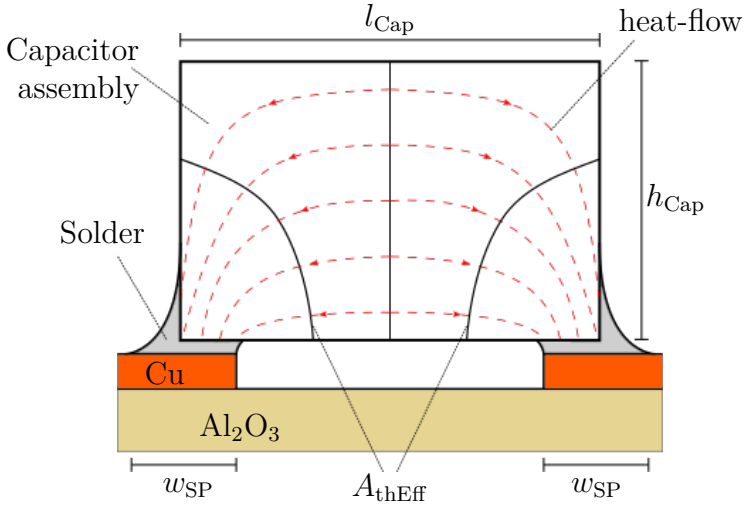


Figure A.5.2: Cross section of a capacitor assembly soldered to the power module substrate with heat flow assumed for modelling

path forming C_{sn}, cf. Fig. 4.6 is estimated. With the datasheet of the capacitors used [99], the measurements of the assembly can be calculated with a length $l_{\mathrm{Cap}} = 5.7\,\mathrm{mm}$, a width of $w_{\mathrm{Cap}} = 5.6\,\mathrm{mm}$ and a height of $h_{\mathrm{Cap}} = 5.0\,\mathrm{mm}$. A cross section of a capacitor assembly soldered on the ceramic substrate of the power module is depicted in Fig. A.5.2. For calculation, it is assumed that the power losses during oscillation occur at the center line of the device. Because heat is dissipated to each solder joint the heat flows non-lateral to the solder joints symmetrically to both sides. This results in a smaller effective area assumed to be 70 % of the capacitor assembly with $w_{\mathrm{Cap}} \cdot h_{\mathrm{Cap}}$ for heat-flow A_{thEff}, cf. Fig. A.5.2 considering the figure depth equal to w_{Cap}. With the measurements of the capacitor assembly, the effective area is approximated to

$$A_{\mathrm{thEff}} \approx w_{\mathrm{Cap}} \cdot 2 \cdot 0.7 h_{\mathrm{Cap}} \approx 5.6\,\mathrm{mm} \cdot 2 \cdot 3.5\,\mathrm{mm} = 39.2\,\mathrm{mm}^2. \tag{A.185}$$

Further, assuming a mean distance for heat transfer to each terminal inside the capacitor of $\frac{l_{\mathrm{Cap}}}{2} = 2.85\,\mathrm{mm}$, the thermal resistance for each capacitor assembly can be estimated to

$$R_{\mathrm{thCapSp}} = \frac{d}{\lambda_{\mathrm{CaZr}} A_{\mathrm{thEff}}} = \frac{2.85 \cdot 10^{-3}\,\mathrm{m}}{2.5\,\frac{\mathrm{W}}{\mathrm{mK}} \cdot 39.2 \cdot 10^{-6}\,\mathrm{m}^2} = 29.1\,\mathrm{K/W}. \tag{A.186}$$

With the width of the solder pads of $w_{\mathrm{SP}} = 1.5\,\mathrm{mm}$, see [99], each capacitor assembly is soldered to the substrate top layer with a total area for both solder pads of

$$A_{\mathrm{thCsold}} = 5.6\,\mathrm{mm} \cdot 2 \cdot 1.5\,\mathrm{mm} = 16.8\,\mathrm{mm}^2. \tag{A.187}$$

With the layer assembly given in Table A.2, the thermal resistance from capacitor assembly including solder joints to heat sink can be calculated to

$$R_{\mathrm{thSpHs}} = 2.4\,\mathrm{K/W}. \tag{A.188}$$

This results in a total thermal resistance for each capacitor assembly of

$$R_{\mathrm{thCapHs}} = R_{\mathrm{thCapSp}} + R_{\mathrm{thSpHs}} = 29.1\,\mathrm{K/W} + 2.4\,\mathrm{K/W} = 31.5\,\mathrm{K/W}. \tag{A.189}$$

Now, treating both paralleled snubber paths as a single device, the thermal resistance of the snubber C_{sn} can be calculated to

$$R_{\mathrm{thSn}} = \frac{R_{\mathrm{thCapHs}}}{2} = \frac{30.8\,\mathrm{K/W}}{2} = 15.4\,\mathrm{K/W}. \tag{A.190}$$

It should be kept in mind that this value is based on various assumptions and needs to be verified. Thus, it can only be taken as a rough estimation.
In the corresponding datasheet [99], it can be found that the used 39 nF capacitor for 2220 size is capable for an root-mean-square (RMS) current of around $I_{\mathrm{ACrms}} = 7\,\mathrm{A}$ within a wide frequency range. With the given measurement conditions at ambient temperature, a maximum device temperature of $\vartheta_{\mathrm{CapMax}} = 150\,^{\circ}\mathrm{C}$ as well as the ESR measurement of $N_{\mathrm{par}} = 4$ paralleled capacitors according Fig. 4.2 with $ESR_{\mathrm{par}} \approx 4\,\mathrm{m\Omega}$ the thermal resistance for the capacitor assembly consisting of four devices can be estimated to

$$R_{\mathrm{thCapSp}} = \frac{\vartheta_{\mathrm{CapMax}} - \vartheta_{\mathrm{Amb}}}{N_{\mathrm{par}}^2 ESR_{\mathrm{par}} I_{\mathrm{ACrms}}^2} = \frac{150\,^{\circ}\mathrm{C} - 25\,^{\circ}\mathrm{C}}{16 \cdot 4\,\mathrm{m\Omega} \cdot (7\,\mathrm{A})^2} \approx 40\,\mathrm{K/W} \tag{A.191}$$

However, in [99] it has been stated that the devices are mounted on a heat sink with no forced cooling. Additionally, it has not been stated whether the devices are mounted in 'low loss' or 'standard' manner according to [154]. Therefore, in case the heat sink suffers from temperature increase, (A.191) would result in a lower value. Further, it is not clear, how the device was mounted and how the mounting orientation affects the thermal resistance. Therefore, (A.186) shall be trusted and is taken for capacitor temperature estimation.

A.6 Inverter Calculation Scheme

This section describes the calculation scheme used to estimate the expectable parameters during inverter operation of the three investigated setups. To calculate the power losses for a drive inverter with sinusoidal output voltage and current, various parameters have to be considered. Besides the semiconductor specific switching losses, cf. Section 5.3.3, the conduction losses have to be considered as well as the modulation index M and the $\cos(\varphi)$. A calculation scheme for an IGBT/diode connection can be found in [155] P. 283ff. However, the IGBT and diode forming a 'system' are usually connected in parallel resulting in losses dissipated at two different locations with two different but coupled thermal resistances. While the calculation scheme given by [155] considers this, the MOSFET body diode used as the free wheeling diode eases the calculation.
The scheme given in [155] calculates the turn-on, turn-off and diode recovery losses at different operation points by relative scaling of losses according to a reference voltage and current point with

$$P_{\mathrm{swOn/Off}} = f_{\mathrm{sw}} W_{\mathrm{on/off}} \frac{\hat{I}_{\mathrm{Load}}}{\pi I_{\mathrm{LoadRef}}} \left(\frac{V_{\mathrm{DC}}}{V_{\mathrm{DCref}}} \right)^{K_{\mathrm{V}}} (1 + TC_{\mathrm{Wsw}} \cdot (\vartheta_{\mathrm{J}} - \vartheta_{\mathrm{ref}})) \tag{A.192}$$

and

$$P_{\mathrm{swRec}} = f_{\mathrm{sw}} W_{\mathrm{rec}} \left(\frac{\hat{I}_{\mathrm{Load}}}{\pi I_{\mathrm{LoadRef}}} \right)^{K_{\mathrm{I}}} \left(\frac{V_{\mathrm{DC}}}{V_{\mathrm{DCref}}} \right)^{K_{\mathrm{V}}} (1 + TC_{\mathrm{Wsw}} \cdot (\vartheta_{\mathrm{J}} - \vartheta_{\mathrm{ref}})). \tag{A.193}$$

However, because the power coefficients K_{V} and K_{I} used in the scaling therms are unknown, the voltage and current dependency is considered by using the already measured values from Section 5.3.3. Furthermore, the temperature coefficient TC_{Wsw} of the switching losses is not considered. Because this value cannot be estimated for the hypothetical optimized MOSFET setup with improved R_{DSon}, the R_{DSon} is taken to be temperature independent. This necessitates a modification of the given scheme in the manner shown below.
First, the switching losses for all inverter variants are derived by fitting a second order polynomial model to the measured switching losses presented in Section 5.3.3 and the on-state resistance given in Section 5.3.5. The resulting model coefficients are given in Table C.1. Now, the equations according to [155] can be written as follows.
The conduction loss for a current flow in drain-source direction can be simplified to

$$P_{\mathrm{condDS}}(I_{\mathrm{Load}}) = \left(\frac{1}{8} + \frac{M \cos(\varphi)}{3\pi} \right) \cdot R_{\mathrm{DSon}}(I_{\mathrm{Load}}) \hat{I}^2_{\mathrm{Load}}, \tag{A.194}$$

where $\hat{I}_{\mathrm{Load}}$ is the peak load current, I_{load} the RMS load current. The modulation index M is defined as

$$M = \frac{\hat{v}_{\mathrm{phase}}}{V_{\mathrm{DC}}/2}, \tag{A.195}$$

with the peak phase voltage $\hat{v}_{\mathrm{phase}}$ with respect to the potential $V_{\mathrm{DC}}/2$. Contrary to that, the conduction loss for inverse current flow is calculated by

$$P_{\mathrm{condSD}}(I_{\mathrm{Load}}) = \left(\frac{1}{8} - \frac{M \cos(\varphi)}{3\pi} \right) \cdot R_{\mathrm{DSon}}(I_{\mathrm{Load}}) \hat{I}^2_{\mathrm{Load}}. \tag{A.196}$$

It has been stated that both snubber circuits strongly reduce the voltage overshoot during turn-off with a maximum voltage peak below of $\hat{v}_{\mathrm{DS}} < 1000\,\mathrm{V}$, cf. Fig. 5.1. Thus, the currently used MOSFET device with a specified breakdown voltage of $V_{\mathrm{BDspec}} = 1200\,\mathrm{V}$ can be optimized in terms of lower breakdown voltage and improved on-state resistance. As introduced in Section 2.1.3, the on-state resistance of the ideal drift region with equal semiconductor properties is a function of V_{BD}^2. This allows to estimate the conduction losses of an optimized device by multiplying (A.194) and (A.196) by the factor

$$\gamma = \left(\frac{\hat{v}_{\mathrm{DS}}}{V_{\mathrm{BDspec}}}\right)^2 = \left(\frac{1000\,\mathrm{V}}{1200\,\mathrm{V}}\right)^2 = 0.69, \tag{A.197}$$

which indicate a reduction in conduction losses of about 30 %.

To fully calculate the semiconductor losses, the switching losses are calculated as

$$P_{\mathrm{swOff}}(I_{\mathrm{Load}}) = W_{\mathrm{off}}(I_{\mathrm{Load}}) f_{\mathrm{sw}}, \tag{A.198}$$
$$P_{\mathrm{swOn}}(I_{\mathrm{Load}}) = W_{\mathrm{on}}(I_{\mathrm{Load}}) f_{\mathrm{sw}} \quad \text{and} \tag{A.199}$$
$$P_{\mathrm{swRec}}(I_{\mathrm{Load}}) = W_{\mathrm{rec}}(I_{\mathrm{Load}}) f_{\mathrm{sw}}. \tag{A.200}$$

This allows to formulate the losses dissipated in the semiconductor for each configuration with

$$\begin{aligned} P_{\mathrm{semHB}}(I_{\mathrm{Load}}) =& P_{\mathrm{condDS}}(I_{\mathrm{Load}}) + P_{\mathrm{condSD}}(I_{\mathrm{Load}}) \\ &+ P_{\mathrm{swOff}}(I_{\mathrm{Load}}) + P_{\mathrm{swOn}}(I_{\mathrm{Load}}) + P_{\mathrm{swRec}}(I_{\mathrm{Load}}), \end{aligned} \tag{A.201}$$

$$\begin{aligned} P_{\mathrm{semSN}}(I_{\mathrm{Load}}) =& P_{\mathrm{condDS}}(I_{\mathrm{Load}}) + P_{\mathrm{condSD}}(I_{\mathrm{Load}}) \\ &+ P_{\mathrm{swOffSN}}(I_{\mathrm{Load}}) + P_{\mathrm{swOnSN}}(I_{\mathrm{Load}}) + P_{\mathrm{swRecSN}}(I_{\mathrm{Load}}), \end{aligned} \tag{A.202}$$

$$\begin{aligned} P_{\mathrm{semSNo}}(I_{\mathrm{Load}}) =& \left(P_{\mathrm{condDS}}(I_{\mathrm{Load}}) + P_{\mathrm{condSD}}(I_{\mathrm{Load}})\right)\gamma \\ &+ P_{\mathrm{swOffSN}}(I_{\mathrm{Load}}) + P_{\mathrm{swOnSN}}(I_{\mathrm{Load}}) + P_{\mathrm{swRecSN}}(I_{\mathrm{Load}}), \end{aligned} \tag{A.203}$$

$$\begin{aligned} P_{\mathrm{semAS}}(I_{\mathrm{Load}}) =& P_{\mathrm{condDS}}(I_{\mathrm{Load}}) + P_{\mathrm{condSD}}(I_{\mathrm{Load}}) \\ &+ P_{\mathrm{swOffAS}}(I_{\mathrm{Load}}) + P_{\mathrm{swOnAS}}(I_{\mathrm{Load}}) + P_{\mathrm{swRecAS}}(I_{\mathrm{Load}}) \quad \text{and} \end{aligned} \tag{A.204}$$

$$\begin{aligned} P_{\mathrm{semASo}}(I_{\mathrm{Load}}) =& \left(P_{\mathrm{condDS}}(I_{\mathrm{Load}}) + P_{\mathrm{condSD}}(I_{\mathrm{Load}})\right)\gamma \\ &+ P_{\mathrm{swOffAS}}(I_{\mathrm{Load}}) + P_{\mathrm{swOnAS}}(I_{\mathrm{Load}}) + P_{\mathrm{swRecAS}}(I_{\mathrm{Load}}). \end{aligned} \tag{A.205}$$

Similarly, the damping and snubber losses have to be calculated. The damping losses are obtained as described in Section 4.1.3 and are modeled as a function of I_{Load} similarly. As shown in Section 5.3.4, the damping losses for the halfbridge are negligible compared to the damping losses in both snubber setups. Therefore, the damping losses only for the snubber setups are considered with equations

$$P_{\mathrm{dampSN}}(I_{\mathrm{Load}}) = f_{\mathrm{sw}} \cdot \left(W_{\mathrm{dampOffSN}}(I_{\mathrm{Load}}) + W_{\mathrm{dampRecSN}}(I_{\mathrm{Load}})\right) \quad \text{and} \tag{A.206}$$
$$P_{\mathrm{dampAS}}(I_{\mathrm{Load}}) = f_{\mathrm{sw}} \cdot \left(W_{\mathrm{dampOffAS}}(I_{\mathrm{Load}}) + W_{\mathrm{dampRecAS}}(I_{\mathrm{Load}})\right). \tag{A.207}$$

Further, it has been already explained that the damping losses caused by the lower frequency high amplitude snubber oscillation are mainly dissipated in the DC-link circuit, cf. Section 2.4.1. To obtain the snubber losses as a fraction of the damping losses, the occurring damping losses are proportionally rated with the relation $0.5 \cdot R_{\mathrm{sn}}/R_{\mathrm{d}}$ considering the oscillation frequency according (4.7), and both paralleled capacitor assemblies.

Hence, the relation can be calculated with the effective damping resistor according (4.9) and (4.12) giving

$$\beta_{\mathrm{SN}} = \frac{R_{\mathrm{sn}}(1.44\,\mathrm{MHz})}{2R_{\mathrm{dSN}}} = \frac{3.2\,\mathrm{m\Omega}}{2 \cdot 49\,\mathrm{m\Omega}} = 33 \cdot 10^{-3} \quad \text{and} \tag{A.208}$$

$$\beta_{\mathrm{AS}} = \frac{R_{\mathrm{sn}}(1.44\,\mathrm{MHz})}{2R_{\mathrm{dAS}}} = \frac{3.2\,\mathrm{m\Omega}}{2 \cdot 59\,\mathrm{m\Omega}} = 27 \cdot 10^{-3}. \tag{A.209}$$

This allows to calculate the snubber capacitor losses from the damping losses with

$$P_{\mathrm{capSN}}(I_{\mathrm{Load}}) = P_{\mathrm{dampSN}}(I_{\mathrm{Load}}) \cdot \beta_{\mathrm{SN}}, \tag{A.210}$$

$$P_{\mathrm{capAS}}(I_{\mathrm{Load}}) = P_{\mathrm{dampAS}}(I_{\mathrm{Load}}) \cdot \beta_{\mathrm{AS}} \tag{A.211}$$

and finally the total losses for all setups within a three phase setup with six switches is calculated by

$$P_{\mathrm{totHB}}(I_{\mathrm{Load}}) = 6 \cdot P_{\mathrm{semHB}}(I_{\mathrm{Load}}), \tag{A.212}$$

$$P_{\mathrm{totSN}}(I_{\mathrm{Load}}) = 6 \cdot P_{\mathrm{semSN}}(I_{\mathrm{Load}}) + P_{\mathrm{dampSN}}(I_{\mathrm{Load}}), \tag{A.213}$$

$$P_{\mathrm{totSNo}}(I_{\mathrm{Load}}) = 6 \cdot P_{\mathrm{semSNo}}(I_{\mathrm{Load}}) + P_{\mathrm{dampSN}}(I_{\mathrm{Load}}), \tag{A.214}$$

$$P_{\mathrm{totAS}}(I_{\mathrm{Load}}) = 6 \cdot P_{\mathrm{semAS}}(I_{\mathrm{Load}}) + P_{\mathrm{dampAS}}(I_{\mathrm{Load}}) \quad \text{and} \tag{A.215}$$

$$P_{\mathrm{totASo}}(I_{\mathrm{Load}}) = 6 \cdot P_{\mathrm{semASo}}(I_{\mathrm{Load}}) + P_{\mathrm{dampAS}}(I_{\mathrm{Load}}). \tag{A.216}$$

The inverter output power is calculated with the well known equation

$$P_{\mathrm{out}} = \sqrt{3} \cdot V_{\mathrm{phase}} I_{\mathrm{rms}} \cos(\varphi), \tag{A.217}$$

where I_{rms} is the RMS phase current and V_{phase} is obtained with

$$V_{\mathrm{phase}} = \sqrt{\frac{3}{2}} \frac{V_{\mathrm{DC}}}{2} M, \tag{A.218}$$

as the effective inverter output voltage with respect to half of the DC-link voltage, see [155].

B Detailed Setup Description

B.1 Gate Driver

In this section, the gate driver design used for the double pulse measurements is explained. The gate driver is desiged to be a conventional power stage without special controlling features. However, due to the target of enabling fastest switching, the gate driver must be capable of providing high peak gate currents to quickly charge and discharge the gate-source capacitance of the corresponding power semiconductor. A low impedance gate-circuit is necessary to keep control of the switching device [156] and suppress parasitic turn-on [157, 158]. The corresponding schematic of its power stage is depicted in Figure B.1.1. The main power stage for fast switching consists of a push-pull circuit with three paralleled MOSFETs, see red area in Fig. B.1.1 T3, T6, T8 for turn-on and T4, T7, T9 for turn-off. The maximum achievable output peak current, limited by the transistors with an ideal zero impedance gate circuit has been simulated to be 60 A. However, the gate circuit parasitics of the real setup, estimated to be $L_\mathrm{G} \approx 35\,\mathrm{nH}$ and $C_\mathrm{iss} \approx 20\,\mathrm{nF}$, is the limiting factor with a characteristic impedance of

$$Z_\mathrm{G} \approx \sqrt{\frac{35\,\mathrm{nH}}{20\,\mathrm{nF}}} = 1.3\,\Omega. \tag{B.1}$$

Additionally, the two parallel resistors R15 and R16 are used as R_Gon and the two resistors R17 and R18 are used as R_Goff. Further, the gate driver is equipped with a rail-to-rail stage, see blue area in Fig. B.1.1, which shall improve the on-state resistance of the power semiconductor during inverter operation. However, this feature has not been used in this work.
Because a fast turn-off during short circuit may lead to a significant overshoot above the specified semiconductor maximum voltage, the power stage is equipped with a soft turn-off element, see green area in Fig. B.1.1, in which a higher R_Goff can be activated, cf. Fig. B.1.1 R14. Both transistors, T5 and T10 are in conduction state acting as a short circuit over R14. During short circuit turn-off, they are turned off and the gate discharge current flows through R14.

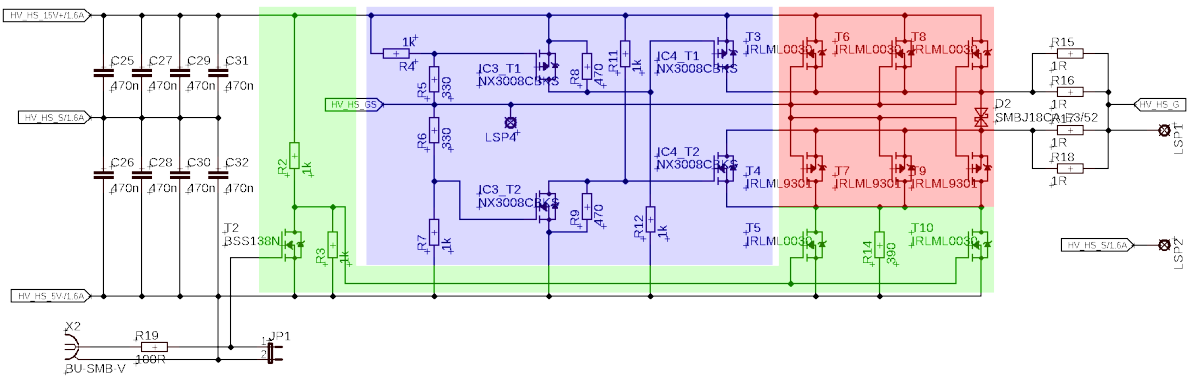


Figure B.1.1: Laboratory driver power stage

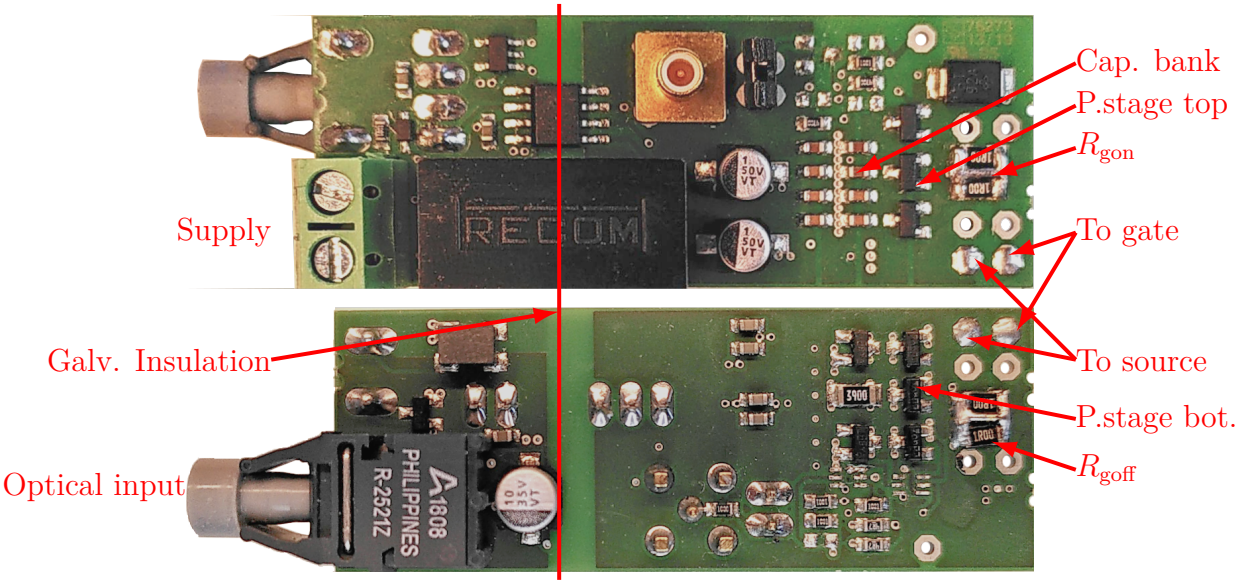


Figure B.1.2: Laboratory driver, top and bottom view

The four layer PCB is shown in Fig. B.1.2. The power stage is supplied by a DC-DC converter with 20 V/−5 V, while the control signal is provided via a fiber optic connection translated to the high voltage side by a driver IC of type 1EDI60N12AF.

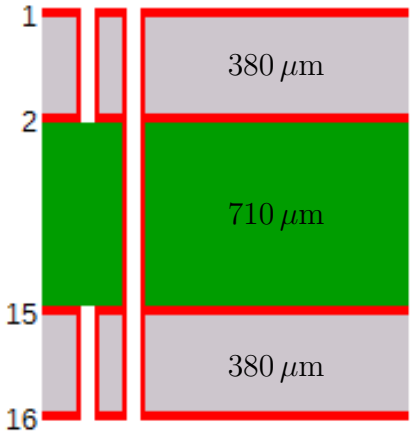


Figure B.1.3: Driver PCB layers

The layer arrangement was chosen to be very close to each other to ensure a low inductive path in the power sage to the gate-source terminal. Layer 2 was chosen to be the source potential to provide a symmetric axis for the positive driver voltage on layer 1 and the negative driver voltage on layer 15 and 16. Further control signals are routed on layer 15 and 16 with respect to not interrupt a laminar current flow in other layers between the gate-source connection, the power stage transistors and the capacitor bank.

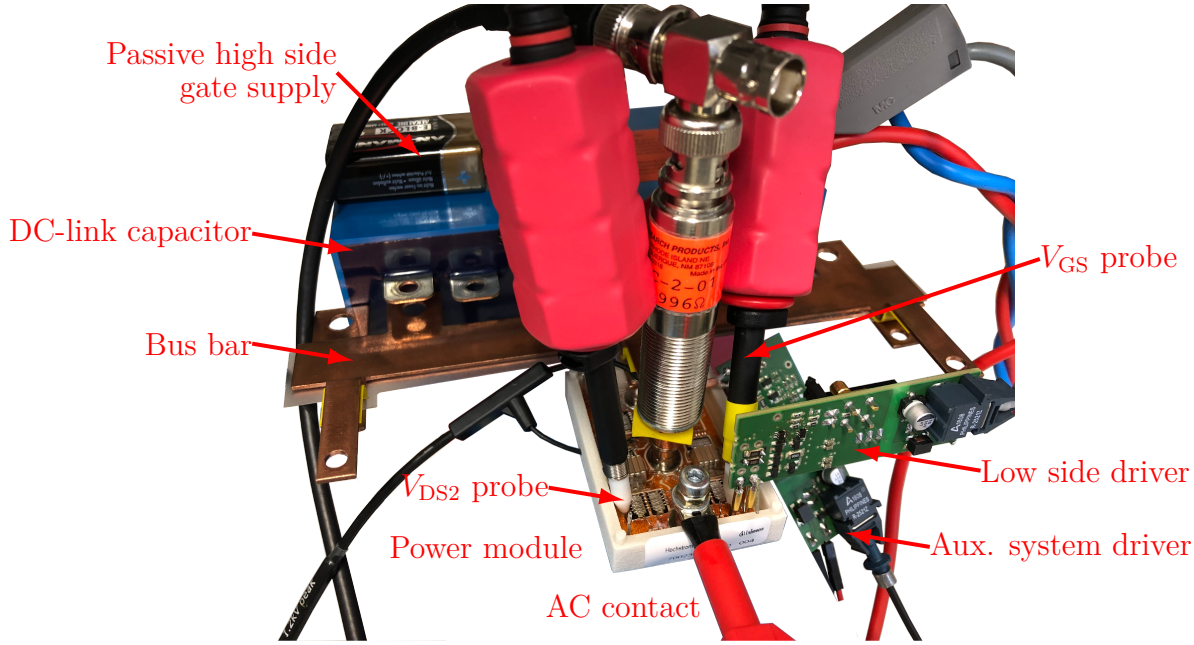


Figure B.2.1: Double pulse setup

B.2 Basic Measurement Setup

This section describes the setup used for double pulse measurements. Figure B.2.1 gives an overview showing all relevant components. The type of components commercially available are given in Table B.1. The DC-link capacitor is connected through a copper band shaped conductor (bus bar) to the power module. To vary the setup inductance for the comparison measurement, the manner of connection from the bus bar to the DC-link capacitor was altered with spacers. The connection to the power module was designed to have a deliberately large stray inductance, which can be noticed in Figure B.2.2 with a wide distance between the DC+ and DC- module terminal. The compact gate driver described in B.1, is mounted to the low-side system of the halfbridge in a vertical manner to free space for the connection of the passive voltage probes.
The high-side system, from which only the body diode is used, is kept in blocking state with a $-9\,\mathrm{V}$ gate source voltage provided by a battery and buffered with $3 \cdot 33\,\mathrm{nF}$ class II ceramic capacitors as shown in Figs. B.2.1 and B.2.2.
The driver of the auxiliary switch is connected with a 2 cm RG316 coaxial wire as adaptation to the corresponding gate-source pins, see Fig. B.2.2.

The measurement of the gate-source and drain-source voltages was done with passive voltage probes. Further, the connection of the reference potential was done using springs to ensure a very small coupling loop and low noise signal measurement. Due to the different reference potential of each passive probe as well as the coaxial shunt, undesired circular currents can be expected. Therefore, each passive probe is equipped with a toroidal ferrit core with adequate frequency behavior and 5 turns close to the oscilloscope connector.

The measurement of the DC-link current was done using a coaxial shunt in the negative DC-link path. As it can be noticed in Figure B.2.2 the current from the module is flowing through the inner side contact of the shunt first and then through the outside to the DC- potential. This lead to a negative output signal, which was inverted mathematically. An

Table B.1: Setup components

Vendor	Type	Component
TDK	B25655	900 V, 15 nH, 120 μF DC-link capacitor
Pemuk	CWT6B-UM	$i_{sn}/2$, Rogowski 30 MHz
PMK	PHV-1000	v_{DS2}, v_{GS}, passive voltage probe with 400 MHz
ib-Billmann	SBNC A-2-01	i_{link}, Coaxial shunt 400 MHz
Ferroxcube	T107/65/26-3F3	Ferrit toroid

insulation paper is used to prevent a short circuit between the negative DC copper stripe from the bus bar to the DC-minus terminal of the module, which would short circuit the current shunt. The current shunt is connected to the oscilloscope with a 50 Ω terminator necessary to prevent reflections. It should be noted that the shunt is not equipped with a toroidal ferrit core acting as a common mode choke because a negative effect on the signal quality was noticed during the first measurements, which might be explained by additional parasitics caused by the windings lead to a mismatched signal termination. However, this was not investigated further.

As mentioned in Section 4.1.3, the current of only one of the two paralleled snubber

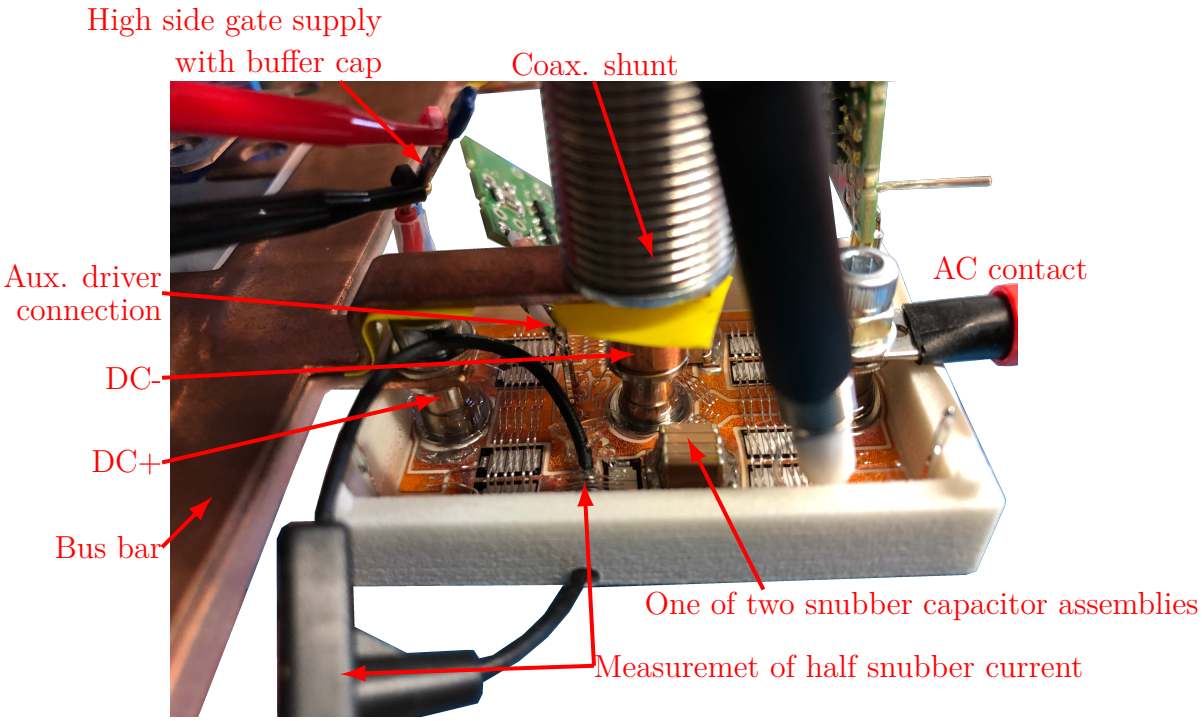


Figure B.2.2: Module and probe connection

capacitors was measured. As it can be seen in Fig. B.2.2, a small Rogowski coil was mounted at the bond wires of one of the two paralleled auxiliary switches. However, influence of the limited bandwidth of commercially available Rogowski coils small enough for this kind of mounting was already discussed in Sect. 4.2.

C Documented Data

C.1 Model Coefficients for Loss Estimation

In this section, the parameters of the models used for inverter loss estimation are documented. Each model is described as a function of I_{Load} according following equation

$$Model(I_{\mathrm{Load}}) = a_2 I_{\mathrm{Load}}^2 + a_1 I_{\mathrm{Load}} + a_0 \tag{C.1}$$

Table C.1: Model coefficients for loss estimation

Model	a_0	a_1	a_2	R^2_{adj}
R_{DSon}	$3.75 \cdot 10^{-3}\,\Omega$	$1.0283 \cdot 10^{-6}\,\Omega/\mathrm{A}$	0	0.953
R_{SDon}	$3.769 \cdot 10^{-3}\,\Omega$	$-1.931 \cdot 10^{-7}\,\Omega/\mathrm{A}$	0	0.541
W_{offHB}	$0\,\mathrm{J}$	$2.42 \cdot 10^{-5}\,\mathrm{J/A}$	$5.2 \cdot 10^{-8}\,\mathrm{J/A^2}$	
W_{onHB}	$176 \cdot 10^{-6}\,\mathrm{J}$	$1.21 \cdot 10^{-5}\,\mathrm{J/A}$	$-2.12 \cdot 10^{-8}\,\mathrm{J/A^2}$	0.938
W_{recHB}	$748 \cdot 10^{-6}\,\mathrm{J}$	$8.6745 \cdot 10^{-9}\,\mathrm{J/A}$	0	-0.998
W_{offSN}	$528 \cdot 10^{-6}\,\mathrm{J}$	$3.6703 \cdot 10^{-6}\,\mathrm{J/A}$	0	0.765
W_{onSN}	$375 \cdot 10^{-6}\,\mathrm{J}$	$1.4127 \cdot 10^{-5}\,\mathrm{J/A}$	0	0.998
W_{recSN}	$397 \cdot 10^{-6}\,\mathrm{J}$	$-7.9507 \cdot 10^{-7}\,\mathrm{J/A}$	0	0.423
$W_{\mathrm{dampOffSN}}$	$9.4131 \cdot 10^{-6}\,\mathrm{J}$	$-3.4821 \cdot 10^{-7}\,\mathrm{J/A}$	$1.877 \cdot 10^{-8}\,\mathrm{J/A^2}$	
$W_{\mathrm{dampRecSN}}$	$1.4684 \cdot 10^{-5}\,\mathrm{J}$	$-1.0152 \cdot 10^{-7}\,\mathrm{J/A}$	$1.4353 \cdot 10^{-8}\,\mathrm{J/A^2}$	
W_{offAS}	$516 \cdot 10^{-6}\,\mathrm{J}$	$4.4144 \cdot 10^{-6}\,\mathrm{J/A}$	0	0.851
W_{onAS}	$184 \cdot 10^{-6}\,\mathrm{J}$	$1.1215 \cdot 10^{-6}\,\mathrm{J/A}$	0	0.963
W_{recAS}	$671 \cdot 10^{-6}\,\mathrm{J}$	$3.9353 \cdot 10^{-7}\,\mathrm{J/A}$	0	-0.823
$W_{\mathrm{dampOffAS}}$	$7.1395 \cdot 10^{-5}\,\mathrm{J}$	$7.1241 \cdot 10^{-8}\,\mathrm{J/A}$	$1.1597 \cdot 10^{-9}\,\mathrm{J/A^2}$	
$W_{\mathrm{dampRecAS}}$	$7.13 \cdot 10^{-5}\,\mathrm{J}$	$1.4439 \cdot 10^{-7}\,\mathrm{J/A}$	$-3.5736 \cdot 10^{-10}\,\mathrm{J/A^2}$	

List of Figures

1.1 Basic inverter schematic with components 3

2.1 Intrinsic carrier concentration over temperature 8
2.2 PIN Diode 9
2.3 Carrier distribution in the drift region for a strong reverse current 10
2.4 Ideal specific on-state resistance over breakdown voltage 11
2.5 Vertical trench MOSFET 12
2.6 Common conductor geometries 14
2.7 Basic commutation circuit 16
2.8 Turn-on event description 16
2.9 Turn-off event description 16
2.10 Notch commutated 3-phase PWM ZVS inverter 20
2.11 DC-snubber equivalent circuits 22
2.12 Turn-off snubber equivalent circuit 25
2.13 Exemplary DC-snubber worst case losses 26
2.14 Exemplary assembly of a KC-Link capacitor 27
2.15 Areas with intrinsic field orientation left:unpolarized, right: polarized . . . 28
2.16 Scheme for polarization over electric field for ferroelectric 28
2.17 Complete capacitor equivalent circuit 29

3.1 Setup equivalent circuit 33
3.2 Active snubber turn-on event description 34
3.3 Active snubber turn-on event description 36
3.4 Model equivalent circuit 40
3.5 t_4 as a function of I_{Load} and t_2 46

4.1 Class I: C_{DUT} as a function of V and ϑ at 2 MHz 49
4.2 Class I: ESR as a function of f and ϑ at 500 VDC 49
4.3 Class II: C_{DUT} as a function of V and ϑ at 2 MHz 50
4.4 Class II: ESR as a function of f and ϑ at 500 VDC 50
4.5 Conventional halfbridge 51
4.6 Halfbridge with DC-snubber 51
4.7 Halfbridge with active snubber 52
4.8 Turn-on event for a load current of 350 A at a DC-link voltage of 750 V . . 53
4.9 C_{oss} of the used SiC-MOSFET dies as a function of v_{DS} 55
4.10 Turn-on event for a load current of 50 A at a DC-link voltage of 750 V . . . 58
4.11 Turn-off event for a load current of 350 A at a DC-link voltage of 765 V . . 62
4.12 Turn-off event for a load current of 50 A at a DC-link voltage of 765 V . . . 68
4.13 Development of snubber voltage over subsequent switching events at 350 A 74
4.14 Development of snubber current over subsequent switching events at 350 A 74
4.15 Simulated damping losses for subsequent switching events at 350 A 75
4.16 Development of snubber voltage over subsequent switching events at 50 A . 78
4.17 Development of snubber current over subsequent switching events at 50 A . 78
4.18 Simulated damping losses for subsequent switching events at 50 A 80

4.19 Development of snubber voltage over subsequent switching events at sinusoidal load current . . . 81
4.20 Development of snubber current over subsequent switching events at sinusoidal load current . . . 81
4.21 Damping losses for sinusoidal load current . . . 82

5.1 Turn-off overvoltage for the three different setups for $V_{\mathrm{DC}} = 750\,\mathrm{V}$ and $I_{\mathrm{Load}} = 350\,\mathrm{A}$ . . . 85
5.2 Active snubber v_{DS2} for different R_{Goff} at 750 V, 350 A . . . 86
5.3 $\hat{v}_{\mathrm{DS}}$ as a function of I_{Load} at $R_{\mathrm{Gon}} = 2\,\Omega$ and 750 V . . . 87
5.4 $\hat{v}_{\mathrm{DS}}$ as a function of R_{gon} at 750 V . . . 87
5.5 DC-snubber v_{DS1} for 750 V, 350 A with $R_{\mathrm{Gon}} = 2\,\Omega$ . . . 88
5.6 AS snubber v_{DS1} for 750 V, 350 A with $R_{\mathrm{Gon}} = 1\,\Omega$ . . . 88
5.7 Turn-off comparison for $L_{\sigma\mathrm{On}} = 37\,\mathrm{nH}$ at 350 A . . . 89
5.8 Turn-off comparison for $L_{\sigma\mathrm{On}} = 37\,\mathrm{nH}$ at 50 A . . . 91
5.9 Comparison between real measurement and ideal simulation for alignment at 50 A . . . 94
5.10 Comparison between real measurement and simulation with a 30 MHz low-pass filtered Rogowski coil and signal deskew at 50 A . . . 95
5.11 Turn-on comparison for $L_{\sigma\mathrm{On}} = 37\,\mathrm{nH}$ at 350 A . . . 96
5.12 Turn-on comparison for $L_{\sigma\mathrm{On}} = 37\,\mathrm{nH}$ at 50 A . . . 97
5.13 Diode recovery comparison for $L_{\sigma\mathrm{On}} = 37\,\mathrm{nH}$ at 350 A . . . 98
5.14 Diode recovery comparison for $L_{\sigma\mathrm{On}} = 37\,\mathrm{nH}$ at 50 A . . . 99
5.15 dv/dt_{max} over I_{Load} for turn-off . . . 100
5.16 dv/dt_{max} over V_{DC} for turn-off . . . 100
5.17 dv/dt_{max} over I_{Load} for turn-on . . . 101
5.18 dv/dt_{max} over V_{dc} for turn-on . . . 101
5.19 dv/dt_{max} over I_{Load} for diode recovery . . . 102
5.20 dv/dt_{max} over V_{DC} for diode recovery . . . 102
5.21 I_{rrm} over I_{Load} . . . 103
5.22 I_{rrm} over V_{DC} . . . 103
5.23 W_{off} over I_{Load} . . . 104
5.24 W_{off} over V_{DC} . . . 104
5.25 W_{on} over I_{Load} . . . 105
5.26 W_{on} over V_{DC} . . . 105
5.27 W_{rec} over I_{Load} . . . 105
5.28 W_{rec} over V_{DC} . . . 105
5.29 W_{swtot} over I_{Load} . . . 106
5.30 W_{swtot} over V_{DC} . . . 106
5.31 W_{dampOff} over I_{Load} . . . 107
5.32 W_{dampOff} over V_{DC} . . . 107
5.33 W_{dampRec} over I_{Load} . . . 108
5.34 W_{dampRec} over V_{DC} . . . 108
5.35 Channel characteristic of the drain-source (DS) and source-drain (SD) path over I_{Load} . . . 109
5.36 On-resistance of the drain-source (DS) and source-drain (SD) path over I_{Load}, $\vartheta_{\mathrm{J}} = 25\,^{\circ}$ . . . 109

5.37 Inverter conduction losses over I_{Load} for non-optimized (NO) and with optimized (WO) semiconductors . . . 111
5.38 Switching losses at $f_{\mathrm{sw}} = 10\,\mathrm{kHz}$ . . . 112
5.39 Switching losses at $f_{\mathrm{sw}} = 30\,\mathrm{kHz}$ . . . 112
5.40 Snubber temperature at $f_{\mathrm{sw}} = 10\,\mathrm{kHz}$ . . . 113
5.41 Snubber temperature at $f_{\mathrm{sw}} = 30\,\mathrm{kHz}$ . . . 113
5.42 Achievable output power with $\vartheta_{\mathrm{HS}} = 65\,^{\circ}\mathrm{C}$ assumed to be constant . . . 114
5.43 Inverter efficiency at $f_{\mathrm{sw}} = 10\,\mathrm{kHz}$ . . . 115
5.44 Inverter efficiency at $f_{\mathrm{sw}} = 30\,\mathrm{kHz}$ . . . 115

6.1 Basic active filter circuit . . . 118
6.2 Active filter principle of operation . . . 118
6.3 LC-Filter bode plot . . . 119
6.4 Discharge pulse . . . 120
6.5 Charge pulse . . . 122
6.6 IGBT turn-on reference . . . 123
6.7 IGBT turn-off reference . . . 124
6.8 Energy comparison . . . 125

A.1.1Energy gap . . . 132
A.1.2Density of states . . . 132
A.2.1Basic RLC circuit . . . 132
A.3.1Active snubber turn-on equivalent circuit . . . 134
A.3.2Active snubber turn-on current and time intervals . . . 134
A.3.3Active snubber turn-on equivalent circuit for the last interval . . . 139
A.4.1Active snubber turn-off equivalent circuit . . . 142
A.4.2Active snubber turn-off current and time intervals . . . 142
A.5.1Vertical layer arrangement from bond wire to heat sink . . . 156
A.5.2Cross section of a capacitor assembly . . . 157

B.1.1Laboratory driver power stage . . . 162
B.1.2Laboratory driver, top and bottom view . . . 163
B.1.3Driver PCB layers . . . 163
B.2.1Double pulse setup . . . 164
B.2.2Module and probe connection . . . 165

List of Tables

2.1 Semiconductor properties at 300K 7
2.2 Application current class analysis of $L_\sigma \cdot I_{\mathrm{nom}}$ 15

5.1 Varied parameter for characterization 84
5.2 Chosen gate resistors 88
5.3 Calculated setups for comparison 110

6.1 Turn-on parameters 124
6.2 Diode recovery parameters 124
6.3 Turn-off parameters 125

A.1 Effective masses of electrons and holes 131
A.2 Thermal stack 156

B.1 Setup components 165

C.1 Model coefficients for loss estimation 166

List of Symbols

Symbol	Unit	Description
β	1	Ratio between the total snubber ESR and the effective damping resistance
δ	1/s	Damping coefficient
δ_{14}	1/s	Damping coefficient in the interval $t_1 \leq t < t_4$
δ_{45}	1/s	Damping coefficient in the interval $t_4 \leq t < t_5$
ε_r	1	Relative permitivity
ε_s	1	Relative permitivity of a semiconductor
η	%	Efficiency, ratio between output power and input power
ϑ	K	Temperature
ϑ_amb	°C	Ambient temperature
ϑ_sn	°C	Snubber capacitor themperature
ϑ_snMax	°C	Maximum allowed snubber capacitor themperature
ϑ_HS	°C	Themperature of the heat sink
ϑ_j	°C	Junction temperature
ϑ_jMax	°C	Maximum allowed junction temperature
λ	$\frac{\mathrm{W}}{\mathrm{mK}}$	Specific thermal conductance
λ_CaZr	$\frac{\mathrm{W}}{\mathrm{mK}}$	Specific thermal conductance of Calcium Zirkonat
μ_0	$\frac{\mathrm{Vs}}{\mathrm{Am}}$	Magnetic field constant with $4\pi \cdot 10^{-7}\,\mathrm{Vs/Am}$
μ_n	$\frac{\mathrm{m}^2}{\mathrm{Vs}}$	Electron mobility
μ_p	$\frac{\mathrm{m}^2}{\mathrm{Vs}}$	Hole mobility
Φ_t	Vs	Total magnetic flux
ω_0	1/s	Angular frequency of an undamped resonant circuit
ω_{034}	1/s	Angular frequency of the undamped resonant circuit in the interval $t_3 \leq t < t_4$
ω_{045}	1/s	Angular frequency of the undamped resonant circuit in the interval $t_4 \leq t < t_5$

ω_d	1/s	Angular frequency of a damped resonant circuit
ω_d34	1/s	Angular frequency of a damped resonant circuit in the interval $t_3 \leq t < t_4$
ω_d45	1/s	Angular frequency of a damped resonant circuit in the interval $t_4 \leq t < t_5$
A_0	A	Auxiliary current coefficient for the turn-off event
A_{34}	A	Auxiliary current coefficient in the interval $t_3 \leq t < t_4$
A_{45}	A	Auxiliary current coefficient in the interval $t_4 \leq t < t_5$
A_th	m^2	Heat dissipating area
A_thEff	m^2	Effective area for heat dissipation
B	T	Magnetic flux density
c_0	$\frac{\mathrm{m}}{\mathrm{s}}$	Speed of light with 299 792 458 m/s
C_D	$\frac{\mathrm{F}}{\mathrm{m}^2}$	Depletion layer capacitance per area
C_DC	F	DC-link capacitance
C_DG	F	Drain to gate capacitance
C_DS	F	Drain to source capacitance
C_f	F	Filter capacitance
C_GS	F	Gate to source capacitance
C_iss	F	Input capacitance as $C_\mathrm{GS} + C_\mathrm{DG}$
C_oss	F	Output capacitance as $C_\mathrm{DS} + C_\mathrm{DG}$
$C_{\mathrm{oss}*}$	F	Output capacitance containing both, the charge stored in C_oss as well as the recovery charge
C_ox	$\frac{\mathrm{F}}{\mathrm{m}^2}$	Gate oxide capacitance per area
C_rss	F	Reverse capacitance as C_DG
C_sn	F	Snubber capacitor
CTE	$\frac{\mathrm{1e{-}6}}{^\circ\mathrm{C}}$	Coefficitent of thermal expansion
E_crit	$\frac{\mathrm{V}}{\mathrm{m}}$	Critical electric fieldstrength
ESR_par	1	Equivalent series resistor of N_par paralleled single capacitors in a stack
f_sw	Hz	Switching frequency

f_{resf}	Hz	First filter resonant frequency
H	$\frac{\mathrm{A}}{\mathrm{m}}$	Magnetic field strength
i_{AK}	A	Current from anode to cathode
i_{C}	A	Collector current
i_{D}	A	Drain current
i_{CDG}	A	Displacement current through drain-gate capacitance
i_{CDS}	A	Displacement current through drain-source capacitance
i_{CGS}	A	Displacement current through gate-source capacitance
i_{ch}	A	Channel current
i_{di}	A	Diode current
i_{linkMin}	A	Minimum DC-link current
i_{linkAC}	A	Alternating part of the DC-link current (without DC offset)
i_{D}	A	Drain to source current at device terminals
i_{D1}	A	Drain-source current of the top-side switch Q_1
i_{D2}	A	Drain-source current of the bottom-side switch Q_2
i_{Dsat}	A	Drain to source saturation current
i_{f}	A	Current in the filter capacitor
$\hat{i}_{\mathrm{f}}$	A	Maximum filter current
i_{fw}	A	Forward diode current
i_{G}	A	Gate current
I_{init}	A	Initial DC-link current before any event
i_{link}	A	DC-link current
I_{linkMin}	A	Minimum DC-link current
I_{Load}	A	Load current
I_{nom}	A	Nominal current of a specific device
i_{sn}	A	Current of the snubber path
i_{snMin}	A	Minimum snubber current
i_{r}	A	Reverse diode current
I_{rrm}	A	Maximum reverse-recovery current of a diode

j	$\frac{\mathrm{A}}{\mathrm{m}^2}$	Current density
k	$\frac{\mathrm{J}}{\mathrm{K}}$	Bolzmann constant
K_{aIb}	[A]	Konstant no. a in interval b where $a, b \,\epsilon\, \mathbb{N}$
$K_{\mathrm{p\_}}$	[A]	Konstant related to the particular solution
L_σ	H	Stray inductance
$L_{\sigma\mathrm{Off}}$	H	Parasitic inductance relevant for turn-off
$L_{\sigma\mathrm{On}}$	H	Parasitic inductance relevant for turn-on
l_{ch}	m	Channel length
L_{con}	H	Parasitic inductance of the DC-link-module connection
L_{f}	H	Filter inductor
L_{G}	H	Gate circuit inductance
L_{hb}	H	Parasitic inductance of the halfbridge (lumped)
L_{link}	H	Parasitic inductance of the DC-link capacitor
L_{main}	H	Main DC-link stray inductance consisting of L_{link} and L_{con}
L_{res}	H	Inductance responsible for the resonance together with a capacitance
L_{S}	H	Source inductance
L_{sn}	H	Snubber inductance
L_{snhb}	H	Total inductance in the halfbride and snubber path
M	1	Modulation index
N_{c}	$\frac{1}{\mathrm{m}}$	Density of states in the conduction band
n_{i}	$\frac{1}{\mathrm{cm}^3}$	Intrinisc charge carrier concentration
N_{par}	1	Number of paralleled single capacitors in a stack
N_{v}	$\frac{1}{\mathrm{m}}$	Density of states in the valence band
P_{condDS}	W	Conduction losses of the drain-source path of a switch
P_{condSD}	W	Conduction losses of the source-drain path of a switch
P_{damp}	W	Damping losses
P_{out}	W	Inverter output power
P_{sem}	W	Total semiconductor losses

P_{swOff}	W	Turn-off switching losses
P_{swOn}	W	Turn-on switching losses
P_{swRec}	W	Losses during diode recovery
q	C	Unit electronic charge with $1.6 \cdot 10^{-19}\,\mathrm{C}$
Q_{rr}	C	Reverse recovery charge
R_{σ}	Ω	Resistance part of the current path leading to L_{σ}
R_{a}	Ω	Accumulation layer resistance
R_{ch}	Ω	Channel resistance
R_{d}	Ω	Damping resistance (lumped)
R_{damp}	Ω	Damping resistor (dedicated)
R_{dr}	Ω	Resistance of a drift region
R_{epi}	Ω	Epi-layer resistance
R_{G}	Ω	Gate resistor
R_{Goff}	Ω	Gate resistor for the turn-off event
R_{Gon}	Ω	Gate resistor for the turn-on event
R_{main}	Ω	Lumped resistance in the main DC-link path (DC-link capacitor and connection)
R_{mainSkin}	Ω	Lumped resistance in the DC-link path under the influence of skin and proximity effect
R_{on}	Ω	On-resistance of a MOSFET
R_{onAux}	Ω	On-resistance of the auxiliary MOSFET
R_{onIdeal}	$\Omega\mathrm{cm}^2$	Ideal specific on-resistance of a MOSFET
R_{onSpec}	$\Omega\mathrm{cm}^2$	Specific on-resistance of a MOSFET
R_{sn}	Ω	Resistance in the snubber path
R_{sub}	Ω	Substrate resistance
R_{th}	$\frac{\mathrm{K}}{\mathrm{W}}$	Thermal resistance
R_{thCapSp}	$\frac{\mathrm{K}}{\mathrm{W}}$	Thermal resistance from the center of a capacitor assembly to the solder pads
R_{thSn}	$\frac{\mathrm{K}}{\mathrm{W}}$	Total thermal resistance from capacitor to heat sink of both paralleled snubber capacitors

T_0	s	Period of an undamped oscillation
$t_{2\text{opt}}$	s	Optimal current independent point in time for semiconductor turn-off for a ZCS of Q_{aux}
t_{f12}	s	Fall time of the voltage during turn-on
t_{f23}	s	Fall time of the current during turn-off
t_{rise}	s	Rise time
V_{BD}	V	Breakdown voltage
V_{BDspec}	V	Breakdown voltage for a specific device
V_{C0}	V	Initial capacitor voltage
v_{CE}	V	Collector emitter voltage
v_{Csn}	V	Voltage accross the C_{sn}
V_{DC}	V	DC-link voltage
v_{DG}	V	Drain-gate voltage
V_{diff}	V	Diffusion voltage
v_{dr}	V	Driver output voltage
v_{DS}	V	Drain to source voltage
v_{DSaux}	V	Drain-source voltage of the auxiliary switch Q_{aux}
v_{DS1}	V	Drain-source voltage of the top-side switch Q_1
$\hat{v}_{\text{DS1}}$	V	Peak voltage during turn-off of the top-side switch Q_1
v_{DS2}	V	Drain-source voltage of the bottom-side switch Q_2
$\hat{v}_{\text{DS2}}$	V	Peak voltage during turn-off of the bottom-side switch Q_2
V_{diff}	V	Diffusion voltage
v_{fw}	V	Forward diode voltage
V_{frm}	V	Diode voltage during forward recovery
v_{Gaux}	V	Gate-source voltage of the auxiliary switch Q_{aux}
v_{G1}	V	Gate-source voltage of the top-side switch Q_1
v_{G2}	V	Gate-source voltage of the bottom-side switch Q_2
v_{GS}	V	Gate-source voltage
v_{KA}	V	Voltage from cathode to anode

$\hat{v}_{\mathrm{KA}}$	V	Peak voltage from cathode to anode
v_{Lmain}	V	Voltage accross L_{main} in the common gate-source path
v_{Ls}	V	Voltage accross the stray inductance in the common gate-source path
v_{Lsn}	V	Voltage accross the lumped stray inductance in the snubber path
$\hat{v}_{\mathrm{phase}}$	V	Peak voltage of the sinusoidal inverter output voltage
v_{r}	V	Reverse diode voltage
v_{Rd}	V	Voltage accross R_{d}
v_{Rdamp}	V	Voltage accross R_{damp}
v_{Rmain}	V	Voltage accross the lumped resistance in the main DC-link and connection
v_{Rsn}	V	Voltage accross the resistance in the snubber path
v_{sat}	$\frac{\mathrm{m}}{\mathrm{s}}$	Saturation drift velocity
v_{sn}	V	Snubber capacitor voltage
V_{sn0}	V	Initial snubber capacitor voltage before the corresponding event
V_{snEnd}	V	Snubber voltage at the end of a switching event
V_{snMaxOff}	V	Highest snubber capacitor voltage after charging during turn-off event
V_{snMaxOn}	V	Highest snubber capacitor voltage after charging during turn-on event
V_{snMean}	V	Snubber voltage averaged over multiple continuous switching events
V_{th}	V	Threshold voltage
W	1	Lambert-W-function
w_{b}	m	Base width
w_{ch}	m	Channel width
W_{Coss2}	J	Energy stored output capacitance of the bottom-side switch Q_2
W_{Csn}	J	Energy stored in the snubber capacitance
w_{D}	m	Width of the depletion region

W_{dampAS}	J	Damping energy lost in the active snubber setup
W_{dampDC}	J	Damping energy lost in the DC-snubber setup
W_{dampOff}	J	Damping energy lost during turn-off
W_{dampOn}	J	Damping energy lost during turn-on
W_{DC}	J	Energy provided by the DC-link
W_{g}	eV	Bandgap energy
$W_{\mathrm{L_{main}}}$	J	Energy stored in L_{main}
W_{link}	J	Energy provided by the DC-link capacitor
W_{off}	J	Switching energy lost during turn-off
W_{on}	J	Switching energy lost during turn-on
W_{rec}	J	Switching energy lost during diode recovery
W_{Rd}	J	Energy dissipated in R_{d}

List of Abbreviations

AC alternating current

AS abbreviation for the active snubber setup in this work

ASo abbreviation for the active snubber setup in this work with optimized MOSFETs

DC direct current

DC+ positive potential of the DC-link

DC- pegative potential of the DC-link

DIBL drain-induced-barrier-lowering

DUT device under test

EMI electromagnetic interference

ESL equivalent series inductor

ESR equivalent series resistor

GaN gallium nitride

HB abbreviation for the conventional haldbridge setup in this work

IGBT insulated gate bipolar transistor

MLCC multilayer ceramic capacitor

MOSFET metaloxide-semiconductor field-effect-transitor

PCB printed circuit board

PWM pulse width modulation

RMS root-mean-square

Si silicon

SiC silicon carbide

SN abbreviation for the DC-snubber setup in this work

SNo abbreviation for the DC-snubber setup in this work with optimized MOSFETs

WBM wide-bandgap material

ZVS zero voltage switching

Bibliography

[1] ECPE e.V., José A. Cobus et al., *Electronics enabling efficient energy usage, Results from the E4U project*, https://www.ecpe.org/index.php?eID=dumpFile&t=f&f=3946&token=79bfabb1784188b0cafc2c01d4d743ce84b79e36, Accessed: 28.08.2021, 2009.

[2] ECPE e.V., *What drives power electronics in the new decade*, https://www.ecpe.org/index.php?eID=dumpFile&t=f&f=26631&token=bb1861c762a107cfd1baf330315b1b391b86f7a9, Accessed: 28.08.2021, 2020.

[3] J. Y. Tsao and Chowdhury et al., "Ultrawide-Bandgap Semiconductors: Research Opportunities and Challenges," *Advanced Electronic Materials*, vol. 4, no. 1, p. 1 600 501, 2018. DOI: 10.1002/aelm.201600501.

[4] J. Lutz, H. Schlangenotto, and U. Scheuermann, *Halbleiter-Leistungsbauelemente: Physik, Eigenschaften, Zuverlässigkeit*, 2. Aufl. Berlin: Springer Vieweg, 2012, ISBN: 978-3-642-29795-3.

[5] J. Millán, P. Godignon, X. Perpiñà, A. Pérez-Tomás, and J. Rebollo, "A Survey of Wide Bandgap Power Semiconductor Devices," *IEEE Transactions on Power Electronics*, vol. 29, no. 5, pp. 2155–2163, 2014. DOI: 10.1109/TPEL.2013.2268900.

[6] A. Elasser and T. Chow, "Silicon carbide benefits and advantages for power electronics circuits and systems," *Proceedings of the IEEE*, vol. 90, no. 6, pp. 969–986, 2002. DOI: 10.1109/JPROC.2002.1021562.

[7] P. Vaculik, "The properties of SiC in comparison with Si semiconductor devices," in *2013 International Conference on Applied Electronics*, 2013, pp. 1–4.

[8] H. Abderrazak and E. S. B. Hadj Hmi, "Silicon Carbide: Synthesis and Properties," in *Properties and Applications of Silicon Carbide*, InTech, 2011, pp. 361–388, ISBN: 978-953-307-201-2. DOI: 10.5772/15736.

[9] Kelsey Horowitz, Timothy Remo, and Samantha Reese, *A Manufacturing Cost and Supply Chain Analysis of SiC Power Electronics Applicable to Medium-Voltage Motor Drives: NREL/TP-6A20-67694*, Clean Energy Manufacturing Analysis Center, 15013 Denver West Parkway Golden, CO 80401, Ed., 3.2017.

[10] T. Liu, R. Ning, T. T. Y. Wong, and Z. J. Shen, "Modeling and Analysis of SiC MOSFET Switching Oscillations," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 3, pp. 747–756, 2016. DOI: 10.1109/JESTPE.2016.2587358.

[11] W. Jakobi, A. Uhlemann, M. Thoben, C. Schweikert, C. Strenger, A. P. Pai, L. Beaurenaut, and M. Muenzer, "Benefits of new CoolSiC MOSFET in HybridPACK Drive package for electrical drive train applications.," in *CIPS 2018; 10th International Conference on Integrated Power Electronics Systems*, 2018, pp. 1–9.

[12] Z. Liang, "Integrated double sided cooling packaging of planar SiC power modules," in *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2015, pp. 4907–4912. DOI: 10.1109/ECCE.2015.7310352.

[13] O. Kreutzer, B. Eckardt, and M. Maerz, "Optimum gate driver design to reach SiC-MOSFET's full potential — Speeding up to 200 kV/us," in *2015 IEEE 3rd Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2015, pp. 41–46. DOI: 10.1109/WiPDA.2015.7369313.

[14] Z. Zhang, J. Dix, F. F. Wang, B. J. Blalock, D. Costinett, and L. M. Tolbert, "Intelligent Gate Drive for Fast Switching and Crosstalk Suppression of SiC Devices," *IEEE Transactions on Power Electronics*, vol. 32, no. 12, pp. 9319–9332, 2017. DOI: 10.1109/TPEL.2017.2655496.

[15] J. Kim, D. Shin, and S.-K. Sul, "A Damping Scheme for Switching Ringing of Full SiC MOSFET by Air Core PCB Circuit," *IEEE Transactions on Power Electronics*, vol. 33, no. 6, pp. 4605–4615, 2018. DOI: 10.1109/TPEL.2017.2731861.

[16] M. Joko, A. Goto, M. Hasegawa, S. Miyahara, and H. Murakami, "Snubber circuit to suppress the voltage ringing for SiC device," in *Proceedings of PCIM Europe 2015; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2015, pp. 1–6.

[17] R. Bayerer and D. Domes, "Power circuit design for clean switching," in *2010 6th International Conference on Integrated Power Electronics Systems*, 2010, pp. 1–6.

[18] Cree, "Industry's First Commercial Silicon Carbide Power MOSFET: Destined to Replace Silicon Devices in High Voltage ($\geq$ 1200V) Power Electronics," *Bodo's Power Systems*, no. 2, pp. 16–17, 2011.

[19] D. Domes, R. Bayerer, and A. Herbrandt, "Overall low inductance module concept for maximum system performance," in *2012 15th International Power Electronics and Motion Control Conference (EPE/PEMC)*, 2012, DS1a.10-1-DS1a.10–5. DOI: 10.1109/EPEPEMC.2012.6397200.

[20] H. Wen, W. Xiao, X. Wen, and P. Armstrong, "Analysis and Evaluation of DC-Link Capacitors for High-Power-Density Electric Vehicle Drive Systems," *IEEE Transactions on Vehicular Technology*, vol. 61, no. 7, pp. 2950–2964, 2012. DOI: 10.1109/TVT.2012.2206082.

[21] P. Liutanakul, S. Pierfederici, and F. Meibody-Tabar, "Application of SMC with I/O Feedback Linearization to the Control of the Cascade Controlled-Rectifier/Inverter-Motor Drive System with a Small DC-Link Capacitor," in *2005 IEEE 36th Power Electronics Specialists Conference*, 2005, pp. 922–928. DOI: 10.1109/PESC.2005.1581738.

[22] S. Hain, M.-M. Bakran, C. Jaeger, F.-J. Niedernostheide, D. Domes, and D. Heer, "The effect of different stray inductances on the performance of various types of IGBTs — Is less always better?" In *2015 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe)*, 2015, pp. 1–9. DOI: 10.1109/EPE.2015.7309166.

[23] K. Wada and M. Ando, "Switching Loss Analysis of SiC-MOSFET based on Stray Inductance Scaling," in *2018 International Power Electronics Conference (IPEC-Niigata 2018 -ECCE Asia)*, 2018, pp. 1919–1924. DOI: 10.23919/IPEC.2018.8507986.

[24] E. Persson, "Transient effects in application of PWM inverters to induction motors," *IEEE Transactions on Industry Applications*, vol. 28, no. 5, pp. 1095–1101, 1992. DOI: 10.1109/28.158834.

[25] X. Shancheng and W. Zhengguo, "Characteristic Research of Bearing Currents in Inverter-Motor Drive Systems," in *2006 CES/IEEE 5th International Power Electronics and Motion Control Conference*, vol. 2, 2006, pp. 1–4. DOI: 10.1109/IPEMC.2006.4778146.

[26] A. Moreira, P. Santos, T. Lipo, and G. Venkataramanan, "Filter networks for long cable drives and their influence on motor voltage distribution and common-mode currents," *IEEE Transactions on Industrial Electronics*, vol. 52, no. 2, pp. 515–522, 2005. DOI: 10.1109/TIE.2005.844237.

[27] J.-P. Strom, J. Tyster, J. Korhonen, K. Rauma, H. Saren, and P. Silventoinen, "Active du/dt filtering for variable-speed AC drives," in *2009 13th European Conference on Power Electronics and Applications*, 2009, pp. 1–10.

[28] M. Willander, M. Friesel, Q.-u. Wahab, and B. Straumal, "Silicon carbide and diamond for high temperature device applications," *Journal of Materials Science: Materials in Electronics*, vol. 17, no. 1, pp. 1–25, 2006. DOI: 10.1007/s10854-005-5137-4.

[29] J. Hudgins, G. Simin, E. Santi, and M. Khan, "An assessment of wide bandgap semiconductors for power devices," *IEEE Transactions on Power Electronics*, vol. 18, no. 3, pp. 907–914, 2003. DOI: 10.1109/TPEL.2003.810840.

[30] S. M. Sze and K. K. Ng, *Physics of semiconductor devices*, 3. ed. Hoboken, NJ: Wiley-Interscience, 2007, ISBN: 978-0-471-14323-9.

[31] Y. Iwahashi, M. Miyazato, M. Miyajima, Y. Yonezawa, T. Kato, H. Fujiwara, K. Hamada, A. Otsuki, and H. Okumura, "Extension of Stacking Faults in 4H-SiC pn Diodes under a High Current Pulse Stress," *Materials Science Forum*, vol. 897, pp. 218–221, 2017. DOI: 10.4028/www.scientific.net/MSF.897.218.

[32] H. Benda and E. Spenke, "Reverse recovery processes in silicon power rectifiers," *Proceedings of the IEEE*, vol. 55, no. 8, pp. 1331–1354, 1967. DOI: 10.1109/PROC.1967.5834.

[33] G. Sozzi, M. Puzzanghera, G. Chiorboli, and R. Nipoti, "OCVD Lifetime Measurements on 4H-SiC Bipolar Planar Diodes: Dependences on Carrier Injection and Diode Area," *IEEE Transactions on Electron Devices*, vol. 64, no. 6, pp. 2572–2578, 2017. DOI: 10.1109/TED.2017.2691280.

[34] S. Oussalah and R. Jerisian, "Carrier lifetime recombination measurement by conductivity modulation for power p-i-n diode," in *Proceedings 1999 IEEE Hong Kong Electron Devices Meeting (Cat. No.99TH8458)*, 1999, pp. 106–109. DOI: 10.1109/HKEDM.1999.836419.

[35] S. Chowdhury, C. Hitchcock, R. P. Dahal, I. B. Bhat, and T. P. Chow, "Effect of carrier lifetime enhancement on the performance of ultra-high voltage 4H-SiC PiN diodes," in *2016 Lester Eastman Conference (LEC)*, 2016, pp. 23–26. DOI: 10.1109/LEC.2016.7578925.

[36] S. Ogata, Y. Miyanagi, K. Nakayama, A. Tanaka, and K. Asano, "5kV class 4H-SiC PiN diode with low voltage overshoot during forward recovery for high frequency inverter," in *2011 IEEE 23rd International Symposium on Power Semiconductor Devices and ICs*, 2011, pp. 296–299. DOI: 10.1109/ISPSD.2011.5890849.

[37] S. Rugen, C. Bödeker, I. Kortazar, I. Larrazabal, P. Friedrichs, and N. Kaminski, "Investigation of the turn-on behaviour of silicon pin-diodes and SiC-Schottky-diodes and its impact on the anti-parallel IGBT," in *2016 18th European Conference on Power Electronics and Applications (EPE'16 ECCE Europe)*, 2016, pp. 1–9. DOI: 10.1109/EPE.2016.7695461.

[38] Yamazaki, Kobayashi, and Shinohara, "Forward transient behavior of PiN and super junction diodes," in *2004 Proceedings of the 16th International Symposium on Power Semiconductor Devices and ICs*, 2004, pp. 197–200. DOI: 10.1109/WCT.2004.239905.

[39] B. J. Baliga, *Gallium nitride and silicon carbide power devices*. New Jersey et al.: World Scientific, 2017, ISBN: 978-981-3109-40-7.

[40] D. Martin, P. Killeen, W. A. Curbow, B. Sparkman, L. E. Kegley, and T. McNutt, "Comparing the switching performance of SiC MOSFET intrinsic body diode to additional SiC schottky diodes in SiC power modules," in *2016 IEEE 4th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2016, pp. 242–246. DOI: 10.1109/WiPDA.2016.7799946.

[41] T. Kimoto, A. Iijima, H. Tsuchida, T. Miyazawa, T. Tawara, A. Otsuki, T. Kato, and Y. Yonezawa, "Understanding and reduction of degradation phenomena in SiC power devices," in *2017 IEEE International Reliability Physics Symposium (IRPS)*, 2017, 2A-1.1-2A–1.7. DOI: 10.1109/IRPS.2017.7936253.

[42] T. Ishigaki, T. Murata, K. Kinoshita, T. Morikawa, T. Oda, R. Fujita, K. Konishi, Y. Mori, and A. Shima, "Analysis of Degradation Phenomena in Bipolar Degradation Screening Process for SiC-MOSFETs," in *2019 31st International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 2019, pp. 259–262. DOI: 10.1109/ISPSD.2019.8757598.

[43] B. J. Baliga, *Fundamentals of Power Semiconductor Devices*. Heidelberg: Springer-Verlag, 2008, ISBN: 978-0387473130.

[44] Baliga, B. Jayant, *Fundamentals of Power Semiconductor Devices*. Cham: Springer International Publishing, 2019, ISBN: 978-3-319-93988-9.

[45] T. Basler, D. Heer, D. Peters, T. Aichinger, and R. Schoerner, "Practical Aspects and Body Diode Robustness of a 1200 V SiC Trench MOSFET," in *PCIM Europe 2018; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2018, pp. 1–7.

[46] T. Dutta, Q. Rafhay, G. Pananakakis, and G. Ghibaudo, "Modeling of the impact of source/drain regions on short channel effects in MOSFETs," in *2013 14th International Conference on Ultimate Integration on Silicon (ULIS)*, 2013, pp. 69–72. DOI: 10.1109/ULIS.2013.6523493.

[47] H. Sun, K. B. Lee, L. Yuan, W. Wang, S. L. Selvaraj, and G.-Q. Lo, "Theoretical study of short channel effect in highly scaled GaN HEMTs," in *2012 IEEE International Symposium on Radio-Frequency Integration Technology (RFIT)*, 2012, pp. 204–206. DOI: 10.1109/RFIT.2012.6401661.

[48] D. D. Bahler, H. A. Owen, and T. G. Wilson, "Predicting performance of power converters operating with switching frequencies in the vicinity of 100 kHz," in *1978 IEEE Power Electronics Specialists Conference*, 1978, pp. 148–157. DOI: 10.1109/PESC.1978.7072347.

[49] T. H. Sloane, H. A. Owen, and T. G. Wilson, "Switching transients in high-frequency high-power converters using power MOSFET'S," in *1979 IEEE Power Electronics Specialists Conference*, 1979, pp. 244–255. DOI: 10.1109/PESC.1979.7081033.

[50] P. Yi, Y. Cui, A. Vang, and L. Wei, "Investigation and evaluation of high power SiC MOSFETs switching performance and overshoot voltage," in *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2018, pp. 2589–2592. DOI: 10.1109/APEC.2018.8341382.

[51] Zheng Chen, "Electrical Integration of SiC Power Devices for High-Power-Density Applications," Ph.D. Virginia Polytechnic Institute and State University, 2013.

[52] G. Lehner and G. N. Lehner, *Elektromagnetische Feldtheorie: Für Ingenieure und Physiker*. Berlin/Heidelberg: Springer Berlin Heidelberg, 2010, ISBN: 978-3-642-13041-0.

[53] J. C. Maxwell, *A Treatise on Electricity and Magnetism: Volume 2*, ser. Cambridge library collection. Physical Sciences. Cambridge and Place of publication not identified: Cambridge University Press and publisher not identified, 1873, ISBN: 9780511709340.

[54] Rayleigh, "LII. On the self-induction and resistance of straight conductors," *The London, Edinburgh, and Dublin Philosophical Magazine and Journal of Science*, vol. 21, no. 132, pp. 381–394, 1886.

[55] S. Ramo, J. R. Whinnery, and T. van Duzer, *Fields and waves in communication electronics*. New York: Wiley, 1965, ISBN: 9780471707202.

[56] W.-K. Chen, *The electrical engineering handbook*. Amsterdam: Elsevier Acad. Press, 2005, ISBN: 9780121709600.

[57] C. R. Paul, *Analysis of multiconductor transmission lines*. Hoboken, New Jersey and Piscataway, New Jersey: Wiley-Interscience IEEE Press and IEEE Xplore, 2007, ISBN: 978-0-470-13154-1.

[58] A. Cangellaris, J. Prince, and L. Vakanas, "Frequency-dependent inductance and resistance calculation for three-dimensional structures in high-speed interconnect systems," *IEEE Transactions on Components, Hybrids, and Manufacturing Technology*, vol. 13, no. 1, pp. 154–159, 1990. DOI: 10.1109/33.52864.

[59] B. Gutsmann, P. Mourick, and D. Silber, "Exact inductive parasitic extraction for analysis of IGBT parallel switching including DCB-backside eddy currents," in *2000 IEEE 31st Annual Power Electronics Specialists Conference. Conference Proceedings (Cat. No.00CH37018)*, vol. 3, 2000, 1291–1295 vol.3. DOI: 10.1109/PESC.2000.880496.

[60] A. D. Callegaro, J. Guo, M. Eull, B. Danen, J. Gibson, M. Preindl, B. Bilgin, and A. Emadi, "Bus Bar Design for High-Power Inverters," *IEEE Transactions on Power Electronics*, vol. 33, no. 3, pp. 2354–2367, 2018. DOI: 10.1109/TPEL.2017.2691668.

[61] Bernd Gutsmann, "Charakterisierung und Einfluß parasitärer elektromagnetischer Effekte in leistungselektronischen Systemen," Ph.D. Universität Bremen, 2007.

[62] Z. Lounis, I. Rasoanarivo, and B. Davat, "Minimization of wiring inductance in high power IGBT inverter," *IEEE Transactions on Power Delivery*, vol. 15, no. 2, pp. 551–555, 2000. DOI: 10.1109/61.852983.

[63] R. W. Maier and M.-M. Bakran, "Optimal Hard Switching as Benchmark for SiC MOSFET Switching Losses with limited du/dt and blocking voltage," in *2019 21st European Conference on Power Electronics and Applications (EPE '19 ECCE Europe)*, 2019, P.1–P.10. DOI: 10.23919/EPE.2019.8915209.

[64] K. Klein, E. Hoene, and K.-D. Lang, "Packages for Fast Switching HV GaN Power Devices," in *PCIM Europe 2014; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2014, pp. 1–8.

[65] P. Beckedahl, M. Spang, and O. Tamm, "Breakthrough into the third dimension - Sintered multi layer flex for ultra low inductance power modules," in *CIPS 2014; 8th International Conference on Integrated Power Electronics Systems*, 2014, pp. 1–5.

[66] Robert W. Maier, Mark-M. Bakran, "Switching SiC MOSFETs Under Conditions of a High Power Module," in *2018 20th European Conference on Power Electronics and Applications (EPE'18 ECCE Europe)*.

[67] E. Hoene, A. Ostmann, and C. Marczok, "Packaging Very Fast Switching Semiconductors," in *CIPS 2014; 8th International Conference on Integrated Power Electronics Systems*, 2014, pp. 1–7.

[68] M. Meisser, D. Hamilton, and P. Mawby, "DCB-based low-inductive SiC modules for high frequency operation," in *CIPS 2014; 8th International Conference on Integrated Power Electronics Systems*, 2014, pp. 1–10.

[69] C. Neeb, J. Teichrib, R. W. De Doncker, L. Boettcher, and A. Ostmann, "A 50 kW IGBT power module for automotive applications with extremely low DC-link inductance," in *2014 16th European Conference on Power Electronics and Applications*, 2014, pp. 1–10. DOI: 10.1109/EPE.2014.6910953.

[70] K. Takao and S. Kyogoku, "Ultra low inductance power module for fast switching SiC power devices," in *2015 IEEE 27th International Symposium on Power Semiconductor Devices IC's (ISPSD)*, 2015, pp. 313–316. DOI: 10.1109/ISPSD.2015.7123452.

[71] C. R. Mueller and R. Bayerer, "Low-inductive inverter concept by 200 A / 1200 V half bridge in an EasyPACK 2B - following strip-line design," in *CIPS 2014; 8th International Conference on Integrated Power Electronics Systems*, 2014, pp. 1–6.

[72] N. R. Mehrabadi, I. Cvetkovic, J. Wang, R. Burgos, and D. Boroyevich, "Busbar design for SiC-based H-bridge PEBB using 1.7 kV, 400 a SiC MOSFETs operating at 100 kHz," in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2016, pp. 1–7. DOI: 10.1109/ECCE.2016.7854903.

[73] S. Tiwari, O.-M. Midtgård, and T. M. Undeland, "Design of low inductive busbar for fast switching SiC modules verified by 3D FEM calculations and laboratory measurements," in *2016 IEEE 17th Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2016, pp. 1–8. DOI: 10.1109/COMPEL.2016.7556689.

[74] P. Nayak and K. Hatua, "Parasitic Inductance and Capacitance-Assisted Active Gate Driving Technique to Minimize Switching Loss of SiC MOSFET," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 10, pp. 8288–8298, 2017. DOI: 10.1109/TIE.2017.2711512.

[75] T. Wu, M. Bellar, A. Tchamdjou, J. Mahdavi, and M. Ehsani, "A review of soft-switched DC-AC converters," in *IAS '96. Conference Record of the 1996 IEEE Industry Applications Conference Thirty-First IAS Annual Meeting*, vol. 2, 1996, 1133–1144 vol.2. DOI: 10.1109/IAS.1996.560222.

[76] V. Agelidis, P. Ziogas, and G. Joos, "An optimum modulation strategy for a novel notch commutated 3- phi PWM inverter," in *Conference Record of the 1991 IEEE Industry Applications Society Annual Meeting*, 1991, 809–818 vol.1. DOI: 10.1109/IAS.1991.178332.

[77] H. Ohashi, "Snubber Circuit for High-Power Gate Turn-Off Thyristors," *IEEE Transactions on Industry Applications*, vol. IA-19, no. 4, pp. 655–664, 1983. DOI: 10.1109/TIA.1983.4504269.

[78] M. Ebli, M. Engel, and M. Pfost, "An Experimental Study of a Zero Voltage Switching SiC Boost Converter with an Active Snubber Network," in *Proceedings of PCIM Europe 2015; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2015, pp. 1–7.

[79] NXP, *AN11160: Designing RC Snubbers: Rev.1 25.April 2012*.

[80] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power electronics: Converters, applications, and design*, 3. Hoboken, NJ: Wiley, 2007, ISBN: 978-0-471-22693-2.

[81] A. Petterteig, J. Lode, and T. Undeland, "IGBT turn-off losses for hard switching and with capacitive snubbers," in *Conference Record of the 1991 IEEE Industry Applications Society Annual Meeting*, 1991, 1501–1507 vol.2. DOI: 10.1109/IAS.1991.178059.

[82] D. Dimos, S. Lockwood, R. Schwartz, and M. Rodgers, "Thin-film decoupling capacitors for multichip modules," *IEEE Transactions on Components, Packaging, and Manufacturing Technology: Part A*, vol. 18, no. 1, pp. 174–179, 1995. DOI: 10.1109/95.370752.

[83] L. Li, P. Ning, Z. Duan, D. Zhang, and X. Wen, "A study on the effect of DC-link decoupling capacitors," in *2017 IEEE Transportation Electrification Conference and Expo, Asia-Pacific (ITEC Asia-Pacific)*, 2017, pp. 1–5. DOI: 10.1109/ITEC-AP.2017.8080909.

[84] L. Qiao, X. Yang, Y. Ren, F. Zhang, L. Wang, X. Ma, and S. Zhang, "Performance of a 1.2kV, 288A full-SiC MOSFET module based on low inductance packaging layout," in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2017, pp. 3038–3042. DOI: 10.1109/APEC.2017.7931129.

[85] M. Liang, Y. Li, Q. Chen, Y. Lu, H. Yu, T. Q. Zheng, H. Guo, and F. Zhao, "Research on an improved DC-side snubber for suppressing the turn-off overvoltage and oscillation in high speed SiC MOSFET application," in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2017, pp. 1358–1365. DOI: 10.1109/ECCE.2017.8095948.

[86] Z. Chen, Y. Yao, D. Boroyevich, K. Ngo, and P. Mattavelli, "Exploration of a switching loop snubber for parasitic ringing suppression," in *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2014, pp. 1605–1612. DOI: 10.1109/ECCE.2014.6953610.

[87] J. Chen, "Design optimal built-in snubber in trench field plate power MOSFET for superior EMI and efficiency performance," in *2015 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)*, 2015, pp. 459–462. DOI: 10.1109/SISPAD.2015.7292361.

[88] B. N. Torsæter, S. Tiwari, R. Lund, and O.-M. Midtgård, "Experimental evaluation of switching characteristics, switching losses and snubber design for a full SiC half-bridge power module," in *2016 IEEE 7th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, 2016, pp. 1–8. DOI: 10.1109/PEDG.2016.7527071.

[89] H. S. Shin, H. A. Huynh, and S. Kim, "Design and optimization of inductive snubber for DC-DC converter," in *2017 Asia-Pacific International Symposium on Electromagnetic Compatibility (APEMC)*, 2017, pp. 148–150. DOI: 10.1109/APEMC.2017.7975448.

[90] H. Sugimura, H. Tanimatsu, H. Muraoka, M. Nakaoka, and H.-W. Lee, "Lossless inductive snubber-assisted soft switching PFM series resonant high frequency inverter for electromagnetic induction eddy current-heated fixing roller," in *The 4th International Power Electronics and Motion Control Conference, 2004. IPEMC 2004.*, vol. 1, 2004, 138–143 Vol.1.

[91] Q. Liu, S. Wang, A. C. Baisden, F. Wang, and D. Boroyevich, "EMI Suppression in Voltage Source Converters by Utilizing dc-link Decoupling Capacitors," *IEEE Transactions on Power Electronics*, vol. 22, no. 4, pp. 1417–1428, 2007. DOI: 10.1109/TPEL.2007.900593.

[92] S. Wang, F. Lee, W. Odendaal, and J. van Wyk, "Improvement of EMI filter performance with parasitic coupling cancellation," *IEEE Transactions on Power Electronics*, vol. 20, no. 5, pp. 1221–1228, 2005. DOI: 10.1109/TPEL.2005.854069.

[93] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power electronics: Converters, applications, and design*, 2. ed. New York: Wiley, 1995, ISBN: 0-471-58408-8.

[94] Michael Schlüter, Andre Uhlemann, "Snubber circuit and power semiconductor module with snubber circuit," EU Patent EP3761492A1, Jan. 2021.

[95] L. Yang, K. Li, J. Dai, M. Corfield, A. Harris, K. Paciura, J. O'Brien, and C. M. Johnson, "Electrical Performance and Reliability Characterization of a SiC MOSFET Power Module With Embedded Decoupling Capacitors," *IEEE Transactions on Power Electronics*, vol. 33, no. 12, pp. 10 594–10 601, 2018. DOI: 10.1109/TPEL.2018.2809923.

[96] R. T. Naayagi, R. Shuttleworth, and A. J. Forsyth, "Investigating the effect of snubber capacitor on high power IGBT turn-off," in *2011 1st International Conference on Electrical Energy Systems*, 2011, pp. 50–55. DOI: 10.1109/ICEES.2011.5725301.

[97] H. Wang and F. Blaabjerg, "Reliability of Capacitors for DC-Link Applications in Power Electronic Converters—An Overview," *IEEE Transactions on Industry Applications*, vol. 50, no. 5, pp. 3569–3578, 2014. DOI: 10.1109/TIA.2014.2308357.

[98] TDK Electronics AG, *Ceralink Datasheet: Low Profile*, 7.01.2019.

[99] KEMET Electronics Corporation, *KC-Link Datasheet*, 25.09.2019.

[100] M. Huh, K. H. Cho, H.-D. Nam, and H. Y. Lee, "Degradation behavior of Ca-doped barium titanate ceramic capacitors," in *Proceedings of 1994 IEEE International Symposium on Applications of Ferroelectrics*, 1994, pp. 572–576. DOI: 10.1109/ISAF.1994.522433.

[101] D. D. Liu, "Insulation Resistance Degradation in Ni–BaTiO₃ Multilayer Ceramic Capacitors," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 5, no. 1, pp. 40–48, 2015. DOI: 10.1109/TCPMT.2014.2374576.

[102] W. Jiang, Y. Hu, S. Bao, S. Lijie, Z. Yuwei, Y. Cui, and L. Qiang, "Analysis on the causes of decline of MLCC insulation resistance," in *2015 16th International Conference on Electronic Packaging Technology (ICEPT)*, 2015, pp. 1255–1257. DOI: 10.1109/ICEPT.2015.7236807.

[103] M.-J. Pan and C. A. Randall, "A brief introduction to ceramic capacitors," *IEEE Electrical Insulation Magazine*, vol. 26, no. 3, pp. 44–50, 2010. DOI: 10.1109/MEI.2010.5482787.

[104] Alexander Teverovsky. "Guidelines for Selection, Screening and Qualification of Low-Voltage Commercial Multilayer Ceramic Capacitors for Space Programs: Rev. A." (2012), [Online]. Available: https://nepp.nasa.gov/files/23923/Guidelines%20for%20selection%20of%20MLCCs%20rev.A.pdf.

[105] A. J. Moulson and J. M. Herbert, *Electroceramics: Materials, properties, applications*. London: Chapman and Hall, 1990, ISBN: 0412294907.

[106] J. Rossi, L. Silva Neto, and A. Silva, "Study of HV dielectric ceramics for applications in compact pulsed power," in *2011 IEEE Pulsed Power Conference*, 2011, pp. 459–464. DOI: 10.1109/PPC.2011.6191465.

[107] R. Xu, Y. Feng, X. Wei, and Z. Xu, "Analysis on nonlinearity of antiferroelectric multilayer ceramic capacitor (MLCC) for energy storage," *IEEE Transactions on Dielectrics and Electrical Insulation*, vol. 26, no. 6, pp. 2005–2011, 2019. DOI: 10.1109/TDEI.2019.008301.

[108] H. Patel, L. Levesque, H. Morales, and L. Dunleavy, "Addressing performance differences in horizontal and vertical orientation mounting of multi-layer capacitors," in *2017 IEEE 18th Wireless and Microwave Technology Conference (WAMICON)*, 2017, pp. 1–3. DOI: 10.1109/WAMICON.2017.7930261.

[109] A. Alqudsi, I. Costanzo, A. Mavretic, and R. Ludwig, "Developing a High-Power Multilayer Ceramic Capacitor Qualification Test Setup for RF Subsystems," *IEEE Transactions on Instrumentation and Measurement*, vol. 68, no. 9, pp. 3396–3404, 2019. DOI: 10.1109/TIM.2018.2874559.

[110] H. Nagasaki, P.-Y. Huang, and T. Shimizu, "Characterization of power capacitors under practical current condition using capacitor loss analyzer," in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2016, pp. 1–7. DOI: 10.1109/ECCE.2016.7854912.

[111] S. Coday, C. B. Barth, and R. C. Pilawa-Podgurski, "Characterization and Modeling of Ceramic Capacitor Losses under Large Signal Operating Conditions," in *2018 IEEE 19th Workshop on Control and Modeling for Power Electronics (COMPEL)*, IEEE, 25.06.2018 - 28.06.2018, pp. 1–8, ISBN: 978-1-5386-5541-2.

[112] L. Dai, F. Lin, Z. Zhu, and J. Li, "Electrical characteristics of high energy density multilayer ceramic capacitor for pulse power application," *IEEE Transactions on Magnetics*, vol. 41, no. 1, pp. 281–284, 2005. DOI: 10.1109/TMAG.2004.839281.

[113] C. Wei, W. Xiaogang, L. Bin, S. Wenyu, L. Qingfeng, and C. Shoutian, "Dielectric loss of BaTiO/sub 3/-based high voltage ceramic capacitor under high field strength," in *Proceedings of 1998 International Symposium on Electrical Insulating Materials. 1998 Asian International Conference on Dielectrics and Electrical Insulation. 30th Symposium on Electrical Insulating Materials (IEEE Cat. No.98TH8286)*, Inst. Electr. Eng. Japan, 27-30 Sept. 1998, pp. 121–122, ISBN: 4-88686-050-8.

[114] H.-J. Ye, X.-S. Qian, J. Lu, H. Gu, S. Zhang, Q. M. Zhang, D.-Y. Jeong, W.-Z. Shao, and L. Zhen, "Dielectric and electrocaloric responses of $Ba(Zr_{0.2}Ti_{0.8})O_3$ bulk ceramics and thick films with sintering aids," *IEEE Transactions on Dielectrics and Electrical Insulation*, vol. 22, no. 3, pp. 1501–1505, 2015. DOI: 10.1109/TDEI.2015.7116344.

[115] S. Haishan and C. Shoutian, "Charge-discharge breakdown of dielectric ceramic," in *Proceedings of the 6th International Conference on Properties and Applications of Dielectric Materials (Cat. No.00CH36347)*, vol. 2, 2000, 1029–1032 vol.2. DOI: 10.1109/ICPADM.2000.876408.

[116] Michael Schlüter, "Semiconductor module arrangement and method for operating the same," EU Patent EP3772180A1, Feb. 2021.

[117] M. Schlüter, A. Uhlemann, and M. Pfost, "A Medium Power SiC Module with Integrated Active Snubber for Lowest Switching Losses," in *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2020, pp. 1496–1500. DOI: 10.1109/APEC39645.2020.9124178.

[118] M. Schlüter and M. Pfost, "A Comprehensive Analytical Description of the Asymmetric Active Snubber," *IET Power Electronics*, vol. 16, no. 1, pp. 102–117, 2023. DOI: 10.1049/pel2.12367.

[119] X. Hou, D. Boroyevich, and R. Burgos, "Characterization on latest-generation SiC MOSFET's body diode," in *2016 IEEE 4th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2016, pp. 247–252. DOI: 10.1109/WiPDA.2016.7799947.

[120] K. Peng, S. Eskandari, and E. Santi, "Characterization and modeling of SiC MOSFET body diode," in *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2016, pp. 2127–2135. DOI: 10.1109/APEC.2016.7468161.

[121] R. Horff, A. Maerz, and M.-M. Bakran, "Analysis of Reverse-Recovery Behaviour of SiC MOSFET Body-Diode - regarding Dead-Time," in *Proceedings of PCIM Europe 2015; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2015, pp. 1–8.

[122] Z. Wang, J. Ouyang, J. Zhang, X. Wu, and K. Sheng, "Analysis on reverse recovery characteristic of SiC MOSFET intrinsic diode," in *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2014, pp. 2832–2837. DOI: 10.1109/ECCE.2014.6953782.

[123] P. Hofstetter, R. W. Maier, and M.-M. Bakran, "Parasitic Turn-On of SiC MOSFETs – Turning a Bug into a Feature," in *PCIM Europe digital days 2020; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2020, pp. 1–7.

[124] P. Sochor, A. Huerner, M. Hell, and R. Elpelt, "Understanding the Turn-off Behavior of SiC MOSFET Body Diodes in Fast Switching Applications," in *PCIM Europe digital days 2021; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2021, pp. 1–8.

[125] Bob Orwiler, *Oscilloscope Vertical Amplifiers / Vertical Amplifier Cirtics (Circuit Concepts Series)*, 1st Edition. Tektronix, Inc., ASIN: B0968WYK2P, 1969.

[126] Infineon Technologies AG, *Datasheet FF6MR12W2M1P_B11: V2.0*, 2019.

[127] S. Jahdi, O. Alatise, R. Bonyadi, P. Alexakis, C. A. Fisher, J. A. O. Gonzalez, L. Ran, and P. Mawby, "An Analysis of the Switching Performance and Robustness of Power MOSFETs Body Diodes: A Technology Evaluation," *IEEE Transactions on Power Electronics*, vol. 30, no. 5, pp. 2383–2394, 2015. DOI: 10.1109/TPEL.2014.2338792.

[128] IEC, *Semiconductor devices - Discrete devices: Part 8: Field-effect transistors*, Standard, Berlin, 2010-12.

[129] D. P. Hamilton, M. R. Jennings, A. Pérez-Tomás, S. A. O. Russell, S. A. Hindmarsh, C. A. Fisher, and P. A. Mawby, "High-Temperature Electrical and Thermal Aging Performance and Application Considerations for SiC Power DMOSFETs," *IEEE Transactions on Power Electronics*, vol. 32, no. 10, pp. 7967–7979, 2017. DOI: 10.1109/TPEL.2016.2636743.

[130] S. Pyo and K. Sheng, "Junction temperature dynamics of power MOSFET and SiC diode," in *2009 IEEE 6th International Power Electronics and Motion Control Conference*, 2009, pp. 269–273. DOI: 10.1109/IPEMC.2009.5157397.

[131] K. Fujisaki, M. Sakai, and S. Takeda, "Motor loss increment of induction motor driven by PWM inverter in comparison with inverter circuit loss," in *2012 15th International Conference on Electrical Machines and Systems (ICEMS)*, 2012, pp. 1–6.

[132] R. Maier and M.-M. Bakran, "SiC Effect on Surge Voltage Distribution in Large Electrical Machines," in *PCIM Europe 2018; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2018, pp. 1–7.

[133] P. Finlayson, "Output filters for PWM drives with induction motors," *IEEE Industry Applications Magazine*, vol. 4, no. 1, pp. 46–52, 1998. DOI: 10.1109/2943.644886.

[134] T. Habetler, R. Naik, and T. Nondahl, "Design and implementation of an inverter output LC filter used for dv/dt reduction," *IEEE Transactions on Power Electronics*, vol. 17, no. 3, pp. 327–331, 2002. DOI: 10.1109/TPEL.2002.1004240.

[135] J. Tyster, J.-P. Ström, J. Korhonen, and P. Silventoinen, "Efficiency measurements on active du/dt output filtering," in *Proceedings of the 2011 14th European Conference on Power Electronics and Applications*, 2011, pp. 1–8.

[136] M. Schlueter and M. Pfost, "Operating a du/dt Filter with a SiC Halfbridge Module and Integrated Active Snubber," in *CIPS 2020; 11th International Conference on Integrated Power Electronics Systems*, 2020, pp. 1–5.

[137] J.-P. Ström, J. Tyster, J. Korhonen, M. Purhonen, and P. Silventoinen, "Active du/dt filter dimensioning in variable speed AC drives," in *Proceedings of the 2011 14th European Conference on Power Electronics and Applications*, 2011, pp. 1–7.

[138] J. Korhonen, J.-P. Ström, J. Tyster, P. Silventoinen, H. Sarén, and K. Rauma, "Control of an inverter output active du/dt filtering method," in *2009 35th Annual Conference of IEEE Industrial Electronics*, 2009, pp. 316–321. DOI: 10.1109/IECON.2009.5414941.

[139] Infineon Technologies AG, *Datasheet FS380R12A6T4B: V3.0*, 2019.

[140] TDK/EPCOS, *Film capacitors – Power electronic capacitors: PCC series for HEV application: B25655P9127K151*, Application note.

[141] T. Kimoto and J. A. Cooper, *Fundamentals of Silicon Carbide Technology*. Singapore: John Wiley & Sons Singapore Pte. Ltd, 2014, ISBN: 9781118313534.

[142] C. Persson, U. Lindefelt, and B. E. Sernelius, "Band gap narrowing in n -type and p -type 3C-, 2H-, 4H-, 6H-SiC, and Si," *Journal of Applied Physics*, vol. 86, no. 8, pp. 4419–4427, 1999.

[143] M. Ruff, H. Mitlehner, and R. Helbig, "SiC devices: physics and numerical simulation," *IEEE Transactions on Electron Devices*, vol. 41, no. 6, pp. 1040–1054, 1994.

[144] M. A. Green, "Intrinsic concentration, effective densities of states, and effective mass in silicon," *Solid-State Electronics*, vol. 67, no. 6, pp. 2944–2954, 1990.

[145] N. T. Son, W. M. Chen, O. Kordina, A. O. Konstantinov, B. Monemar, E. Janzén, D. M. Hofman, D. Volm, M. Drechsler, and B. K. Meyer, "Electron effective masses in 4H SiC," *Applied Physics Letters*, vol. 66, no. 9, pp. 1074–1076, 1995.

[146] C. Persson and U. Lindefelt, "Relativistic band structure calculation of cubic and hexagonal SiC polytypes," *Journal of Applied Physics*, vol. 82, no. 11, pp. 5496–5508, 1997.

[147] A. Sewergin, A. Stippich, and A. H. W. R. W. De Doncker, "Comparison of High Performance Cooling Concepts for SiC Power Modules," in *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2019, pp. 2822–2825. DOI: 10.1109/APEC.2019.8722147.

[148] B. McPherson, B. McGee, D. Simco, K. Olejniczak, and B. Passmore, "Direct liquid cooling of high performance Silicon Carbide (SiC) power modules," in *2017 IEEE International Workshop On Integrated Power Packaging (IWIPP)*, 2017, pp. 1–5. DOI: 10.1109/IWIPP.2017.7936760.

[149] D. Schweitzer and L. Chen, "Heat spreading revisited – effective heat spreading angle," in *2015 31st Thermal Measurement, Modeling Management Symposium (SEMI-THERM)*, 2015, pp. 88–94. DOI: 10.1109/SEMI-THERM.2015.7100145.

[150] G. Brechmann, *Elektronik-Tabellen Betriebs- und Automatisierungstechnik*, 1. Aufl., Dr. 6. Braunschweig: Westermann, 2010, ISBN: 978-3-14-235035-6.

[151] Curamik, *Datasheet curamik CERAMIC SUBSTRATES: Version 1.19 en*, 2019.

[152] Electrolube, Ed., *Datasheet HTCP: Heat Transfer Compound Plus*, 2013.

[153] Ondřej Jankovský et. al., "Towards highly efficient thermoelectrics: Ca3Co4O9 · n CaZrO3 composite," *Ceramics-Silikáty*, no. 58, pp. 106–110, 2014.

[154] KEMET Electronics Corporation, Ed., *KC-LINK™ with KONNEKT™ Technology for High-Efficiency: Commercial & Automotive Grade*, Application note, 14.10.2020.

[155] A. Wintrich, U. Nicolai, W. Tursky, and T. Reimann, *Application manual power semiconductors*, 2nd revised edition. Ilmenau: ISLE Verlag, 2015, ISBN: 978-3-938843-83-3.

[156] R. Bayerer and S. R. Suleri, "Low impedance gate drive for full control of voltage controlled power devices," in *2014 IEEE 26th International Symposium on Power Semiconductor Devices IC's (ISPSD)*, 2014, pp. 438–441. DOI: 10.1109/ISPSD.2014.6856070.

[157] A. März, T. Bertelshofer, M. Helsper, and M.-M. Bakran, "Comparison of SiC MOSFET gate-drive concepts to suppress parasitic turn-on in low inductance power modules," in *2017 19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe)*, 2017, P.1–P.10. DOI: 10.23919/EPE17ECCEEurope.2017.8099044.

[158] P. Vaculík, "Application note for the construction of SiC medium power converter with high switching frequency," in *Proceedings of the 2014 15th International Scientific Conference on Electric Power Engineering (EPE)*, 2014, pp. 563–568. DOI: 10.1109/EPE.2014.6839455.

List of own Publications

Publications

1. M. Schlüter, A. Uhlemann, and M. Pfost, "A medium power SiC module with integrated active snubber for lowest switching losses", in 2020 IEEE Applied Power Electronics Conference and Exposition (APEC), 2020, pp. 1496-1500.
2. M. Schlueter and M.Pfost, "Operating a du/dt filter with a SiC halfbridge module and integrated active Snubber", in CIPS 2020; 11th International Conference on Intregrated Power Electronics Systems, 2020, pp. 1-5.
3. M. Schlüter and M. Pfost, "A comprehensive analytical description of the asymmetric active snubber", IET Power Electronics, submitted to.

Patent Applications

1. M. Schlüter, A. Uhlemann "Snubber circuit and power semiconductor module with snubber circuit",

Patent number	Published	Filed	Granted	Application number
EP 3761492 B1	06.01.2021	05.07.2019	04.01.2023	EP 19184691 A
CN 112188730 A	05.01.2021	29.06.2020		CN 202010606317 A
US 11631974 B2	07.01.2021	02.07.2020	18.04.2023	US 202016919518 A

2. M. Schlüter, "Semiconductor module arrangement and method for operating the same",

Patent number	Published	Filed	Granted	Application number
EP 3772180 A1	03.02.2021	30.07.2019		EP 19188978 A
US 11398768 B2	04.02.2021	17.07.2020	26.07.2022	US 202016931865 A
CN 112332635 A	05.02.2021	28.07.2020		CN 202010736763 A
KR 20210015690 A	03.02.2021	29.07.2020		KR 20200094659 A

Danksagung

Die hier vorliegende Arbeit entstand während meiner Promotionstätigkeit sowie im Fortgang meiner Tätigkeit als elektrischer Entwickler bei der Infineon Technologies AG in Zusammenarbeit mit der Technischen Universität Dortmund.

Im Besonderen gilt mein Dank Herrn Univ.-Prof. Dr.-Ing. Martin Pfost für die Betreuung meiner Promotion sowie für die wertvollen konstruktiven wissenschaftlichen Anregungen und Hinweise.
Für die Übernahme des Korreferates und sein fachliches Interesse an meiner Arbeit danke ich Herrn Univ.-Prof. Dr.-Ing. Andreas Lindemann.

Bei meinem Betreuer seitens der Infineon Technologies AG, Herrn Dr. Andre Uhlemann bedanke ich mich für seine Ratschläge und Erfahrung im betrieblichen Entwicklungskontext ohne dessen diese Arbeit wahrscheinlich unnötigen Verzögerungen unterlegen wäre.

Nicht zuletzt möchte ich meine Familie, insbesondere meine Frau Astrid und meine Kinder Erik und Jakob hervorheben, die mit ihrer Geduld, Unterstützung und ihrem Verständnis die Entstehung dieser Arbeit erst ermöglicht haben.

Soest, 2022
Michael Schlüter