



# Impact of electrode materials on the performance of amorphous IGZO thin-film transistors

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## Abstract

This study reports on the fabrication and characterization of thin-film transistors (TFTs) based on indium–gallium–zinc–oxide (IGZO) with various source- and drain-region metals (Pt, W and Ti). The performance of the IGZO transistors is compared to TFTs based on hydrogenated amorphous silicon (a-Si:H) with Pt source- and drain-regions. From the output characteristics maximum saturation mobilities of  $\mu = 0.45 \text{ cm}^2/\text{Vs}$  for a-Si:H, and  $\mu = 24$  to  $50 \text{ cm}^2/\text{Vs}$  for IGZO TFTs are extracted, which are competitive to high-performance thin-film transistors. The study reveals a general influence of the source- and drain-electrode material on the maximum saturation mobility and inverse sub-threshold slope.

## Introduction

Thin-film transistors based on metal source- and drain-regions are easy and cheap to fabricate, and are used in many applications including display technology and biosensing [1]. A number of fabrication techniques (including pulsed laser deposition [2] and sputtering [3]) have been used to deposit amorphous TFT-semiconductor materials including hydrogenated silicon (a-Si:H) [4], and indium–gallium–zinc–oxide (IGZO) [5]. TFTs can be fabricated on conventional silicon wafers, silicon on insulator [6], and flexible substrates [7]. Since many thin-film semiconductor materials are transparent, even optically transparent transistors can be fabricated [8].

TFTs are similar to Schottky–Barrier transistors (SBMOS) [9], since in both devices Schottky junctions are formed between source and channel, and drain and channel, respectively. In TFTs these Schottky junctions are made of metal/semiconductor contacts, whereas for SBMOS these junctions are typically made of metal-silicides such as NiSi [10]. Since ion-implantation is not required for SBMOS fabrication, atomically abrupt junctions can be fabricated offering a high scalability and suppressed drain-induced barrier lowering [11]. Despite the similarity to the SBMOS, TFTs

target different applications due to the significantly lower charge carrier mobility in amorphous semiconductors. For example, a-Si:H lacks of band conduction and conductivity is driven by hopping between localized tail-states. This results in significantly smaller charge carrier mobilities ( $\mu_n \approx 0.1\text{--}2 \text{ cm}^2/\text{Vs}$  of electrons and  $\mu_p \approx 10^{-4} \text{ cm}^2/\text{Vs}$  of holes [12]) in a-Si:H TFTs compared to CMOS-transistors ( $\mu_n \approx 10^3 \text{ cm}^2/\text{Vs}$  and  $\mu_p = 10^2 \text{ cm}^2/\text{Vs}$  [13]). In contrast to a-Si:H, IGZO is naturally transparent and offers higher charge carrier mobilities ( $\mu > 10 \text{ cm}^2/\text{Vs}$  [14]), which makes it attractive for fast-response TFTs used for LED displays. Further improvement of the performance of IGZO-based transistors is in focus of research to fabricate even larger high-resolution (8 K) and more energy-efficient displays, or even unlocking the device potential for new application fields such as cheap and flexible analogue or digital electronics.

This study reports on the fabrication of IGZO-based TFTs with various source/drain metals. The device performance is compared to a-Si:H TFTs. IGZO-devices are fabricated completely at room temperature without any post-thermal treatment, which is highly attractive for fabrication of TFTs for displays. Special attention is paid to the transistor characteristics, in particular the saturation mobility and sub-threshold behavior by finding the right choice of the source-/drain-electrode material.

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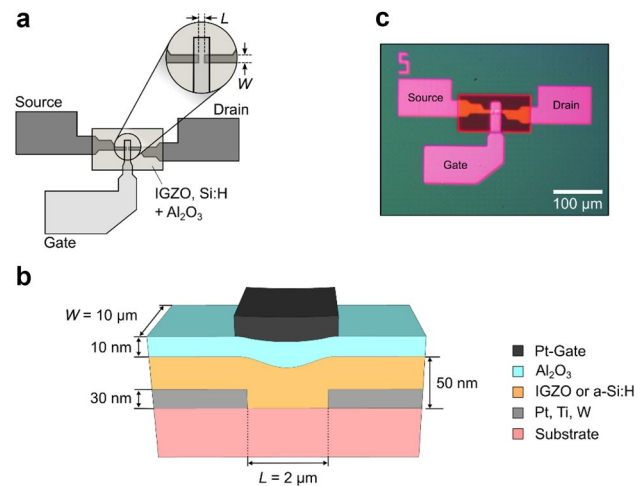
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## Experimental details

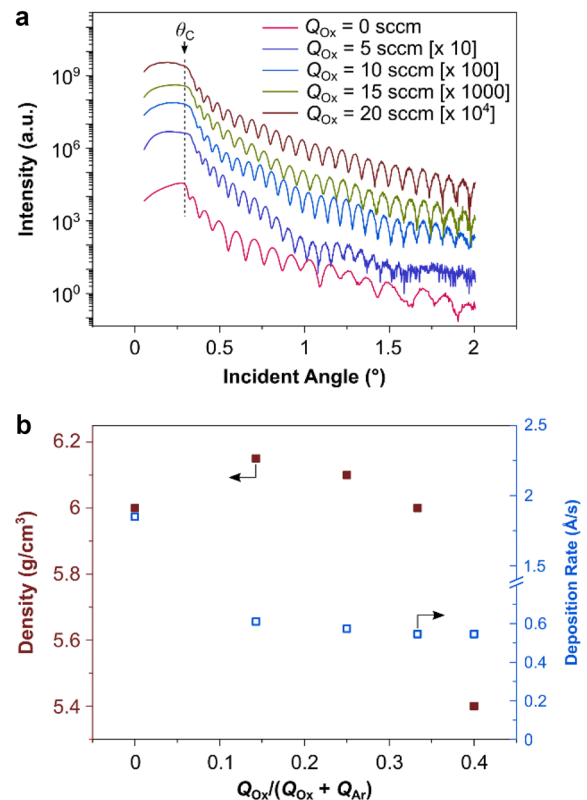
Top-gated thin-film transistors based on IGZO have been fabricated with a channel width  $W = 10 \mu\text{m}$  and a channel length  $L = 2 \mu\text{m}$ . a-Si:H TFTs were fabricated in a previous study [15] and are used as reference transistors here. Oxidized silicon wafers ( $\text{SiO}_2$  thickness  $650 \mu\text{m}$ ) with an additional  $\text{TiO}_2$  adhesion layer (thickness  $10 \text{ nm}$ ) were used as substrates. The source- and drain-regions (S/D-regions, thickness  $30 \text{ nm}$ ) were prepared by direct-current (DC) sputtering. For substrative pattern transfer of source and drain UV lithography and reactive ion-etching (RIE) were used. For this step, AZ 5214E image reversal resist was diluted 6:5 in 1-methoxy-2-propanol acetate for patterning of S/D-regions. For a-Si:H TFTs only Pt is used as source- and drain-contacts. In case of IGZO TFTs the S/D regions were made of Pt, Ti and W, respectively. Afterwards, the amorphous semiconductor was deposited at room temperature (thickness  $50 \text{ nm}$ ). IGZO was RF-sputtered (IGZO target, purity 5 N) using a mixture of Ar and  $\text{O}_2$  with a total constant flowrate  $Q_{\text{tot}} = Q_{\text{Ox}} + Q_{\text{Ar}} = 30 \text{ sccm}$ , where  $Q_{\text{Ox}}$  is the flowrate of oxygen, yielding again a process pressure of  $5.4 \times 10^{-3} \text{ hPa}$ . Best electrical characteristics were found for  $Q_{\text{Ox}} = 0$ , which is used for device fabrication. X-ray reflectivity (XRR) was used for characterization of the thin-film density (see below). While no additional heat treatment was used for IGZO based TFTs, a-Si:H based TFTs were annealed in forming gas (4%  $\text{H}_2$  in  $\text{N}_2$ ) using rapid thermal annealing ( $800 \text{ }^\circ\text{C}$  for  $5 \text{ min}$ ) after Si deposition. Further details on the fabrication of a-Si:H TFTs can be found in Ref. [15]. In a next step,  $10 \text{ nm}$  thick  $\text{Al}_2\text{O}_3$  was electron-beam evaporated and is acting as gate-dielectric. The semiconductor +  $\text{Al}_2\text{O}_3$  layers were microstructured using a single UV lithography step followed by RIE in Ar-plasma. Afterwards,  $30 \text{ nm}$  Pt was deposited as gate-electrode and patterned using a lift-off process. A schematic of the sample structure is shown in Fig. 1a (lateral view) and Fig. 1b (cross-sectional view). An optical microscopy image of a fabricated transistor is shown in Fig. 1c. For device characterization a HP 4155B Semiconductor Analyzer was used.

## Results and discussion

For IGZO TFTs special attention was paid to the deposition process. The densities and thickness of thin-films fabricated by different oxygen flows were extracted from simulated fitting-curves of their XRR spectra (Fig. 2a). For readability in Fig. 2a, the XRR spectra are shifted by a fixed scale factor (between  $1$  and  $10^4$ ): e.g. the spectrum



**Fig. 1** **a** Schematic of the TFT structure. The inset depicts a zoom into the channel region. **b** Cross-sectional view of a TFT structure. **c** Optical microscopy image of a fabricated IGZO-based transistor



**Fig. 2** **a** XRR-spectra of IGZO thin-films sputtered with different oxygen flows. The XRR spectra are shifted by a fixed factor (between  $1$  and  $10^4$ ) for readability. **b** Density and deposition rate of IGZO thin-films for various oxygen flows

for  $Q_{\text{Ox}} = 5 \text{ sccm}$  is multiplied by a factor of  $10$ . From the thickness the deposition rate can be calculated, which decreases by increase of  $Q_{\text{Ox}}$  from  $1.85$  to  $\approx 0.6 \text{ Å}/\text{s}$

(Fig. 2b), as expected for reactive sputtering. Total reflection is present at the critical angle  $\Theta_C$  which is proportional to the square root of the density [16]. Based on the measurements, simulated fitting curves reveal a density of 5.4–6.15 g/cm<sup>3</sup> (Fig. 2b) which is slightly lower than single-crystal IGZO (6.4 g/cm<sup>3</sup>) but similar to reports in literature [17]. For larger oxygen flows one finds a density of up to 6.15 g/cm<sup>3</sup>. For  $Q_{Ox}=0$  the density is 6 g/cm<sup>3</sup>. The smallest density of 5.4 g/cm<sup>3</sup> is found for  $Q_{Ox}=0.4$ . Formation of a mesoporous morphology could be a reason for such a drop of the density.

The output characteristics (i.e. drain current  $I_D$  vs. drain-source-voltage  $V_{DS}$ ) of IGZO and a-Si:H TFTs are depicted in Fig. 3a to d for variable gate-source-voltage  $V_{GS}$ . a-Si:H based TFTs [15] are used as reference devices. The drain current in the saturation regime is:

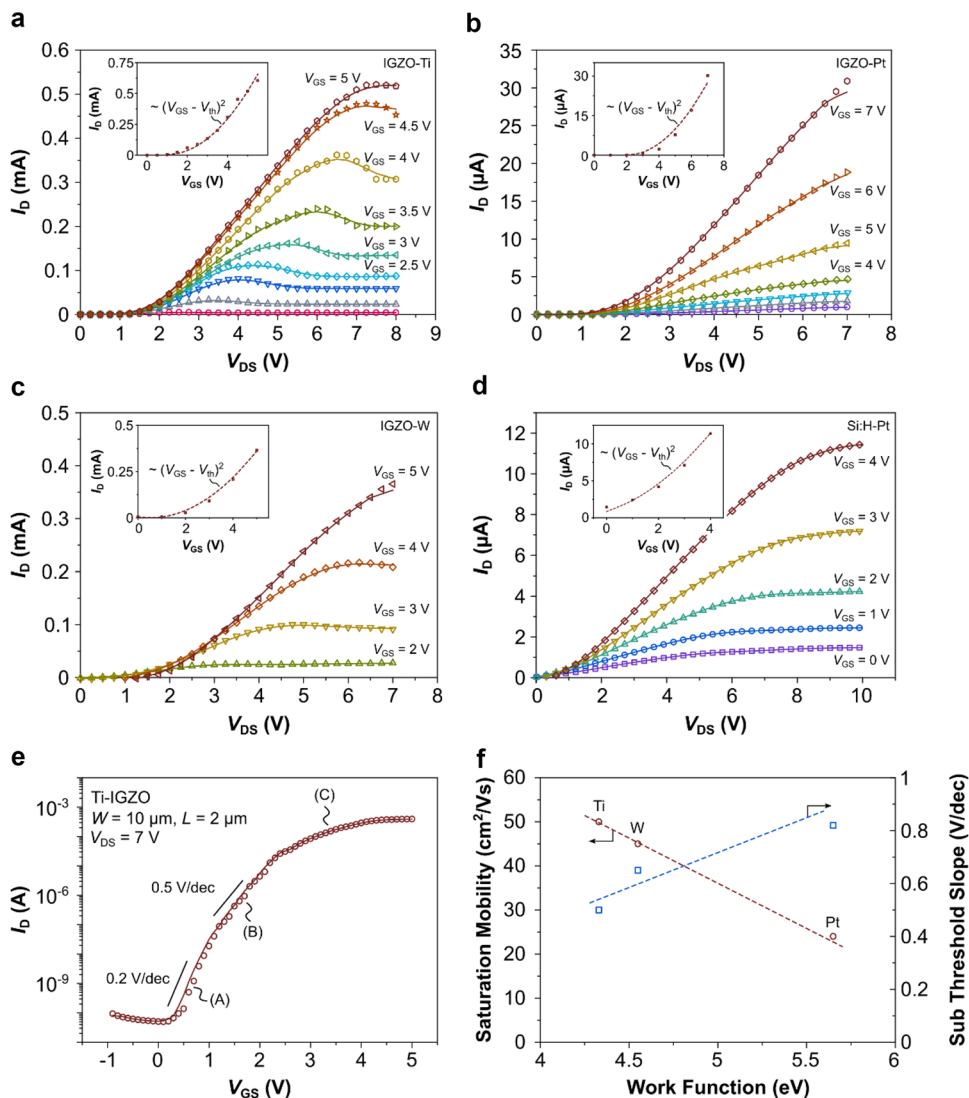
$$I_D = \frac{1}{2} g_m (V_{GS} - V_{th})^2, \quad (1)$$

where  $g_m$  is the transconductance parameter, and  $V_{th}$  is the threshold voltage. Using the transconductance parameter  $g_m \sim dI_D/dV_{GS}|_{V_{DS}} \sim \mu \cdot C'_G \cdot W/L$  the charge carrier saturation mobility  $\mu$  is found, which is an important performance parameter:

$$\mu = \frac{2L}{C'_G W} \times \left( \frac{d\sqrt{I_D}}{d\sqrt{V_{GS}}} \right)^2 \quad (2)$$

Here,  $C'_G \approx 0.8 \times 10^{-6}$  F/cm<sup>2</sup> is the specific gate capacity. For IGZO based transistors a mobility of  $\mu \approx 24$  cm<sup>2</sup>/Vs for S/D=Pt,  $\mu \approx 45$  cm<sup>2</sup>/Vs for S/D=W, and  $\mu \approx 50$  cm<sup>2</sup>/Vs for S/D=Ti is found, respectively. These are competitive values compared to  $\mu \approx 70$  cm<sup>2</sup>/Vs for high mobility IGZO TFTs [14]. For a-Si:H one finds  $\mu \approx 0.45$  cm<sup>2</sup>/Vs [15], which is in

**Fig. 3** a–c Output characteristics of IGZO-based TFTs with S/D-regions made of Ti, Pt, and W, respectively, for variable  $V_{GS}$ . d Output characteristics of an a-Si:H based TFT with S/D-regions made of Pt, for comparison for variable  $V_{GS}$ . Redrawn from Ref. [15] with permission from IOP Publishing. The inset in a–d depict the transfer-characteristics ( $I_D$  vs  $V_{GS}$ ) in linear scale of each device, respectively. e Transfer-characteristic in semi-log scale of a Ti-based IGZO TFT. f Comparison of the saturation mobility and inverse sub-threshold slope vs. work function of the source/drain metals for IGZO TFTs



the range of values reported in the literature ( $\mu \approx 0.1\text{--}2\text{ cm}^2/\text{Vs}$  [12]). In contrast to a-Si:H TFTs, the slope for IGZO TFTs for  $V_{\text{DS}} < 2\text{ V}$  is relatively flat which could be attributed to a parasitic diode-behavior of one of the metal/semiconductor junctions. This behavior has been observed for all metals studied here, including inert Pt. Therefore, this effect cannot be explained by formation of oxide interfaces during processing. Since IGZO was sputtered without additional oxygen flow, a decrease of the defect density, and thus, a decrease of the electron concentration could lead to a drain-side diode-behavior, similar to what has been observed for Schottky-type drain-IGZO junctions [18].

In addition, a local maximum of  $I_{\text{D}}$  between the linear and saturation regime is observed. This behavior has been observed mainly for W and Ti based S/D-regions. Since this signature tends to increase by increase of the gate-source-voltage (and thus drain-current) a reason for this effect could be drain-current induced local heating of the semiconductor. Several studies demonstrated a self-heating induced shift of the threshold-voltage [19–21], however, usually reported for relatively large channel-widths (i.e.  $W > 100\text{ }\mu\text{m}$ ) [22]. Here, the channel-width is much smaller but the normalized drain-current ( $I_{\text{D}}/W > \mu\text{A}/\mu\text{m}$ ) is similar or even higher compared to studies reporting self-heating effects. It should be noted that this effect did not result in a device degradation in this study. Relatively low drain currents are measured for Pt-based devices (e.g.  $I_{\text{D}} \approx 10\text{ }\mu\text{A}$  for Pt-IGZO at  $V_{\text{GS}} = 5\text{ V}$  and  $V_{\text{DS}} = 7\text{ V}$ ; compared to  $I_{\text{D}} \approx 550\text{ }\mu\text{A}$  for Ti-, and  $I_{\text{D}} \approx 380\text{ }\mu\text{A}$  for W-based transistors for  $V_{\text{GS}} = 5\text{ V}$  and  $V_{\text{DS}} = 7\text{ V}$ , respectively). Thus, the self-heating effect in IGZO may be here more dominant in W- and Ti-based devices than in Pt-IGZO TFTs due to the higher drain currents. In fact, this self-heating effect is also not observed for low-drain currents in Ti- and W-IGZO (e.g.  $V_{\text{GS}} < 2\text{ V}$ ).

An example of a transfer-characteristic, i.e.  $I_{\text{D}}$  (in semi-log-scale) vs.  $V_{\text{GS}}$ , of an IGZO-based TFT with Ti S/D-regions for a fixed  $V_{\text{DS}} = 7\text{ V}$  is shown in Fig. 3e. From Fig. 3e, the inverse sub-threshold slope (SS) can be calculated:

$$\text{SS} = \left( \frac{\delta \log I_{\text{D}}}{\delta V_{\text{GS}}} \right)^{-1} \quad (3)$$

The inverse sub-threshold slope is an important transistor property determining the switching behavior of the transistor. Here, three regimes can be identified: A deep-sub-threshold regime (A) is present for  $V_{\text{GS}}$  approx.  $< 1\text{ V}$  with a SS of  $0.2\text{ V/dec}$ , (B) a weak ON-state sub-threshold regime [18] for approx.  $1\text{ V} < V_{\text{GS}} < 2.5\text{ V}$  with a swing of  $\text{SS} = 0.5\text{ V/dec}$ , and an ON-state (C) for  $V_{\text{GS}} > 2.5\text{ V}$ .

A relation between the S/D material, and saturation charge carrier mobility and the inverse sub-threshold slope is depicted in Fig. 3f. The largest mobility and smallest SS

is found for Ti (work function  $4.33\text{ eV}$ ). In contrast, Pt (work function  $5.65\text{ eV}$ ) S/D regions resulted in a mobility almost twice as low compared to Ti and a SS of  $0.82\text{ V/dec}$ .

Only little has been reported on the impact of the S/D material on the TFT properties. Choi et al. reported higher saturation mobilities for Ti compared to Ag [23]. Barquinha et al. investigated the impact of Mo, Ti and Ti/Au as S/D materials on the TFT performance. The authors reported higher saturation mobilities for Au and Mo compared to Ti. The inverse sub-threshold slope ( $\approx 1\text{ V/dec}$ . for all Mo, Ti and Ti/Au) were not specifically mentioned in the study but can be approximated from the transfer characteristics. Yim et al. [24] investigated Mo-, Cu- and Al-based IGZO-TFTs with and without air-annealed thermal treatment, respectively. Without thermal treatment, Mo- and Cu-based devices showed inverse sub-threshold slopes of  $0.5\text{ V/dec}$ . A transistor behavior was not observed for Al-based devices at first, but the device behavior changed after thermal treatment. With Time-of-Flight Secondary Mass Spectroscopy the authors found that Cu diffused into IGZO after annealing, whereas Al forms an oxide interface between S/D regions and channel. The Al-based devices showed conventional transistor characteristics after thermal treatment. The authors contributed this to the formation of an interface resulting in a higher electron concentration in IGZO and therefore a negative threshold voltage. In case of Cu, interdiffusion leads to an increase of  $V_{\text{th}}$  and an increase of SS. For Mo, SS kept constant, but  $V_{\text{th}}$  decreased due to a reduction of the oxygen vacancy concentration.

Table 1 summarizes important thin-film transistor characteristics reported in this study and literature. The devices are based on either bottom-gate, top-gate or even source-gated transistor structures [28] with different geometries. These differences result in different threshold-voltages, maximum saturation mobilities, inverse sub-threshold slopes, drain-side diode phenomena, and potential inter-diffusion or interface reactions. Thus, device comparison is difficult. In this study, one finds higher saturation mobilities for relatively low work function metals (e.g. Ti and W compared to Pt). However, this trend is not observed in all cases. For example, Lin et al. reported of  $\mu = 26\text{ cm}^2/\text{Vs}$  for Ti [30] compared to  $\mu = 10\text{ cm}^2/\text{Vs}$  for Ni as reported by Sporea et al. [28], Barquinha et al. reported of higher mobilities in case of Ti/Au ( $\mu = 18.7\text{ cm}^2/\text{Vs}$ ) and Mo ( $\mu = 17.4\text{ cm}^2/\text{Vs}$ ) compared to Ti ( $\mu = 16.9\text{ cm}^2/\text{Vs}$ ) [29]. Nevertheless, there is qualitative evidence that the work function of the S/D material has a general impact on the transistor performance. In this study, where transistors with the same geometry and fabrication methods are prepared, a higher work function results in a smaller saturation mobility and a larger inverse sub-threshold slope. This could be attributed to the drain-channel contact: by increase of  $V_{\text{DS}}$  the electron concentration at the drain-side is lowered, which leads to the

**Table 1** Overview of important TFT characteristics reported in this study and literature for a-Si:H- and IGZO-based TFTs

Channel	S/D material	Gate-dielectric	Drain-side diode	$\mu$ (cm <sup>2</sup> /Vs)	SS (V/dec)	References
a-Si:H	Pt (5.65 eV)	Al <sub>2</sub> O <sub>3</sub>	Yes	0.45		[15]
IGZO	Al (4.06 eV)	Al <sub>2</sub> O <sub>3</sub>	No	0.97	0.17	[25]
a-Si:H	Al/Cr (4.5 eV)	a-SiN <sub>x</sub> :H	No	1.45	0.3	[26]
a-Si:H	Cr	SiO <sub>2</sub>	No	2	1.5	[4]
IGZO	Ag (4.26 eV)	SiO <sub>2</sub>	No	7.12	0.88	[23]
IGZO	Ti (4.33 eV)	SiO <sub>2</sub>	No	8.48	0.87	[23]
IGZO	Ag	Al <sub>2</sub> O <sub>3</sub> :Nd		8.73	0.37	[27]
IGZO	Cu (4.53 eV)	SiN <sub>x</sub>		9.64		[24]
IGZO	Ni (5.04 eV)	Al <sub>2</sub> O <sub>3</sub>	Yes	10		[28]
IGZO	Ti	SiO <sub>2</sub>		16.9	≈ 1	[29]
IGZO	Mo (4.36 eV)	SiO <sub>2</sub>		17.4	≈ 1	[29]
IGZO	Ti/Au (5.1 eV)	SiO <sub>2</sub>		18.7	≈ 1	[29]
IGZO	Pt	Al <sub>2</sub> O <sub>3</sub>	Yes	24	0.82	This study
IGZO	Ti	SiN <sub>x</sub>	No	26	0.6	[30]
IGZO	ITO (4.4 eV)	SiO <sub>2</sub>		28	0.35	[19]
IGZO	W (4.55 eV)	Al <sub>2</sub> O <sub>3</sub>	Yes	45	0.654	This study
IGZO	Ti	Al <sub>2</sub> O <sub>3</sub>	Yes	50	0.2–0.5	This study
IGZO	ITO	Al <sub>2</sub> O <sub>3</sub>	Yes	9.9–74	0.26–0.34	[14]

The work function (for ITO the electron affinity) is given for each S/D material in braces

formation of a space-charge layer in the saturation regime. The electron concentration at the source-channel junction keeps relatively constant and the junction is in forward bias. Thus, the drain-channel junction could play a dominant role for both the mobility and the inverse sub-threshold slope, presumably due to the formation of an additional material-dependent diode-behavior.

## Conclusions

This study reports on the fabrication of thin-film transistors based on a-Si:H and IGZO with different source/drain metals (Pt, W and Ti). From the output-characteristics one finds saturation mobilities of 0.45 cm<sup>2</sup>/Vs of Pt/a-Si:H, and  $\mu \approx 24$  cm<sup>2</sup>/Vs for Pt/IGZO,  $\mu \approx 45$  cm<sup>2</sup>/Vs for W/IGZO, and  $\mu \approx 50$  cm<sup>2</sup>/Vs for Ti/IGZO. These values are competitive to high-performance IGZO-transistors. From the transfer-characteristics two slopes (0.2 V/dec and 0.5 V/dec) in the deep-sub-threshold and weak ON-state regime are found, which are similar to literature values. As a rough estimate, the study finds that high saturation mobilities and small inverse sub-threshold slopes are found for S/D metals with relatively low work functions, which could be caused by a diode-behavior of the drain-channel junction.

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**Data availability** The data that support the findings of this study are available on request from the corresponding author.

## Declarations

**Conflict of interest** The author has no conflict to disclose.

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