Characterisation of Ionisation-Induced Surface Effects for the Optimisation of Silicon-Detectors for Particle Physics Applications

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Contents

Chapter 1

Introduction

The Standard Model of particle physics has been extremely successful in describing the elementary composition of matter and the fundamental interactions of particles. It is the most crucial basis for modern particle physics. However, although the Standard Model can answer a lot of questions, there are still some basic phenomena left unexplained. For example, it is not clear yet by what mechanism mass is assigned to particles and why different particles have different masses. Theoretically, the *Higgs* mechanism proposes a solution here, but the experimental evidence is still missing. Another actual research topic are the *Grand Unified Theories* (GUT), which aim at the unification of all particle interactions on high energy scales. In this field, *super-symmetric* (SUSY) concepts provide promising basic ideas, but the experimental proof is still open.

Experimental tests of e.g. the Higgs mechanism or super-symmetric extensions of the Standard Model require complex instruments. Basic principle of measurement is to observe the collision of two elementary particles like an electron and a proton or two protons using particle accelerators. From the energy which is set free by the collision other elementary particles are created. The characteristic properties like momentum, charge and energy are measured and provide insight into the fundamental interactions and reactions. High resolution detection systems are required as well as very high collision energies for the observation of new physics.

For these research topics, a new proton-proton accellerator called LHC[1] is presently being installed at the European Laboratory for Particle Physics (CERN) in Geneva, Switzerland. The machine will provide two proton beams colliding with a centre-of-mass energy of 14 TeV. An event rate of 40 MHz and a luminosity of $10^{34}/\mathrm{cm}^2\mathrm{s}$ will allow the observation of processes of interest with good statistics. ATLAS is besides CMS one of the two multi purpose experiments currently being assembled at the LHC accellerator ring, mainly aiming for the search of the Higgs boson and tests of supersymmetric theories as well as b-physics and τ-physics. Data acquisition is foreseen for 100 days per year over a total runtime of 10 years.

The inner part of the ATLAS tracking system is equipped with silicon sensors. The use of silicon supports fast read-out speeds because of signal rise times in the range of a

[1]Large Hadron Collider

few nano seconds. Silicon strip and pixel sensors can also be optimised for high spatial resolution of a few micrometres. Additionally, their production is based on commercial production processes which is a major advantage for large scale series productions.

Especially the detection of short-lived particles requires good secondary vertex finding capabilities close to the interaction point, where track density is high. The use of strip detectors in this region is ruled out by the high track density because of possible ambiguities of track points, which would be a severe problem. Thus, the optimum choice here are hybrid silicon pixel sensors providing three dimensional space points.

The hybrid pixel systems must fulfil various requirements. First of all, high reliability and fault tolerance is crucial because within the 10 years runtime of ATLAS it is not foreseen to replace any parts.

The most significant reason for the drift of operation points in the sensor is performance degradation due to radiation damage. The pixel sensors must cope with a particle fluence of 10^{15}particles/cm^2 (1 MeV neutron equivalent in silicon), mostly consisting of charged hadrons and an ionisation induced energy deposition of 500 kGy (in silicon oxide). Thus, radiation tolerance is one of the most important requirements.

The development and optimisation of silicon sensors for their use in harsh radiation environments requires a good knowledge of the damage mechanisms occuring and of their impact on the sensor performance. Generally it has to be distinguished between displacement damage taking place in the silicon volume due to displacement of silicon atoms and ionisation induced effects at the sensor surface. According to the particular damage, different parts of the sensor must be optimised. Displacement damage is controlled by an appropriate choice of the silicon, whereas the introduction of surface damage is influenced by the sensor design and specific properties of the sensor surface.

Displacement damage due to non-ionising energy loss (NIEL), has been successfully under investigation for a long time now. Based on a large amount of experimental data, parameter models have been developed which allow a precise prediction of radiation induced alteration of bulk parameters like fluence and time-dependent changes of the depletion voltage or the volume generation current or trapping.

In case of ionisation induced surface effects the basic mechanisms of damage generation were known already. But this knowledge was up to now not systematically translated into a set of rules which could predict radiation damage levels of particular processes and for specific sensor designs. It therefore was the aim of this work to find a set of characteristic surface parameters and the according experimental techniques for their proper determination with the intention to study systematically the influence of surface effects on sensors developed for particle physics experiments. The studies within this work shall enable a full implementation of surface damage effects into device simulations, allowing the optimisation of a sensor design already in the computer. Furthermore, when thinking of large scale series sensor productions as for ATLAS or CMS, quality assurance, process monitoring and regular tests of radiation hardness will be required. The groundwork for these concepts and routines concerning surface related effects is intended to be provided within this work.

These aims can only be reached by keeping to a systematic working plan, which is reflected by the concept of this thesis. First, it is necessary to identify the crucial requirements for radiation tolerance coming from particle physics experiments. For this work the Pixel Detector of the ATLAS experiment is chosen because of its challenging demands on radiation hardness. An overview of the pixel detector specifications is given in chapter 2 of this thesis as the basic motivation of this work. Then an introduction to the operating principle of a silicon sensor is given in chapter 3 and a subsequent introduction to different sensor concepts, which are included in the tests presented in this thesis. A brief overview of displacement damage effects is given also because an elementary understanding of volume related defects is needed for later discussions. In chapter 4 the microscopic nature of particular aspects of the sensor surface, i.e. of thermal silicon oxide films, is presented. Remaining on the microscopic level, damage creation mechanisms due to ionising radiation are discussed in the second part of the chapter. Under consideration of these mechanisms conclusions are drawn concerning generic dependencies of ionisation induced surface effects on the ionisation dose like e.g. the electric field in the oxide. Following these conclusions, appropriate monitor devices and the according measurement techniques for an electrical characterisation of surfaces are developed in chapter 5 for the utilized devices. The optimisation of the measurement techniques and the correct interpretation of the obtained results require a good understanding of the device physics which is introduced at the beginning of chapter 5. In chapter 6 generic radiation induced surface effects are discussed, which are used to define the suitable irradiation scenarios for the evaluation of processes and sensors presented in chapters 7 and 8. Radiation induced effects on materials and processes are studied in chapter 7. The applied systematic is developed on the basis of the discussions of the previous chapters. Two key aspects concerning material tests are the relation of surface quality to the crystal orientation of the silicon and to a high temperature diffusion process which introduces oxygen into the silicon crystal. The latter one is motivated by a recent development of the ROSE collaboration [ROS99] which discovered that a high oxygen concentration in the silicon makes its electrical parameters much less sensitive to displacement damage. Thus, both aspects are important for actual discussions. Radiation induced surface effects on silicon sensors are dealt with in chapter 8, accounting for different sensor concepts. Conclusions from the individual studies and their relevance for sensor development and quality assurance are finally discussed in chapter 9 before going to the conclusions.

The appendix includes the complete characterisation procedures used for the process evaluation and a very special but important aspect concerning high frequency measurements.

Chapter 2

Motivation

2.1 Requirements of the ATLAS Experiment

2.1.1 Experimental purpose

The well established Standard Model is the groundwork of modern particle physics. It provides explanations for various important phenomena observed in nature like the composition of matter on an elementary particle scale. Although the Standard Model is capable of answering a lot of questions, there are some basic phenomena left unexplained. For example, it is still unclear by what mechanism mass is assigned to particles and for what reasons different particles have different masses. There are theories which provide a mechanisms for the generation of masses, i.e. the *Higgs* mechanism. But experimental evidence for the existance of Higgs bosons is still missing. Another actual research topic is based on the aim to unify all particle interactions at very high energy scales, which is called *Grand Unified Theories* (GUT). In this field, *super-symmetric* (SUSY) theoretical approaches lead to good results, but again, the experimental proof has to be delivered, still.

For the research of the above topics and other particle physics questions, two multi-purpose experiments, namely ATLAS [ATL97] and CMS [CMS98], are presently being installed at the large hadron collider ring (LHC) at the European Laboratory for Particle Physics (CERN) in Geneva, Switzerland. The LHC machine provides two proton beams colliding with a centre-of-mass energy of 14 TeV. The collisions occur every 25 ns, corresponding to an physical event rate of 40 MHz. Together with a high luminosity of $10^{34}\text{cm}^{-2}\text{s}^{-1}$ the 40 MHz event rate will allow to observe particle physics processes of interest with sufficient statistics. The experiments are designed to take data for 100 days per year over a total periode of 10 years.

It is not foreseen to replace or renew parts of the detector of the ATLAS experiment due to limited technical access to detector components when installed once. Therefore, besides excellent capabilities for the detection of new particle physics events, all detector components must have an excellent reliability as well as longterm stability and fault tolerance. The full ATLAS detector is described in [ATL99].

Generally, silicon sensors have been successfully employed in a large number of particle physics experiment already. But the development of silicon pixel sensors for the ATLAS Experiments is the most challanging task among present day experiments. Pixel sensors are employed in the innermost part of the ATLAS Inner Detector.

2.1.2 The Pixel Detector of the ATLAS Experiment

The Pixel Detector is located in close distance to the interaction point where track density is highest, optimised for secondary vertex and track finding. A pixel detector is the optimum choice here because it provides a three dimensional space point without any ambiguities, even when track densities are high. The utilization of silicon strip sensors is ruled out immediately in this region due to possible ambiguities in track point determination. They can be used at larger radii where the occupancy is lower and a lower number of read-out channels is sufficient. The use of silicon pixel and strip sensors is summarised in tab. 2.1.

Detector	Position	Area [m^2]	Resolution [μm]
Pixels	b-physics layer	0.2	Rϕ=12, z=66
	layer 1+2	1.4	Rϕ=12, z=66
	2·4 end-cap discs	0.7	Rϕ=12, z=77
SCT	4 barrel layers	34.4	Rϕ=16, z=580
	9 end-cap wheels	26.7	Rϕ=16, z=580

Table 2.1: *Silicon detectors in the Inner Detector [ATL99].*

From the particle physics point of view the following requirements must be fulfilled by the Pixel Detector. First, a spatial resolution of 12 μm perpendicular to the beam direction (Rϕ-plane) and of 100 μm in the z-direction is needed for a sufficient track separation capability in the high track density area. Second, at least three space points of a track are required to be measured over the full acceptance range, i.e. for pseudo rapidities of $|\eta| < 2.5$. Third, the total efficiency must be better than 97 percent while keeping the radiation length of the pixel detector system as low as possible to avoide multiple scattering. Finally, the innermost pixel detector layer is required to be located as close as possible to the interaction point for a good sensitivity to b-physics and other short-lived events.

Due to its close distance to the interaction point and the high luminosity of the LHC machine the pixel detector must withstand an intense radiation field. An overall particle fluence of $1{\cdot}10^{15}$n/cm^{-2} (normalised to 1 MeV neutrons) is expected as well as an ionising dose of 500 kGy (in silicon oxide). All pixel detector components have to cope with this design fluence and dose levels. The demands are even higher for the innermost pixel layer to be installed at a radius of 4.3 cm. It is needed for the observation of b-physics events. The so-called b-physics layer is intended to be operated at least for 5 years but as long as possible. At this position the design radiation levels are reached in the fifth year already. An overview of the demands on radiation hardness depending on the location in the Inner Detector are compiled in tab. 2.2, containing the NIEL[1] particle fluences and the ionising dose levels for silicon oxide. Generally, the predicted fluences and dose levels have an uncertainty of 50 percent which must be considered for radiation hardness tests.

	r [cm]	z [cm]	total fluence [10^{14}cm^{-2}]	total dose [kGy (SiO_2)]
b-layer (5 years)	4.3	0.0	10.44	500
1st-layer	10.1	0.0	6.64	390
2nd-layer	13.2	0.0	4.00	145

Table 2.2: *Total fluence (normalised to 1 MeV neutrons) levels reached after 10 years at the design luminosity of 10^{34}cm^{-2}s^{-1} [ATL99] and the accumulated dose levels.*

The pixel detector is cooled during operation down to -7^{o}C to slow down the performance degradation due to radiation damage and achieve stable operating points. Therefore a powerful cooling system is needed. Furthermore, when once installed, it is hardly possible to access the pixel detector for replacing defective components or even for other maintenance procedures. Thus, an excellent long term stability and fault tolerance of the individual components is obligatory, which requires an effective and systematic quality control of the pixel detector during production and before assembly.

2.2 Conclusions for this work

Within ATLAS a total area of more than 60 m^2 will be equipped with silicon strip and pixel sensors. The large amount of sensors will require a mass production on the basis of commercial processes. The challanging demands for long-term stability, fault tolerance and radiation hardness require a systematic quality controll process which is capable of rejecting defective or low quality sensors at the earliest possible stage of production or assembly. Because of the large amount of sensors, very effective and reliable routines are needed, providing sufficient information about the performance of every single sensor. Beside the performance information criteria for a rejection of a sensor must be defined. Another aspect of importance is to develop parameters and methods which allow a complete performance prediction for the irradiated sensors.

Main goal of this work therefore is to develop a set of quality control parameters which can be used for monitoring the production process quality during the production as well as of radiation tolerance against ionising radiation. Before this is achievable, a fundamental understanding of ionisation induced radiation effects in silicon materials and sensors have to be worked out. Therefore it was necessary to develop measurement techniques and to define the measurement conditions according to the radiation ambient present in the ATLAS Pixel detector. Furthermore, an irradiation scenario and a suitable irradiation facility had to be developed which allows to simulate the radiation damage levels in laboratory experiments.

[1]Non Ionising Energy Loss

Chapter 3

Silicon detectors

3.1 Introduction

Ionising particles can easily be detected using a reverse biased silicon diode. The diode is formed by an abrupt asymmetrically doped pn-junction. Applying a reverse bias to the pn-junction causes depletion of free charge carriers in the junction region. A through passing ionising particle ionises silicon atoms and therefore creates numerous electron-hole pairs along its track which drift to the electrodes following the electric field in the depletion zone. The resulting signal can be detected by a charge sensitive amplifier. In silicon the average energy for the creation of electron-hole pairs is 3.6 eV, a *minimal ionising particle* creates around 24000 charges crossing a 300 μm thick depletion layer.

3.2 Asymmetric pn-junction

In fig. 3.1 the doping profile and the electric field distribution within an asymmetric pn-junction are depicted. Following the gradient in the concentration of free charge carriers, free positive charges diffuse from the p-doped region to the n-doped part and vice versa. Due to the redistribution of charges, an electric field builds up and generates a drift current which compensates for the diffusion current. In equilibrium the net charge transport is equal to zero, the region around the pn-junction is depleted from free charge carriers, and therefore is called *depletion zone.*

By applying an additional reverse bias voltage to the pn-junction, the depletion region can be extended further into the silicon bulk to increase the sensitive volume. Furthermore, the field inside the depletion region grows and charge separation becomes more efficient.

One of the most important operation parameters of a detector is the minimum voltage to be applied to the pn-junction to reach full depletion, i.e. achieve a maximum sensitive volume. The dependence of the depth of the depletion zone from the applied bias voltage can be calculated by solving Poisson's equation. The line of argumentation is mainly adopted from [LEO92].

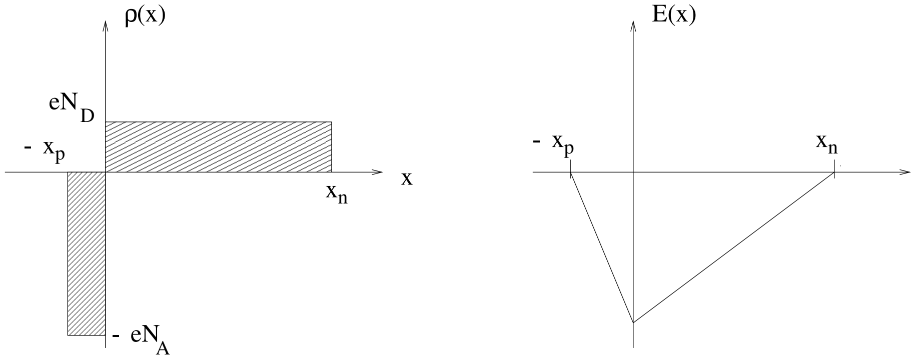


Figure 3.1: *Doping profile and gradient of the electric field of an asymmetric pn-junction. N_A and N_D are the acceptor- and donor concentration ($N_A \gg N_D$), ρ represents the charge density and E the electric field. [LEO92]*

A one-dimensional charge distribution is assumed as depicted in fig. 3.1,

$$\rho(x) = \begin{cases} eN_\mathrm{D} & 0 < x < x_\mathrm{n} \\ -eN_\mathrm{A} & -x_p < x < 0. \end{cases} \tag{3.1}$$

N_A and N_D represent the aceptor respectively donor concentration, x_n and x_p the depth of the depletion zones in the n-region and p-region. Solving Poisson's equation for this charge distribution

$$\frac{d^2V}{dx^2} = -\frac{\rho(x)}{\varepsilon_\mathrm{Si}\varepsilon_0}, \tag{3.2}$$

provides the gradient of the electric field and the potential of the pn-junction. ϵ_Si is the permittivity of silicon.

As is indicated in fig. 3.1, the doping concentration of the p-region is several orders of magnitude higher than in the n-region, the depletion zone therefore will mainly grow into the n-doped silicon, it is $x_\mathrm{n} \gg x_\mathrm{p}$. This is one of the most important features of an asymmetric pn-junction.

Charge conservation requires, that

$$N_A x_p = N_D x_n. \tag{3.3}$$

As a consequence of the concentration gradient in free charge carriers a so-called diffusion potential[1] V_0 builds up between p-side and n-side contact.

The electric field distribution of fig. 3.1 is calculated by an integration of equation 3.2,

$$E(x) = -\frac{dV}{dx} = \begin{cases} \frac{eN_D}{\varepsilon\varepsilon_0}(x - x_n) & 0 < x < x_n \\ \\ -\frac{eN_A}{\varepsilon\varepsilon_0}(x + x_p) & -x_p < x < 0 \end{cases} \tag{3.4}$$

[1]which is sometimes called *build-in voltage*, too

Finally, the potential is obtained from a further integration,

$$V(x) = \begin{cases} -\frac{eN_D}{\varepsilon\varepsilon_0}(\frac{x^2}{2} - x_n x) + C & 0 < x < x_n \\ \\ \frac{eN_A}{\varepsilon\varepsilon_0}(\frac{x^2}{2} + x_p x) + C' & -x_p < x < 0 \end{cases} \tag{3.5}$$

Applying an outer bias voltage to the asymmetric pn-junction can increase the depletion width,

$$x = \sqrt{\frac{2\varepsilon\varepsilon_0}{e_0 N_D}(V + V_0)}, \tag{3.6}$$

with $x_n \gg x_p$ and therefore $x \approx x_n$. Typical operation voltages for several hundred micron thick detectors are much larger than the diffusion potential (≈1 V) which therefore can be neglected.

For the above calculations it was assumed that the doping concentrations N_A and N_D reflect the density of all electrically active centres. Even in high purity silicon there are always unwanted impurities of acceptor and donor type present which contribute to the doping concentration as well. Especially irradiation introduces various defects with acceptor respectively donor beaviour, which will be discussed later. All these effects are summed up in the effective doping concentration,

$$|N_{\text{eff}}| = |N_{\text{donor}} - N_{\text{acceptor}}|. \tag{3.7}$$

where N_{donor} and N_{acceptor} are the concentration of all electrically active donors respectively acceptors in the silicon. N_{eff} is the effective density of all electrically active dopants and other impurities.

Finally, the voltage dependence of the depletion depth is found to be

$$x := x_n = \sqrt{\frac{2\varepsilon\varepsilon_0}{e_0 N_{\text{eff}}}} \cdot \sqrt{U}. \tag{3.8}$$

The voltage which corresponds to the maximum possible depletion width d is called *depletion voltage* V_{depl}.

3.3 Detector concepts

A single pn-junction as described in the previous section can be used for detecting an ionising particle but it cannot provide any position information about the particle track. For this purpose it is necessary to segment the diode into an array of smaller individual pn-junctions.

3.3.1 Strip and pixel sensors

One of the most popular detector designs used in particle physics bases on a segmentation of the p^+ implantation into a periodic arrangement of strips. Such a detector is

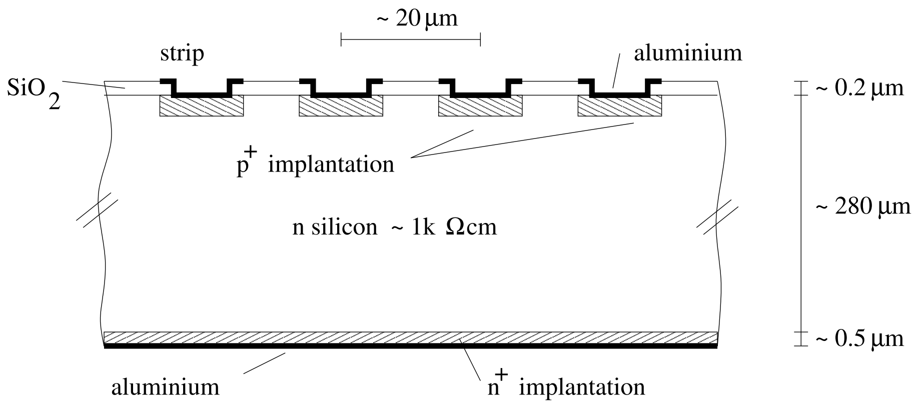


Figure 3.2: *Cross-section of a strip-detector, schematic drawing.*

called *strip-detector* and a schematic cross-section perpendicular to the strips is shown in fig. 3.2.

Each strip-like p-implantation forms an asymmetric pn-junction with the underlying lightly n-doped silicon substrate. Typically, the strip length extends to several centimetres whereas the pitch, i.e. the periodic length of the strip cells, is in the order of 50-100 μm. Therefore, strip detectors provide one-dimensional position information of a particle transit, only. The spatial resolution is determined for binary read-out by the pitch,

$$\sigma = \frac{pitch}{\sqrt{12}}. \tag{3.9}$$

The unimplanted sensor surface is protected by a silicon oxide film. A metal layer (aluminium) is deposited on top of each strip and provides electrical contact to the underlying p-implantation through an opening in the oxide layer (dc-contact).

On the unsegmented side of the detector an ohmic contact is needed, which is formed by a high dose n-implantation and an aluminium back-side electrode.

As already mentioned, strip detectors provide one dimensional track information. The second dimension can be obtained by either glueing two strip detectors back to back rotated by a certain angle (stereo angle ϕ), by segmenting the ohmic back contact into strips rotated by certain angle (double-sided strip-detector) [RIC96] or by segmenting the strips of a single-sided detector into an array of diodes (pixel-detector).

A disadvantage of strip-detectors is the presence of ambiguities as soon as two or more particles pass the detector simultaneously. This may become a severe problem for high track densities and detector occupancies. Pixel detectors provide a solution here. They consist of a two dimensional array of pn-junctions. The high degree of segmentation with typical pixel size of 100 μm by 100 μm provides high resolution position information in two dimensions. Pixel detectors are quite robust and can be successfully operated even after exposure to intense radiation.

3.3.2 n^+n versus p^+n design

In fig. 3.2 a schematic cross-section of a typical p-in-n strip detector is depicted. The strips are formed by a segmentation of the p^+n-junction whereas the ohmic contact is formed by a large area n^+-implantation. The opposite concept is followed in n-in-n sensor designs, i.e. the ohmic contact is segmented into individual pixels or strips and a large area p^+n-junction is used.

Although the basic operation principle based on the depletion of pn-junctions is completely identical, there are intrinsic differences in the performance of both designs. A brief comparison of the specific advantages of both concepts is given in the following.

Unirradiated p-in-n sensors do not necessarily have to be operated fully depleted. Even for bias voltages lower than the full depletion voltage a depletion zone is formed around the pixel implantations, maintaining a proper charge separation and interpixel isolation. This is different for n-in-n senor designs. Here the field region grows from the unsegmented junction side into the sensor volume. A good charge separation cannot be obtained before the field zone reaches the pixel implantations, charges must diffuse through the undepleted bulk to the pixels, charges are spread over several pixels. Generally, it is no problem to establish full depletion in unirradiated sensors because the depletion voltages are rather low. This changes after radiation damage.

High radiation damage in the silicon crystal leads to a significant increase of the depletion voltage and it might be impossible to operate a heavily damaged sensor fully depleted. Besides of a growing depletion voltage radiation damage can lead to a type conversion of the silicon substrate, i.e. originally n-type silicon is converted to p-type silicon due to radiation damage effects.

The type conversion of the silicon certainly implies a change of the depletion behaviour of p-in-n and n-in-n sensors. In p-in-n sensors the pn-junction moves to the unsegmented n^+-implantation whereas in n-in-n detectors it is now on the segmented side. As a consequence operation under partial depletion after type conversion becomes a problem in p-in-n sensors whereas it is now possible for n-in-n sensors. This is an important advantage of n-in-n sensors when operated in high radiation environments.

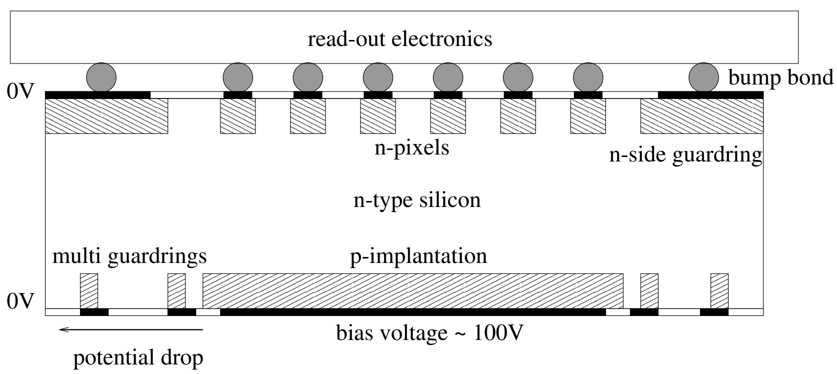
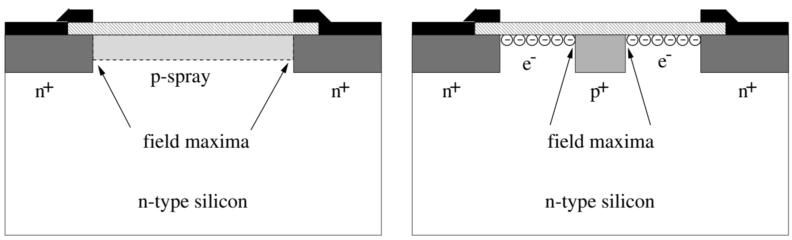


Figure 3.3: *Concept of the ATLAS Pixel sensor [ROH98].*

By using n-in-n sensors it is possible to hold the whole segmented side of the sensor on ground potential. This is of great importance for e.g. the ATLAS hybrid pixel detector, the concept is illustrated in fig. 3.3. A multi guardring structure on the p-side is used for a controlled voltage drop from the high voltage region to the cutting edges of the sensor which has a low resistance due to high defect density as a result of the cutting process. It is essential that the segmented side is kept on ground potential because the read-out chip is mounted directly above the sensor in a very close distance of 20 μm. Otherwise the read-out chip would be harmed due to sparking.

For n-in-n sensor designs it has to be considered that there is always a positive charge density present in the silicon oxide layer (see chapter 4). Consequently negative charges are accumulated at the interface between silicon and silicon oxide passivation. They form a conductive channel and cause a shortage between neighbouring pixels. Thus, an additional interpixel isolation is needed.



(a) p-spray isolation. (b) p-stop isolation.

Figure 3.4: Interpixel isolation techniques utilized in n-in-n sensors.

There are two basic isolation techniques available, i.e. the *p-stop* isolation and the *p-spray* isolation. Both concepts are illustrated in fig. 3.4. Fig. 3.4(a) shows the p-spray isolation technique. In this technology a low dose p-spray implant is applied to the whole wafer, which compensates the accumulated electrons everywhere on the wafer. The p-spray dose must be chosen high enough to provide sufficient compensation capabilities but low enough to keep the risk of electrical break downs near the n^+ pixel implantations due to the high charge gradient low. The gradient of charge concentration decreases after irradiation because the positive oxide charge density grows. Thus a higher voltage stability is obtained after irradiation. This can be even more improved by using a p-spray with a high concentration in the middle of the gap between the pixel implants and a reduced concentration in the neighbourhood of the pixels, reducing electric fields even before irradiation. This technique is referred to as *moderated p-spray* [RIC]. The moderated p-stop isolation technique was chosen for the ATLAS Pixel Sensor.

The p-stop isolation technique is depicted in fig. 3.4(b). Individual p^+ implantations located in the gap between the pixel implantations are used to interrupt the conductive electron channel. The alignment of the p-stop implants has to be done with high precision and requires an extra mask for the process. This makes it more cost intensive than the p-spray option. High electric fields are generated at the border of the p-stop implants being a severe risk for electrical break downs. After irradiation the electric fields are even higher because of the increased oxide charge density which leads to a higher electron density at the silicon surface.

3.4 Characteristic properties

3.4.1 Depletion voltage and backside capacitance

In the previous section it was shown that the depth of the depletion zone depends on the applied bias voltage. Highest sensitivity for particle detection requires a maximal size of the depletion region, which is the sensitive volume. Assuming a total thickness d of the detector, the minimum bias voltage then is

$$V_{depl} = \frac{e_0 \cdot N_{\text{eff}}}{2\varepsilon\varepsilon_0} \cdot d^2. \tag{3.10}$$

The depletion voltage is proportional to the effective doping concentration of the silicon and to the square of the device thickness. In practice, usually even higher voltages are applied to the device to separate signal charges more efficiently, especially near the x=d region where the electric field is low.

The depletion voltage can be experimentally extracted from the capacitance-voltage characteristic of a pn-junction. Therefore, the dynamic capacitance is measured as a function of the bias voltage,

$$C := \frac{dQ}{dU}. \tag{3.11}$$

A small change dU in the bias voltage causes the border of the depletion zone to slightly move which results in charge movements,

$$\Delta Q = e_0 |N_{\text{eff}}| A \cdot \Delta x. \tag{3.12}$$

From equation 3.8 follows that the capacitance of the pn-junction itself, called back-side capacitance, is

$$C_{bs} = A\frac{\varepsilon\varepsilon_0}{x}. \tag{3.13}$$

or, expressed as a function of the operating voltage,

$$C_{bs} = A \cdot \sqrt{\frac{e_0 \varepsilon\varepsilon_0 |N_{\text{eff}}|}{2V}}, \tag{3.14}$$

Therefore, the capacitance is proportional to $\frac{1}{\sqrt{V}}$ for bias voltages smaller than the depletion voltage. For higher bias voltages the capacitance is constant,

$$C_{\text{depl}} = A\frac{\varepsilon\varepsilon_0}{d} \tag{3.15}$$

3.4.2 Interpixel capacitance

Beside the backside capacitance further capacitive contributions have to be considered in a strip detector as well as in a pixel sensor, e.g. the capacitive coupling of detector elements to their neighbour cells as illustrated in fig. 3.5. The magnitude of these

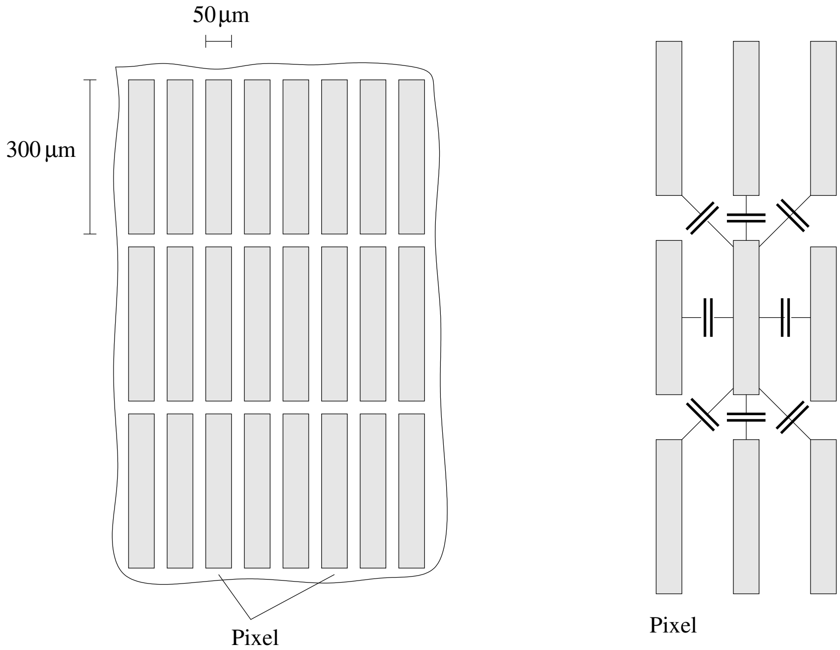


Figure 3.5: *Excerpt of a pixel matrix, capacitive coupling of a pixel cell to its neighbour cells.*

coupling depend on the particular sensor design, i.e. the cell length and the distance between neighbour cells [WUE97].

3.4.3 Volume generation current

Due to thermal activation there are charge carriers generated within the field zone of a depleted diode. Drifting along the electric field to the electrodes the moving charge carriers result in a current, which is proportional to the depleted volume and strongly dependent on the temperature,

$$I_{\mathrm{Vol}} = \frac{e_0 n_{\mathrm{i}} x A}{2\tau}, \tag{3.16}$$

where x is the width of the depletion zone, A is the area of the junction and τ the life-time of the minority charge carriers. n_i represents the intrinsic carrier concentration [MOR54],

$$n_{\mathrm{i}}^2 = 1.5 \cdot 10^{33} cm^{-6} \left(\frac{T}{K}\right)^3 \cdot e^{\frac{-1.21\mathrm{eV}}{kT}}. \tag{3.17}$$

The charge generation centres are impurities or crystal defects which form energy levels in the silicon band gap. For bias voltages less than the depletion voltage, the voltage dependence of the volume generation current follows from equation 3.8,

$$I_{\mathrm{Vol}} = \frac{e_0 n_i A}{2\tau}\sqrt{\frac{2\varepsilon\varepsilon_0}{e|N_{\mathrm{eff}}|}} \cdot \sqrt{U}, \tag{3.18}$$

according to the depleted volume. Characteristically, the current increases with the square root of the applied voltage until full depletion is reached.

3.4.4 Diffusion current

Minority carriers which diffuse into the depletion region contribute as diffusion current to the total reverse current. Minority carriers must be closer than the mean free path to the field zone. The diffusion current can be neglected under typical operating conditions of silicon detectors in high energy physics.

3.4.5 Interface generation current

As is indicated in fig. 3.2, the silicon surface is passivated by a silicon dioxide film. The interface between silicon and oxide is characterised by high mechanical stress and high defect densities. Various defects at the interface have levels in the silicon band gap and act as charge carrier generation centres. As soon as the silicon surface at the interface gets depleted, the generated carriers drift along the electric field and contribute to the reverse current of a nearby pn-junction, e.g. the strip or pixel cell. Because of the generation process at the interface, this current is called interface generation current,

$$I_{ox} = e_0 n_i S_0 A_{gate}, \tag{3.19}$$

with n_i beeing the intrinsic charge carrier concentration, S_0 the surface recombination velocity and A_{gate} the depleted silicon surface area.

The interface generation current depends on the manufacturing process of the device as well as on the particular sensor design, as e.g. discussed in [WUE97]. Due to its sensitivity to ionising radiation it will be a major item of investigation in this work.

3.5 Radiation damage

3.5.1 Introduction

There are two different damage mechanisms, respectively ionisation induced damage in the silicon oxide layer and displacement damage occuring in the silicon bulk. Ionisation induced radiation effects are subject of this thesis and will be introduced in detail later in this work. In the following a brief introduction to bulk damage is given which is helpful for a discussion of the overall radiation hardness of silicon detectors later on.

Traversing particles loose energy by interactions with the silicon lattice. This can either happen by ionisation, which is fully reversible in semi-conductors or by knocking out lattice atoms and causing their displacement. Displacement damage is not reversible and leads to the so-called radiation induced bulk damage. As a consequence of lattice damage, detector parameters degenerate and the operation points change. Defect clusters, i.e. regions of high defect densities and quasi amorphous structure, are assumed to be responsible for an increase in volume generation current over several orders of magnitude, increasing the noise and power consumption of a detector. Singular defects (point defects) alter the effective doping concentration of the substrate and all operating parameters related to it like the full depletion voltage. Defects can act as charge traps in the bulk, too. Trapping centres capture fractions of the created signal charge which is then lost for read-out. A review of radiation damage in silicon can be found e.g. in [WUN96b].

3.5.2 Basic mechanism

To remove an atom from its lattice place an average energy of 25 eV must be transfered [VLI80]. The first atom hit by incident radiation is called *primary knock on atom.* As far as its remaining energy after being removed from the lattice is high enough, it can knock out further atoms. When the PKA transferred its energy it remains on an interstitial position in the lattice.

The minimum energy of the incident particle required for transferring the 25 eV to a lattice atom depends on the particle mass. In tab. 3.1 the minimum energies for

particle	mass [MeV]	$E_{\min}$ [eV]
electron	0.511	270000
proton, neutron	938	188
pions	140	1188
silicon ions	26300	25

Table 3.1: *Minimum energy for PKA creation from head-on collision, [Wun92].*

the most important particles are listed. The according cross-sections for the energy transfer are given in tab. 3.2.

The non-ionising energy loss (NIEL) can be calculated from the damage function D(E) [ROS00]. Input parameters for the calculation are the cross-sections of the interaction and the fraction of energy lost by ionisation. NIEL is proportional to the damage function,

$$\frac{dE_{\mathrm{NIEL}}}{dx}(E) = \frac{N_A}{A} D(E). \tag{3.20}$$

For a comparison of damage introduced from particles with individual energy spectra, their damage efficiency is studied relatively to the damage of neutrons with an

particle	T_{max} [eV]	<T> [eV]	interaction	cross-section [b]
electron	155	46	Coulomb	44
proton	133700	210	Coulomb	17950
neutron	133900	50000	elastic nuclear scattering	3.7
Si ions	1000000	265	Coulomb	502500

Table 3.2: *Maximum and average energy transfer to a silicon atom by particles of 1 MeV incident energy, [Wun92].*

energy of 1 MeV. Therefore, for each type of particle and energy there can be obtained a normalisation factor κ,

$$\kappa = \frac{\int\limits_{E_{\min}}^{E_{\max}} \phi(E)D(E)dE}{D_{\mathrm{n}}(1\ MeV) \int\limits_{E_{\min}}^{E_{\max}} \phi(E)dE}. \tag{3.21}$$

ϕ denotes the particle fluence and D_n the damage function for 1 MeV neutrons (D_n(1 MeV)=95 MeVmb).

3.5.3 Influence on characteristic parameters

3.5.3.1 Volume generation current

Exposure to radiation causes the reverse current to increase significantly. From systematic studies it was observed that the current increase is proportional to the particle fluence,

$$\Delta I = \alpha \phi_{eq} V, \tag{3.22}$$

with α being the current related damage factor, ϕ_{eq} the normalised particle fluence and V the volume of the depletion zone. This linear dependence on the particle fluence was found to be valid for various kinds of silicon substrates, which were for example grown by the Czochralski or the float-zone method or as an epitaxial film as well as for different initial effective doping concentrations [MOL99].

Beside the fluence dependence, the radiation induced current increase is a function of time, too. More precisely, the current related damage factor decreases with time. Generally, an exponential decrease was observed which, for long observation times, changes into a logarithmical annealing [MOL99],

$$\alpha(t) = \alpha_I \cdot \exp(-\frac{t}{\tau_I}) + \alpha_0 - \beta \cdot \ln(t/t_0) \tag{3.23}$$

with

$$
\begin{aligned}
\alpha_I &= (1.23 \pm 0.06) \cdot 10^{-17} A/cm \\
\frac{1}{\tau_I} &= k_{0I} \cdot \exp(-\frac{E_I}{k_B T_a}) \\
k_{0I} &= 1.2^{+5.3}_{-1.0} \cdot 10^{13}\ s^{-1} \\
E_I &= (1.11 \pm 0.05)\ eV \\
\beta &= (3.07 \pm 0.18) \cdot 10^{-18}\ A/cm \\
\alpha_0 &= -(8.9 \pm 1.3) \cdot 10^{-17}\ A/cm + (4.6 \pm 0.4) \cdot 10^{-14}\ AK/cm \cdot \frac{1}{T_a}
\end{aligned}
$$

3.5.3.2 Effective doping concentration

Radiation induced changes of the defect concentrations in the silicon bulk lead to a alteration of the effective doping which directly determines the depletion voltage.

Systematic investigations have shown that the effective doping depends on the particle fluence as well as on time. It can generally be parametrised by

$$\Delta N_{eff}(\phi_{eq}, t(T_a)) = N_{eff,0} - N_{eff}(\phi_{eq}, t(T_a)), \tag{3.24}$$

where $N_{eff,0}$ represents the doping of the unirradiated device, ϕ_{eq} the equivalent fluence and $t(T_a)$ the duration at a certain temperature. It has to be noted here that the annealing is accelerated at high temperatures whereas it can be almost frozen in for low temperatures, e.g. -20 ^{o}C or less.

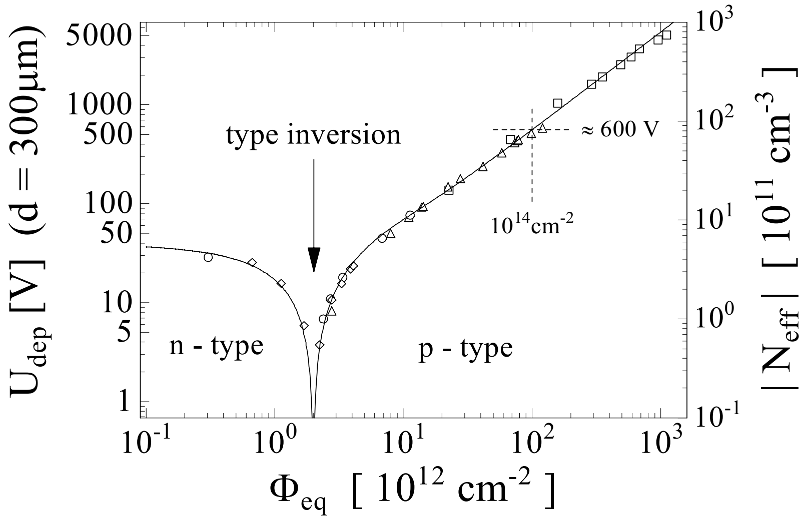


Figure 3.6: *Effective doping concentration as a function of particle fluence. [WUN92]*

Fig. 3.6 shows the development of the effective doping as a function of particle fluence for n-type silicon. For low fluences N_{eff} decreases with fluence which is mainly due to a removal of donor states and the creation of acceptor like states. Therefore, at a certain fluence, the conduction type of the n-type silicon is inverted to p-type which becomes more pronounced for increasing fluences.

As it was the case for the radiation induced leakage current, there is annealing of N_{eff} occuring, too. There are three different components of the effective doping with individual annealing behaviour,

$$\Delta N_{eff}(\phi_{eq}, t(T_a) = N_A(\phi_{eq}, t(T_a)) + N_C(\phi_{eq}) + N_Y(\phi_{eq}, t(T_a)), \qquad (3.25)$$

where N_A denotes the *beneficial annealing*, N_C the *stable damage* and N_Y the *reverse annealing* component. The development of N_{eff} with time and the annealing components are depicted in fig. 3.7. Beneficial annealing dominates the change in N_{eff} on

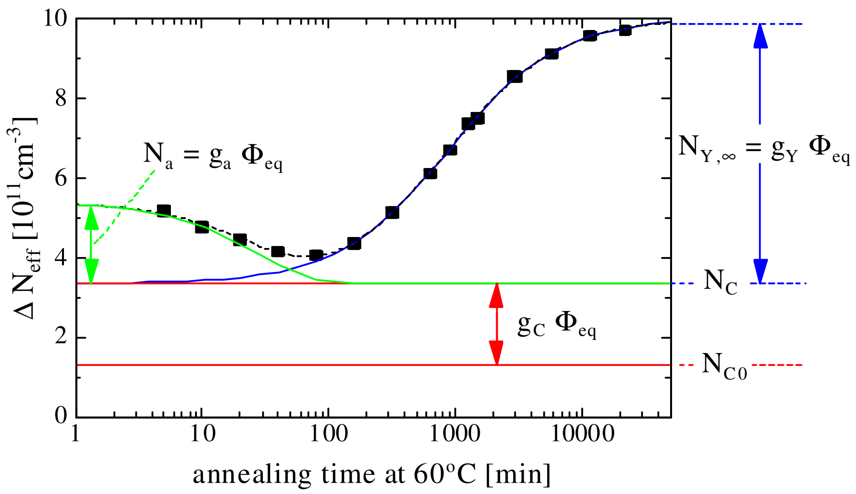


Figure 3.7: *Annealing behaviour of the effective doping concentration after irradiation. [MOL99]*

short time scale. It can be accelerated or decelerated by heating or cooling a detector. The beneficial annealing is dominated by a reverse annealing which causes the effective doping to increase again. In the transition of beneficial to reverse annealing N_{eff} has a minimum which is roughly determined by the stable damage component which does not show any annealing respectively time dependency at all.

3.5.3.3 Oxygen diffused silicon

In the framework of the RD48 project at CERN a technique was developed reducing the sensitivity of the effective doping concentration to displacement damage [ROS99]. This was achieved by introducing an oxygen concentration in the order of 10^{17}cm^{-3} in the silicon bulk employing a simple high temperature diffusion process. The wafers remain in the oxidation furnace after the standard oxidation procedure in an inert ambient. Diffusion times between 16 hours and 72 hours as well as diffusion temperatures around 1100^oC have been tested: the beneficial effect of the oxygen is independent of the particular diffusion time and temperature within the tested range.

In particular, the higher oxygen concentration provides two crucial improvements. First, the effective doping concentration is significantly less altered by radiation than for standard silicon. This effect was observed for irradiations with charged hadrons whereas no beneficial effect was found for neutron irradiations. Concerning the reverse current, there is no difference between the oxygen diffused and the standard material. As a second improvement the maximum effective doping concentration which is obtained after full reverse annealing saturates on a certain level which is independent of the particle fluence. In standard silicon no such saturation occurs. This effect may not be mixed up with the saturation of the effective doping cocentration after reverse annealing occuring for a single fluence level.

Although the exact underlying mechanisms are not fully understood, these results have been confirmed now in large statistics. The full performance of the oxygenated silicon is obtained for applications mainly suffering from charged hadrons like the b-physics layer of the ATLAS Pixel Detector, where more than 80 percent of the expected total fluence is contributed by pions. Fig. 3.8 shows the calculated development of the

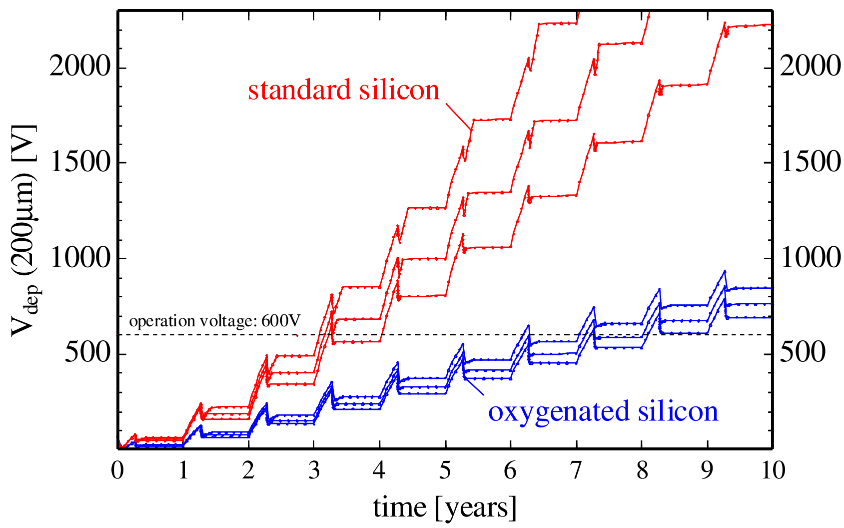


Figure 3.8: *Calculated development of the depletion voltage of pixel sensors of the b-physics layer versus operating time. The differences between curves of the same colour are due to different maintenance and warm-up scenarios assumed for the calculations.*

depletion voltage as a function of time for the ATLAS b-physics layer. The blue curves have been obtained for the oxygen diffused silicon whereas the red curves referre to standard silicon. The maximum operation voltage for the sensors is indicated by the dashed line at 600 V. The advantage of using oxygenated silicon for the pixel sensors can be clearly seen in fig. 3.8. It is possible to operate these sensors almost fully depleted for at least seven years, whereas the depletion voltage of the standard silicon sensors exceeds 600 V at the end of the second year already. The differences between the blue lines and between the red lines are due to assuming slightly different maintenance scenarios and warm-up times.

Chapter 4

Surface properties

4.1 Thermal Oxides

4.1.1 Introduction

For position resolving silicon detectors as well as for optical sensors like CCDs[1] high quality silicon mono-crystals are required to achieve good sensitivity and signal properties. Further aspects for the processed final devices are good long-term and high-voltage stability.

Detector graded silicon is produced using the float-zone technique, which provides high purity silicon and a high periodicity of the lattice structure. Before processing, the cylindric mono-crystals have to be sliced into single discs, i.e. wafers.

The surface of the wafers is characterised by the abrupt termination of the highly periodic lattice structure. As is characteristic, silicon surface atoms (Si_s) are only partially surrounded by neighbour atoms, so there are free valencies left, which are called *dangling bonds.* For this reason it is obvious that the untreated wafer surface is electrically and chemically highly reactive. E.g. even small changes in the electric surface potential will lead to significant change in the charge distribution. Furthermore, an agglomeration of impurity atoms from the surrounding atmosphere is possible due to the high reactivity, in presence of oxygen a spontaneous oxidation of the surface silicon atoms occurs. Also a characteristic of untreated surfaces is that impurities can easily diffuse into the originally high purity silicon and change its properties.

With respect to producing high quality sensors, the silicon surface has to be passivated electrically as well as chemically, otherwise it is unusable for device production. In other words, a barrier agains diffusion and agglomeration of impurity atoms is needed and the dangling silicon bonds must be fixed to obtain electrical stability.

A very reliable and reproduceable way to solve the above problems is to passivate the silicon surface by a thermally grown silicon oxide film. The oxide has good insulation and mechanical properties and stabilises the crystal surface with respect to electrical and chemical reactivity. Furthermore, oxide films are a barrier agains uncontrolled

[1] Charge Coupled Devices

diffusion and, appropiately opended by structured etching, can be used as a mask for later dopant implantations.

Although there is great benefit from oxidising the silicon, there are some intrinsic problems left which are crucial to be solved for high end processes. First of all, there is still a transition region existing between the mono crystalline silicon and the silicon oxide film. As is typical for such transition regions, there are high defect concentration which strongly affect the performance of the final device. The quality, that is the amount of electrically acive defects, strongly depends on the wafer treatment before the thermal oxidation like polishing and cleaning. But the oxidation technique and process itself is of the same importance to the defect density created. In the following sections the crucial mechanisms and defects are discussed, being the base for a systematic comparison of different oxide and radiation hardness.

4.1.2 Thermal oxide films

The challenge for high quality processes is to produce oxide films of high quality, i.e. low defect densities and high voltage stability. This is basicaly done by a reaction of oxygen with silicon surface atoms at high temperature, which is called *thermal oxidation.* Compared to room-temperature oxidation, much larger growth rates are achievable as well as a precise control of the chemical composition of the oxide film and its thickness.

Thermal oxiations are performed either in a pure oxygen atmosphere (dry oxidation) or in a water vapour ambient (wet oxidation). The fundamental reation schemes are

$$\mathrm{Si\ (solid)} + \mathrm{O_2\ (gas)} \longrightarrow \mathrm{SiO_2\ (solid)} \tag{4.1}$$

and

$$\mathrm{Si\ (solid)} + \mathrm{H_2O\ (gas)} \longrightarrow \mathrm{SiO_2\ (solid)}. \tag{4.2}$$

During the growth process silicon atoms are continuously consumed from the crystal, approximately 44 % [STE56] of the total film depth is grown into the former silicon substrate.

Thermally grown silicon oxides on silicon are characterised by an amorphous structure (*fused silica*) with a melting point around 1710 ^{o}C. Below the melting point it is thermodynamically unstable and tends to form crystalline oxide (quartz). This process is called devitrification and is nearly completely frozen in at temperatures below 1000 ^{o}C.

According to the model of Stevels and Kats [STE56], the microscopic structure of silicon oxide is schematically depicted in fig. 4.1. The elementary cell of the film is formed by a single silicon ion (Si^{4+}) which is bonded to four surrounding oxygen atoms (SiO_4^{4-}). These tetrahedical cells are interconnected by the oxygen atoms (bridging oxygen, Si-O-Si) to a flexible network. The physical properties of the oxide film are mainly based on the partially covalent and ionic nature of the Si-O bond. Bonding angels may vary between 120^o and 180^o with a probability maximum at 147^o, allowing local rearrangements of the network. The distance of a Si-O bond is $d_{Si-O} = 1.62$ Å and

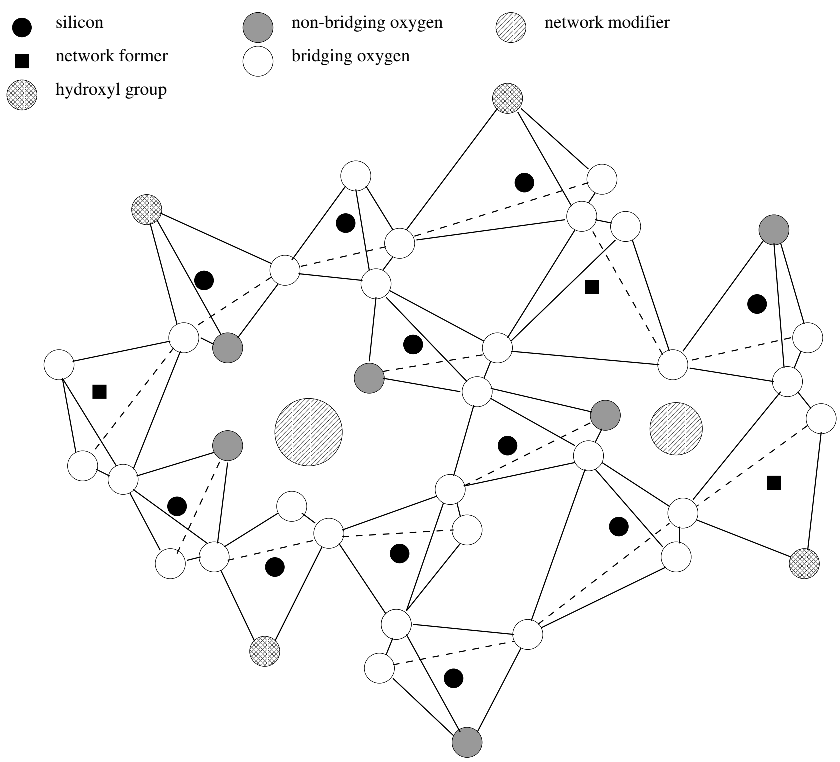


Figure 4.1: *Schematic structure of fused silica. [REV65]*

between two oxygen atoms of a tetrahedron $d_{O-O} = 2.27$ Å. Due to the "open" geometry of the film, diffusion of atoms and small molecules is enhanced. Table 4.1 summarises the most important properties of amorphous silicon oxide films.

As indicated in fig. 4.1 there are various kinds of defect or impurity induced local modifications of the network possible which have implications on the physical properties of the film.

One of the most characteristic defects is the non-bridging oxygen atom (Si-O·). It is still part of a tetrahedical cell but the bridging bond to a neighbour cell is missing. Non-bridging oxygen atoms are responsible for the more open structure of the amorphous film and its lower density compared to quarz-like films. Furthermore, the diffusion of atoms is enhanced by this.

Local rearrangements of the network are mainly due to migration of oxygen atoms because the silicon atoms are tightly fixed by four bonds to the tetrahedron and cannot move. A typical defect due to oxygen movement is the oxygen vacancy, which can either be a bridging oxygen or a non-bridging oxygen. The latter one is more likely because it is less tightly bonded. A missing oxgen (oxygen vacany) always creates a positive space charge.

Beside oxygen vacancies, the diffusion of impurities into the oxide film modifies the local cell structure. Impurity atoms which replace an oxygen or silicon are called

oxide property	magnitude
density	2.27 $\frac{g}{cm^3}$
dielectric constant	3.4 (O_2 ambient), 3.8 (H_2O ambient)
dielectric strength	5-10·10^6 $\frac{V}{cm}$
energy gap	8.8 eV
linear expansion coefficient	5·10^{-7} $\frac{cm}{cm^oC}$
melting point	1710 ^{o}C
molecular density	2.3·10^{22} $\frac{1}{cm^3}$
refractive index	1.46
specific heat	1 $\frac{J}{g^oC}$
stress in film on silicon	2-4·10^9 $\frac{dyn}{cm^2}$

Table 4.1: *Properties of thermally grown silicon oxide. [WOL86]*

substitutional defects, whereas interstitial atoms are not integrated into the tetrahedical structure.

Substitutional atoms like B^{3+} or P^{5+} tend to replace a silicon atom. Those *network formers* modify the local bonding network and are the origin of glassy cells, i.e. B_2O_3 or P_2O_5. The additional electron of the phosphorous atom is used for the formation of a bridging oxygen, but the missing electron of the boron cracks up an oxygen bridge. Boron therefore weakens the polyhedra network.

Oxidized Na, K, Pb or Ba occupy interstitial positions in the oxide network. They give away their oxygen atom to the network which there consumes a bridging oxygen to form two non-bridging atoms. As a consequence, the oxide becomes porous and the diffusion of other impurities is enhanced. Metal oxides on interstitial positions are called network modifiers.

The most important contamination of thermal oxides is water vapour, either coming from the atmosphere or from the oxidation ambient during a wet oxidation. The water molecule reacts inside the film with a bridging oxygen atom and forms two stable hydroxyl groups,

$$\mathrm{H_2O + Si - O - Si \longrightarrow Si - OH + OH - Si.} \quad (4.3)$$

These defects have been identified by infrared absorption experiments and are the origin for various defects and for the sensitivity to ionising radiation.

4.1.3 Crucial growth parameters

For the planar process a high quality oxidation is crucial. An overview of different oxide films used in the planar process is given in tab. 4.2. Much care must be taken to control film composition, growth rate and defect densities.

The absolutely most important task is to control the composition of the oxidation ambient, because there are always traces of contamination gasses left which are introduced from several sources, affecting growth rate and defect densities. However,

thickness [Å]	use
60-100	tunnel oxide (e.g. for EAROMs)
150-500	gate-oxide, dielectric layer (MOS devices)
200-500	isolation (LOCOS)
2000-5000	mask for ion-implantation and diffusion
	electrical and chemical passivation
3000-10000	field oxide

Table 4.2: *Use of silicon oxide in the planar process [WOL86].*

additives in the oxidation ambient must not necessarily have negative effect on the film quality, they can even improve it.

In the following paragraphs, the most important additives, regardless wether they are an unwanted or well directed, and their meaning for the oxidation process will be addressed. Although it might be impossible to trace back certain effects evaluated on oxide films to the process parameters, the basic knowledge is essential for a broad-banded discussion later on.

4.1.3.1 Water vapour

It has been observed that water vapour significantly increases the oxidation rate. This may become a problem with respect to controlling film thickness and reproducibility in case of changing or unknown water concentrations. The main water source is the oxygen gas itself. Another source is the water diffusion through the oxidation furnace from outside. Additionally, at high temperatures, hydrogen carbonat dissociation and a reaction of molecular hydrogen with oxygen produce water,

$$\mathrm{H_2CO_3} \longrightarrow \mathrm{H_2O} + \mathrm{CO_2} \tag{4.4}$$

$$2 \cdot \mathrm{H_2} + \mathrm{O_2} \longrightarrow 2 \cdot \mathrm{H_2O}. \tag{4.5}$$

Nevertheless, in modern process lines there are various techniques implemented to reduce the water concentration to 1 ppm (parts per million) or less. Therefore, in case of detectors processed by an experienced vendor, there is no risk from water contamination to be expected.

4.1.3.2 High dopant surface concentration

As may be the case for an oxide growing on heavily doped silicon or with an inhomogeneous distribution of impurity densities, high surface concentration (10^{18} cm^{-3} or higher) of e.g. boron, arsenic, phosphorous or antimony will change the oxidation rate by diffusing into the oxide network or segregating in the transition region. Depending on the distribution at the surface, local variations of the film thickness have to be taken into account due to locally different oxidation rates. This, for example, will cause local variations of characteristic parameters of the processed final devices.

In the detector production process the most important high concentration (10^{19} cm^{-2} or higher) impurities are Boron and Phophorous as standard dopant atoms.

Boron for example segregates into the oxide during the growth process. As discussed in the previous section, boron weakens the network and increases diffusion of water and oxygen. As long as the film growth rate is determined by the diffusion process of oxygen into the transition region, boron improves diffusion. This is the case for oxidations in a wet ambient at temperatures around 1000^oC or below.

Other than boron, phosphorous piles up at the silicon surface without diffusing into the oxide. The phosphorous increases the reaction rate in the transition region by shifting the Fermi-level and increasing the vacancy concentration, which then enhance the oxidation rate. Phosphorous pile-up has to be considered especially at low oxidation temperatures (900^oC).

4.1.3.3 Crystal orientation

The effect of the crystal orientation can be explained by Ligenza's model [LIG61] which is based on the reaction of water molecules with a Si-Si bond at the silicon surface. It predicts a rate dependence on the density of available bonds for the oxidation at the silicon surface. Here the large water molecules block each other from reacting with the silicon. Furthermore, the activation energy for the oxidising reaction changes with the substrate orientation because the bonding angels differ. Applying the identical oxidation process to substrates with different orientations will lead to different oxide thicknesses. And, as a result of the different bond densities, the defect concentrations are a function of the substrate orientation. In particular, higher defect densities must be expected for surfaces of <111> silicon, assuming that the defect density at the interface is determined by the bonding density only[2]

4.1.3.4 Chlorine additives

Several device and oxide properties can be enhanced by chlorine additives in the oxidation ambient. Typical chlorine additives are anhydrous hydrogen chloride (HCL), molecular chlorine (Cl_2), tri-chloro-ethylene (TCE) and tri-chloro-ethane (TCA).

Chlorine was found to reduce mobile oxide charges which reduce long-term stability, the lifetime of minority carriers is increased in the underlying surface silicon, which improves the performance of silicon sensors and MOSFETs[3]. Furthermore, the defect and charge densities in the oxide bulk as well as at the interface are reduced and the number of stacking faults in the interface region is reduced. Therefore chlorine additives improve radiation tolerance as well as electrical stability of the final device. TCA or TCE oxidations are common practice in modern processing lines. A typical oxidation cycle might look as follows,

dry oxidation at 850 ^{o}C

[2] In practice numerous preparation steps and process parameters determine the defect density as for example the polishing procedure of the wafer before processing.

[3] Metal Oxide Semiconductor Field Effect Transistor

$\downarrow$
TCA or TCE oxidation at 850 ^{o}C
$\downarrow$
TCA oxidation at low partial pressure at 1050 ^{o}C
$\downarrow$
N_2 annealing[4] at 1050 ^{o}C

4.2 Intrinsic defects

4.2.1 Nomenclature

In the previous sections either the silicon surface, the transition region or the silicon oxide bulk have been merged into the collective term *surface*. For the following discussion a more precise nomenclature is needed which allows a physically accurate distinction between different defect locations and their response to electrical signals used for characterisation later on. An appropriate nomenclature is given in [FLE93] which has been adopted for this work and will be introduced here.

In fig. 4.2 a schematic cross-section of the surface is given, indicating the different regions. On top of the silicon oxide bulk a metal layer is deposited, as is e.g. known as gate-contact from MOS capacitors. Most of the silicon oxide film consists of stoichiometric oxide, which is called oxide bulk. The border region is located between the stoichiometric oxide and the silicon crystal. It has got a thickness of approximately 30 Å and is characterised by high mechanical stress. In this layer defect density is higher due to bond stress which forms a sink for impurities like gold, nickel, iron or alkali metals and chlorine, too. The transition between mono-crystalline substrate and oxide occurs rather sharp at the interface, which extends over a few nanometers only. Viewing from the border region, it is built-up of a mono-layer of high stress SiO_2, followed by two layers of incompletely oxidised Si_2O_2 and Si_2.

According to [FLE93], the term *trap* is used in connection with the spatial position of a defect (see fig. 4.2(b)), whereas the electrical behaviour of a defect is meant by *state* (compare fig. 4.2(c)).

Due to their position deep in the oxide bulk, far away from the crystal, oxide bulk traps (ot) are unable to exchange charge with the underlying silicon. This is completely different for border traps (bt) and interface traps (it). Located closely to the interface, they are able to exchange charges with the underlying crystal and thus alter their charge state. Interface traps for example can recharge with frequencies in the order of MHz.

With respect to their electrical behaviour border traps and interface traps are summarised as switching-states, whereas fixed-states consist of oxide bulk traps.

4.2.2 Oxide bulk defects

Thermally grown oxide films on silicon substrates always contain various kinds of intrinsic network defects, although concentration in high quality oxides is low.

[4] Annealing effects are discussed in the next section

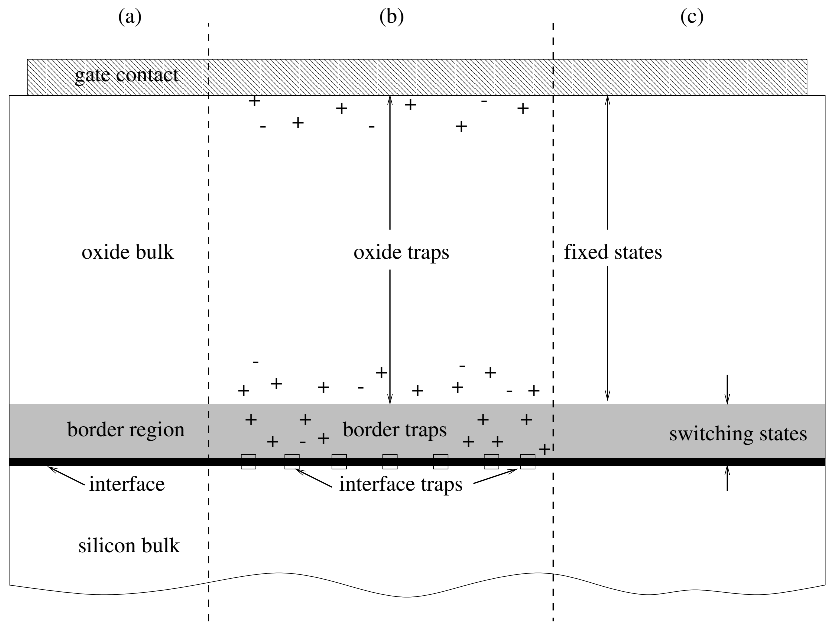


Figure 4.2: *Schematic diagramme of silicon surface. (a) Surface regions, (b) trap locations, (c) state nomenclature. [FLE93]*

Tab. 4.3 gives an overview of oxide network defects, the most important are the tri-valent silicon, the non-bridging oxygen, interstitial oxygen and all defects which are associated with hydrogen. Hydrogen ions are of special importance because they passivate dangling bonds by attaching to them.

The estimated energy levels of the network defects are depicted in fig. 4.3. It has to be stressed, that most defects are donor levels, which is the reason that net oxide charge density is always positive.

Altough net oxide charge is always positive, there are two mechanisms proposed for negative charge build-up which then reduces the effective oxide charge density. Due to the high electron affinity of the interstitial oxygen, it can act as an acceptor level and contribute negative space charge. For the non-bridging oxygen, is is possible to complete its outer shell by accepting a bond electron,

$$\equiv \mathrm{Si} - \mathrm{O}\cdot \longrightarrow \equiv \mathrm{Si} - \mathrm{O} : + \mathrm{h}^{+}, \tag{4.6}$$

with h^{+} denoting a hole. Altough negative space charge is oberved rarely only, these mechanisms should be kept in mind for the final discussion of chapter 9.

Beside intrinsic network defects, traces of alkali ions in the oxide film are risky, too. They are mobile even at room temperature and drift in an applied electric field. Thus, when considering MOS devices for example, a change of charge distribution during operation leads to uncontrollable shifts of operation points etc. However, alkali ions are mainly introduced by improper handling, whereas a contamination during processing

defect	symbol	behaviour
tri-valent silicon	$\equiv$Si$\cdot$	single donor
non-bridging oxygen	$\equiv$Si-O$\cdot$	single acceptor
oxygen vacancy V_O	$\equiv$Si$\cdot$ $\cdot$Si$\equiv$	double donor
silicon vacancy V_{Si}		single donor
oxygen interstitial O_I		single donor
silicon interstitial Si_I		double donor
pair and higher complexes O_2, SiO, $V_O V_O$		
silicon oxide	$\equiv$Si-O-Si$\equiv$	
Hydrogen impurity	$\equiv$Si-H	
Hydroxyl group	$\equiv Si^+:OH^-$	
Metallic ion		

Table 4.3: *Intrinsic network defects of thermally grown silicon oxide films [SAH76].*

is unlikely.

Fig. 4.4 gives a summarising overview of the different types of charges in the silicon oxide.

4.2.3 The Si/SiO$_2$ interface

The generation and existance of interface traps is of major importance for the electrical performance of a processed device. Interface states create energy levels in the silicon band gap which for example act as charge traps or charge generation centres.

Although the physical mechanisms of interface state build-up are not fully understood yet, models have been developed which suggest physical explanations for interface state generation.

One modeling approach is to trace back the formation of interface traps directly to typical interface defects like stacking faults, excess silicon atoms, excess oxygen atoms or molecule fragments remaining from incomplete oxidation as well as impurities. These defects are supposed to create states within the silicon band gap by disturbing the periodical order of the underlying crystal lattice. Nevertheless, this model does not account for radiation induced damage as well as a correlation between oxide bulk states and interface states which have been observed.

The correlation between oxide charges and interface states in particular is considered in the *Coulombic model* [GOE68]. Oxide charges are proposed to induce deformations of the potential distribution at the interface. Quantum states in these potential wells result in interface states.

Another approach is proposed by the *bonding model* [LAU80], which employs the distribution of bonding angels and stretched bonds to explain the presence of interface traps. As basic origin the non-stoichiometric composition of the interface and mechanical stress are likely.

Starting on the existence of two intrinsic defects, i.e. the tri-valent silicon and the

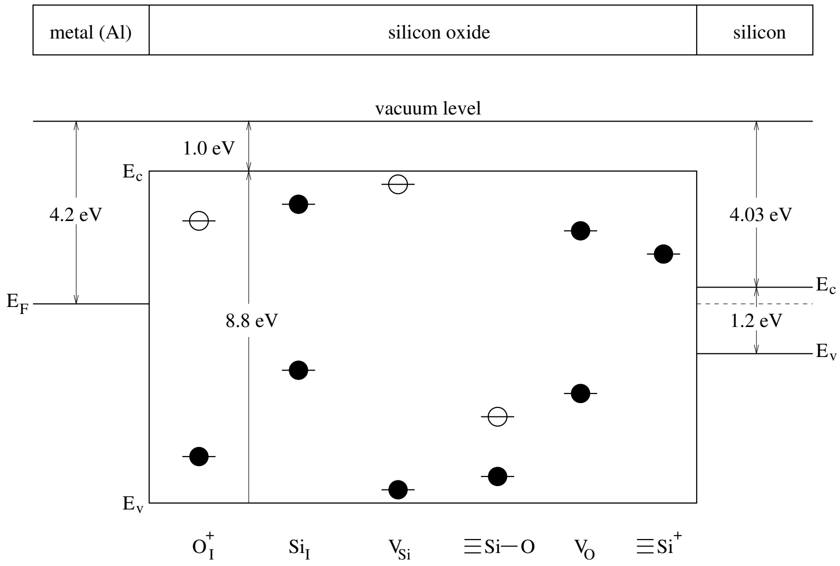


Figure 4.3: *Schematic diagramme of defect levels in the oxide band gap. The dark circles represent donator levels, the open acceptor levels. [SAH76]*

oxygen interstitial, Sah [SAH76] characterises the interface as follows. In high temperature non-oxidising ambients oxygen deficient centres are produced in high conentration due to missing oxygen (≡Si· ·Si≡ or the tri-valent silicon). These centres disturb the charge and valence bands of the silicon and generate new states in the band-gap.

4.3 Annealing techniques

Bulk defects as well as interface states worsen the quality of the oxide film and have to be kept as low as possible. For this reason annealing techniques are needed to inactivate the defects. The basic idea of all annealing methods is to passivate defects by a hydrogen or hydroxide agglomeration.

Interface state densities can be efficiently reduced by a low-temperature (350^{o}C-500^{o}C) annealing step in an hydrogen enriched ambient, like forming-gas (H_2-N_2) or water atmosphere. The hydrogen or hydroxide ions diffuse to the interface where they react with the characteristic defects like tri-valent silicon or a silicon surface atom with a dangling bond,

$$\equiv \mathrm{Si}^+ \cdot + \mathrm{OH}^- \longrightarrow \equiv \mathrm{Si} - \mathrm{OH}, \tag{4.7}$$

$$\mathrm{Si}_s^- \cdot + \mathrm{H} \longrightarrow \mathrm{Si}_s - \mathrm{H}. \tag{4.8}$$

It has to be noted that a low-temperature water annealing can only be done after metal deposition, because the hydrogen has to be produced by a chemical reduction of the metal,

$$2\mathrm{Al} + 3\mathrm{H_2O} \longrightarrow \mathrm{Al_2O_3} + 3\mathrm{H_2}. \tag{4.9}$$

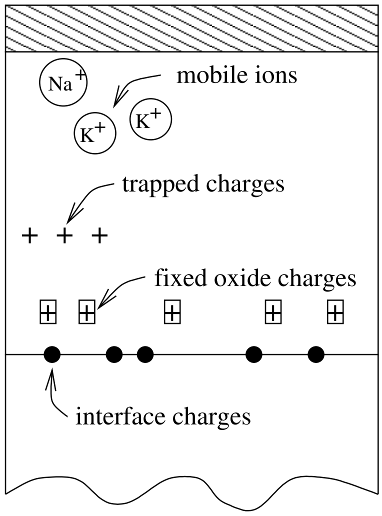


Figure 4.4: *Charges in the silicon oxide. [DEA80]*

However, further treatment at high temperature (1000^{o}C) will lead to a dissociation of the silicon to hydrogen bond. Instead of the missing hydrogen, a reaction of the silicon surface atom with a non-bridging oxygen defect is possible,

$$\mathrm{Si_s} \cdot + \cdot \mathrm{O} - \mathrm{Si} \equiv \longrightarrow \mathrm{Si_s} - \mathrm{O} - \mathrm{Si} \equiv, \tag{4.10}$$

which then is fully annealed.

Hydrogen enriched atmosphere can also be used for annealing of oxide bulk defects. Again, the idea is to reduce the number of dangling bonds by hydrogen or hydroxide agglomeration,

$$\equiv \mathrm{Si} \cdot + \cdot \mathrm{O} - \mathrm{Si} \equiv + \mathrm{H_2O} \longrightarrow \equiv \mathrm{Si} - \mathrm{OH}\ \mathrm{HO} - \mathrm{Si} \equiv. \tag{4.11}$$

4.4 Radiation effects

4.4.1 Introduction

Exposure to ionising radiation has significant impact on the defect generation and activation in silicon oxide films, because radiation damage mainly is a regeneration process of deactivated defects. It is necessary to understand the basic mechanisms of ionisation induced damage before a systematic evalution of different oxide films with respect to radiation sensitivity can be done. As will come out in the following, the film processing, preparation and temperature treatments have crucial influence on the performance after radiation.

As discussed in the previous sections, there are various defects present even in freshly produced high quality oxide films, although there are methods to anneal those defects. Radiation damage, induced by ionising radiation, generally reactivates the passivated defects, this is called regeneration process. Because an efficient annealing of defects is strongly related to hydrogen, hydrogen also is of special importance for radiation tolerance.

As was proven in many experiments, exposure to ionising radiation causes the positive space charge density to increase as well as the interface state density. In the following models are presented which are an attempt to described the underlying mechanisms. It is unavoidable to employ different models here because the exact physic mechanisms are not fully understood, yet.

4.4.2 Oxide charge

The build-up of positive space charge due to ionising radiation can be described employing the two most important intrinsic network defects, i.e. the tri-valent silicon and the oxygen interstitial [SAH76],

$$\equiv \mathrm{Si}\cdot \;+\; \mathrm{rad} \longrightarrow \equiv \mathrm{Si}^{+} + \; \mathrm{e}^{-}, \tag{4.12}$$

$$\mathrm{O_I} + \mathrm{rad}(\mathrm{h}^{+}) \longrightarrow \mathrm{O_I^{+}}. \tag{4.13}$$

It is necessary to distinguish between both reactions, because the underlying mechnism is slightly different.

The ionisation of the tri-valent silicon, shown in equation 4.12, is based on impact ionisation by an energetic electron, represented by the term *rad*.

In equation 4.13 the ionisation of an interstitial oxygen is described by capturing a radiation induced hole, *rad(h^+)*.

The generated electrons and holes are charged. For this reason a dependence of the induced radiation damage on the applied electric field during exposure must be expected. Assuming a positively biased gate electrode, negative charge drifts towards the electrode whereas positive charge is moved towards the interface. In this scenario maximum damage efficiency must be expected and was observed, indeed. In case of the reverse field polarity less damage is introduced. At zero field, recombination of electron-hole pairs is enhanced, thus the created damage is lowest.

According to equation 4.11, the number of dangling bonds in the oxide bulk could be reduced by water or hydrogen annealing. Exposing such annealed oxides to ionising radiation causes a dissociation of the silicon to hydrogen bonds. The hydrogen atoms then initiate a production of tri-valent silicon centres,

$$\equiv \mathrm{Si} - \mathrm{O} - \mathrm{Si} + \mathrm{H} \longrightarrow \equiv \mathrm{Si}^{+} - \mathrm{OH}^{-} + \equiv \mathrm{Si}^{+}\cdot \tag{4.14}$$

and

$$\equiv \mathrm{Si} - \mathrm{O}^{-}\cdot + \mathrm{H}^{+} \longrightarrow \equiv \mathrm{Si} - \mathrm{OH}. \tag{4.15}$$

a passivation of non-bridging oxygen defects by forming an agglomerated hydroxyl group. This results in an overall reduction of non-bridging oxygen defects a radiation induced increase in tri-valent silicon defects which results in positive space charge.

Some of the created positive space charge can be reduced by an electron trapping process occurring at a hydroxide group,

$$\equiv \mathrm{SiOH} \ + \ \mathrm{e}^- \longrightarrow \equiv \mathrm{SiO} :^- \ + \ \mathrm{H}^+. \tag{4.16}$$

A hydrogen atom is released and the negatively charged $\equiv$SiO recombines with a hole,

$$\equiv \mathrm{SiO} :^- \ + \ \mathrm{h}^+ \longrightarrow \equiv \mathrm{SiO}\cdot. \tag{4.17}$$

4.4.3 Interface states

Similar to oxide bulk damage, interface state density increases due to irradiation by hole trapping at the interface. Depending on the biasing conditions during irradiations, holes drift to the interface and induce states within the silicon band gap. The build-up time for these states depends at first on the drift time of the holes. This correlation is in agreement with the Coulombic model. But, nevertheless, interface state build-up continues over a much longer time than can be explained by hole drift. This motivates to assume a more complex generation process basing on chemical reactions [REV65]. As consequence from this, macroscopic device parameters must be expected to alter even during several months after the end of irradiation. Long-term stability for example is severely affected by this. A parameter model will be needed to predict those effects.

After [REV65], interface states are generated by breaking-up bonds between surface silicon atoms and hydrogen,

$$\mathrm{Si_s} - \mathrm{H} \ + \ \mathrm{h}^+ \ \longrightarrow \ \mathrm{Si_s}\cdot \ + \ \mathrm{H}^+, \tag{4.18}$$

$$\mathrm{Si_s} - \mathrm{H} \ + \ \mathrm{h}^+ \ \longrightarrow \ \mathrm{Si_s^+} \ + \ \mathrm{H}\cdot. \tag{4.19}$$

The silicon surface atoms now are able to electrochemically react with the underlying silicon to form interface states by providing dangling bonds,

$$\equiv \mathrm{Si_s^+} + \mathrm{e}^- \longrightarrow \equiv \mathrm{Si_s}\cdot. \tag{4.20}$$

Another model proposed for interface state generation assumes tri-valent silicon to be the major responsible defect. Originally passivated by hydroxide ions, radiation breaks up this connection,

$$\equiv \mathrm{Si} - \mathrm{OH} + \mathrm{rad} \longrightarrow \ \equiv \mathrm{Si}^+ \ + \ \mathrm{OH}^-, \tag{4.21}$$

and produces tri-valent silicon interface states. This reaction can either be started by electron impact ionisation or hole capture [SAH76].

The electron impact mechanism is depicted in fig. 4.5. The incident radiation produces energetic electron-hole pairs along its track (1) which then lose energy by plasma oscillations (2). The tri-valent silicon, originally passivated by a hydroxil group from previous annealing, captures the electron and shifts the hydroxide ion into an excited state (3). Then, after consuming two electrons from the silicon valence band, the

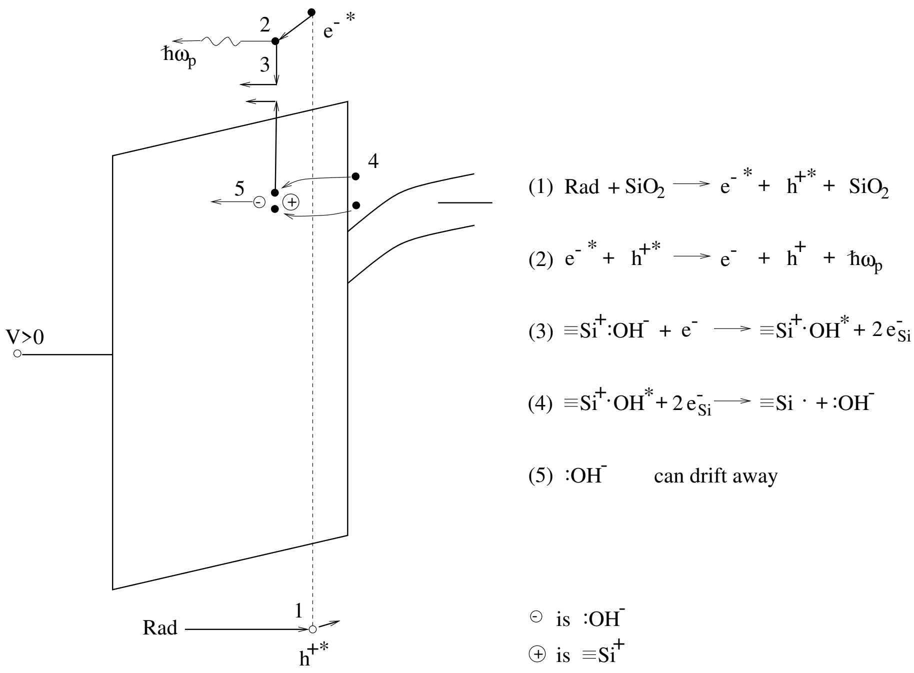


Figure 4.5: *Interface state build-up due to electron impact ionisation.[SAH76]*

hydroxide de-excites and separates from the tri-valent silicon (4). Now the negatively charged hydroxide can drift away in an applied electric field.

Hole capture occurs in a similar way, which is shown in fig. 4.6. The only difference is step (3), where now a hole is captured by the hydroxide ion, which compensates its negative charge.

Following the hydroxide model, only defects get activated which have been passivated by hydroxide ions before. Therefore on one hand the post-irradiation performance allows conclusions about the interface quality of the processed film, on the other hand radiation induced increase in interface state density is limited by the number of originally passivated tri-valent silicon centres. A saturation must be expected for high doses.

Considering that the negatively charge OH-ion is mobile in the oxide film, also here a dependence of the induced damage on the applied electric field must be considered. In case of a positively biased gate electrode the hydroxide will drift away from the interface. It is unlikely that the hydroxide will be captured again by the tri-valent silicon. Maximum damage has to be expected under these conditions. If the field polarity is vice-versa, the capture probability increases because the hydroxide drifts to the interface, less damage is created. If there is no field applied, the radiation induced increase of states will be minimised because immediate recombination is enhanced.

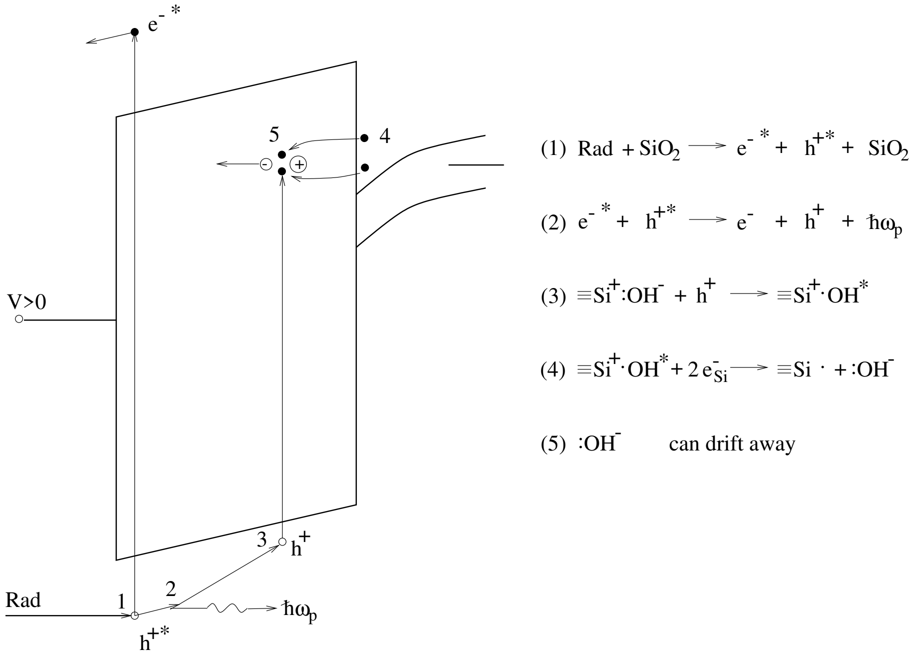


Figure 4.6: *Hole-capture mechanism. [SAH76]*

4.5 Characteristic parameters

4.5.1 Needs for quality assurance

In the previous sections it was shown that there are a large variety of different microscopic defects present in silicon oxide films. The wafer preparation, the thermal oxidation process and especially ionising radiation influence the defect densities. Consequently, the electrical properties of e.g. a MOS capacitor, a MOSFET or a silicon sensor are altered by these mircoscopic effects. It therefore is necessary to achieve a sufficient understanding of the correlation between mircoscopic effects and their impact on electrical characteristics of processed devices.

For this purpose a set of characteristic parametes is needed which allows a determination of oxide film and interface properties by applying electrical characterisation methods, aiming for a quantitative determination of defect densities and thus for an evaluation of surface quality. Furthermore, it must be possible to monitor radiation induced effects by these parameters, too.

Especially for systematic tests of ionisation induced radiation damage effects, a basic knowledge of the microscopic mechanisms is inevitable to understand and account for generic damage dependencies on e.g. the dose, the electric field applied during irradiation or saturation effects of damage components.

In the following the relevant surface parameters are introduced. They are be obtained from electrical measurements on e.g. MOS capacitors or gate-controlled diodes and are of great importance for process and quality control as well as monitoring of radiation induced effects.

4.5.2 Positive oxide charge density

Instead of referring to the individual charge contribution, an effective net sheet charge density N_{ox} if often employed to evaluate oxide quality, sufficiently describing their influence on the macroscopic operating parameters of MOS capacitors or MOSFETs.

The effective sheet charge density, which in the following will be referred to as *oxide charge density*, is assumed to be located close to the interface in the oxide,

$$N_{\mathrm{ox}} = N_{\mathrm{fs}} + N_{\mathrm{m}} + N_{\mathrm{ot}} + N_{\mathrm{it}}, \tag{4.22}$$

with

$$N_{\mathrm{m}} = \frac{1}{d}\int_0^d x\rho(x)_{\mathrm{m}} dx \tag{4.23}$$

$$N_{\mathrm{ot}} = \frac{1}{d}\int_0^d x\rho(x)_{\mathrm{ot}} dx. \tag{4.24}$$

$$\tag{4.25}$$

The fixed oxide charges N_{fs} and the interface trapped oxide charge N_{it} are by definition closely located to the interface and an intergration is not necessary.

4.5.3 Interface state density

Experimentally it is impossible to distinguish between different interface trap levels. Therefore it is useful to introduce a probability $D_{it}(\xi_s)$ per unit area to find an interface trap level within the energy range between ξ_s and $\xi_s + d\xi_s$ [NIC82]. $D_{it}(\xi_s)$ is often referred to as the interface state density per unit area and per electron volt, whereby ξ_s denotes the energy in the silicon band gap, measured relatively to the intrinsic level at the silicon surface. Because the intrinsic level at the silicon surface is shifted by band-banding, ξ_s is a function of band-bending, too. Assuming that an interface trap is located at an energy ξ relatively to the intrinsic level in the silicon bulk, its according energy at the interface is $\xi_s = \xi + \psi_s$.

Regarding to $D_{it}(\xi + \psi_s)$, the interface charge density Q_{it}, which is necessary for the understanding of capacitance-voltage curves later on, can be obtained as a function of band-bending,

$$Q_{it}^d(\psi_s) = q\int_{E_v/q-\psi_s}^{E_c/q-\psi_s} d\xi[1 - f_0(\xi - \phi_B)]D_{it}^d(\xi + \psi_s) \tag{4.26}$$

$$Q_{it}^a(\psi_s) = q\int_{E_v/q-\psi_s}^{E_c/q-\psi_s} d\xi f_0(\xi - \phi_B)D_{it}^a(\xi + \psi_s) \tag{4.27}$$

depending if the interface states are of donor or acceptor type. A transformation of the integration variable from ξ to $\xi + \psi_s$ and differentiating the interface charge by the band-bending results in

$$C_{it} \equiv \frac{dQ_{it}}{d\psi_s} = q \int_{E_v/q}^{E_c/q} d\xi \left(\frac{kT}{q}\right) f_0(\xi_s - \phi_B \psi_s)[1 - f_0(\xi_s - \phi_F - \psi_s)] \cdot [D_{it}^a(\xi_s) + D_{it}^d(\xi_s)]. \tag{4.28}$$

Summarising, the variation of interface charge with band-bending is dependent on the sum of both donor and acceptor like interface state densities.

From experiments it can be concluded that interface states in the upper half of the band-gap act as donor levels whereas there is no information about the type of levels in the lower half [NIC82].

4.5.4 Effective capture cross-section

The effective capture cross-sections for electrons and holes at the interface describes the capture efficiency of interface traps and thus is defined by the capture probability,

$$\sigma_n = \frac{c_n}{v_{th}} \tag{4.29}$$

$$\sigma_p = \frac{c_p}{v_{th}} \tag{4.30}$$

with c_n and c_p representing the capture probabilities. The capture probabilities themselves are determined by the interface trap response time τ_n and τ_p by

$$c_n = \frac{1}{\tau_n N_D} \cdot \exp(- < q\psi_s > /kT) \tag{4.31}$$

and

$$c_p = \frac{1}{\tau_p N_A} \cdot \exp(< q\psi_s > /kT), \tag{4.32}$$

with $< \psi_s >$ being the average band-bending.

For an experimental determination of the capture probabilities both the average surface band bending and the effective doping profile must be known. In practice this is nearly impossible because the surface doping profile very close to the interface is experimentally not accessible and an error in the flat-band voltage is multiplied by the exponential dependence, too. Thus, a prediction of the capture cross-section cannot be much better than an order-of-magnitude estimate [NIC82]. Within this range it can e.g. be used to predict the interface state density from the surface recombination velocity.

4.5.5 Surface recombination velocity

The defect related generation-recombination process at the interface is of great importance because it has significant impact on the reverse current of a segmented silicon detector, as was briefly mentioned in section 3.4.5.

Defect levels located in the silicon band gap act as recombination-generation centres. They are stepping stones for charge carrier movement between valence and conduction band. The transition probability is dependent on the energy difference of the defect level and the band edges. Therefore, defect related generation-recombination processes may have severe impact on the overall transition probability. Fig. 4.7 depicts possible

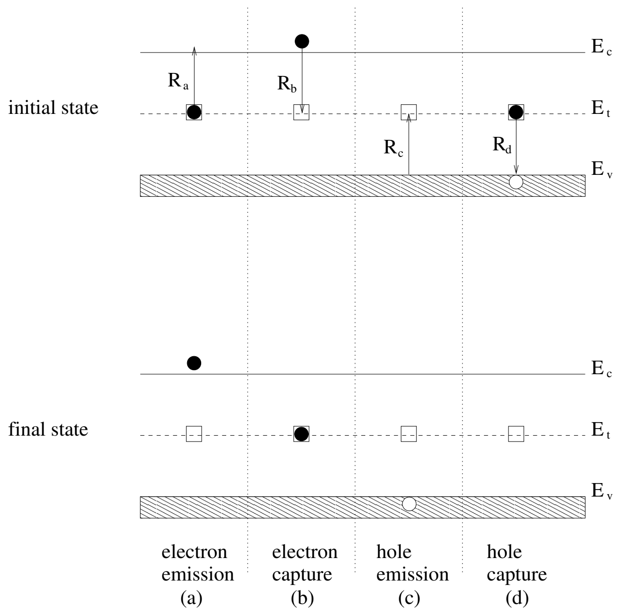


Figure 4.7: *Generation-recombination process in thermal equilibirum. After [SZE85]*

transition processes in thermal equilibirum.

In fig. 4.7(a) an electron from the charge band is captured by a defect level E_t (electron capture process). The capture rate is proportional to the density of un-occupied electron traps. Assuming a total trap density N_{it}, then according to the Fermi distribution F, $N_{it}(1-F)$ is the density of un-occupied levels. In equilibrium the Fermi distribution is

$$F = \frac{1}{1+\exp(E_t - E_f)/kT}. \tag{4.33}$$

The capture rate for electrons then is

$$R_b = v_{th}\sigma_n n N_t(1-F), \tag{4.34}$$

with v_{th} being the thermal velocity, σ_n the capture cross-section for electrons, and n the electron concentration.

After [SZE85] the rates for the remaining processes can be achieved by similar arguments and are found to be

$$R_a = e_n D_{it} F \tag{4.35}$$

$$R_c = v_{th}\sigma_p p D_{it} F \quad (4.36)$$
$$R_d = e_p D_{it}(1-F) \quad (4.37)$$

with

$$e_n = v_{th}\sigma_n n_i \exp(E_t - E_F)/kT \quad (4.38)$$
$$e_p = v_{th}\sigma_p n_i \exp(E_i - E_t)/kT \quad (4.39)$$
$$(4.40)$$

being the emission rates for electrons and holes.

In addition to thermal equilibrium processes the carrier generation by light injection must be considered as a further generation-recombination process. In this case electrons are entering and leaving the conduction band directly and continuously. In steady state the according rates must be equal. Following this *principle of detailed balance* [SZE85], the net recombination rate can be calculated,

$$U_s \equiv R_a - R_b = \frac{v_{th}\sigma_n\sigma_p N_{st}(p_n n_n - n_i^2)}{\sigma_p[p_n + n_i \exp(E_i - E_t)/kT] + \sigma_n[n_n + n_i \exp(E_t - E_i)/kT]}, \quad (4.41)$$

with n_s and p_s denoting the electron and hole concentration at the surface and N_{st} the recombination centre density in the surface region.

Assuming low-injection condition [SZE85] and $n_s \gg p_s$, equation 4.41 simplifies to

$$U_s \simeq v_{th}\sigma_{eff} N_{st}(p_s - p_{no}). \quad (4.42)$$

The capture cross-sections for electrons and holes are assumed to be equal and thus can be described by an effective capture cross-section σ_{eff}. Because of having the dimensions of a velocity,

$$S_0 = v_{th}\sigma_{eff} N_{st} = v_{th}\sigma_{eff} kT D_{it,mg} \quad (4.43)$$

is called *surface recombination velocity.*

The surface recombination velocity is determined by the density of recombination centre at the silicon surface and by the effective capture cross-section for electrons and holes at the interface. According to equ. 3.19 the interface generation current grows proportionally to S_0. As a consequence from this, the surface recombination velocity can be obtained directly from a measurement of the interface generation current. Using equ. 4.43 and the effective capture cross-section, it is possible to calculate the interface state density at midgap level from it.

Chapter 5

Monitor devices and characterisation methods

5.1 Device physics

5.1.1 MOS capacitor

MOS capacitors are a good instrument for studying surface and oxide properties of silicon devices. They are well established as a monitor device in process control sequences in semi-conductor industry as well as powerful tools for investigating radiation tolerance of silicon surfaces and oxides. Therefore, MOS devices play an important role in detector development and production.

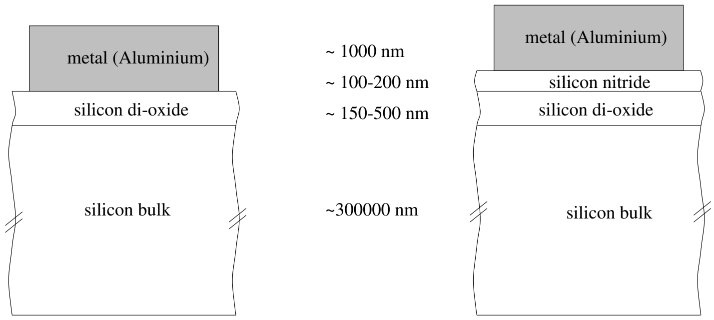
Surface parameters are measured on MOS devices by applying electrical signals to the device and observing the answer. The correct interpretation of observed effects requires a good understanding of the device physics which is introduced in the following.

Static behaviour

A schematic cross-section of a MOS capacitor is shown in fig. 5.1(a). It is formed by a sandwich-like structure of a metal film (gate contact) deposited on an oxide layer (dielectric), which is grown on a semi-conductor substrate. In the following, only a special kind of MOS capacitors is discussed, i.e. aluminium is used for the metal contact, the dielectric film is made of silicon oxide grown on crystalline high purity silicon substrate.

Detector designs often employ an additional nitride layer which is deposited on top of the oxide. Beside further protection of the silicon surface and better mechanical stability, it enhances the potential distribution on the silicon surface. The advantage of an additional silicon nitride layer will be picked-up in more detail later in this work. Fig. 5.1(b) illustrates the structure of a MOS device with an additional silicon nitride layer.

Energy band diagrammes are very helpful for discussing the physics of MOS devices; starting with an ideal MOS capacitor, which band diagramme is drawn in fig. 5.2.



(a) Metal-Oxide-Silicon (b) Metal-Nitride-Oxide-Silicon

Figure 5.1: *Cross-section through a MOS capacitor. (a) Standard, (b) additional silicon nitride layer between oxide and metal.*

Ideal in this context implies the following assumptions, which allow to explain basic characteristics before the discussion is extended to *real* MOS devices later on,

- no charge transport across the oxide film
- charges can only be located on either the gate-contact or in the silicon
- without applied bias voltage the energy bands are flat (flat-band case)
- without applied bias voltage the work functions of the metal and the silicon are equal, $\phi_m = \phi_s$.

Fig. 5.2 shows the band-diagramme of an n-type MOS capacitor in thermal equilibrium, the fermi-levels of both metal and silicon have adopted to the same energy. Furthermore, the energy bands are flat at the silicon surface, which is known as the *flat-band* case. It is characterised by charge neutrality at the crystal surface.

As will be discussed in detail below, applying a bias-voltage to the gate-contact of a MOS capacitor changes the shape of the energy bands at the silicon surface. A characteristic parameter of MOS devices is the so-called *flat-band* voltage, which is the gate bias corresponding to flat-band conditions. In case of an ideal device, it is equal to zero and determined by the work-function differences only,

$$V_{fb} := \phi_m - \phi_s \equiv 0. \tag{5.1}$$

The energy gap ϕ_B between intrinsic fermi-level and the fermi-energy depends on the doping concentration of the silicon,

$$\phi_B = k_B T \cdot \ln(\frac{N_D}{n_i}), \tag{5.2}$$

with k_B being the Boltzmann's constant, T the absolute temperature, N_D the doping concentration and n_i the intrinsic charge carrier concentration of the silicon.

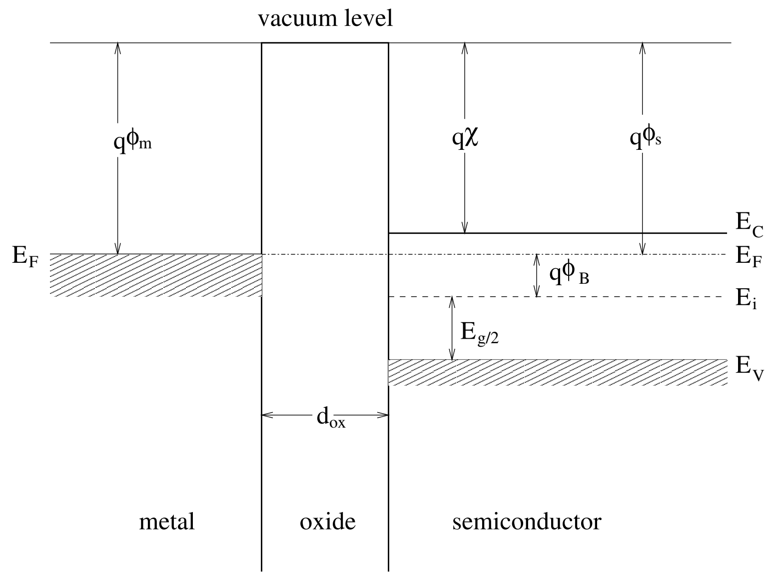


Figure 5.2: *Band diagrammes for an ideal MOS capacitor (n-type silicon). [SZE85]*

Although in measurements the answer of MOS devices is observed as a function of applied gate-bias, it is useful to explain the MOS behaviour in dependence of the silicon surface band-bending ψ_s, and correlated ψ_s to the gate bias afterwards.

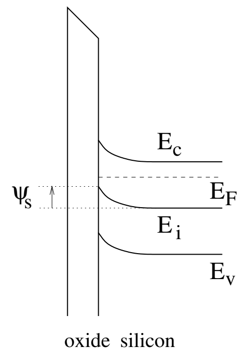


Figure 5.3: *Silicon surface potential ψ_s.*

In fig. 5.3 the band-bending ψ_s is illustrated. It denotes the shift of the intrinsic fermi-level at the silicon surface with respect to the level deep in the silicon bulk; in case of an upward bending ψ_s is positive, otherwise it is negative and the flat-band condition is determinde by zero band-bending.

Thus ψ_s determines the charge state of the surface silicon. It is necessary to distinguish five cases, which are described in the following.

A slight upward bending, i.e. $\phi_B > \psi_s > 0$ as depicted in fig. 5.4(a) shifts the

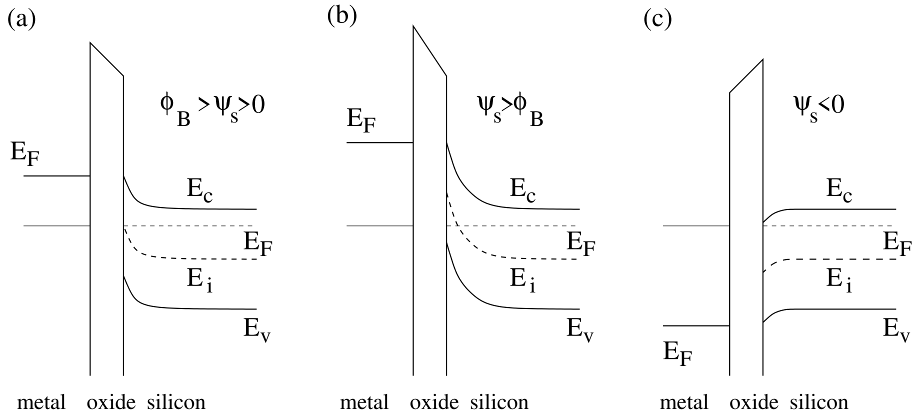


Figure 5.4: *Biasing conditions of a MOS capacitor. (a) depletion, (b) inversion, (c) accumulation. [SZE85]*

intrinsic fermi-level close to the extrinsic fermi-energy. Subsequently, the concentration of free surface electrons, i.e. the majority carriers, is decreasing or in other words, a depletion of electrons from the surface silicon is occuring. This is called *depletion case* of a MOS device. Quantitatively, the electron and hole concentrations depend on the band-bending,

$$[p_n] = n_i \cdot e^{-q(\phi_B - \psi(x))/kT}, \tag{5.3}$$

$$[n_n] = n_i \cdot e^{-q(\psi(x) - \phi_B)/kT}, \tag{5.4}$$

where $\psi(x)$ is the band-bending in an arbitrary distance x from the silicon surface and $\psi(x = 0) = \psi_s$. In depletion the hole concentration of equation 5.3 slightly grows whereas the electron density 5.4 decreases.

The dependence between band-bending and depth of the surface depletion zone is obtained from Poisson's equation,

$$\frac{d^2\psi(x)}{dx^2} = -\frac{\rho_s(x)}{\epsilon_{Si} \cdot \epsilon_0}, \tag{5.5}$$

where $\rho_s(x)$ is the space charge density

$$\rho_s = -q \cdot N_D \cdot A_{gate} \tag{5.6}$$

of the depleted silicon. An integration gives the potential distribution which is similar to potential of a p^+n-junction,

$$\psi(x) = \psi_x \left[1 - \frac{x}{x_d}\right], \tag{5.7}$$

x_d beeing the maximum depletion depth. The according surface potential is

$$\psi_s = \frac{qN_D x_d^2}{2 \cdot \epsilon_{Si}\ \epsilon_0}. \tag{5.8}$$

When the energy bands are bent further, i.e. when the intrinsic fermi-level is shifted across the midgap position, then the silicon surface is *inverted*. Therefore, for $\psi_s > \phi_B$ as is indicated in fig. 5.4(b), the hole concentration becomes larger than the electron concentration, as can be seen from equations 5.3 and 5.4.

The silicon surface hole concentration n_s becomes dominant, when it is equal to the space charge of the depleted silicon,

$$n_s = N_D. \tag{5.9}$$

From equations 5.3, using $\psi = \psi_s$ and 5.9 follows the required band bending for strong inversion,

$$\psi_s \approx 2 \cdot \phi_B = 2 \cdot kT \cdot \ln[\frac{N_D}{n_i}]. \tag{5.10}$$

Increasing ψ_s further than strong inversion results in a very rapid increase of the hole concentration.

The surface depletion zone stops growing as soon as strong inversion is reached. Then, the gate charge is compensated by the constant space charge of the depleted silicon and the fast growing inversion layer charge,

$$Q_{gate} = Q_{inv}(\psi_s) + Q_{depl}, \tag{5.11}$$

with $Q_{depl} = \rho_s \cdot x_d$.

In case of a negative band-bending, as is depicted in fig. 5.4(c), the silicon conduction band is coming closer to the extrinsic fermi-energy, electrons are accumulated at the semiconductor surface. This is called *accumulation*. As can be seen from equ. 5.4, the electron concentration is growing exponentially with the band-bending. In accumulation the gate-charge is fully compensated by the accumulation layer charge, $Q_{gate} = Q_{acc}$.

band-bending ψ_s [eV]	charge state
$\psi_s < 0$	accumulation of electrons
$\psi_s = 0$	flat-band condition (surface is neutral)
$\phi_B > \psi_s > 0$	depletion of electrons
$\psi_s = \phi_B$	midgap position (intrinsic carrier concentration)
$2\phi_B > \psi_s > \phi_B$	weak inversion
$\psi_s > 2\phi_B$	strong inversion

Table 5.1: *Charge state of the silicon surface as a function of band-bending.*

Up to now the discussion was restricted to ideal MOS devices. It was assumed that the oxide film as well as the interface region are perfect, i.e. there have no charge traps and interface states been considered. Recalling what was said about real surfaces and oxide films in chapter 4, ideal MOS devices certainly do not describe reality and an extension of the theory to real MOS capacitors is necessary.

Refering to fig. 4.4 of section 4.2.2, there are various kinds of positive charges distributed across the silicon oxide film. Their influence on the flat-band voltage and the surface band-bending is subject of the following paragraphs.

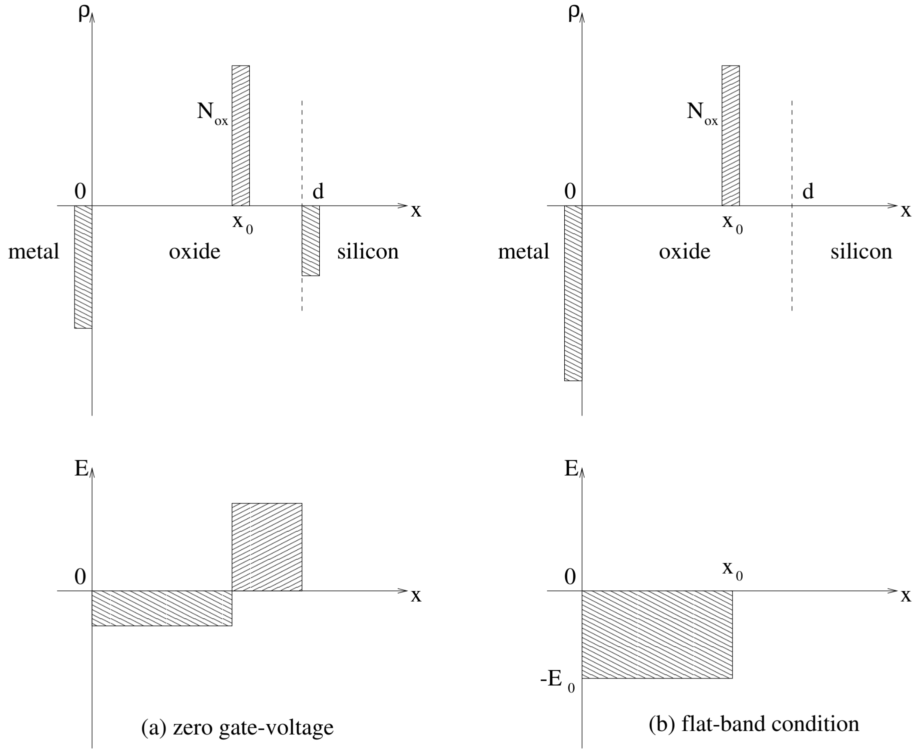


Figure 5.5: *Charge density ρ and electric field E at the MOS capacitor for (a) zero gate-bias and for flat-band case (b). [SZE85]*

It is useful to summarise all oxide charges by an effective sheet charge N_{ox} located at an arbitrary position x_Q in the oxide as is depicted in fig. 5.5.

Starting with zero volt gate-bias, the positive sheet charge induces negative charges on the gate-contact as well as at the silicon surface. There is a constant electric field across the oxide between gate contact and oxide sheet charge and an electric field with opposite sign between sheet charge and silicon surface as is indicated in fig. 5.5(a). Therefore, the MOS device is kept in accumulation and the energy bands are bent downwards. This is a major difference to an ideal MOS capacitor, where zero gate-bias was equivalent to flat-band conditions and charge neutrality at the semi-conductor surface.

To achieve flat-band conditions, it is necessary to compensate the electric field between oxide charge and silicon surface. Charging up the gate-contact negatively by applying a negative gate-voltage, reduces the electric field at the semi-conductor surface. It vanishes completely at the flat-band voltage, as is shown in 5.5(b).

Assuming that the electric field between gate and oxide charge sheet is E_0, the flat-band voltage is

$$V_{fb} = -\int_0^{x_q} E_0 \cdot dx = E_0 \cdot x_Q, \tag{5.12}$$

with the electric field

$$E_0 = \frac{N_{ox}}{\epsilon_0 \epsilon_{ox}}. \tag{5.13}$$

Presuming that C_{ox} is the capacitance of the oxide layer per unit area, the electric field is given by

$$E_0 = \frac{N_{ox}}{C_{ox}} \cdot \frac{1}{d}. \tag{5.14}$$

and the flat-band voltage finally is

$$V_{fb} = -\frac{N_{ox}}{C_{ox}} \cdot \frac{x_Q}{d}. \tag{5.15}$$

From the above calculations it is clear that the flat-band voltage of a real MOS device depends on both the density of the oxide sheet charge and its position from the gate-contact. Maximum influence must be expected for a sheet charge located very close to the oxide / semi-conductor interface whereas its influence decreases with distance.

Beside oxide charges, it must be taken into account, that the work-function difference in real devices is not zero. The work-function of silicon is dependent on the doping concentration,

$$\phi_s = q \cdot \chi + \frac{E_g}{2} + q \cdot \phi_B, \tag{5.16}$$

with χ being the semi-conductor electron affinity and E_g the energy band gap, see fig. 5.2. The doping concentration is taken into account in ϕ_B. The work-function of silicon is always larger than of the metal. In conclusion, the flat-band voltage is

$$V_{fb} = \phi_m - \left[q \cdot \chi + \frac{E_g}{2} + q \cdot \phi_B \right] < 0. \tag{5.17}$$

Concluding, the flat-band voltage of a real MOS capacitor depends on the effective oxide charge density and the charge distribution within the oxide film as well as on the work-function difference between metal and silicon,

$$V_{fb} = \phi_m - \phi_s + d\epsilon_{ox}\epsilon_{ox} \cdot N_{ox}. \tag{5.18}$$

The most important method for evaluating interface and surface properties is to measure the dynamic capacitance of a MOS device. It is voltage dependent and therefore measured as a function of the gate-bias. Besides any voltage dependence, the frequency of the applied electrical test signal is of great importance because it determines in how far different effects contribute to the measurement. Low and high frequency capacitance-voltage (C-V) characteristics are introduced separately in the following two sections.

Low frequency capacitance

Generally, the dynamic capacitance is defined as the change of charges on the field plates occuring under a small change of bias voltage,

$$C_{dyn} = \frac{dQ_{plate}}{dV_{bias}}. \tag{5.19}$$

For MOS capacitors the dynamic capacitance in steady state is of interest. It is determined at a static gate-bias with a superimposed small ac voltage signal.

For a certain gate-bias, the electric field across the oxide film is

$$E_0 = \frac{V_{ox}(t)}{d} = \frac{V_{gate}(t) - \psi_s(t)}{d}, \tag{5.20}$$

with V_{ox} beeing the voltage drop across the oxide layer, V_{gate}(t) and ψ_s(t) the time-dependent gate-voltage and the according band-bending.

For a capacitance of the oxide layer C_{ox}, the surface charge of the silicon is

$$Q_s(t) = C_{ox} \cdot [V_{gate}(t) - \psi_s(t)]. \tag{5.21}$$

In case of a superimposed small ac voltage signal,

$$V_{gate}(t) = V_{gate} + \delta V_{gate}(t), \tag{5.22}$$

the band-bending varies with time, too,

$$\psi_s(t) = \psi_s + \delta\psi_s(t). \tag{5.23}$$

As a result from this, the surface charge is undergoing small changes following the ac signal,

$$Q_s(t) = Q_s(\psi_s + \delta\psi_s(t)), \tag{5.24}$$

which can in first order be approximated by a Taylor series,

$$Q_s(t) = Q_s(\psi_s) + \left(\frac{dQ_s}{d\psi_s}\right) \cdot \delta\psi_s(t). \tag{5.25}$$

The second term of equation 5.25 denotes the small change in surface charge due to the variation in band-bending. It is correlated to the low-frequency differential capacitance of the silicon,

$$C_s(\psi_s) \equiv -\frac{dQ_s}{d\psi_s}. \tag{5.26}$$

Equation 5.26 is valid only for low frequencies, because the substitution in equation 5.24 requires thermal equilibrium. High frequency ac signals are too fast for minority carriers to follow.

In case of a static gate-voltage without superimposed ac signal, the surface charge is

$$-Q_s = C_{ox}(V_{gate} - \psi_s). \tag{5.27}$$

A substitution of equations 5.22, 5.23 and 5.24 into 5.21 and eleminating the time independent terms by subtraction of equation 5.27 one obtains

$$C_{ox}(\delta V_{gate} - \delta\psi_s) = C_s(\psi_s)\delta\psi_s \tag{5.28}$$

or

$$\frac{\delta\psi_s}{\delta V_{gate}} = \frac{C_{ox}}{C_{ox} + C_s(\psi_s)}. \tag{5.29}$$

The total capacitance of the MOS device then is

$$C_{lf} \equiv -\frac{\delta Q_s}{\delta V_{gate}} = -\frac{\delta Q_s}{\delta\psi_s}\frac{\delta\psi_s}{\delta V_{gate}} = C_s(\psi_s) \cdot \frac{C_{ox}}{C_{ox} + C_s(\psi_s)}, \tag{5.30}$$

or rewritten,

$$\frac{1}{C_{lf}} = \frac{1}{C_s(\psi_s)} + \frac{1}{C_{ox}}. \tag{5.31}$$

From equation 5.31 is becomes clear that the total capacitance of a MOS capacitor is determined by a series circuit of the oxide capacitance, which is voltage independent, and the silicon surface capacitance, beeing a function of the gate-bias.

In the flat-band case the silicon surface capacitance is determined by the extrinsic Debye-length of the substrate,

$$C_s(V_{fb}) \equiv C_{fbs} = \frac{\epsilon_0\epsilon_{Si}A_{gate}}{\lambda_n}, \tag{5.32}$$

with A_{gate} representing the gate-area and λ_n being the extrinsic Debye-length,

$$\lambda_n = \left(\frac{\epsilon_0\epsilon_{Si}kT}{q^2N_D}\right). \tag{5.33}$$

For a MOS device in strong accumulation, the silicon capacitance increases exponentially with band-bending,

$$C_s \equiv C_A = \frac{C_{fbs}}{\sqrt{2}} \cdot \exp(\frac{q\psi_s}{2kT}). \tag{5.34}$$

The depletion capacitance is determined by the surface depletion depth, similar to the capacitance of a pn-junction.

$$C_s \equiv C_D = \frac{\epsilon_0\epsilon_{Si}A_{gate}}{x_d}. \tag{5.35}$$

Finally, in inversion the surface capacitance increases exponentially with band-bending again,

$$C_s \equiv C_I = \frac{C_{fbs}}{\sqrt{s}}\frac{n_i}{N_D} \cdot \exp(-\frac{q\psi_s}{2kT}). \tag{5.36}$$

In fig. 5.6 a characteristic low-frequency C-V curve is depicted over the whole gate-bias range. In strong inversion as well as in strong accumulation the silicon capacitance becomes very large and therefore the total capacitance is determined by the oxide capacitance. Near the inversion voltage, if the silicon surface is depleted and C_s is small, a minimum in the C-V characteristic occurs.

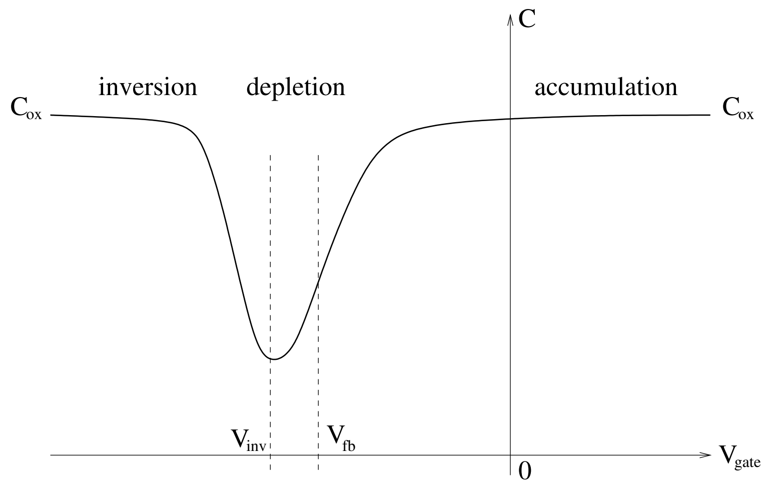


Figure 5.6: *Theoretical low frequency C-V curve of a MOS capacitor. [NIC82]*

High frequency capacitance

In case of high frequency ac signals applied to the MOS capacitors, minority carrier relaxation time is much too high to follow the ac voltage. Changes of charge carrier concentrations are the result of gate-bias changes, only. Therefore, high frequency capacitance of a MOS device differs from the low frequency value in case of high minority carrier densities at the silicon surface, i.e. in weak and strong inversion.

For a proper calculation of the high frequency silicon capacitance, two things have to be considered [NIC82]: first, the concentration of the inversion layer charges is determined by the static gate-bias only, it is not altered by the ac bias component. Second, the inversion layer can move spatially at the silicon surface. Inversion layer depth therefore grows and shrinks following the ac signal. The volume density of charges changes while the total density per unit area is kept constant. This effect is often referred to as inversion layer *polarisation* [NIC82].

The extension and contraction of the surface depletion zone due to the ac signal results in spatial redistribution of the inversion layer charge. When the depletion zone extends for a half-cycle of the ac signal, the inversion layer width shrinks due to a higher electric field at the interface. During the other half of the cycle, the contrary effects happens [NIC82].

A narrow inversion layer is equivalent to a high hole density at the silicon surface. To keep the density per unit area constant, lower levels of the charge band must be emptied than in thermal equilibrium. On the other hand, a widening corresponds to a lower hole density at the interface, thus higher levels of the charge band must be filled compared to thermal equilibrium. This effect can be described introducing a quasi fermi-level E_{Fp} for holes which oscillates with the ac gate voltage and adjusts the correct filling of energy levels. It is assumed to be uniform across the inversion layer and therefore in phase with the a signal [NIC82].

An appropriate calculation of the high frequency silicon surface capacitance including spatial re-distribution requires to solve Poisson's equation, which can e.g. be found in [NIC82] and results

$$C_s = 2 \cdot C_{fbs} \left\{ 1 - \exp(v_{s,0}) + \left(\frac{n_i}{N_D}\right)^2 \left[(\exp(-v_{s,0}) - 1)\frac{\Delta}{1+\Delta} + 1 \right] \right\} \cdot F^{-1}(v_{s,0}, u_B) \tag{5.37}$$

with

$$\begin{aligned}
F(v_{s,0}, u_{Fp}, u_B) &= \sqrt{2}\lambda_n^{-1} \left\{ v_s + \exp(-v_s) - 1 + \exp(u_B + u_{Fp})[\exp(v_s) - 1] \right\}^{1/2} \\
v_{s,0} &\equiv \frac{q\psi_{s,0}}{kT} \\
u_B &\equiv \frac{q\phi_B}{kT} \\
u_{Fp} &\equiv \frac{E_i - E_{Fp}}{kT} \\
\Delta &\approx \frac{F(v_{s,0}, u_B)}{\exp(-v_{s,0}) - 1} \left\{ \int_0^{v_{s,0}} dv_s \left[\frac{\exp(-v_s) - \exp(v_s) + 2v_s}{F^3(v_s, u_B)} \right] - 1 \right\}.
\end{aligned}$$

$v_{s,0}$ is the dimensionless band-bending established by static gate-bias.

Equation 5.37 is the accurate expression for the high frequency silicon surface capacitance [NIC82]. Δ takes into account the constance of the inversion layer charge and the spatial redistribution [NIC82],

$$\frac{\delta u_{Fp}}{\delta v_{s,0}} = \frac{1}{1+\Delta}. \tag{5.38}$$

To evaluate the influence of Δ on the surface capacitance, the change of the quasi-static fermi-level for holes with band-bending from equ. 5.38 must be as a function of the silicon doping N_D.

The analysis given in [NIC82] shows that in depletion and weak inversion ($2\phi_B > \psi_{s,0} > 0$) equation 5.37 simplifies to

$$C_s = C_{fbs} \left[1 - \exp(v_{s,0}) \right] \cdot F^{-1}(v_{s,0}, u_B), \tag{5.39}$$

with the dimensionless surface field beeing

$$F(v_{s,0}, u_B) = \sqrt{2}[v_{s,0} - 1 + \exp(v_{s,0})]^{1/2}. \tag{5.40}$$

In depletion and weak inversion the minority carrier concentration at the surface is small, therefore the spatial redistribution has negligible effect on the capacitance.

This becomes different in strong inversion ($\psi_{s,0} > 2\phi_B$),

$$C_s = C_{fbs} \left[1 - \exp(v_{s,0}) + \left(\frac{n_i}{N_D}\right)^2 \left[(\exp(-v_{s,0}) - 1)\Delta + 1 \right] \right] \cdot F^{-1}(v_{s,0}, u_B). \tag{5.41}$$

Closed Form approximation

As was shown in the previous section, an exact calculation of the surface capacitance requires an intergration to obtain Δ. Another possibility is the *close form* approximation which is an extension of the Lindner [LIN62] approach by including the spatial redistribution of inversion layer charge.

For the close form approximation the gate-bias dependent surface capacitance of equation 5.39 is used, whereas in strong inversion a gate-bias independent constant capacitance is used. Both capacitances must be equal at the so-called *match point* $v_{s,0} = v_m$ for a steady transition. The match point is chosen thus the maximum error between calculated and approximated capacitance has its minimum.

Therefore, in accumulation, depletion and weak inversion ($v_{s,0} < v_m$) the surface capacitance is according to equtION 5.39

$$C_s(v_{s,0}) = C_L(v_{s,0}) \tag{5.42}$$

and in strong inversion ($v_{s,0} > v_m$)

$$C_s(v_{s,0}) = C_L(v_m) \equiv const, \tag{5.43}$$

with

$$C_L = \frac{1}{\sqrt{2}} Sgn(v_{s,0}) \cdot C_{fbs}[\exp(v_{s,0}) - 1][-(v_{s,0}+1) + \exp(v_{s,0})]^{-1/2}. \tag{5.44}$$

After [NIC82] the optimal match point is

$$v_m = 2.10 u_B + 1.33, \tag{5.45}$$

which is a function of the doping concentration, too. The error, which is defined as

$$error \equiv \frac{C_s(accurate) - C_s(approximate)}{C_s(accurate)} \tag{5.46}$$

is less than 1.5 % regardless of the doping concentration [NIC82]. Therefore, the closed form approximation is very useful to describe high frequency MOS capacitance curves.

Deep depletion

Deep depletion occurs when the response time of minority carriers is too slow to follow the change in gate-bias, i.e. when the gate-bias sweep is too quick. As a consequence, inversion layer build-up is not possible, the gate-charge must be completely neutralised by space charge. Therefore, the surface depletion layer depth exceeds its thermal equilibrium value and the silicon capacitance decreases further. This can be observed from the high frequency capacitance characteristic of a MOS device measured in the bias-range where strong inversion is expected.

Finally a further increase of the depletion zone is stopped either by avalanche break downs in the silicon or when the generation rate of charge carriers in the depleted volume is high enough to maintain steady state.

Influence of interface states

As discussed in section 4.2.3, interface traps are present in real MOS devices. They come-up either as acceptors or donors with energy levels in the band-gap at the silicon surface. Acceptor states are neutral when empty and negative when filled, donor levels are charged positively when empty and neutral when filled.

The occupancy of interface states varies with gate-bias, which results in a bias-dependent charge density at the interface Q_{it}. Charge neutrality in a MOS capacitor with interface states now requires

$$\delta Q_{gate} = -\delta Q_{it} - \delta Q_s. \tag{5.47}$$

A change in gate charge produces smaller change in surface charge in a MOS capacitor with interface traps than without traps. Thus, the band-bending in case of present Q_{it} is less than for an ideal device.

Employing Gauss' law,

$$C_{ox}(V_{gate} - \psi_s) = -Q_{it}(\psi_s) - Q_s(\psi_s), \tag{5.48}$$

results for an infinitesimal small change dV_{gate} of gate-bias in

$$C_{ox} dV_{gate} = [C_{ox} + C_{it}(\psi_s) + C_s(\psi_s)] \cdot d\psi_s, \tag{5.49}$$

with

$$C_{it}(\psi_s) \equiv -\frac{dQ_{it}}{d\psi_s} \tag{5.50}$$

$$C_s(\psi_s) \equiv -\frac{dQ_s}{d\psi_s} \tag{5.51}$$

being the interface trap and surface capacitance. Therefore, the band-bending $d\psi_s$ corresponding to dV_{gate} is less in a device with interface traps than without,

$$d\psi_s(Q_{it} \neq 0) = \frac{C_{ox}}{C_{it} + C_s + C_{ox}} \cdot dV_{gate} < \frac{C_{ox}}{C_s + C_{ox}} \cdot dV_{gate} = d\psi_s(Q_{it} = 0). \tag{5.52}$$

Interface trap response is not immediate. Therefore, measured interface trap capacitance is a function of frequency. For quasi-static or very low frequency signals all traps are able to respond to the ac swing,

$$\frac{dC_{it}(\omega)}{d\omega} = 0, \tag{5.53}$$

the trap capacitance is independent of ω. With increasing frequency, more and more traps, depending on their position in the band gap, are unable to follow and the measured C_{it} decreases,

$$\frac{dC_{it}(\omega)}{d\omega} < 0, \tag{5.54}$$

unless at high frequencies no trap response is visible at all,

$$C_{it}(\omega \to \infty) = 0. \tag{5.55}$$

Therefore, high frequency C-V curves are altered by stretch-out only, but interface trap capacitance itself is not visible.

At very low frequencies the total capacitance is

$$C_{tot} \equiv \frac{dQ_{gate}}{dV_{gate}}, \tag{5.56}$$

and

$$Q_{gate} = -(Q_s + Q_{it}). \tag{5.57}$$

However, the total device capacitance at low frequencies therefore is

$$C_{tot} = \frac{dQ_{gate}}{d\psi_s} \cdot \frac{d\psi_s}{dV_{gate}} = (C_s + C_{it}) \cdot \frac{C_{ox}}{C_{ox} + C_{it} + C_s}, \tag{5.58}$$

which is a series circuit of the oxide capacitance and a parallel circuit of surface and interface trap capacitance. Low frequency C-V characteristics are fully sensitive to interface trap contributions.

How this can be used for the extraction of interface trap densities as a characteristic device parameter will be described later in this chapter.

5.1.2 Gate-controlled diode

Gate-controlled diodes, which were first introduced in [GRO66], were used to study the surface space charge regions. A schematic cross-section of a gate-controlled diode design is shown in fig. 5.7. The centre of the device is formed by a circular asymmetric p^+n-junction which is surrounded by a gate-ring at close distance.

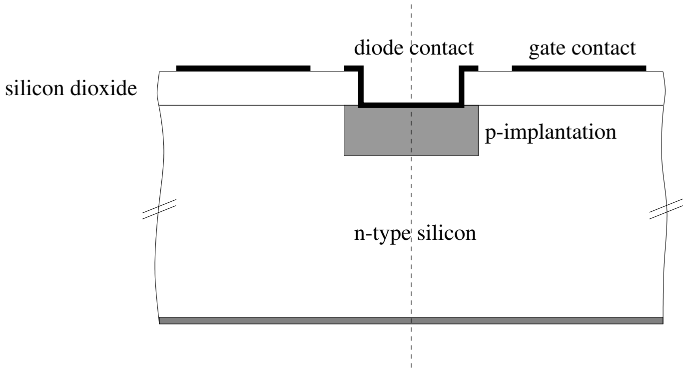


Figure 5.7: *Cross-section of a gate-controlled diode.*

A standard method to access surface space charge parameters is to measure the reverse current of the diode at a fixed bias-voltage as a function of the gate-potential, as is schematically shown in fig. 5.8. Dependening if the surface region under the gate is accumulated, depleted or inverted, different current components contribute to the reverse current of the diode and allow an extraction of characteristic parameters.

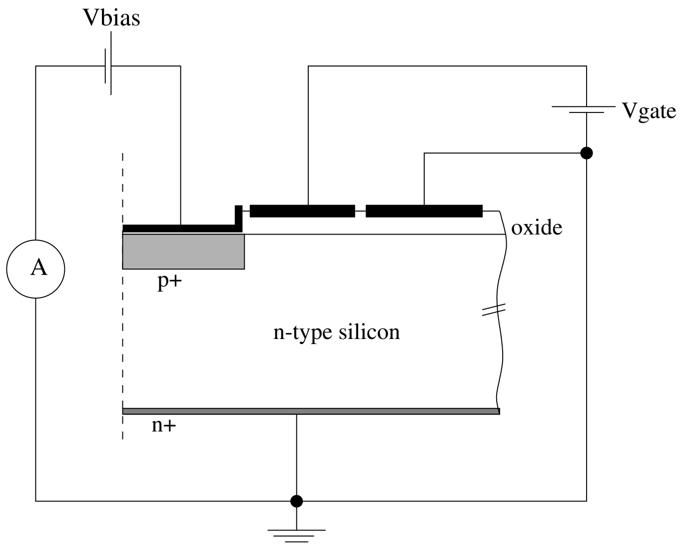


Figure 5.8: *Setup for current-voltage measurements on a gate-controlled diode with additional outer gate rings kept in accumulation.*

To be able to describe the behaviour of a gate-controlled diode theoretically, MOS theory must be extended to non-equilibrium conditions as soon as non-zero bias is applied to the diode. A detailed discussion of non-equilibrium theory can be found e.g. in [GRO66].

For an interpretation of measured current-voltage characteristics, the simplified *depletion approximation* is sufficient to describe device physics. The depletion approximation is valid when surface depletion is reached but before the onset of strong inversion, i.e. as long as minority carrier density is low.

Integrating Poisson's equation directly leads to the potential as a function of depth,

$$\phi(x) = \phi_s(x) \left(1 - \frac{x}{x_d}\right)^2, \tag{5.59}$$

with

$$\phi_s = \frac{qN_{eff}x_d^2}{2\epsilon_{Si}\epsilon 0}, \tag{5.60}$$

being the surface potential.

The maximum allowed band-bending is limited by the onset of strong inversion, therefore

$$\psi_{s,inv} = V_R - 2 \cdot \phi_B. \tag{5.61}$$

Other than in a simple MOS device in thermal equilibirum, the inversion point now is dependent on the reverse bias-voltage of the diode [GRO66]. Furthermore, from equations 5.59 and 5.61 it is obtained that

$$x_{d,max} = \left[\frac{2\epsilon_{Si}\epsilon 0(-V_R + 2\phi_F)}{qN_{eff}} \right] \tag{5.62}$$

the maximum depletion depth changes with reverse bias, too.

current-voltage characteristic

A typical current-voltage (I-V) characteristic of a gate-controlled diode is depicted in fig. 5.9. Generally, a gate-bias sweep in a certain range drives the silicon surface under

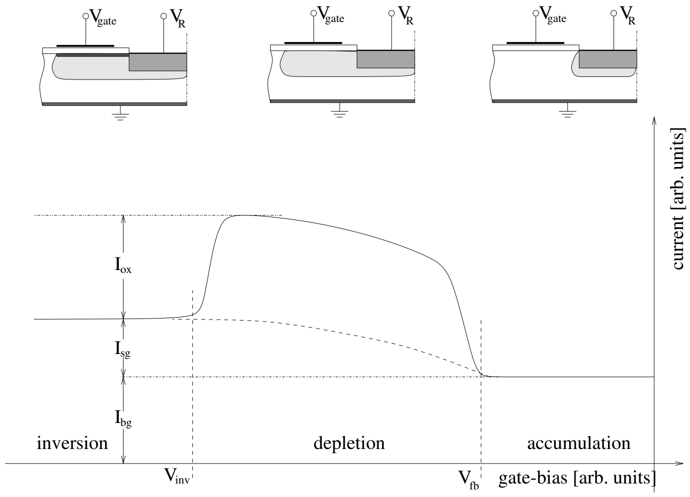


Figure 5.9: *Theoretical I-V characteristic of a gate-controlled diode [GRO66].*

the gate-ring either into accumulation, depletion or inversion.

On n-type substrate, the surface is accumulated at zero gate-bias due to the presence of positive oxide charges. The I-V curve thus only consists of volume generation current I_{bg} originating from the depletion zone of the diode as already known from chapter 3.

As soon as the depletion of the surface sets on, the surface depletion region connects to the depletion zone of the diode. Now two additional current components alter the I-V characteristic, i.e. volume generation current I_{sg} coming from the surface depletion region and interface generation current I_{ox} which is due to charge carrier generation at the interface. Whereas the voltage independent interface generation current is turned on when flat-band condition is established and forms a characterstic step in the curve, I_{sg} increases proportionally to the growing depth of the surface depletion zone.

In strong inversion, surface depletion depth remains constant and therefore I_{sg}, too. Furthermore, the inversion layer decouples the interface from the field region and I_{it} is turned off again.

For the measurement of the interface generation current on a gate-controlled diode S_0 can be determined conveniently. According to equ. 3.19 the surface recombination velocity can be calculated easiliy from the interface generation current.

5.1.3 MOSFET

Generally, the electrical behaviour of a MOSFET[1] is determined by surface related effects. It therefore is a useful tool which provides further insight into particular surface aspects before and after irradiation. For example it is possible to measure the minority carrier mobility at the interface or evaluate in how far a radiation induced increase of oxide charge density and interface state density affect the device performance. This was systematically used in this work to study the interpixel isolation capabilities of the p-spray isolation after surface damage.

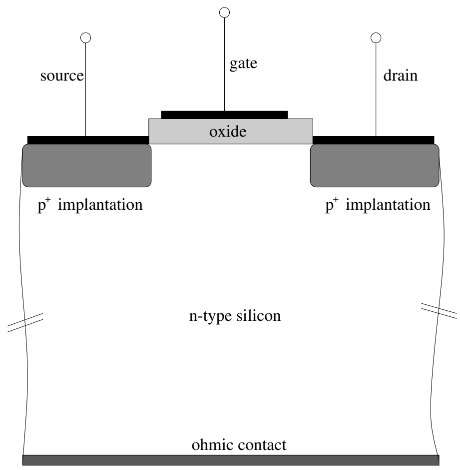


Figure 5.10: *Cross-section of a p-channel enhancement type MOSFET and drain-current characteristics.*

Fig. 5.10 shows a schematic cross-section of a MOSFET. Similar to *emitter*, *collector* and *base* of a bipolar device, a MOSFET consists of *source*, *drain* and *gate*. Whereas the gate-contact controlls the current flow between source and drain, i.e. the gate is used to switch the MOSFET on or off.

Source and drain are formed by two p-implantations which are embedded in n-type silicon. They are separated by the gate in between, which itself is fully comparable to a MOS capacitor. For using a MOSFET as a switch, a small constant voltage $V_{sd} = V_d - V_s$ is applied to the drain, keeping the source grounded. The current I_{sd} flowing from source to drain is controlled by the gate potential.

As long as the silicon surface under the gate is depleted or accumulated, there is no current flow from source to drain, the MOSFET is *off* condition. But when strong

[1]Metal Oxide Semiconductor Field Effect Transistor

inversion is established at the silicon surface between source and drain, the MOSFET opens. The according gate voltage is often referred to as threshold voltage V_{th}.

Above threshold

Fig. 5.11 illustrates different bias conditions of the MOSFET and depicts the corresponding drain current as a function of the drain voltage. As long as the drain bias is

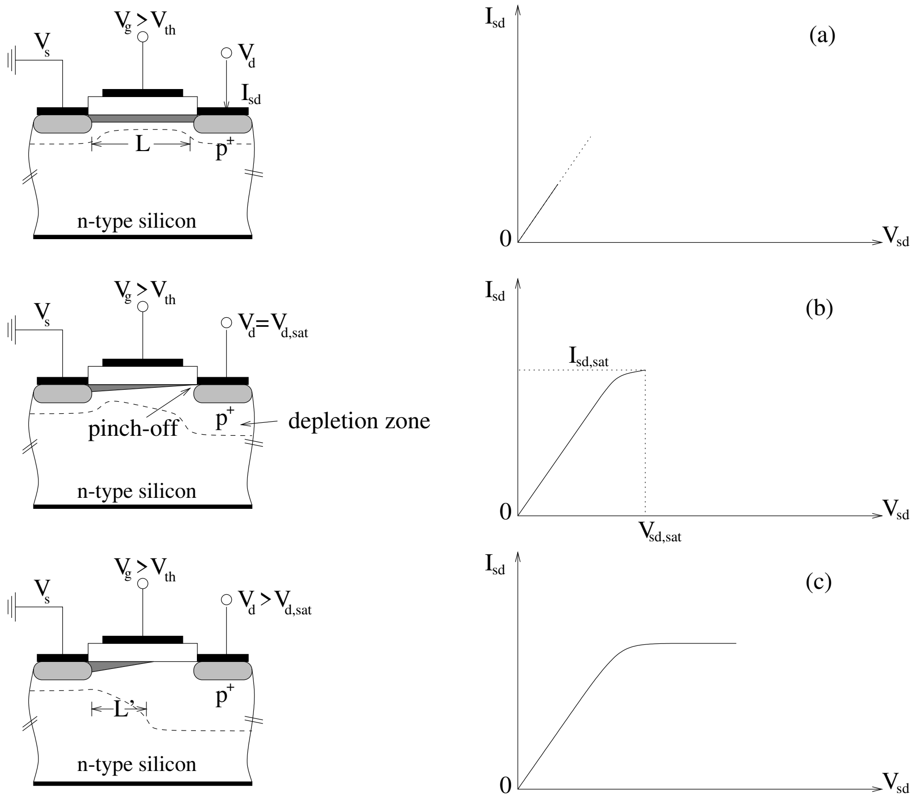


Figure 5.11: *Cross-section of a p-channel enhancement type MOSFET and drain-current characteristics.*

much smaller than the gate potential (see fig. 5.11(a)), the inversion layer thickness is constant everywhere underneath the gate. Therefore, the layer resistance is ohmic and the current increases linearly with the drain voltage,

$$R = \frac{L}{W \cdot \mu_h \cdot Q_n}, \tag{5.63}$$

with L being the layer width, W the channel length, μ_h the hole mobility and Q_n the inversion layer charge density.

When the drain voltage is increased further, the surface potential close to the gate is shifted. Thus the potential difference between gate and silicon surface is decreased until it becomes too low to maintain strong inversion. The inversion layer is *pinched-off* from the drain (see fig. 5.11(b)). For further increasing drain bias 5.11(c) the drain current remains constant, because the potential difference between drain implantations and pinch-off point is constant. Therefore, charge carrier injection into the space charge is not affected by the growing gap between drain and pinch-off point although the pinch-off point slightly moves towards the source.

Subthreshold

For gate biases below threshold, the silicon surface is either accumulated, depleted or weakly inverted. In case of accumulation and depletion obviously no I_{sd} current can

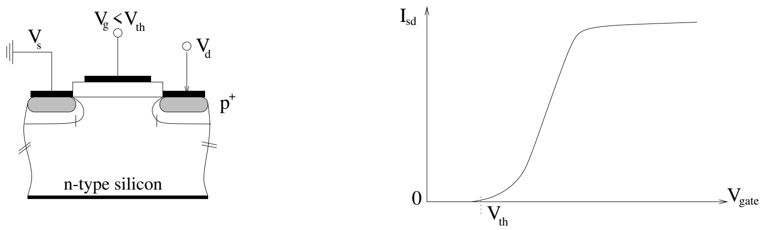


Figure 5.12: *Source-drain current of a MOSFET measured in the subthreshold region, i.e.* $V_{gate} < V_{th}$.

be observed.

In weak inversion the source drain current is mainly controlled by the minority carrier density in the inversion channel. The concentration grows exponentially with the surface band bending ψ_s

$$[p] \propto \exp(\frac{q\psi_s(V_{gate})}{kT}), \tag{5.64}$$

where the band bending is a function of the applied gate potential.

The subthreshold characteristics of a MOSFET provide information about the correlation of gate bias and band bending and about the minority charge carrier concentration at the surface..

5.2 Experimental methods

5.2.1 Oxide charge density

Extraction from high-frequency C-V curve

Equation 5.18 shows that the oxide charge density and the flat-band voltage are directly correlated. The flat-band voltage can be accessed experimentally from a measured capacitance-voltage characteristic as is depicted in fig. 5.13 by calculating the total device capacitance under flat-band conditions and then identifying the corresponding

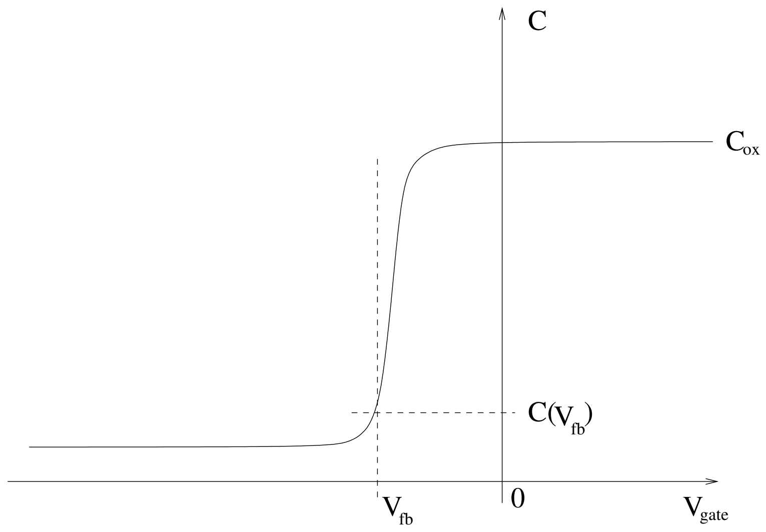


Figure 5.13: *High frequency C-V characteristic of a MOS capacitor.*

gate-voltage as the flat-band voltage. The formalism for the calculation was already introduced already. It must be noticed that the effective doping concentration as well as the oxide capacitance and the oxide permittivity ϵ_{ox} must be known. The doping concentration for example can be determined using a simple diode of the pn-junction of a gate-controlled diode. The oxide capacitance is taken from the C-V characteristic in strong accumulation.

A typical setup for a C-V measurement is shown in fig. 7.7. Basic instrument is an LCR-meter for the capacitance measurement. Its terminals are connected to the gate-electrode and the ohmic back-contact of the MOS device. This is either done using a probe station or wire bonds.

When wide ranges of gate-bias sweeps are afforded, a so-called bias-box is connected between the measurement terminals of the LCR meter and the device. The bias-box couples a static bias voltage into the measurement signal without any interference. And, the sensitive LCR is thus protected against the high voltage.

An LCR-meter measures the dynamic capacitance by applying a small ac sinus-shaped test signal to the device and evaluating the phase shift introduced by the capacitor between output and answer signal. It is possible to adjust the signal amplitude as well as the signal frequency according to the experimental needs.

For the data presented in this thesis was obtained using an Hewlett-Packard 4284A LCR meter [HP42]. It provided correction features which allowed a correction for stray capacitances and resistance due to e.g. probe tips or simply introduced by the used cables.

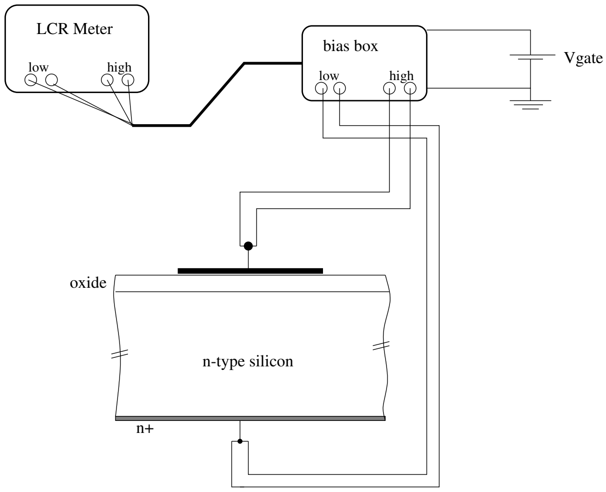


Figure 5.14: *Setup for high-frequency capacitance measurement.*

Discussion of experimental errors

There are various error sources which have physical and device intrinsic origins and which might introduce deviations of a measured high frequency curve from the ideal curve. For a systematic study, mainly basing on high frequency C-V data, it is necessary to understand these sources and estimate its influence on the total error. The different problems are discussed in great detail in [NIC82], in the following only the most relevant issues are addressed as far as they affect the data analysis later on.

First of all, in practice frequencies up to 100 kHz or perhaps 1 MHz can be used whereas the optimum frequencies are above 1 GHz. Thus a measured C-V curve does not represent the true high frequency C-V curve for the full gate bias range. The response of interface traps cannot be neglected completely for all gate biases [NIC82]. In fact, when high majority carrier concentrations are present, i.e. in strong accumulation, interface trap response times get significantly shorter and more traps respond to the ac signal. This leads to significant errors in extracting the silicon surface capacitance before the flat-band voltage is reached. This issue will be addressed again when a method for extracting the interface state density is described because it has major impact on it.

Another source of error is a non-homogeneous doping profile at the silicon surface, i.e. a variation of N_{eff} with the depth. Due to impurity re-distribution during thermal oxidation or additional implanting steps, a certain doping profile is produced. As mentioned in chapter 4, boron atoms tend to segregate into the oxide film during oxidation and result a depletion of boron at the silicon surface. For phosphorous the opposite effect was observed, it piles up at the surface. As summarised in [NIC82], the error introduced by non-uniform doping profiles becomes significant for doping concentrations[2] of $10^{16}/\mathrm{cm}^3$ and above. Non-uniform doping again affects the silicon surface capacitance and therefore becomes important when determining the interface state density. The doping concentrations of the materials evaluated in this work are in the order of $10^{12}/\mathrm{cm}^3$. Errors due to non-uniform doping do not have to be considered thus.

Especially after ionisation induced radiation damage, lateral inhomogenities in the distribution of interface states and oxide charges alter the shape of the C-V curve, too. The inhomogenities directly lead to variations in band bending across the surface and become significant when small changes in gate-bias result in large changes of band-bending, i.e. near flat-bands, whereas for depletion and weak inversion these variations are negligible [NIC82] affecting the silicon capacitance.

5.2.2 Interface state density

Combined high-low frequency method

One of the main differences between high and low frequency capacitance curves was that the (ideal) high frequency C-V curve was free of interface trap response, i.e. that C_{it} did not contribute to the total capacitance whereas in case of very low frequencies interface traps do fully contribute. This characteristic behaviour will be used now for an extraction of the interface state density as the difference between both signals. This method was invented by *Castagne* and *Vapaille* [CAS71]. Both the high and low frequency C-V characteristic are plotted in fig. 5.15.

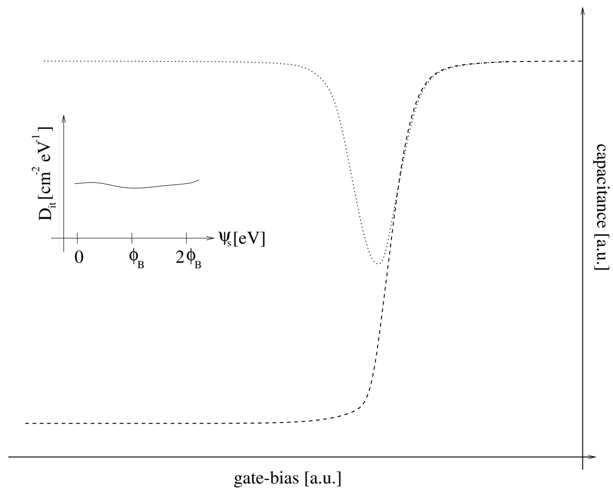


Figure 5.15: *High and low frequency capacitance curves. The insert shows the interface state density vs. band bending which computed from the C-V curves.*

[2]denotes a theoretical uniform profile used for simulations

From the high-frequency curve the silicon capacitance can be obtained easily, as

$$C_s = \left(\frac{1}{C_{hf}} - \frac{1}{C_{ox}}\right)^{-1}, \tag{5.65}$$

and then the interface trap capacitance is

$$C_{it} = \left(\frac{1}{C_{lf}} - \frac{1}{C_{ox}}\right)^{-1} - \left(\frac{1}{C_{hf}} - \frac{1}{C_{ox}}\right)^{-1}. \tag{5.66}$$

Equation 5.65 is not valid near or in inversion because minority carriers do not follow the high frequency ac signal and therefore C_s does not represent the silicon capacitance in thermal equilibirum.

Generally, the difference between high and low frequency capacitances is

$$\Delta C = C_{lf} - C_{hf}, \tag{5.67}$$

and then

$$C_{it} = \Delta C \left(1 - \frac{C_{hf} + \Delta C}{C_{ox}}\right)^{-1} \left(1 - \frac{C_{hf}}{C_{ox}}\right) \equiv q \cdot D_{it}. \tag{5.68}$$

Equation 5.68 allows the calculation of interface state density as a function of gate bias in depletion and weak inversion, where the above formula is valid. Still, it is necessary to convert the applied gate-bias of the MOS device into band-bending to plot D_{it} as a function of energy, as is depicted in the insert of fig. 5.15.

The band-bending can experimentally be related to the gate-bias by using a low-frequency C-V curve. For the following steps thermal equilibrium is required because all types of charge carriers must fully contribute to the total capacitance. It then follows that

$$\psi_s = \psi_{s0} + \int_{V_{G0}}^{V_g} dV_g \frac{C_{ox}}{C_{ox} + C_{it} + C_s}. \tag{5.69}$$

and

$$\psi_s = \psi_{s0} + \int_{V_{g0}}^{V_g} dV_G \left[1 - \frac{C_{lf}(V_g)}{C_{ox}}\right] \tag{5.70}$$

gives the wanted correlation of gate-bias and band-bending by a numerical intergration of the measured data.

Measurement setup

The setup for measuring the high frequency capacitance was already introduced in section 5.2.1. The setup for quasi-static C-V measurements looks very similar with the only difference that the LCR-Meter is replaced by a quasi-static C-V meter. A detailed description of the Keithley K595 C-V meter can be found in [KEI86] which was employed for this work.

A quasi-static CV meter applies a small rectangular voltage pulse to the test capacitance and integrates over the current flowing through the capacitor. Using pulse height and integrated charge, the capacitance is determined.

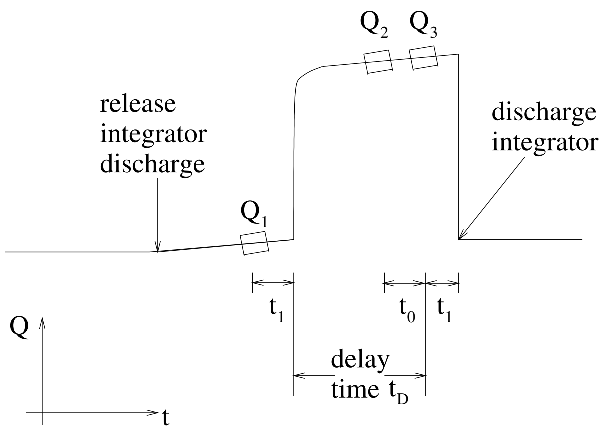


Figure 5.16: *Integrator charge vs time for a capacitance measurement cycle. [KEI86].*

Fig. 5.16 shows the integrator charge as a function of time. The integration is started when the switch for discharging the integrator capacitance is released. Even before the voltage pulse is applied, some charge is already integrated in case of any leakage current of the test capacitance, which is indicated by Q_1. After a well defined time t_1 the pulse is applied and integrated charge promptly increases sharply. After a certain delay time t_D Q_3 is measured. Then, the capacitance simply results from

$$C_x = \frac{Q_3 - Q_1}{V_{step}}, \tag{5.71}$$

with V_{step} being the voltage pulse height. As already mentioned, leakage current is included in the integration which must be corrected for this effect. For this reason, a third integration Q_2, which is performed t_0 before the last one, is required which then provides the leakage component,

$$\frac{Q}{t} = \frac{Q_3 - Q_2}{t_0}, \tag{5.72}$$

where $\frac{Q}{t}$ denotes the charge increase with time due to current leakage.

Taking it all together, the corrected capacitance then is

$$C_{x,corr.} = C_x - \frac{\frac{Q}{t}(t_D + t_1)}{V_{step}}. \tag{5.73}$$

Selecting sufficiently large delay-times allows to always reach thermal equilibrium during a measurement cycle. Moreover, individual pulse heights are adjustable. Details about the parameter ranges are given in [KEI86].

Limitations and errors

The obtained interface state density depends on the quality of both C-V characteristics. Therefore, when the relevant physics processes are not described correctly by the C-V curves the combined method will fail. As was discussed in section 5.2.1 this is the case for strong accumulation and for gate voltages around flat-band when majority carrier densities are high.

When approaching strong inversion, again significant uncertainties are introduced because the inversion layer capacitance becomes dominant for the low-frequency capacitance. Thus, instead of the interface trap capacitance, the sum of interface state capacitance and inversion layer capacitance is extracted and may falsely be interpreted as interface trap capacitance which leeds to an over estimate.

Another crucial point is that for practical frequencies of 100 kHz or 1 MHz some interface states still contribute to the total capacitance. This directly leads to a slight under estimate of interface states.

The combined C-V method of *Castagne* and *Vapaille* has a major advantage compare to other methods of D_{it} extraction like the *Terman* method [TER62]. Namely it does not require the knowledge of the silicon surface capacitance, which experimentally is always afflicted with large systematic errors.

Concluding, it must be stated that the combined C-V method allows to determine the interface state density in depletion and weak inversion. In this work the interface state density at midgap level was of interest. It is not significantly affected by the discussed error sources.

5.2.3 Surface recombination velocity

Extraction from I-V characteristic

A gate-controlled diode is used for a measurement of S_0. The according current-voltage characteristic and the extraction of the interface generation current I_{ox} was already introduced in section 5.1.2.

The surface recombination velocity is obtained from the interface generation current by

$$S_0 = \frac{I_{ox}}{q n_i A_{gate}}. \tag{5.74}$$

Uncertainties are introduced when the contributing gate area, i.e. the size of the depleted surface region, is not exactly known. This problem can be minimized by adding a second gate-contact which closely surrouds the inner one. When the outer ring is biased into accumulation, the lateral extension of the surface depletion is terminated by the outer ring.

5.2.4 Effective capture cross-section

The effective capture cross-section is calculated from the experimentally determined surface recombination velocity and the interface state density at mid-gap position, which must be distributed uniformly near mid-gap,

$$\sigma_{eff} = \frac{S_0}{v_{th} k T D_{it}}. \tag{5.75}$$

Therefore, the errors and limitations concerning the experimental extraction of S_0 and D_{it} propagate to the precision of σ_{eff}, too.

5.2.5 Surface doping profile

It is possible to access the surface doping profile from a measurement of the differential capacitance of a MOS capacitor [NIC82]. The doping profile can only be determined from the capacitance measurement when the profile is closely related to the free charge carrier concentration flowing in response to the ac gate voltage swing, which is the case in depletion only.

Adding an additional charge dQ_{gate} to the gate electrode, the surface depletion layer edge will move by dw to compensate dQ_{gate},

$$dQ_{\text{gate}} = -qN(w)dw, \tag{5.76}$$

with N(w) being the doping concentration in the depth w. The amount of dQ_{gate} added by a change of the gate voltage dV_{gate} is determined by the capacitance,

$$dQ_{gate} = C \cdot dV_{gate}. \tag{5.77}$$

The depletion depth w and the change of the depth dw can be obtained from the depletion capacitance,

$$C_{depl}/A_{gate} = \frac{\epsilon_0 \epsilon_{Si}}{w}. \tag{5.78}$$

From the change in 1/C_{depl} caused by a gate bias variation of dV_{gate} it is found that

$$dw = \epsilon_0 \epsilon_{ox} \cdot d\left(1/C_{depl}\right). \tag{5.79}$$

Considering that the oxide capacitance is voltage independent, in equ. 5.79 the depletion capacitance can be replaced,

$$dw = \epsilon_0 \epsilon_{ox} \cdot d\left(1/C_{ox} + 1/C_{depl}\right) = \epsilon_0 \epsilon_{ox} \cdot d\left(1/C\right) \tag{5.80}$$

After a few substitutions, the surface doping profile is obtained as a function of the depletion depth,

$$N(w) = -2 \cdot \left[\epsilon_0 \cdot \epsilon_{\text{Si}} \cdot \frac{d\frac{1}{C^2}}{dV}\right]^{-1}. \tag{5.81}$$

Chapter 6

Generic radiation induced surface effects

6.1 Experimental realisation of surface damage

6.1.1 Experimental demands

There are various demands on the design of an irradiation experiment, originating from the questions to be answered. How this looked like in particular in the context of this work is explained in the following.

The main goal was to enable the evaluation of radiation tolerance of oxide films produced by different vendors. A crucial requirement for the experiment was that all sets of test samples had to be irradiated under exactly the same conditions. Otherwise, it was impossible to distinguish between generic irradiation induced differences in characteristic parameters and effects due to systematic errors caused by unstable or unreproducable experimental conditions.

Radiation induced surface damage is not only a function of the exposure dose, but furthermore is correlated to numerous other parameters. Therefore it was necessary to develop an irradiation scenario which is equivalent to the radiation stress of the final application. This was crucial for a successful transfer of the obtained results into predictions for the radiation damage to be expected in the application.

The choice of the employed radiation source had to be done carefully. Using the wrong particle type or energy would make an extraction of the parameters of interest difficult or even impossible. A misinterpretation of the results would be likely, too.

Thinking of a run-time of 10 years in total of the ATLAS experiment, it was inevitable to find irradiation scenarios which allowed to investigate the crucial parameters on a much shorter time scale in laboratoy experiments. Beside this simple time argument, during large scale mass production it will be necessary to test radiation tolerance of e.g. silicon devices regularly. This, in case of any detected problems, will require very short reaction times because otherwise production will continue and finally might result in unusable devices.

Although it is an absolutely basic requirement for all experiments, it shall be mentioned here that a proper determination of all relevant parameters connected to the irradiation was crucial. A special focus had to be set on the dosimetry and the energy spectra of the particles used for the irradiations.

6.1.2 Gamma-ray irradiation

Electronic devices and semiconductor sensors are exposed to x-ray or gamma radiation in many applications, e.g. in medicine, material science and space applications. Gamma radiation experiments are therefore ideal to emulate the according radiation exposure in the laboratory. Common sources for those tests are e.g. Co-60 or Am-241 as well as x-ray tubes or synchrotron radiation.

Gamma quants transfere their energy to the material by either photo electrical absorption, Compton scattering or pair production.

Beside ionisation induced surface damage, gamma radiation can produce displacement damage in the silicon crystal, depending on the energy. Mainly due to secondary Compton electrons single point defects are created which alter the effective doping concentration as was discussed previously. This is not wanted in any case. A proper evaluation of pure radiation induced surface effects for example is complicated by this. Especially high resistivity detector graded silicon is much more affected by bulk damage than low resistivity silicon employed as substrates in micro electronics. On the other hand, for tests of the overall radiation tolerance of e.g. micro electronics the introduction of displacement damage is even wanted according to the expected damage occuring operation.

6.1.3 Charged hadron irradiation

Charged hardrons, as are mainly found as radiation background in space applications and high energy physics experiments, induce surface damage as well as bulk damage. This results in significant changes of bulk parameters, i.e. the effective doping and the volume generation current density.

Samples exposed to charged hadrons cannot be used for an extraction of surface parameters because a proper seperation of bulk and surface effects is often impossible. Instead, charged hadron irradiations are the most realistic test for overall radiation hardness of e.g. silicon detectors designed for high energy physics experiments.

In many cases those experiments are performed using protons or pions. The ratio of introduced surface damage, determined by the ionisation induced energy loss, and bulk damage, occuring by non-ionising energy loss (NIEL) in the silicon, can be adjusted by choosing a suitable energy and particle type. For example, the proton synchrotron (PS) at CERN provides 23 GeV proton beams, which generate bulk and surface damage similar to the particle fields predicted for the ATLAS experiment.

6.1.4 Electron irradiation

Using low energy electrons is the easiest and cleanest way to introduce surface damage. As long as the electron energy is below 260 keV, no bulk damage is produced. Thus, there is no alteration of the effective doping and other bulk parameters, which is ideal for a systematic and quantitative analysis. The DEBE-facility, which is designed for a systematic investigation of pure surface effects, will be presented in detail in section 6.2.

6.1.5 Neutrons

Neutrons do not cause any ionisation at all in silicon oxide[1]. Thus, surface properties are not affected by neutron irradiations. Nevertheless, neutrons still can be of interest for studying surface damage. Namely, together with low energetic electrons, experiments are possible which allow to add surface damage and bulk damage to a device separately in all wanted ratios by irradiating a device with neutrons with a subsequent electron irradiations or vice versa. This technique for example allows to distinguish between bulk and surface effects which in contrast is not possible for charged hadron irradiated devices, although the produced total radiation damage is the same.

6.2 DEBE facility

6.2.1 Purpose

The DEBE[2] was designed for the purpose of systematic investigations of ionisation induced surface effects on test-devices and fully operational silicon detectors as well as for regular tests of radiation tolerance as part of quality assurance procedures for sensor productions.

One of the major needs for a systematic study of ionisation induced surface effects was to experimentally emulate the surface damage which the sensors will encounter in the final application. As a conclusion from the previous paragraphs, low energetic electrons were the appropriate choice for this purpose. Furthermore, a methodic variation of crucial irradiation parameters had to be possible to allow an investigation of their influence on the total induced damage. Thus, a suitable setup had to fulfil numerous criteria, which were,

- introduction of surface damage only, i.e. leave all silicon bulk parameters unchanged
- high precision online dose measurement
- adjustable dose rate
- pre-selection of the beam energy

[1] In neutron irradiation experiments ionisation can still occur due to secondary particles.

[2] Dortmunder Elektronen Bestrahlungs-Einrichtung

- heating or cooling of the device during irradiation
- irradiation of full size detectors as well as small monitor devices
- homogeneous illumination
- possibility for online measurements on the devices and applying bias voltages

The above demands have been carefully implemented in the DEBE facility concept.

6.2.2 Setup

The central part of the DEBE facility, i.e. the electron source and the optical system for beam adjustment, consists of a former transmission electron microscope EM300G from Philips. Certainly, numerous modifications had to be done to match the experimental requirements. The key features of the setup are described in the following paragraphs, a photo is shown in fig. 6.1.

First of all, the imaging unit of the EM300G was completely removed and replaced by a high-vacuum chambre containing the sample holder and the Faraday-cup system for online dose measurements. In the front plate of the chambre feed-throughs have been implemented suitable for any kind of connections, e.g. for online measurements. The interior of the chamber can be seen in fig. 6.1.

The sample holder was desgined for samples with up to 14 cm diameter like full size 3-inch wafers. Using a Peltier-cooler, the device temperature is adjustable between -60 ^{o}C and 100 ^{o}C.

The electron beam energy is preselectable from 20 keV up to 100 keV in steps of 20 keV, which still is an original feature of the EM300G. Thus the maximum energy is far below the critical threshold for the introduction of unwanted bulk damage. The beam optics provide a continuously alterable beam spot size from 5 mm up to 14 mm diameter.

To ensure that the device illumination with electrons is homogeneous, it was necessary to measure the intensity profile of the beam spot. Here, a Faraday-cup system of 2.5 mm diameter mounted on an xy-stage was employed. The step width δx and δy of the motor movement determined the resolution. Beside profile measurements, the cup is used for online dosimetry.

For this purpose the current flowing from the cup to ground is measured by a pico amperemeter. Then, after considering the cup geometry, the electron fluence is

$$\Phi = \frac{1}{qA} \cdot \int_{t_0}^{t_1} I \cdot dt, \tag{6.1}$$

determined between t_0 and t_1. A denotes the effective area of the Faraday-cup.

According to Bethe-Bloch's formular, the specific energy loss in a certain material layer S is a function of the electron energy E and the density of the exposed material ρ. In case of e.g. MOS devices an aluminium layer on top of the silicon oxide must be

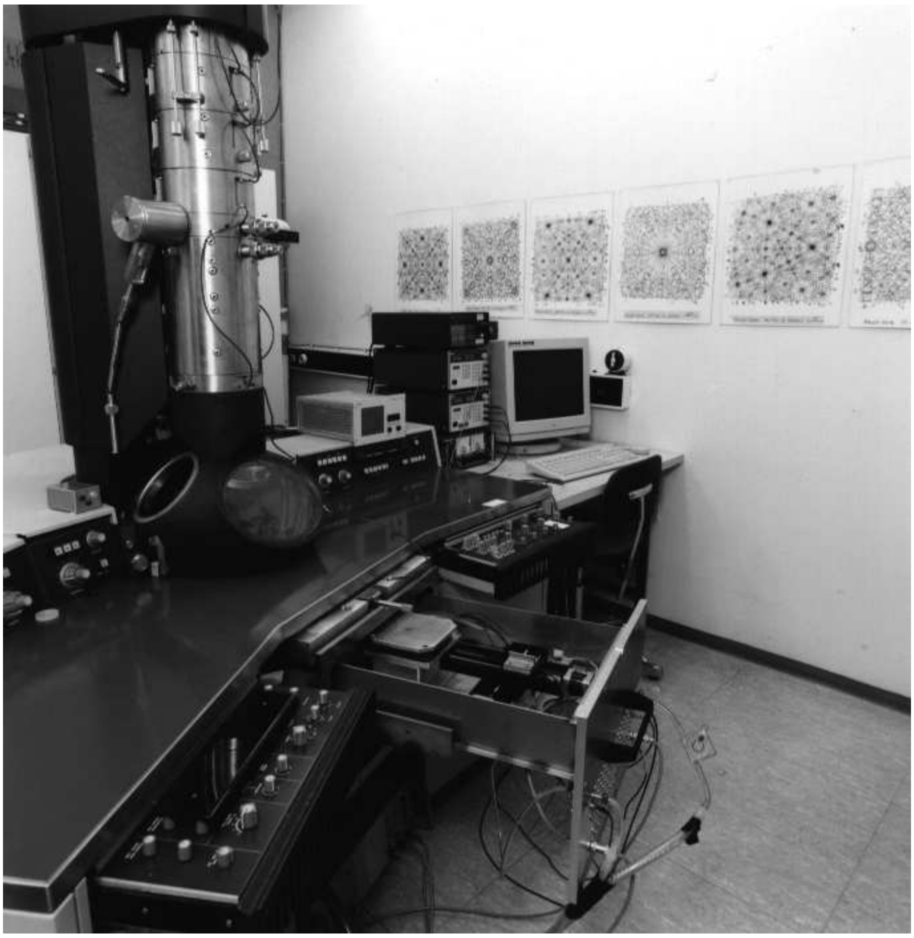


Figure 6.1: *DEBE irradiation setup. In the lower part of the picture the control panels for beam adjustment can be seen, enclosing the (opened) probe chambre. On the left hand side parts of the beam pipe are visible.*

taken into account. Assuming a reasonable thickness of 1 μm and an electron energy of 20 keV, 2.8 keV energy is lost within the metal.

Thus, the specific energy loss in the silicon oxide film is

$$S_{\mathrm{ox}} = 11.82\ \frac{\mathrm{MeVcm}^2}{\mathrm{g}}. \tag{6.2}$$

The ionising dose then is

$$D = S_{\mathrm{ox}} \cdot \Phi. \tag{6.3}$$

according to equ. 6.1. The DEBE allows to reach electron fluxes up to 100 Gy/s, which is more than enough to emulated ten years of ATLAS operation in a few hours.

Finally, the standard vacuum pump system of the EM300G was replaced, because it consisted of an oil diffusion pump and a piston pre-vacuum pump. In case of technical problems both pumps could cause an oil cantamination of the device chambre and immedeately destroy the sensitive device surface. To overcome this danger, a turbo molecular pump for the high vacuum together with a membran pre-vacuum pump was installed. Another advantage from this was to have much faster pumping times before the irradiation could be started and maintenance intervals were prolonged. This is of major importance for using the DEBE for quality assurance and radiation hardness monitoring facility in a frequent operating mode.

6.3 Generic damage dependencies

6.3.1 Dose

In chapter 4 was discussed that ionisation induced surface damage is a regeneration process, i.e. previously annealed and electrically passivated defects are re-activated by exposure to ionising radiation. Therefore, it is obvious to expect both an increase of observed damage with dose for low and medium doses, whereas for high dose levels saturation of surface damage is likely.

This indeed was experimentally observed for the positive oxide charge density as well as for surface recombination velocity.

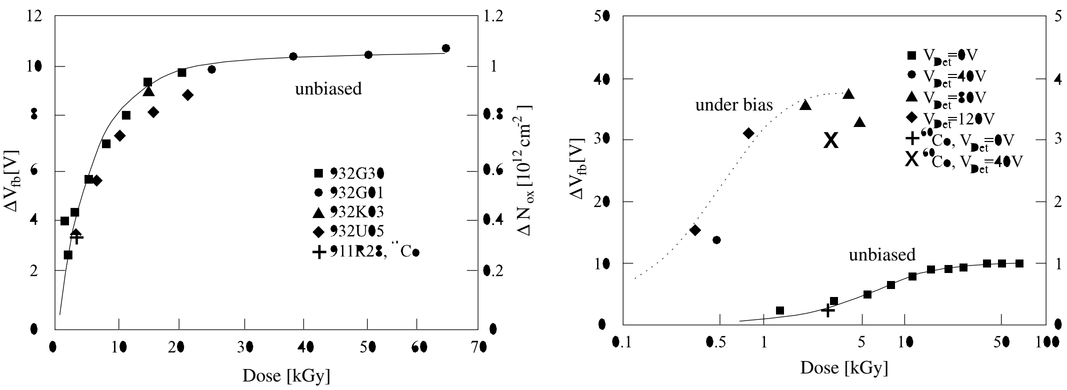


Figure 6.2: *Flat-band voltage shift as a function of dose (left) and flat-band voltage shift observed for different bias voltages as a function of dose [WUN96].*

Both graphs of fig. 6.2 show the increase of flat-band voltage, respectively oxide charge density, as a function of dose. The data depicted in the left picture were taken on an unbiassed device. A steep increase of damage with dose for lower dose levels is clearly recognizable. For dose levels higher than 20 or 30 kGy the damage levels remains constant at a saturation level of 10^{12} cm^{-2}.

In the right plot damage increase with dose is compared of biased and unbiased devices. In case of the biased sample saturation occurs for a much lower dose level around 2 kGy and the saturation oxide charge density is roughly a factor of four higher. This can be explained by a much higher generation efficiency of electron hole pairs because under an applied electric field a recombination of generated charge carrier becomes less likely. Furthermore, according to section 4.4.2, oxide charge build-up is higher in case of holes drifting to the interface.

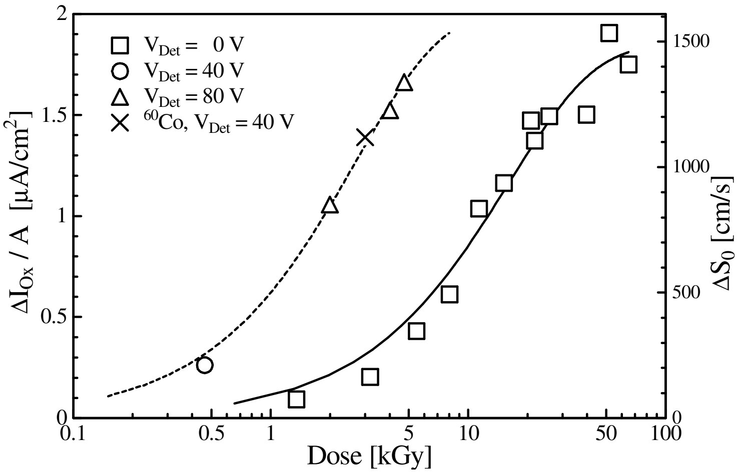


Figure 6.3: *Increase of interface generation current as a function of dose [WUN96].*

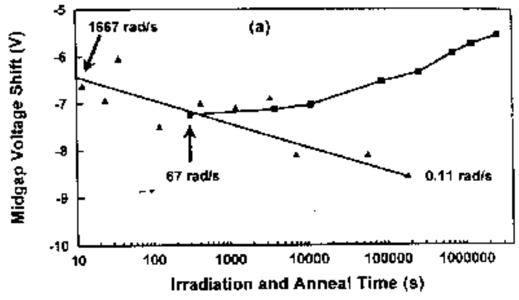
Fig. 6.3 shows the increase of interface generation current as a function of dose for unbiased and biased devices. Under both conditions instating saturation can be observed, although the saturation level itself is not reached up to 100 kGy dose. Similar to the oxide charge build-up, biased samples already show much higher surface generation current at lower doses for the same reasons as explained above. Generally, a saturation of the interface generation current is observed for doses above several mega gray [NIC82].

6.3.2 Dose rate

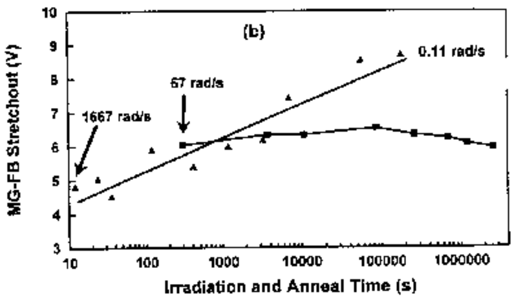
Beside the total integrated dose, the time over which this dose was received, i.e. the *dose rate*, plays an important role for the amount of surface damage created.

Assuming an irradiation with zero electric field in the oxide film, damage increase is enhanced for low dose rates. This is true for both oxide charge concentration and interface trapped charge density.

Figure 6.4 shows the increase of oxide charge density (a), respresented by the midgap voltage shift, and interface trapped charge density (b), measured by the voltage stretch-out of a high-frequency C-V characteristic, as a function of dose rate. All samples were irradiated up to a dose level of 200 Gy at zero volts without any postirradiation anneal. The according data points are represented by the triangles in fig. 6.4, whereas the squares denote an irradiation with a rate of 0.67 Gy/s and a subsequent anneal at room-temperature. Fig. 6.4(a) clearly indicates that the introduced oxide charge density is enhanced for long irradiation times, i.e. low dose rates. The same



(a) Mid-gap voltage shift versus dose rate.



(b) Stretch-out voltage versus dose rate.

Figure 6.4: Mid-gap voltage shift and voltage stretch-out versus dose rate and/or 25^{o}C anneal time for n-substrate capacitors with an oxide thickness of 1080 nm irradiated upto 200 Gy with 10 keV x-rays. Triangles are irradiations at 0 V at different dose rates, with no postirradiation anneal. Squares are 67 rad/s irradiation at 0 V, followed by 0 V 25^{o}C anneal [FLE96].

behaviour is found for the stretch-out voltage in fig. 6.4(b), where increasing voltage stretch-out is equivalent to growing interface trapped charge densities.

In fig. 6.5 two quasi-static capacitance-voltage characteristics are shown, measured after 5 kGy on MOS capacitors irradiated with different dose rates at 0 V bias. The dose rates have been chosen according to the range of dose rates used at the DEBE facility. Furthermore, the tested MOS devices were of the same CiS standard process which will be discussed in chapter 7. It was found that the minimum capacitance, which is determined by the interface trap capacitance, is higher for the low dose rate sample. This is another example showing that the creation of surface damage is enhanced by low dose rates. Additionally, using the same material, the dose rate dependence of the interface generation current was checked, too. The according current curves are depicted in fig. 6.6. For a total dose of 5 kGy, the interface current of the low dose rate sample is enhanced by a factor of six.

Generally, there are several models suggested in literature to explain the above described effects. Unfortunately, these models are only able to correctly describe particular aspects. The most powerful model is based on the building-up of space charge in the oxide bulk during irradiation [FLE96]. This is schematically illustrated in fig. 6.7. At the beginning of the irradiation there is a low electric field across the oxide which is caused by the work function difference of the gate metal and the silicon substrate. Thus, when the irradiation sets on, hole drift to the interface and electrons towards the gate contact as is shown in fig. 6.7(a). Under irradiation now positive charge builds up in the oxide bulk. When this build-up process is faster than the transport time of the hole to the interface, then high dose rate irradiaten is occuring (b), otherwise the dose rate is low (c).

For high dose rates, positive space charge builds-up as depicted in fig. 6.7(b). There-

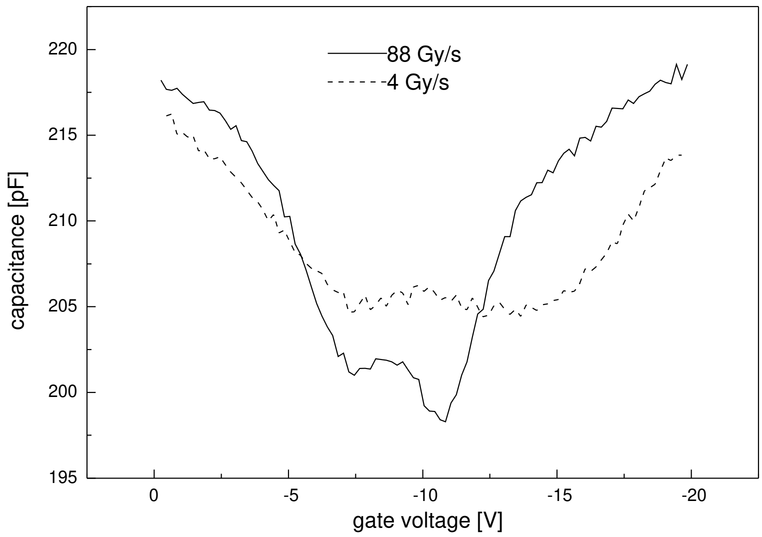


Figure 6.5: *Quasi-static capacitance-voltage characteristic of a MOS capacitor for two different dose rates. The minimum capacitance is larger for the low dose rate due to higher interface trap capacitance.*

fore, electrons generated above this spread charge drift towards it and holes move to the gate electrode. In the region between space charge and interface, electrons drift up to the positive charges and holes are transported to the interface. Contrary, low dose rate exposure cannot generate a positive space charge within the oxide film, and all generated holes drift to the interface. Qualitatively, the space charge model is able to explain the dose rate dependence of the introduction of surface damage.

6.3.3 Electric field across the oxide

Surface damage is caused by ionisation and is determined by the drift of holes and electrons through the oxide. Thus, a strong dependence of the introduced damage on the electric field during irradiation must be expected.

Fig. 6.8 shows a schematic drawing of an array of circular MOS capacitors which have especially been designed for testing the electric field dependence of the introduced damage. The complete device is small enough to be irradiated homogeneously in one step while the individual capacitors are biased with different voltages. A *common gate* surrounds the MOS devices which is used to accumulate the surface during measurements. Thus, the contributing surface area of the MOS capacitors is well defined for high precision measurements.

Fig. 6.9 shows a measurement of the oxide charge density after 5 kGy as a function of the electric field in the oxide, which was computed using a device simulator [ISE99]. As expected, the lowest introduced damage is found for zero field conditions. As soon as a non-zero field is present, oxide charge generation is enhanced because recombination

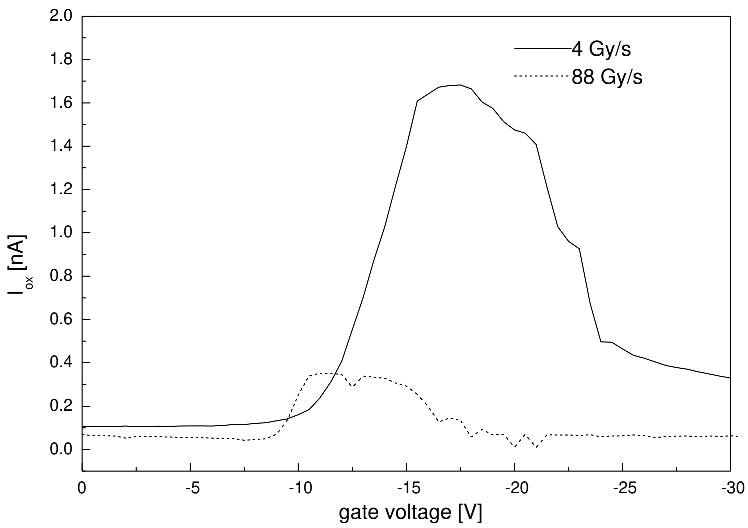


Figure 6.6: *Current-voltage characteristics measured on gate-controlled diodes after 5 kGy dose for two different dose rates. The current steps are caused by interface generation current.*

probability of freshly generated electron hole pairs is significantly reduced within an electric field.

For detector operation the electric fields present under depletion and inversion are important, which are denote with a negative sign in fig. 6.9. For fields up to -1.5 MV/cm the oxide charge density increases linearly with the field, whereas a strong enhancement is observed around -2 MV/cm. This can be explained by the efficiency of electron-hole pair generation. As discussed in [NIC82], the fraction of recombining charge carrier pairs decreases linearly for low electric fields. For a field strength of 2 MV/cm and higher, recombination is nearly completely suppressed and all charge carriers drift to the electrodes. Thus, for even higher fields the introduced damage starts to saturate.

The same MOS capacitor array as mentioned above was used to determine the interface state density as a function of the electric field, too. As described in the previous chapter, D_{it} was determined from the combined high-low frequency C-V analysis.

Other than for the oxide charge density, the damage minimum is not found for zero field but is shifted close to the initial flat-band voltage of the unirradiated device. For low fields either under accumulation or depletion conditions a linear increase is observed whereas damage enhancement saturates for higher fields. The saturation level is higher for accumulation case than for inversion.

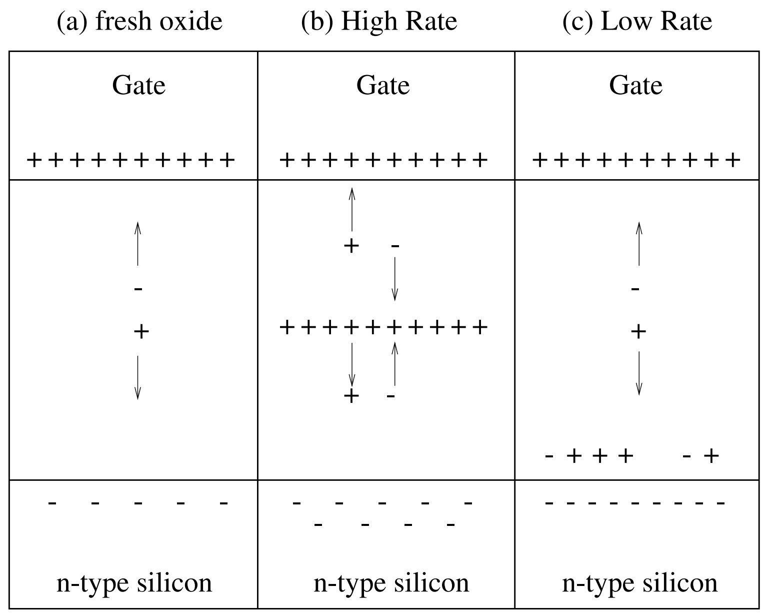


Figure 6.7: *Schematic illustration of electron and hole transport for three cases: (a) at the tart of irradiation, before trapped charge begins to build up, (b) during high-rate exposure, when holes are captured by metastable traps in the oxide bulk, causing space charge effects, and (c) during low-rate exposure, when some holes in metastable traps are emitted and transport to the interface [FLE96].*

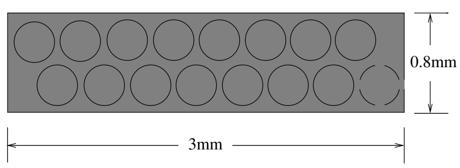


Figure 6.8: *Array of MOS 15 identical MOS capacitors which was designed for measuring the dependence of surface damage on the electric field during irradiation.*

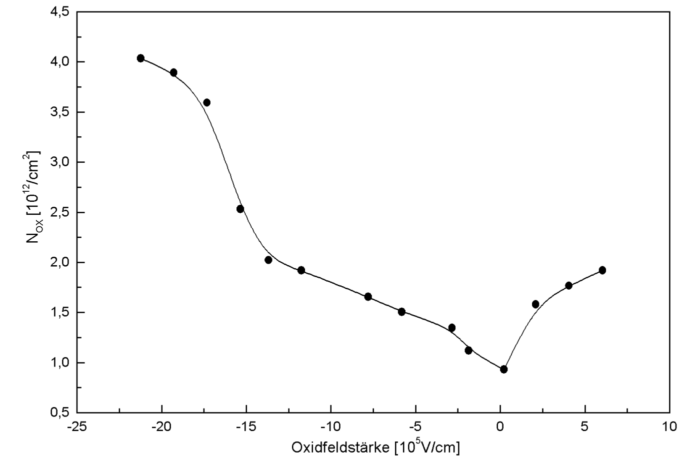


Figure 6.9: *Irradiation induced increase of oxide charge density as a function of the electric field across the oxide after a total dose of 5 kGy.*

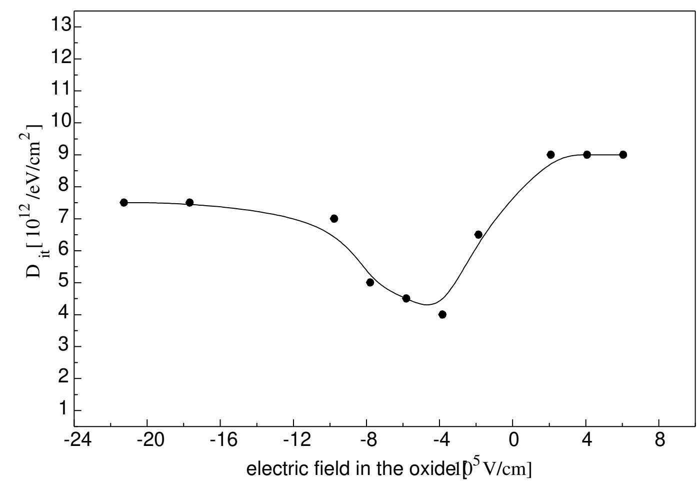


Figure 6.10: *Irradiation induced increase of interface state density as a function of the electric field across the oxide after a total dose of 5 kGy.*

Chapter 7

Radiation hardness of surfaces produced by different vendors

7.1 Test-field monitor device

The test-field [WUN00], as schematically depicted in fig. 7.1, was designed for the p^+-side of the wafer as a monitor device for systematic evaluation of surface effects. The test-field can be implemented as monitor device into various wafer mask layouts[1]. Indeed, presently it is included into the sensor wafer masks of numerous experiments like ATLAS and CMS. The ROSE collaboration at CERN has included the test-field into its test production masks as well as some vendors already implemented it as a standard monitor-device.

The standard test-field consists of two circular MOS capacitors of 1.5 mm diameter and two gate-controlled diodes of 1.0 mm size. The redundancy in both device elements provides either an identical reference sample when needed or allows to irradiate two identical devices under different electrical boundary conditions.

The gate-controlled diode itself is formed by a $7.9 \cdot 10^{-3}\mathrm{cm}^2$ circular p^+-implantation which is surrounded by 5 individual gate rings, each 50 μm wide seperated by 5 μm gaps. Enhanced by four additional gate rings, the gate-controlled diode of the test-field provides further possibilities of testing than the original gate-controlled diode first introduced by Grove et al. [GRO66]. First, the lateral extension of the surface depletion region is precisely known when the outer gates are kept accumulated. Second, the size of the gate region is variable by connecting several rings emulating a large area gate. This e.g. is important for the evaluation of the interface generation current or studies on the dependence of effects on the lateral distance from the diode. Furthermore, even C-V methods are applicable to individual gates, eliminating the influence of neighbour rings by accumulating them. When thinking of irradiation tests, individual potentials are adjustable to particular rings.

[1] There are test-field layouts available for the n^+-side with p-stop and with p-spray isolation technique, too. GDS-II files are available on request from atlas.pixel@physik.uni-dortmund.de

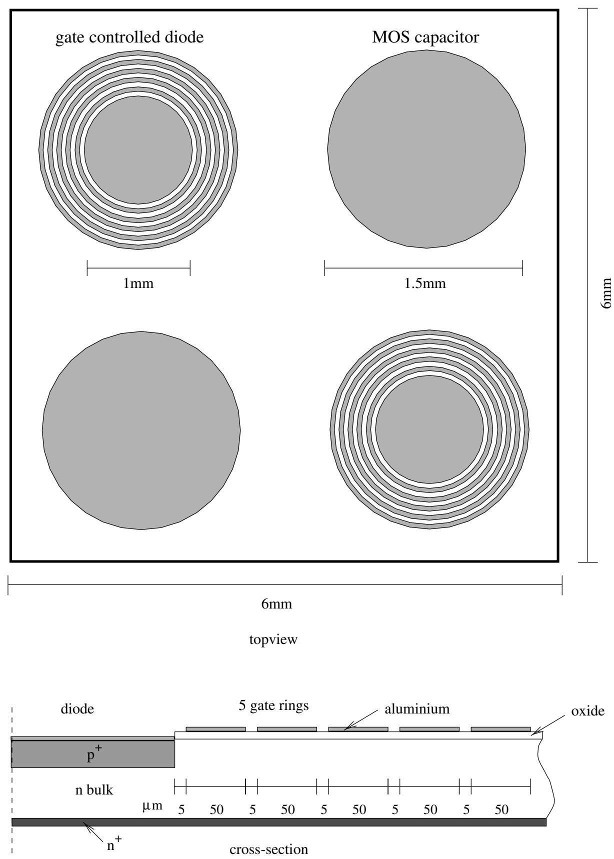


Figure 7.1: *Test-field consistent of two gate-controlled diodes and two MOS capacitors [WUN00].*

7.2 Systematics of the tests

7.2.1 Selection of vendors and materials

Preparation, oxidation process and choice of the substrate are responsible for the surface quality and radiation hardness. For these reasons a comparative study of surfaces must include a reasonable selection of different substrate types and parameters in combination with process variations. Generally, there is a large variety of possible combinations to be investigated. However, this study focusses only on those which are relevant for sensor development, although the applied systematics and characterisation techniques are fully applicable to electronic chip production processes etc.

Silicon sensors require high purity mono-crystalline silicon grown by the float-zone process. Intrinsically defect densities and concentration of contaminations are low. Most often lightly n-type doped float-zone silicon with resistivities between ≈100 Ωcm and 5 kΩcm is used. Silicon crystals with either <100> or <111> orientation are commonly employed.

Kemmer [KEM84] introduced the use of thermal oxide for silicon sensors. This technique is now well established and most vendors have implemented it into their particular process.

Typically, oxide films found on silicon sensors are thermally grown according to the Kemmer process with a thickness range of 100 nm up to 1000 nm. Due to better high voltage stability of the films, the oxidation is most often done in a dry ambient. In tab. 7.1 common properties of silicon sensors are summarised.

oxide thickness	200-500 nm
oxide growth process	thermal, 850-1250^{o}C
oxidation ambient	dry (ϵ_{ox}=3.4)
substrate orientation	<100> or <111>
substrate growth	float-zone
substrate resistivity	high, $\rho \approx 1$ kΩcm
substrate doping	n-type

Table 7.1: *Common oxide and substrate properties of silicon sensors.*

The test-field design has been systematically distributed to sensor design groups and sensor vendors to be produced with different processes. An overview of the included vendors and materials is contained in tab. 7.2.

substrate	process	diff. time	vendor
Polovodice, <111>	non-diffused	-	Canberra (Olen)
Topsil, <100>	oxygen diff.	24h	CiS (Erfurt)
Topsil, <100>	non-diffused	-	CiS
Wacker, <111>	non-diffused	-	CiS
Wacker, <111>	oxygen diff.	16h	CiS
Wacker, <111>	oxygen diff.	24h	CiS
Topsil, <111>	non-diffused	-	IRST (Trentino)
Topsil, <111>	oxygen diff.	24h	IRST
Topsil, <111>	oxygen diff.	72h	Sintef (Oslo)
Wacker, <111>	oxygen diff.	72h	Sintef

Table 7.2: *Processes and vendors of the test-fields.* non-diffused *labels standard float-zone material without oxygen diffusion.* oxygen diff. *denotes an additional oxygen diffusion step of the given duration.*

The choice of processes listed in tab. 7.2 was limited to interesting processes which are relevant for sensor production, although it can easiliy be extended by including other vendors or materials like e.g. epitaxially grown silicon substrates. In fact the intention here was to focus on the development and testing of characterisation methods and procedures for quality assurance and monitoring of radiation hardness. Certainly, materials and processes actually under discussion have been considered.

Silicon substrates with two crystal orientations were included because it is still an open discussion if sensor performance is enhanced for <100> silicon over <111> orientation.

Special attention was drawn to the oxygen diffusion processes. According to the recent results of the RD48 project [ROS99], high temperature diffusion of oxygen is of great importance for all applications suffering from charged hadron particle fields. Although the beneficial effects for bulk properties are observed now with large statistics, the influence of the diffusion on surface quality and ionisation induced radiation damage was not investigated yet. This test was still missing before a full approval of the oxygen diffused material was possible as much more radiation tolerant than standard silicon. Thus, the evaluation of surface properties of the diffusion oxygenation processes was actually of major importance and therefore part of this work.

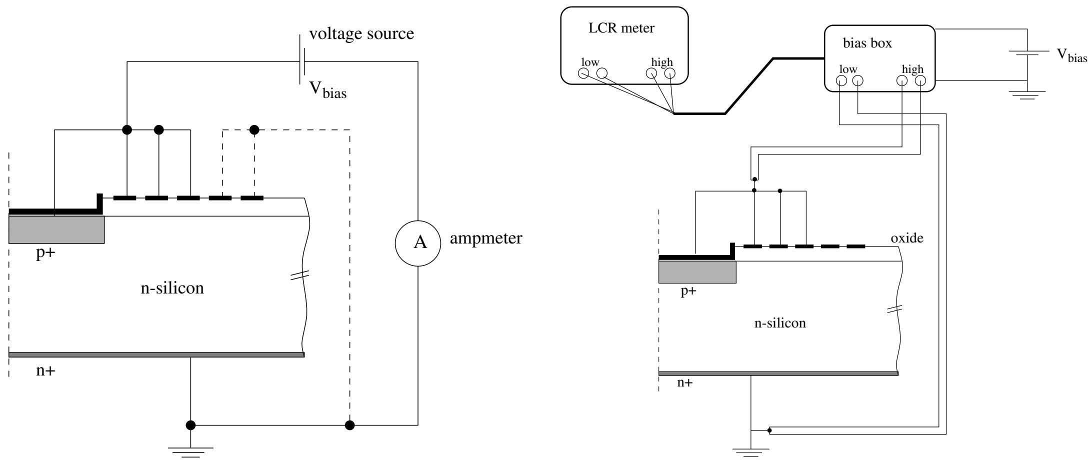
7.2.2 Characterisation procedure

A systematic extraction and evaluation of surface parameters implies various requirements to be considered for the development of an optimised characterisation procedure.

- Defective test-fields must be identified and rejected before a detailed characterisation is started, as unidentified defects are sources for misinterpretations.
- A complete set of all relevant characteristic parameters has to be obtained for each test-field, representing a certain process.
- It is a must that all samples undergo identical treatment and characterisation routines to avoid systematic errors.
- It must be considered that some measurements cannot be repeated under identical conditions due to annealing or electric field induced redistribution effects. This is of special importance for irradiated devices. Thus, a strict and detailed book keeping of all steps and especially errors and problems is obligatory

The flow-chart depicted in fig. B.2 in the appendix gives a general overview of the different steps and phases of the developed and applied characterisation procedure. It splits up into a pre-characterisation part and the main test programme.

The pre-testing was begun with an optical inspection of the test-field to identify visible defects, traces of dirt or electrical shortages between aluminium contacts and so on. Subsequently, when the optical inspection was successfully passed, an I-V curve of the diode with MOS overlap, realised by the three innermost gates connected to the diode potential, was taken. Under the same conditions the capacitance characteristic was determined. A flow-chart containing the details is attached as fig. B.3 in the appendix, the setups used for the measurements are shown in fig. 7.2.



(a) I-V measurement.

(b) C-V measurement.

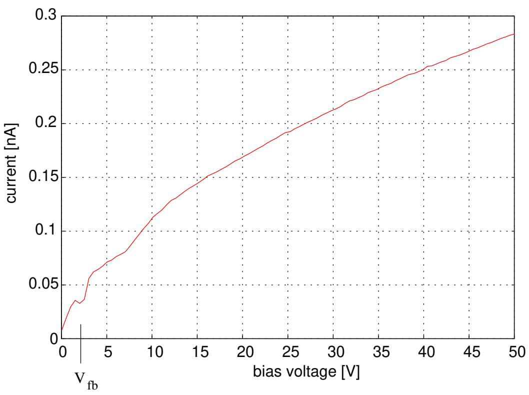
Figure 7.2: Setups used for pre-characterisation of a gate-controlled diode.

Fig. 7.3 contains examples of curves obtained in the pre-characterisation. The I-V characteristic 7.3(a) is mainly determined by the increasing volume generation current growing with the reverse bias. Around two volts a small current step was observed, which was due to the contributing interface generation current coming from the gate region. Therefore, the corresponding voltage was the flat-band voltage. Beside these physical results the I-V curve is a good help to see if the electrical performance of the gate-controlled diode is as expected or not.

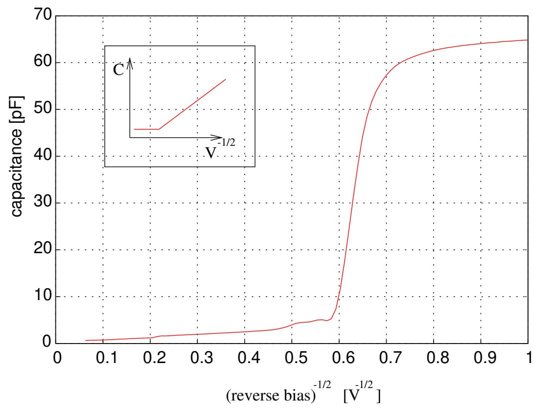
The C-V characteristic 7.3(b) is dominated by the MOS overlap for low voltages and is in agreement with the flat-band voltage of 2.3 V taken from the current-voltage curve. For higher reverse biases, the capacitance decreases in the same way as expected for a diode (insert of fig. 7.3) and thus enables to obtain the depletion voltage and then the doping concentration from it. It is a big advantage to be able to determine N_{eff} that close to the MOS devices and gate rings because then the usual lateral variation across the wafer diameter is eliminated providing higher precision.

When the pre-characterisation was successfully finished, the main testing was done, first measuring the gate-controlled diodes and then the MOS capacitors. First, a high precision measurement of the interface generation current was performed by the standard method, applied to the innermost gate. It was repeated for five different reverse bias voltages, resulting a band of current curves, see fig. 7.4(a). From the measurements the inversion voltage could directly be read as a function of the reverse bias beside the interface generation current and the flat-band voltage determination.

Then the inversion method was applied, measuring the interface generation current of the third gate-ring only while inverting both inner rings. As example an I-V curve is shown in fig. 7.4(b). On first sight this additional measurement seems to be redundant, but it is not. The third gate ring has a favoured position having an electrically identical



(a) I-V curve.



(b) C-V curve.

Figure 7.3: I-V and C-V curves measured for precharacterisation.

neighbourhood on the left and right hand sight. Therefore, it is ideal to apply C-V methods to it. Thus, it is possible to determine the interface state density on a MOS device of which the surface recombination velocity was measured.

Consequently, the next measurements are a high frequency and a quasi-static C-V curve of the third gate ring. The influence of the neighbour gates was eliminated by keeping them in strong accumulation. The C-V characterisations were repeated for the large area MOS capacitors, shown in fig. 7.5.

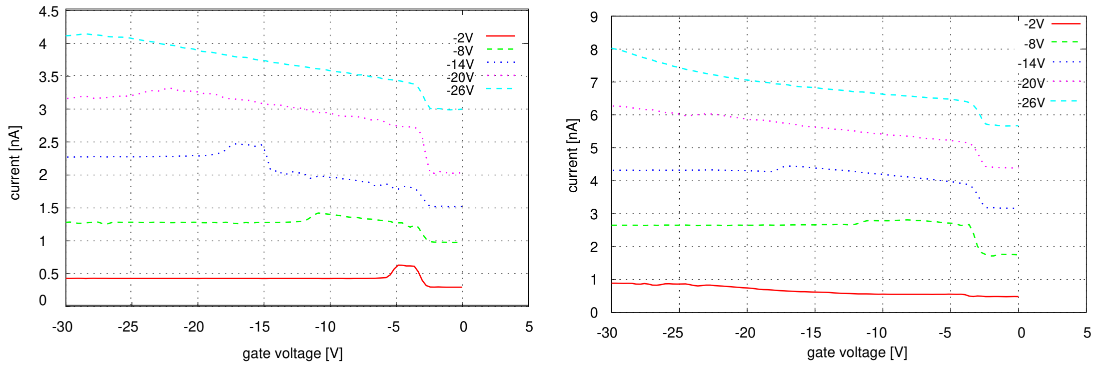
7.2.3 Irradiation scenario

Major requirement for the irradiation scenario was to generate the same level of surface damage as is predicted for silicon sensors in the ATLAS Inner Detector. Thus, a total integrated ionisation dose of 500 kGy had to be received by the test-fields at the end. Instead of dispensing the full dose in one step, a successive irradiation with

step	dose step [kGy]	integr. dose [kGy]	anneal. time [min]
1	5	5	120
2	45	50	180
3	450	500	180

Table 7.3: *Dose steps and annealing time.*

intermediate dose levels had been prefered. These intermediate dose levels according to tab. 7.3 had been included to observe the saturation behaviour of surface damage components, focussed on vendor and process dependent differences. After each irradiation



(a) Standard method. (b) Inversion method.

Figure 7.4: I-V curves obtained on a gate-controlled diode.

step a room-temperature annealing was performed for two respectively for three hours after the high dose levels to avoid time dependent changes during the characterisation procedures. The annealing behaviour was measured on an additional sample before beginning the tests. Subsequently to the annealing the test-fields were remeasured in the same way as before irradiation, just adapting voltage ranges to the induced changes like flat-band voltage shift etc.

dose rate	≈100 Gy/s
electron energy	20 keV
device temperature	293 K
gate potential	0 V (if not otherwise stated

Table 7.4: *Crucial parameters used for the irradiation tests.*

All gates were grounded during irradiation to minimise effects due to non-uniform electric field distributions, especially at the border of metallised to non-metallised regions. The field dependence was studied separately, see chapter 6. The device temperature was kept constant at 21 ^{o}C. The dose rate was adjusted to 100 Gy/s which was an unavoidable compromise between total irradiation time and the low dose rate of the LHC experiments. For the irradiation itself an electron beam energy of 20 keV was used. The chosen energy was high enough for the electrons to penetrate the full depth of the silicon oxide bulk up to the interface but low enough to prevent the introduction of bulk defects. Tab. 7.4 summarises the crucial irradiation parameters.

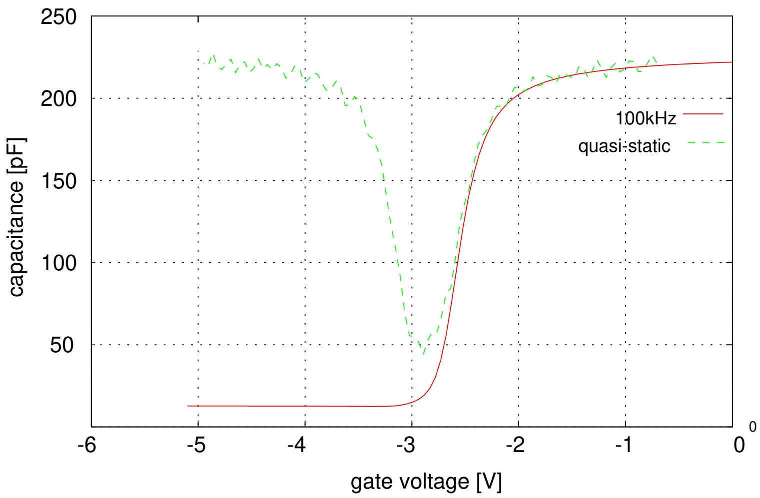


Figure 7.5: *Highfrequency and quasi-static capacitance signal of an unirradiated MOS capacitor.*

7.3 Results and discussion

7.3.1 Before irradiation

The analysis of the measured results is shown in detail along the procedure, *pars pro toto* for one sample before the surface parameters of all investigated processes and vendors will be presented.

Fig. 7.6 shows a C-V characteristic measured on the pn-junction of a gate-controlled diode. The capacitance is plotted against the square root of the bias voltage, resulting a linear curve. N_{eff} was calculated from the depletion voltage and resulted in

$$N_{\mathrm{eff}} = 7.1 \cdot 10^{12}\ \mathrm{cm}^{-3} \tag{7.1}$$

which corresponds to a resistivity of

$$\rho = 0.6\ \mathrm{k\Omega cm}. \tag{7.2}$$

The oxide capacitance was taken from a high-frequency C-V curve, see fig. 7.7 of one of the MOS capacitors of the test-field. For this device a total oxide capacitance of

$$C_{\mathrm{ox}} = 330\ \mathrm{pF}, \tag{7.3}$$

which is a capacitance per unit area of

$$C_{\mathrm{ox}}/A_{\mathrm{gate}} = 18.6\ \frac{\mathrm{nF}}{\mathrm{cm}^2}. \tag{7.4}$$

Using the effective doping of equ. 7.1, the extrinsic Debye length is calculated to be

$$\lambda_{\mathrm{n}} = 1.5\ \mu\mathrm{m}. \tag{7.5}$$

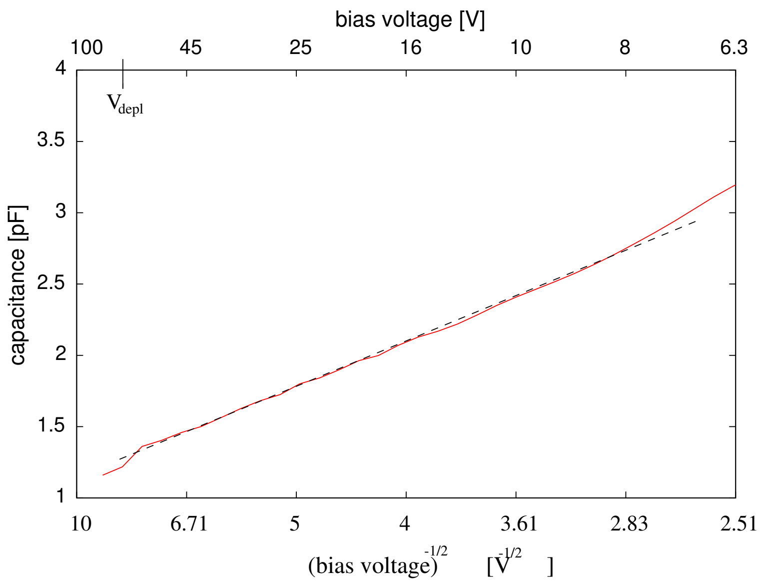


Figure 7.6: *C-V curve of the diode of a gate-controlled diode. The effective doping conentration was calculated from the depletion voltage.*

Accordingly, the silicon surface capacitance in the flat-band case is

$$C_{\text{fbs}} = 122 \text{ pF}, \tag{7.6}$$

and the total flat-band capacitance

$$C_{\text{tot}}(V_{\text{fb}}) = 90 \text{ pF}. \tag{7.7}$$

As is indicated by the dash-dotted line in fig. 7.7, the flat-band voltage now is identified by the corresponding total capacitance and is

$$V_{\text{fb}} = 2.2 \text{ V}. \tag{7.8}$$

Before the oxide charge density can be determined from the flat-band voltage, the thickness of the oxide film is needed. It is calculated from the oxide capacitance,

$$d_{\text{ox}} = \frac{\epsilon_{ox}\epsilon_0 A_{\text{gate}}}{C_{ox}} = 160 \text{ nm}. \tag{7.9}$$

Then, the oxide charge density finally resulted as

$$N_{\text{ox}} = 2.5 \cdot 10^{11} \text{ cm}^{-2}. \tag{7.10}$$

The correlation between gate voltage and band bending at the silicon surface and subsequently the interface state density as a function of band bending are assessed. For

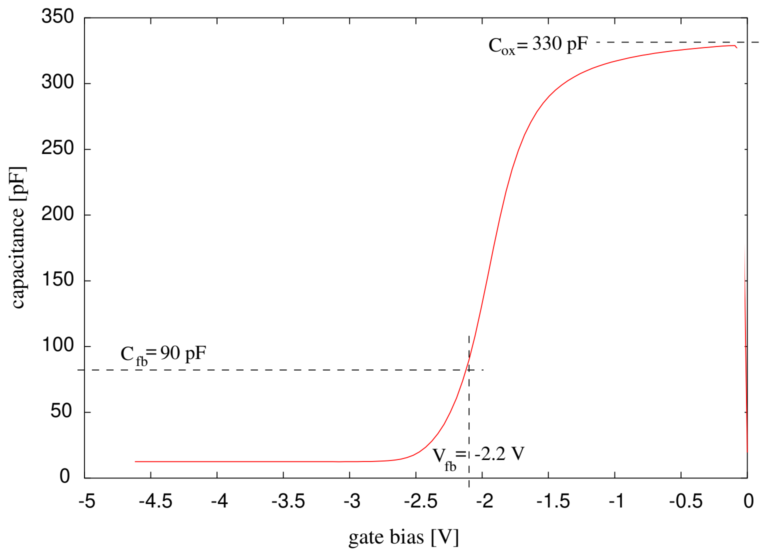


Figure 7.7: *High frequency (100 kHz) C-V curve of a MOS capacitor. The gate area is* $1.77{\cdot}10^{-2}\,cm^2$.

this the quasi-static capacitance is needed, the measured curve is plotted in fig. 7.8. In accumulation it smoothly fits to the high frequency curve, which is a nice cross-check that there are no stray capacitance differences etc present which would disturb the combined C-V analysis.

First, it is necessary to compute the band bending which corresponds to the gate bias by numerically integrating the quasi-static C-V curve as described in chapter 5. Fig. 7.9 shows the computed band bending. The points of weak and strong inversion ϕ_B and $2\phi_B$ were calculated from the effective doping concentration,

$$\phi_{\mathrm{B}} = 0.17 \text{ eV}. \tag{7.11}$$

As expected, band bending starts saturating when reaching strong inversion or accumulation. Between the flat-band point and the onset of strong inversion, the correlation of ψ_s and gate voltage is approximately linear.

In the next step the interface state density is computed using equ. 5.68. The interface state density of the Polovidoce device is depicted as a function of gate bias in fig. 7.10. Interface generation current is mainly determined by interface states in the middle of the band gap. Thus, the interface state density at midgap position is of special interest, for this device it is

$$D_{\mathrm{it,mg}} = 1.3 \cdot 10^{10} \text{ cm}^{-2}\text{eV}^{-1}. \tag{7.12}$$

The interface generation current of the device was

$$I_{\mathrm{ox}} = 16 \text{ pA}, \tag{7.13}$$

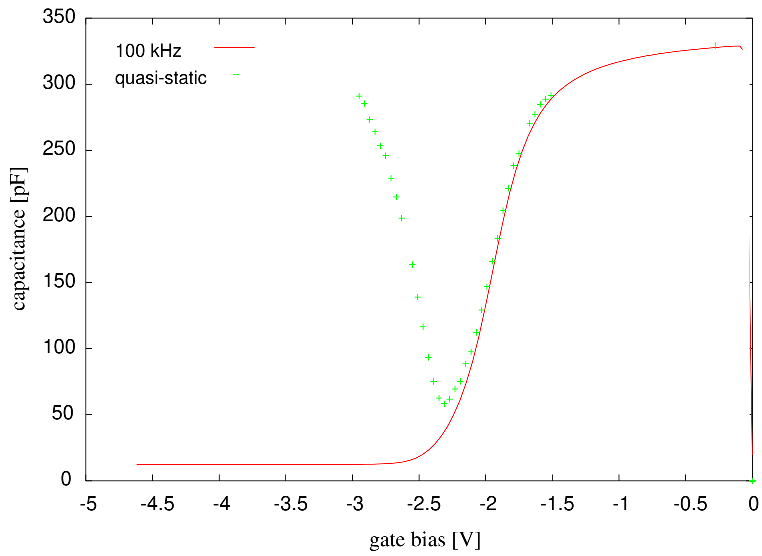


Figure 7.8: *High frequency and quasi-static C-V curves, measured on the MOS capacitor.*

being determined by the standard current method applied to the innermost gate ring. The measured curve is shown in fig. 7.11. Accounting for the size of the gate-ring, the surface recombination velocity is

$$S_0 = 7.0 \, \frac{\mathrm{cm}}{\mathrm{s}}. \tag{7.14}$$

Another value which can be evaluated from fig. 7.11 is the flat-band voltage, denoted by the onset of the surface generation current, which is in good agreement with the value obtained from the high frequency C-V analysis.

Since $\mathrm{S_0}$ and $\mathrm{D_{it}}$ are known now, the effective capture cross-section for charge carriers can be calculated and is

$$\sigma_{\mathrm{eff}} = 2.9 \cdot 10^{-16} \ \mathrm{cm}^2. \tag{7.15}$$

The above explained analysis steps have been identically applied to all evaluated samples. Tab. 7.5 is a compilation of the extracted surface parameters, i.e. oxide charge density $\mathrm{N_{ox}}$, surface recombination velocity $\mathrm{S_0}$, the interface state density $\mathrm{D_{it}}$ and the effective capture cross-section of charge carriers at the interface σ_{eff}.

The aim of a systematic analysis of the obtained data sets now is to find correlations between process parameters and vendors and the measured surface parameters. Therefore it is obligatory to compare devices which differ from each other just in the variation of the parameter of interest. In the following the data sets of tab. 7.5 are tested for those correlations.

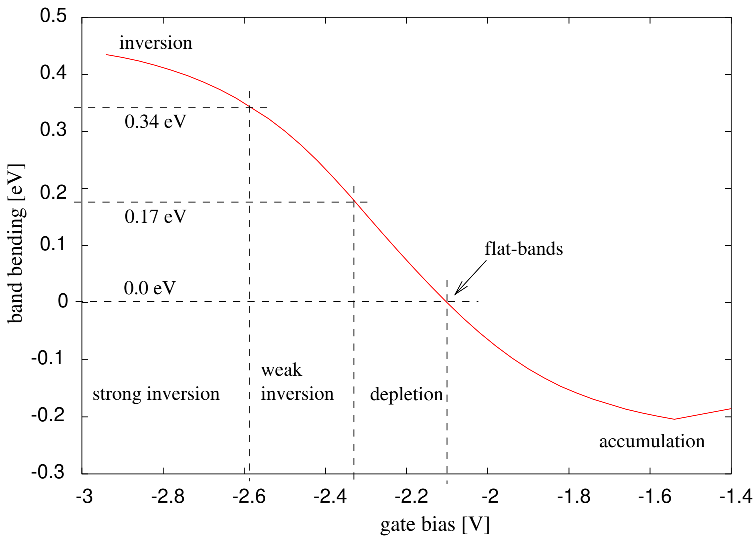


Figure 7.9: *Correlation of band bending and gate voltage.*

Diffusion oxygenation

There are several sets of samples which are qualified for an evaluation of the influence of the diffusion oxygenation process on surface quality. For example there are three CiS samples produced on Wacker <111> substrates by the standard process as well as with 16 hours resp. 24 hours oxygen diffusion. The oxygen distribution and concentration level of course depend on the diffusion time. Refering to tab. 7.5, all three samples have the same oxide charge concentration of $5.6{\cdot}10^{11}\mathrm{cm}^{-2}$ as well as an identical density of interface states of $1.7{\cdot}10^{10}\mathrm{cm}^{-2}\mathrm{eV}^{-1}$. Also the surface recombination velocity is not changed by the extra diffusion step. But there are two more sets of samples suitable for an evaluation of the oxygen diffusion process, namely the IRST test-fields on <111> Topsil substrate with standard process and 24h diffusion and the CiS samples made of <100> Topsil silicon with and without diffusion step. Concerning the oxide charge density, both sets do not show any difference between these processes. However, comparing the interface state densities there is an indication that the standard process induces less interface states than for the oxygen diffusion process. In case of the IRST <111> samples the oxygen enrichment step increases the density of interface states by a factor of ten. The CiS oxygenation of <100> substrates almost doubles the interface state density, for <111> silicon the CiS diffusion process does not alter the interface quality at all. The IRST devices show a variation in the surface recombination velocity, too, so that S_0 is four times higher for the oxygenated test-field. Unfortunately, a comparison of S_0 for the CiS processes on <100> substrate is not possible because it was not measureable due to a mechanical defect on the gate-controlled diodes.

As a conclusion here should be noted that the oxygen diffusion process does not affect the density of positive oxide charges, regardless of the diffusion time. This state-

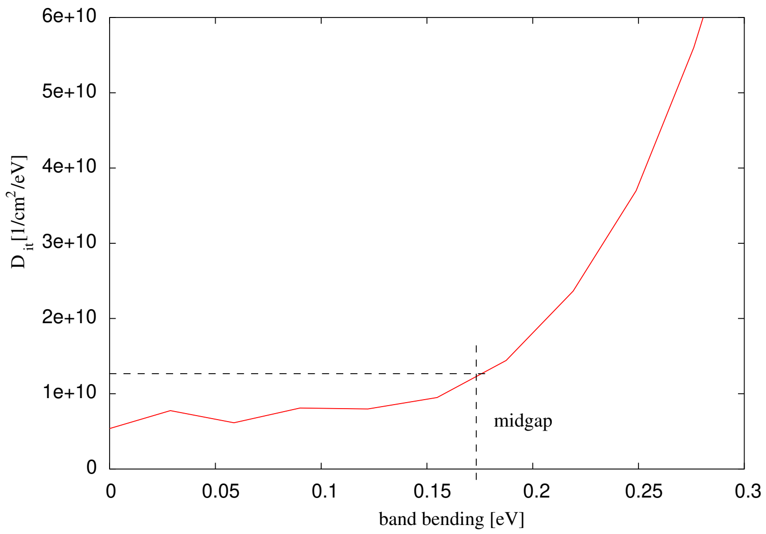


Figure 7.10: *Obtained interface state density as a function of band bending. For the further discussion the mid-gap value is use because it determines the generation of interface current.*

ment is valid for both crystal orientations and was verified on three independent parameter sets. Regarding to the interface state density, indications have been found that the performance of standard float-zone silicon is slightly better than for the oxygen diffused material. However, no differences could be identified for <111> test-fields produced by CiS. Also the surface recombination velocity might be slightly lower for the standard process. Nevertheless, regardless of the process, all measured parameters indicate high quality surfaces and are in a completely uncritical range.

Crystal orientation

To study effects of the crystal orientation on the surface quality, again the CiS samples are the best choice. As can be seen from tab. 7.5, all <111> samples have the same oxide charge concentration and this is true for the set of <100> devices, too. Therefore, both groups can be directly compared without a further differentiation. The result is, that the performance of <100> surfaces is better by a factor of three in regard to N_{ox}. For the interface state density a further distinction of the <100> group is needed because the measured D_{it} values are different. Nevertheless, the two standard process samples must be compared. It is found that the interface state density of the <100> sample is about a factor of two lower than for the other crystal orientation. Contrary, no difference in this parameter is observed for the oxygenated device. Concerning the surface recombination velocity, the standard process devices have the same performance, the diffusion oxygenated samples cannot be compared because of the defective gate-controlled diode.

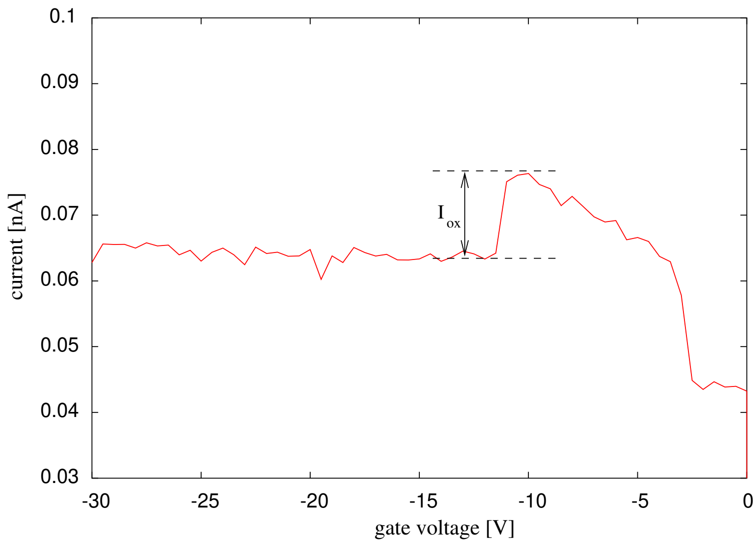


Figure 7.11: *Measurement of the interface generation current by the standard method. The reverse bias applied to the diode was -8 V.*

Summarising, CiS surfaces on <100> silicon show a factor of three less oxide charge density than according <111> samples. This is in agreement with theoretical predictions considering a difference in the bonding density at the silicon surface by the same value. But when comparing the performance of <100> surfaces to the full set of evaluated processes, it is within the same range as <111> surfaces.

Concerning the surface recombination velocity, no difference was detected at all, although S_0 is even more sensitive to the difference in interface bonding density. But this crucial dependence is probably masked by vendor specific treatments and preparation procedures like surface polishing which the wafers undergo before being processed further. Thus, no advantage using <100> silicon was found here.

Vendor

For reasons of comparison, the CiS devices processed on <100> silicon are excluded from the discussion now because according counterparts of other vendors were not available.

According to the data compiled in tab. 7.5, it is possible to identifiy varieties between different vendors altough it is not useful to define a ranking of vendors here because the variations are almost marginal. Instead, a more important outcome of the investigations here is that the applied methods and processes provide good sensitivity for an evaluation of even small performance variations, e.g. providing the results discussed below. Therefore, the developed and tested procedures are a powerful tool for e.g. quality assurance tests.

The CiS devices had the highest oxide charge density of $5.6{\cdot}10^{11}\,\mathrm{cm}^{-2}$. Slightly lower

process	N_{ox} $[10^{11}\mathrm{cm}^{-2}]$	$D_{it,mg}$ $[10^{10}\mathrm{cm}^{-2}\mathrm{eV}^{-1}]$	S_0 [cm/s]	σ_{eff} $[10^{-16}\mathrm{cm}^2]$
Polov. <111> diff.ox., Canberra	2.5	1.5	7.0	2.9
Topsil <100> diff.ox., CiS	2.1	1.7	[1)]	-
Topsil <100> Std.FZ, CiS	2.1	0.9	8.0	5.6
Wacker <111> Std.FZ, CiS	5.6	1.7	8.0	2.8
Wacker <111> diff.ox. 16h, CiS	5.6	1.7	7.6	2.8
Wacker <111> diff.ox 24h, CiS	5.5	1.8	8.0	2.8
Topsil <111> Std.FZ, IRST	3.9	<1.1	< 4.4	2.5
Topsil <111> diff.ox 24h, IRST	4.2	12.0	12.0	0.6
Topsil <111> diff.ox 72h, Sintef	0.6	0.4 [2)]	1.7	2.5 [3)]
Wacker <111> diff.ox 72h, Sintef	0.6	0.4 [2)]	1.7	2.5 [3)]

Table 7.5: *Surface parameters obtained on the unirradiated devices.* [1)] *The parameter was not measurable due to a mechanical defect on the gate-controlled diode.* [2)] *The mid-gap interface state densities have been calculated using the capture cross-sections* [3)]. diff.ox. *denotes an additional high temperature oxygen diffusion step of the given duration.*

N_{ox} was measured on the IRST surface with $3.9{\cdot}10^{11}\mathrm{cm}^{-2}$ oxide charges. Already enhanced by a factor of two compared to the CiS process is the Canberra device. Looking at the surface recombination velocities, the CiS surface has the highest velocity of 8 cm/s, followed by Canberra with 7 cm/s and, showing the best performance, IRST with less than 4 cm/s. An equivalent order is determined for the interface state density, too.

The Sintef values are completely out of range compared to the above group of devices. Surface quality is significantly better than for all other test-field sets. The oxide charge density is nearly a factor of ten less than for the CiS devices. An enhancement over the other samples is found for the surface recombination velocity, too, being eight times less compared to CiS. Apparently the Sintef oxdiation process introduces less interface states[2], too. The outranging performance of the Sintef process was observed already in the past.

The effective capture cross-section

In the last column of tab. 7.5 the effective capture cross-section is given. It was calculated employing the surface recombination velocity and the interface state density measured at mid-gap position. The values are in the order of $10^{-16}\mathrm{cm}^2$, which is in good agreement with literature data, being determined with other independent methods [NIC82]. On the one hand it is a cross-check that the applied measurement techniques are appropriate and provide reliable results. On the other hand, it is possible to use generalised cross-section of e.g. $2.5{\cdot}10^{16}\mathrm{cm}^{-2}\mathrm{eV}^{-1}$ and calculate for example the mid-gap interface state density without introducing significant error while only using the surface recombination velocity. A practical advantage from this result is that the rather complex combined C-V analysis is avoidable for quality assurance procedures.

7.3.2 After irradiation

After each step of the irradiation programme described in section 7.2.3 all test-fields were characterised again in the same way as before irradiation. Thus, the identical treatment sustains full comparability between the different process and vendor combinations. First, general observations concerning radiation induced effects will be discussed, using the Polovodice samples as example. Then the studies are extended by an evaluation of the radiation hardness of all tested processes.

A set of high frequency C-V curves measured on a MOS capacitor after several dose levels is depicted in fig. 7.12. The curves are shifted to more negative gate bias voltages with increasing dose. For doses of 50 kGy and above saturation is almost reached, because the 50 kGy and the 500 kGy curve are identical. With the help of the dotted line marking the flat-band capacitance, it is possible to directly read the flat-band voltages from the plot and calculate the according oxide charge densities. The obtained results are depicted in fig. 7.13, showing the oxide charge density as a function of ionisation dose. Even for low dose levels starting saturation is observed which is almost reached at 50 kGy, as was already seen from the C-V curves. The saturation level of oxide charges for this sample is $2.3{\cdot}10^{12}\mathrm{cm}^{-2}$.

Going back to the C-V characteristics of fig. 7.12, a growing stretch-out of the curves is observed beside the flat-band voltage shift. This indicates a radiation induced increase of interface states, responding to the voltage ramp of the measurement. More about the interface state density can be learned from the combined C-V analysis, the evaluated D_{it} distributions are shown in fig. 7.14. Whereas the initial D_{it} was around

[2] It must be mentioned here, that the interface state density of the Sintef samples had been calculated using the surface recombination velocity while defining an effective capture cross-section of $\sigma_{\mathrm{eff}}{=}2.5{\cdot}10^{-16}\mathrm{cm}^2$ as a typical value for such processes. This procedure will be motivated and justified further later in this chapter.

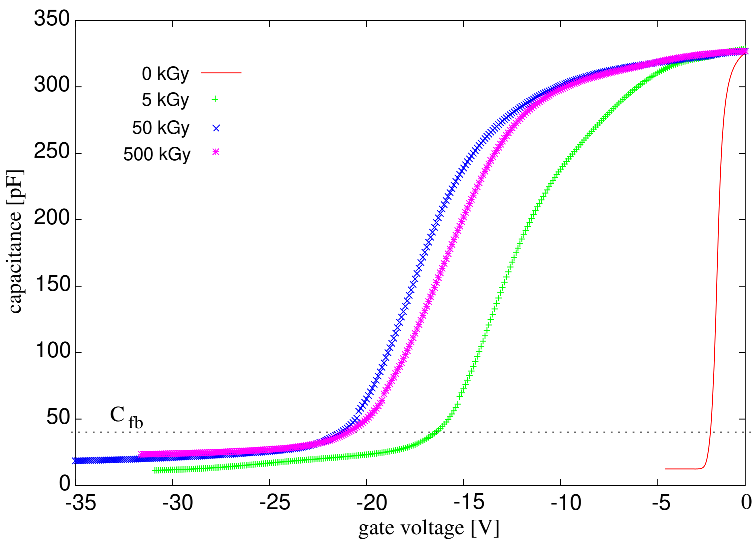


Figure 7.12: *High frequency C-V curves of a MOS capacitor after different dose levels.*

$1{\cdot}10^{10}\mathrm{eV}^{-1}\mathrm{cm}^{-2}$, it is two orders of magnitude higher after 5 kGy and further increasing up to $4{\cdot}10^{10}\mathrm{eV}^{-1}\mathrm{cm}^{-2}$. The detection limit of this method is about $1.2{\cdot}10^{13}\mathrm{eV}^{-1}\mathrm{cm}^{-2}$.

Fig. 7.15 depicts a set of interface generation current measurements performed on a gate-controlled diode as a function of dose. Measured from the pedastal at small gate voltages to the maximum, I_{ox} is strongly growing with increasing ionisation dose. Whereas it is in the order of 10 pA for the unirradiated device, it increases by two orders of magnitude after irradiation. The typical shape of the current curve is altered slightly by irradiation, which is caused by a change in the correlation between gate voltage and silicon surface band bending. Radiation induced alterations of band bending as a function of gate voltage is addressed in chapter 8. The total current increase must be due to charge carrier generation at the interface, because an introduction of bulk related defects is csystematically ruled out by using a 20 keV electron beam. The surface recombination velocity was calculated from the measured interface generation current values and is shown in fig. 7.16.

Below 500 kGy dose a saturation of the radiation induced increase of S_0 was observed although the saturation level was not reached yet. Apparently the saturation dose for the surface recombination velocity is much higher than that observed for the oxide charge density of fig. 7.13. Similar results concerning the saturation behaviour have been reported e.g. in [NIC82].

Fig. 7.17 summarises the measured oxide charge density obtained for all tested devices as a function of the exposed ionising dose. As was already asserted for the example device above, N_{ox} is strongly growing with dose for small dose levels and then quickly turning into saturation at about 50 kGy. Above this dose no further increase is observed anymore. It must be noticed here that all process and vendor combinations

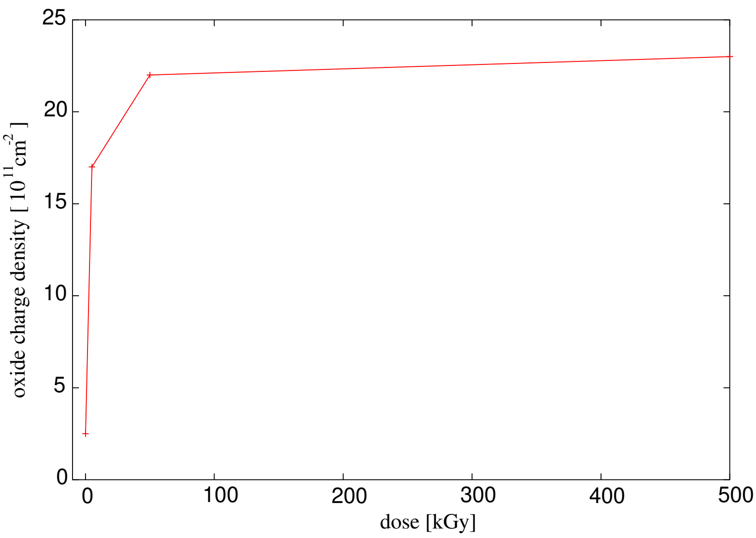


Figure 7.13: *Oxide charge density versus ionisation dose. Measurements were done after 0 kGy, 5 kGy, 50 kGy and 500 kGy dose. The data points have been spliced by lines.*

show the same general behaviour, especially the saturation dose is identical for all samples. Being always of great interest, the highest oxide charge density reached in saturation does not exceed $3.5{\cdot}10^{12}\mathrm{cm}^{-2}$ as an upper limit. Indeed, many sensor designs have been tuned to cope a maximum oxide charge density of around $3{\cdot}10^{12}\mathrm{cm}^{-2}$ which was an "educated" estimate. The data presented in fig. 7.17 now can confirm this design value, which turns out to be valid as worst case for all process and vendor combinations. The dimensioning of the doping concentration used for the p-spray isolation[3] is mentioned here as an example for an application which success strongly depends on the maximum expected oxide charge density. A first important conclusion here is that all tested devices, even after very high dose levels, are still well within the "specified" maximum oxide charge density requirement.

As well after irradiation, correlations between process parameters and radiation hardness are of interest. Employing the CiS devices, the influence of the oxygen diffusion step on surface parameters is studied. First, comparing the samples processed on <111> substrates, the final oxide charge density for the longest diffusion time is $2.6{\cdot}10^{12}\mathrm{cm}^{-2}$ compare to $2.0{\cdot}10^{12}\mathrm{cm}^{-2}$ of the standard processed test-field. In between the device with medium diffusion time is located. This is the opposite ranking of what was evaluated on the unirradiated devices. In case of <100> crystal orientation, more oxide charges were produced in the standard process samples, $3.2{\cdot}10^{12}\mathrm{cm}^{-2}$ than in the diffused one with $2.6{\cdot}10^{12}\mathrm{cm}^{-2}$. Thus, from the results shown in fig. 7.17 no systematic indications are found that the oxygen diffusion process has any influence on the

[3]The investigation of radiation tolerance of p-spray is subject of this work, too. The results are presented and discussed in chapters 8 and 9.

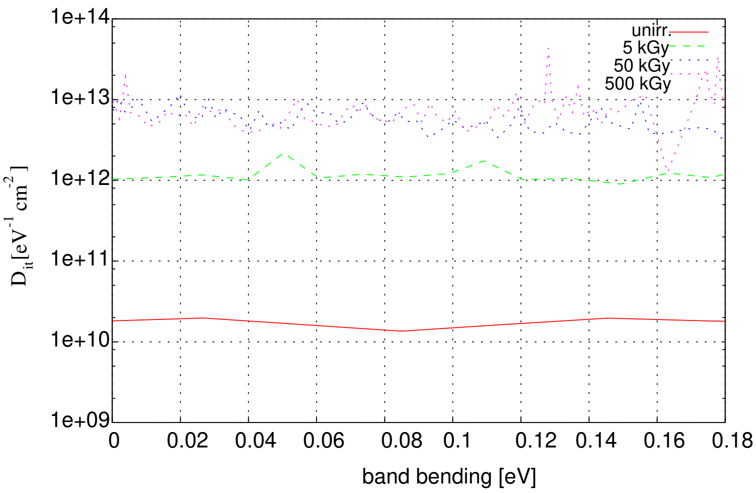


Figure 7.14: *Distribution of interface states across the band-gap after several dose levels.*

radiation hardness of surfaces at all. All values are in agreement within 35 percent.

Including the results of all test-fields except the Sintef processes, the performance of devices produced on <100> substrates was found to be within the same range as for surfaces grown on <111> silicon, regardless if before irradiation or after exposure to 500 kGy dose. The maxmimum oxide charge conentration found after 500 kGy was $3.2{\cdot}10^{12}\mathrm{cm}^{-2}$ and the lowest around $2.0{\cdot}10^{12}\mathrm{cm}^{-2}$, corresponding to an overall variation range of 35 percent.

After irradiation there is no systematic difference in the surface performance recognisable which might be correlated to the vendors. All samples are, despite minor deviations, within the same performance range. But there is one important exception, namely the Sintef devices. It must be mentioned here, that the Sintef process had only been investigated up to a total dose of 200 kGy because the irradiation tests were performed earlier. A slightly different scenario was used but it does not limit the comparability to the other data. As before irradiation, the performance of the Sintef process is much better than for the rest. The oxide charge density is still below $0.5{\cdot}10^{12}\mathrm{cm}^{-2}$ at 200 kGy.

The increase of S_0 with dose is depicted in fig. 7.18 for all tested samples[4]. The surface recombination velocities of the unirradiated devices were in the order of 10 cm/s. As can be seen from fig. 7.18, after exposure to 50 kGy an increase by two orders of magnitude occurs, but not reaching the saturation level befoe 500 kGy. This has major consequences for the increase of interface generation current because it grows proportionally to the surface recombination velocity. It strikes out that the spreading of S_0 is almost 400 percent, which, compared to a varitation of N_{ox} of 35 percent at

[4]The CiS test-field of the DOFZ 16h <111> process could only be measured up to 50 kGy dose, because it did not survive the high dose step. The reason for the fail could not be determined

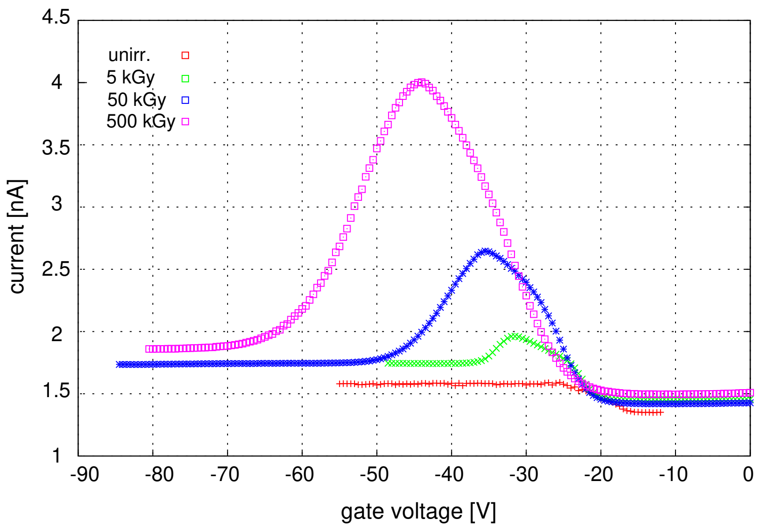


Figure 7.15: *Surface generation current measurement on a gate-controlled diode by the standard method after different dose levels.*

the same dose level, is significantly larger.

Looking closely to the data of fig 7.18, the following observations could be made. Concerning the oxygen diffusion, the data points of the standard CiS process and of the 24h diffused sample are almost identical. Nevertheless, this is completely different for the <100> standard and diffusion oxygenated samples, the measured recombination velocities differ by 2000 cm/s ! Focusing on vendor specific performance, the interface was more damaged for the CiS processes than for the IRST and especially the Canberra test-fields, having an S_0 of less than 1000 cm/s. Furthermore, the Canberra process is the only one which already shows saturation. Contrary to what was observed before, the Sintef performance shows no difference anymore. After 200 kGy dose a surface recombination velocity of 2600 cm/s was measured, being in the upper range of what was observed.

It is most surprising that <100> silicon samples do not have a significantly lower surface recombination velocity than their <111> counter parts. This is expected due to a lower bonding and defect density at the interface which should have beneficial effects for the <100> crystal orientation.

Although there were individual differences discussed above, within the complete range of observed S_0 values no systematic difference was found.

As already demonstrated for the unirradiated devices, it is possible to calculate the effective capture cross-section from the surface recombination velocity and the measured interface state density, obtained by the combined C-V analysis. As is stated in [NIC82], the effective capture cross-section for charge carriers is not affected by irradiation and is thus expected to remain constant. Therefore, the cross-sections computed for the unirradiated samples must be valid after irradiation, too. The idea here is to calculate

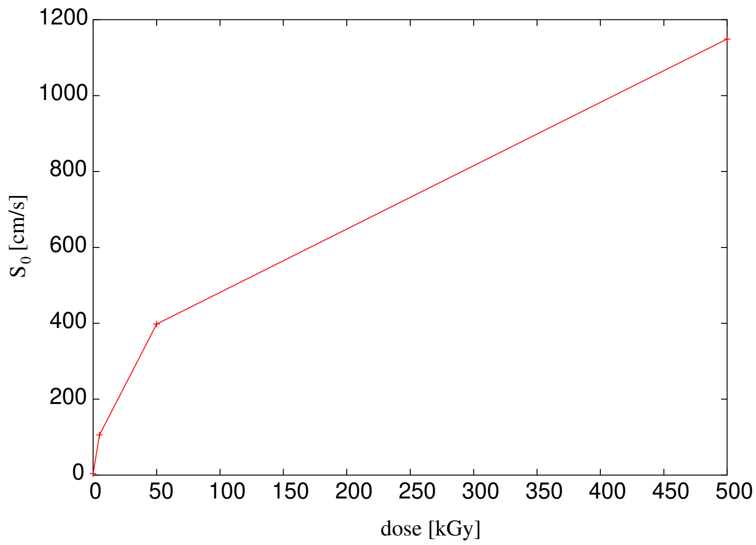


Figure 7.16: S_0 *versus dose.*

the interface state density at midgap level from the measured S_0 and $\sigma_{\rm eff}$ of tab. 7.5 and compare the achieved results with the measured numbers. This was done after the 50 kGy dose step, because for 500 kGy the measurement of $D_{\rm it,mg}$ is not possible anymore as explained before.

Tab. 7.6 contains the calculated and measured results, showing a fairly good agreement. The agreement of both results implies a good cross-check of the measurements done, because it was achieved from two completely independent measurements. It therefore is not necessary to include the powerful but complex combined high-low frequency C-V analysis into standard quality assurance procedures.

For example, the capture cross-section can now be used to calculate the interface state density for 500 kGy dose using the measured surface recombination velocity. Doing this e.g. for the CiS <100> oxygen diffused sample,

$$D_{\rm it,mg}(500\ {\rm kGy}) = \frac{S_0(500\ {\rm kGy})}{S_0(50\ {\rm kGy})} \cdot D_{\rm it,mg}(50\ {\rm kGy}) = 1.0 \cdot 10^{13} {\rm eV}^{-1}{\rm cm}^{-2}. \qquad (7.16)$$

Comparing this number with fig. 7.14, measured on the identical sample, indeed agreement is found.

7.3.2.1 Conclusion

From the above results conclusions can be drawn concerning the choice of processes and vendors suitable for silicon sensor productions. It has turned out that surfaces of the diffusion oxygenated silicon are of the same high quality than those of the standard process, regardless of the particular process, the diffusion time or the received ionising dose. There have no limitations found concerning performance and radiation hardness

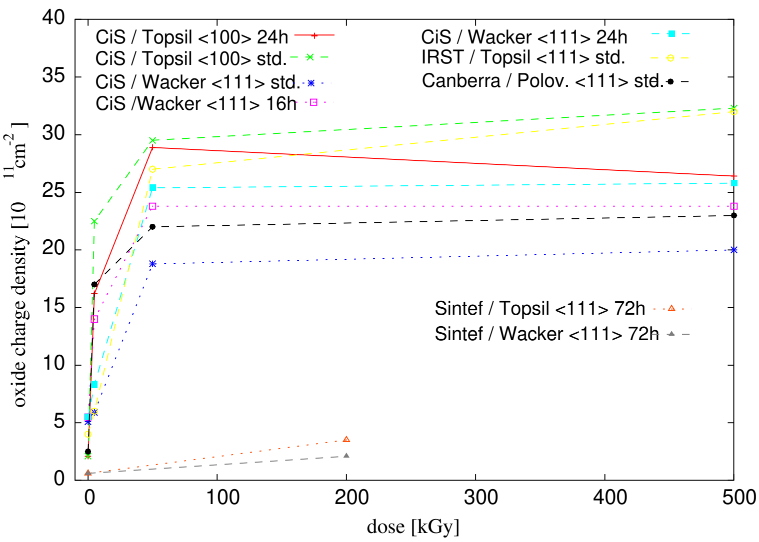


Figure 7.17: *N_{ox} versus dose.*

of surfaces of the diffusion processes. Thus, the full performance enhancement of these materials with respect to bulk damage is usable for silicon sensors operated in particle fields which are dominated by charged hadrons like in the LHC experiments. Furthermore, no indications have been found that <100> oriented crystals provide better performance before or after surface damage than <111> substrates.

The commonly assumed upper limit for N_{ox} of $3{\cdot}10^{12}\text{cm}^{-2}$ was confirmed as saturation level which e.g. the ATLAS Pixel Sensors must cope with. Saturation was also observed for the surface recombination velocity, although the saturation level was not reached up to the ATLAS Pixel Designs dose of 500 kGy.

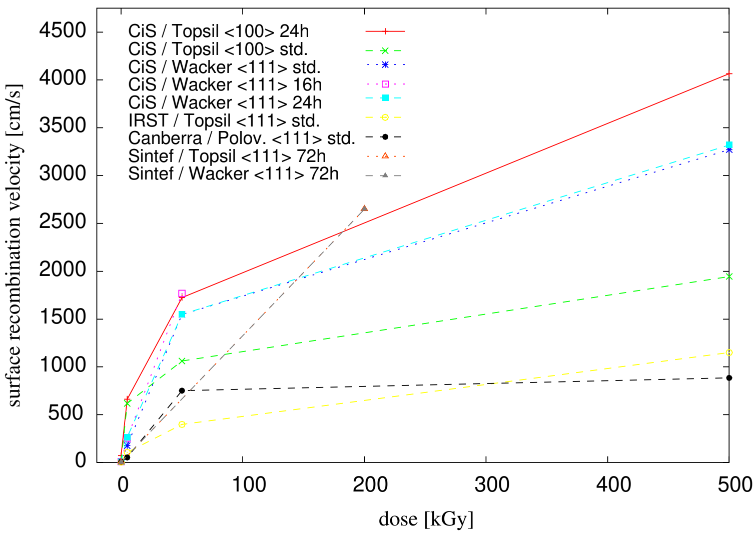


Figure 7.18: *S_0 versus dose.*

process	$D_{it,mg}$ (calc.) $[10^{10}cm^{-2}eV^{-1}]$	$D_{it,mg}$ (meas.) $[10^{10}cm^{-2}eV^{-1}]$
Polov. <111> diff.ox., Canberra	2.0	3.7
Topsil <100> diff.ox., CiS	4.4	4.0
Topsil <100> Std.FZ, CiS	2.7	3.4
Wacker <111> Std.FZ, CiS	4.0	2.0
Wacker <111> diff.ox. 16h, CiS	4.5	2.8
Wacker <111> diff.ox. 24h, CiS	3.9	3.7
Topsil <111> Std.FZ, IRST	1.0	-

Table 7.6: *Interface state density after 50 kGy dose. The calculated values were computed from σ_{eff} and S_0 taken from I_{ox} measurements. The measured values were determined directly from the combined C-V method. The quasi-static C-V curve of the IRST device was determined by noise for some reason and thus the interface state density could not be determined.* diff.ox. *denotes an additional high temperature oxygen diffusion step of the given duration.*

Chapter 8

Influence of ionising radiation on segmented detectors

8.1 Introduction

Contrary to radiation damage occuring in the silicon bulk, surface effects, regardless if observed on unirradiated or irradiated devices, are strongly correlated to the particular sensor design. Therefore it is not sufficient to investigate surface effects on MOS capacitors or gate-controlled diodes only without knowing what the impact of the obtained results on the sensor performance will be. In other words, a set of rules is required which correlates surface parameters and sensor design.

Before this can be achieved, it is necessary to identify the design parameters which might affect the contribution of surface effects to the sensor performance characteristics like total current, capacitance, electrical break down behaviour or noise. In this chapter p^+n and n^+n sensors are treated separately although the basic radiation induced surface effects are the same. But the problems correlated to them are different. Whereas surface effects in p^+n sensors are mainly determined by the size of the unimplanted area between neighbour strips or pixels, radiation tolerance of n^+n detectors is intrinsically determined by the design of the interpixel isolation. In the following section radiation induced effects on both types of sensors are systematically investigated.

8.2 p-in-n sensors

8.2.1 Relevant design parameters

Generally, it is the question for which sensors and for what particular design surface effects must be taken into account. A good criterium for this need is to calculate the ratio of unimplanted area and total area of e.g. a single design cell,

$$r := \frac{\text{unimplanted cell area}}{\text{full cell size}}. \tag{8.1}$$

Whereas for "simple" pad detectors r is much smaller than unity, it approaches unity for highly segmented designs like a pixel detector. Pure volume effects dominate the device performance for a small r parameter, surface effects become important for larger r values.

Taking a pixel sensor as an example, the total cell size is determined by the pitches in x and y direction for small cells [WUE97]. The unimplanted cell area is defined by the gap between the neighbouring implantations and the cell length. Fig. 8.1 shows a schematic cross-section of two pixel cells, illustrating the meaning of gap and pitch. For a constant pitch, fig. 8.1(a) depicts a *wide gap* design, characterised by a small

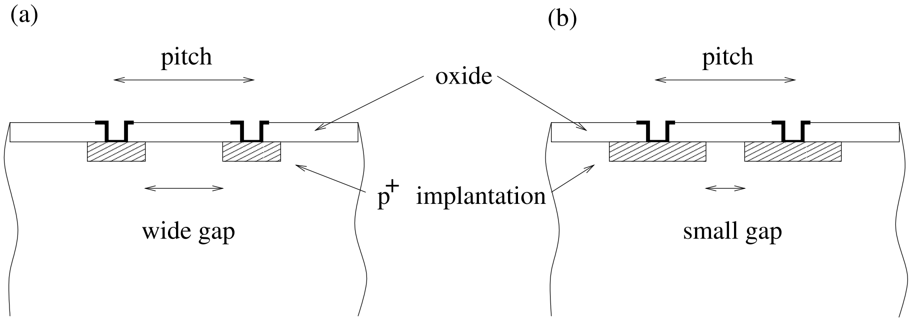


Figure 8.1: *Schematic cross-section of a segmented pn-detector. Different cell designs with (a) wide gap, (b) small gap at constant pitch.*

implantation and a wide gap to the neighbour implants. A *small gap* cell is shown in fig. 8.1(b), the implantation nearly extends over the full cell width.

I-V characteristics measured on single pixel cells at a constant pitch of 100 μm with 10 μm and 50 μm gap are depicted in fig. 8.2. Although the total cell size is equal for both pixels, the reverse current levels are different. This of course cannot be explained by bulk effects because the volume generation current is equal for the same contributing bulk volume. Instead, the origin for the observed difference are surface effects. In fig. 8.2 the calculated volume generation current level is indicated by a dashed line. It was gained from a current measurement on a large area diode, fully determined by bulk effects. The current level measured on the small gap cell is slightly above the bulk level, whereas the wide gap design shows twice as much current. Apparently, the additional current is correlated to the gap respectively to the unimplanted cell region.

For the following analysis the volume contribution to the total current was determined from the current measurement on a large area monitor diode and then subtracted from the current measured in the I-V curve. The remaining fraction then was plotted against the unimplanted surface area of the pixel cells. This was done for pixel cells with different gap and length parameters. Fig. 8.3 shows the obtained result, the surface related current increases linearly with the unimplanted surface area. It therefore must be identified with the interface generation current.

Beside the reverse current, the interstrip respectively interpixel capacitance is

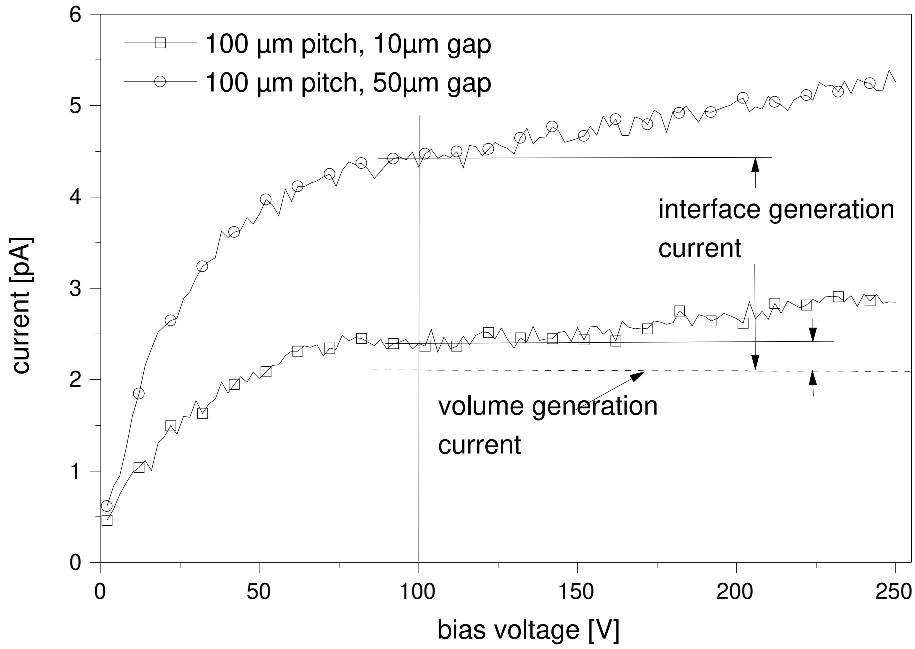


Figure 8.2: *Reverse current characteristics of small and wide gap pixel cells. Although the volume generation current is equal for both cells due to identical depletion volume, a difference is observed which is caused by interface generation current [WUE99].*

mainly influenced by the gap width, as is shown in fig. 8.4. The interpixel capacitance was measured between a pixel cell and its two neighbours as a function of the gap between the implantations. In fig. 8.4 the interpixel capacitance was normalised to the backside pixel capacitance to better visualise its relative influence. As can be seen, the interpixel capacitance is about seven times higher than the total capacitance for 10 μm gap, whereas it already decreases to a relative capacitance of 1.3 at 50 μm gap for this specific device [WUE97].

The above examples clearly show that the design parameters gap and pitch determine the performance of a pixel or strip cell. Apparently, these are the parameters which must be systematically tested with respect to the introduction of surface damage and performance degradation. Thus, a suitable test device should include systematically varied pixel cell designs taking account for gap and pitch values commonly met in particle detector designs. Such a test device is described in the next section.

8.2.2 Test device

For the investigation of radiation induced surface effects on segmented silicon sensors a special test device was used [WUE99]. Main part of the device consists of a p^+n pixel matrix, processed on high resistivity n-type float zone substrate with <111> orientation. The design includes all features of a real detector, extended by additional

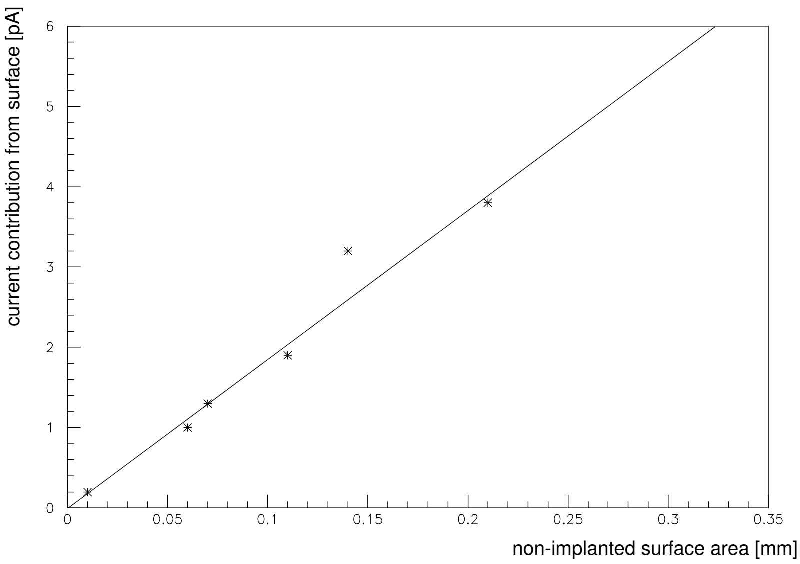


Figure 8.3: *Current contribution resulting from surface effects versus the non-implanted surface area [WUE97].*

test options. Fig. 8.6 shows a photo of the whole device of 12·12 mm^2 size. A multi-guardring structure surrounds the pixel matrix which is divided into clusters of pixels with identical design. To achieve realistic biasing conditions for laboratory measurements and for testability reasons a *punch-through* bias grid was implemented [WUE97], which is schematically depicted in fig. 8.5. Monitor devices such as a large area diode and two MOS capacitors for measurements (at the bottom of fig. 8.6) of global bulk and surface parameters have been included as described in tab. 8.1 as well.

monitor device	length [μm]	width [μm]	area [μm^2]
diode	1430	1320	1887600
MOS	364	506	184184

Table 8.1: *Dimensions of the monitor devices.*

All pixels have got an aluminium dc contact to the p^+ implantation which is slightly smaller than the implant to avoid a metal overlap. The range of the design variations allows a projection of the gained results to "real" detectors. As was already mentioned, the most sensitive design parameter is the distance between neighbouring implantations,

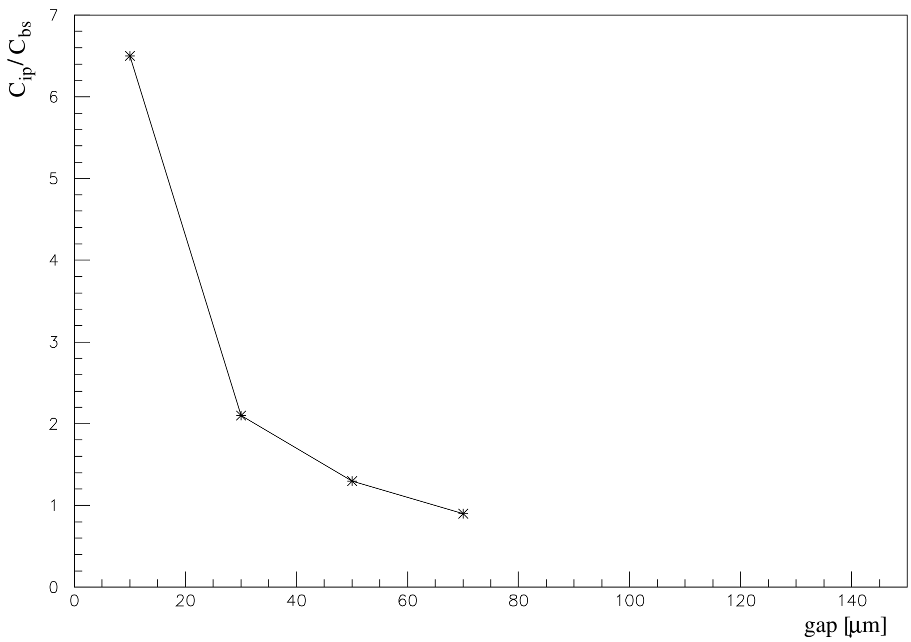


Figure 8.4: *Interpixel capacitance normalised to the back-side capacitance versus gap [WUE97].*

i.e. the gap. It was systematically altered in different clusters by altering the width of the p-implants at constant pitches from 10 μm to 100 μm. The pitch itself was varied like 1:2:4 from 50 μm to 200 μm and the cell length like 1:2:3 from 1000 μm to 3000 μm.

The performance of the unirradiated device is analysed in detail in [WUE97]. As key result it was found that the total unimplanted surface area of a pixel cell fully contributes to the interface generation current. From this it was concluded that it is possible to deplete this area completely when applying reverse bias. Furthermore, it was shown that the active area of a pixel cell is determined by the cell length and the pitch,

$$A_{\text{cell}} = \text{length} \cdot \text{pitch}. \tag{8.2}$$

Thus, it is valid to assume identical bulk contributions for cells with equal outer dimensions but different gaps. As a consequence from this, it is possible to calculate e.g. the volume generation current for a particular cell and assign the difference between observed and calculated current fully to surface effects.

8.2.3 Radiation induced effects

The pixel test device was irradiated in three steps up to integrated dose levels of 11 kGy, 170 kGy and 300 kGy, using the 20 keV electron beam of the DEBE facility. The pixel matrix was unbiased during irradiation and kept at room-temperature. After

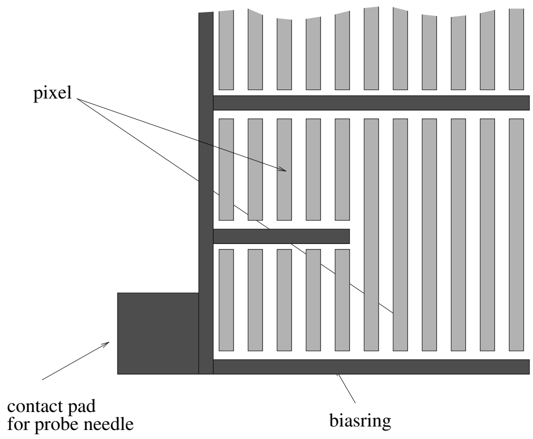


Figure 8.5: *Schematic drawing of an excerpt of the punch-through bias network surrounding the pixel clusters. The dark grey lines represent the p^+-implantation of the bias grid, the light grey lines are the pixel implants [WUE97].*

each dose step an annealing of 3 days at room-temperature was included to avoid time dependencies during the electrical characterisation.

Subsequently to each dose step, a high frequency C-V curve was measured on the MOS monitor capacitor, providing the radiation induced increase of the oxide charge density. Then, the I-V characteristic of the particular pixel cells have been measured as well as the interpixel capacitance to the first order neighbour pixels. For a determination of a proper I-V curve of a single pixel, the bias grid was grounded as well as at least one neighbour on each side of the measured pixel as described in [WUE97] to eliminate current contributions from the pixel surrounding. A schematic illustration of the used setups is depicted in fig. 8.7(a) and fig. 8.7(b).

In fig. 8.8(a) high frequency C-V curves measured on the MOS capacitor after each dose level are shown. The characteristics are shifted with increasing dose to higher gate bias voltages as well as they get stretched out, which is caused by radiation induced increase in the oxide charge density and the interface state density. From the analysis of the according flat-band voltages, N_{ox} could be determined and is plotted versus ionising dose in fig. 8.8(b). The saturation value of $1.5 \cdot 10^{12} \mathrm{cm}^{-2}$ is reached for a dose below 170 kGy, which is in agreement with the data presented in chapter 7. From this analysis using the MOS monitor device the damage levels are known for the particular dose steps.

Reverse current

After each dose level the current-voltage characteristics of all different pixel designs were measured. For the measurement a voltage ramp of 2 V/5 s was applied, starting at zero and ending at 200 V. As described above, the bias grid as well as the neighbour

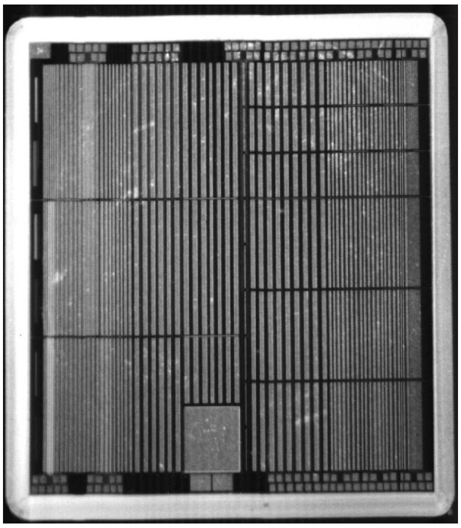
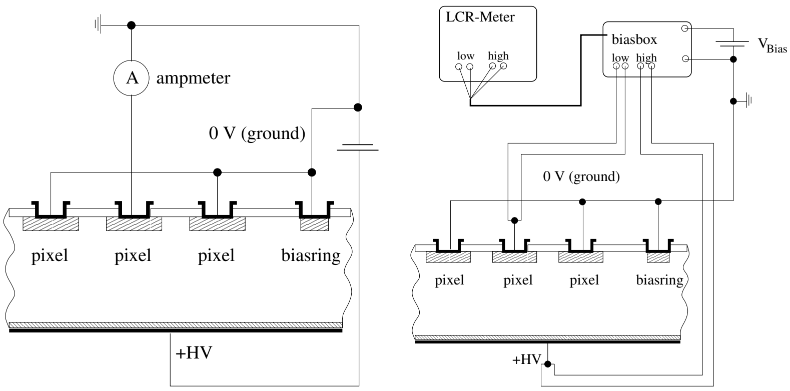


Figure 8.6: *Photo of the test device. The pixel cells are enclosed by a punch-through bias grid. A large monitor diode and two MOS capacitors can be seen at the bottom of the device. The active area is surrounded by a multi-guardring structure. [WUE99]*

pixels were connected to ground. Generally, only those pixels were characterised which had at least one neighbour pixel on each side of the identical design to avoid asymetric edge effects.

Fig. 8.9 shows the I-V curves after each dose step for different pixel cell designs. After irradiation the current levels are, as expected, significantly higher than before irradiation. As before, this cannot be explained by volume effects, because the irradiation did not affect bulk parameters at all. For example, comparing the I-V curves of two pixel cells with 10 μm gap but two different pitches of 50 μm and 100 μm, it strikes that both characteristics are identical. In case of significant volume contributions they should not. Instead this strongly supports that the current increase is caused by surface effects. Neglecting the absolute current, the shape of the curves of a particular design is similar after all dose levels. As before irradiation, pixels with wide gaps have higher leakage currents than those with smaller gaps. Additionally, the current-voltage characteristics of the wide gap designs are dominated by an exponentially growing current while for the small gaps the current level remains constant for higher bias voltages. In case of the high dose the exponential increase is even more pronounced.

Using a pixel with 100 μm gap, the I-V curve after 11 kGy was remeasured after a pre-biasing at 100 V for 10 minutes. The pre-biasing increased the current level by 50 percent. This can be explained by a long time constant for the adjustment of the potential on the sensor surface because the device was not equipped with a silicon nitride passivation enhancing this. Comparing with MOS devices, it is obvious that surface related effects strongly depend on the potential distribution on the surface and might therefore show some drift in time unless the potential is fixed. The according



(a) I-V curve. (b) C-V curve.

Figure 8.7: Measurement setups used for single pixel characterisation. The bias grid as well as neighbour pixels were grounded to eleminate parasitic currents from the surrounding.

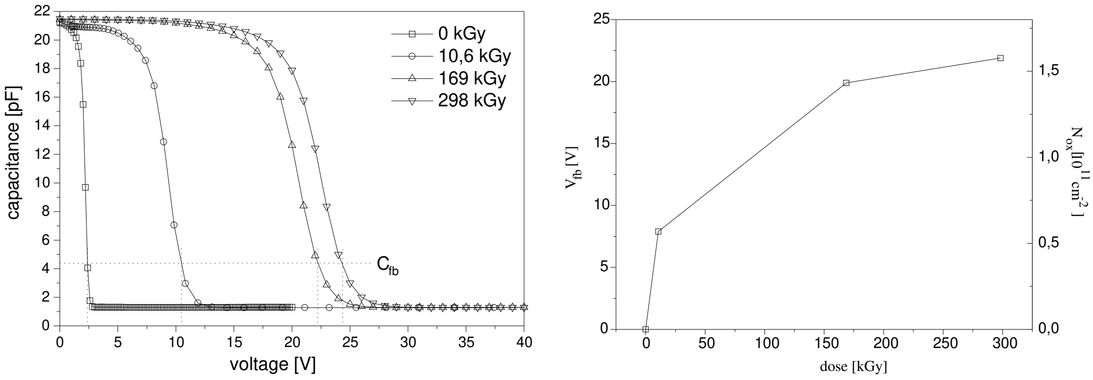
time constant is determined by environmental conditions like humidity and cleanliness of the sensor surface.

Discussion

As an explanation for these described observations concerning the design dependence of the I-V characteristics of pixel cells after irradiation, the following mechanism is proposed.

Even in an unirradiated sensor, the silicon surface is initially forced into accumulation because of the presence of positive oxide charges. When starting to apply a reverse bias to a sensor depletion sets on immediately around the p-implantations of the pixels, growing mainly into the depth with increasing reverse bias. Beside the depletion zone around the implants, the behaviour of the silicon surface in the gap is of great importance. Assuming that the potential on the oxide layer between the aluminium contacts of the pixels is very similar to the pixel potential, the silicon surface remains in accumulation unless the flat-band voltage is reached. Then the accumulation layer is removed and surface depletion sets on, immediately connecting to the depletion zones of the nearby pn-junctions. In case of unirradiated sensors, i.e. with low flat-band voltages, it is possible to deplete the whole surface by increasing reverse bias, which then fully contributes to the reverse current due to charge generation at the interface. This model view is in agreement with the I-V characteristics depicted in fig. 8.2 and the analysis of fig. 8.3.

Exposing the same detector to ionising radiation, electron-hole pairs are generated everywhere in the silicon oxide layer by the mechanisms introduced in chapters 4 and 6. Thus, the flat-band voltage is shifted to more negative gate bias voltages with increasing



(a) High-frequency C-V curves.

(b) Oxide charge density vs. dose.

Figure 8.8: Determination of the oxide charge density versus dose using high frequency C-V curves of the MOS monitor device. The data points in (b) are jointed by lines.

dose. In other words, a higher reverse bias applied to the sensor is required to establish surface depletion in the silicon. In case of significant radiation damage, i.e. for high flat-band voltages, it is now possible that the depletion zones of neighbouring pixels connect somewhere deeper in the silicon bulk before the flat-band voltage in the gap area is reached. Under these conditions, it is impossible to remove the electron accumulation from the surface at all, a fraction of them is enclosed, as is schematically depicted in fig. 8.10. As a consequence, it is even at high reverse bias voltages impossible to fully deplete the sensor ! Furthermore, electrical break down occurs due to peaking electric fields at the border of the accumulation layer, resulting in an exponentially growing reverse current.

From current-voltage measurements nothing can be concluded about the particular geometry or distribution of the enclosed accumulation layer or the surface depletion zone. Therefore, device simulations might give additional information which are not accessible by static I-V characterisation.

In [RIC96] a very similar problem has been investigated using two dimensional device simulations for two pixel cell designs with 10 μm and 65 μm gap width. Surface damage was introduced by including a homogeneous oxide charge density of $3{\cdot}10^{12}\mathrm{cm}^{-2}$, which is in good agreement with the saturation value determined in this work. An oxide thickness of 220 nm was used as well as an effective doping concentration of $N_{\mathrm{eff}}=2{\cdot}10^{12}\mathrm{cm}^{-3}$, both values are typical for these applications. The results of the calculations under gate boundary conditions for a bias voltage of 100 V are shown in fig. 8.11, i.e. the potential, the electron concentration and the electric field. One of the main results here is that in case of the small gap design a potential minimum for electrons builds-up at the silicon surface, leading to an enclosure of accumulated electrons. In contrast to this, for the wide gap option the depletion zone extends over the complete silicon surface, no enclosure is found, compare fig. 8.11(c) and (d).

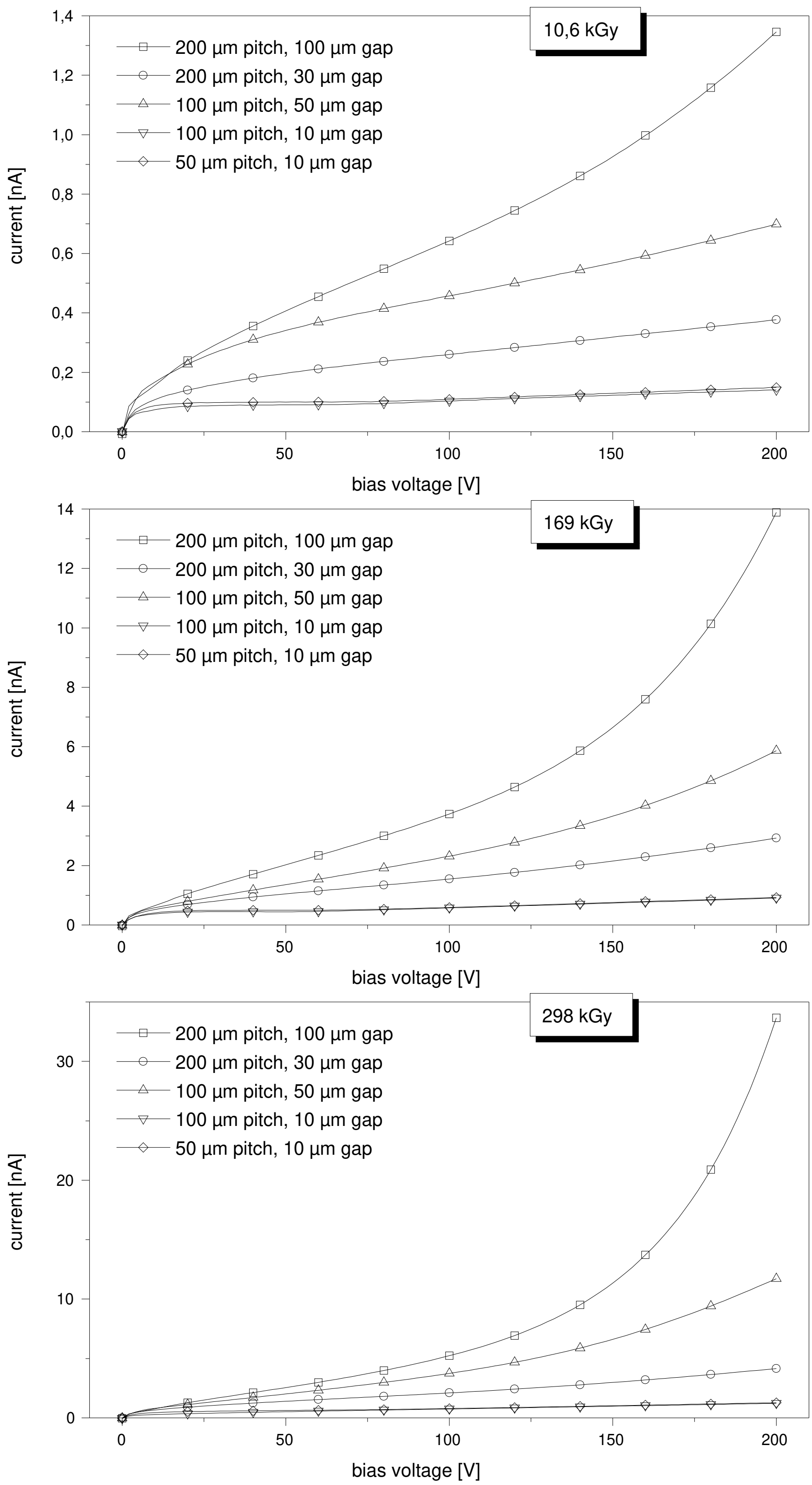


Figure 8.9: I-V curves of different pixel designs after irradiation with 20 keV electrons.

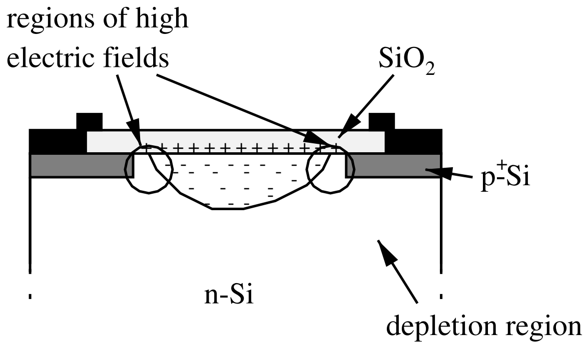


Figure 8.10: Regions of high electric fields under full depletion.

Concerning the electric field in fig. 8.11(e) and (f), high field regions are found next to the implants in both designs, the absolute field strength is higher for the wide gap option, enhancing electrical break down.

Although the results of [RIC96] predict an enclosure of accumulated electron especially for the small gap design, they cannot fully describe reality because a homogeneous distribution of damage was assumed. This is not true for the irradiated test device. Other than in large area MOS devices, the electric field distribution is non-uniform in a segmented detector, even without applied bias. Thus, the distribution of surface damage is non-uniform, too. Therefore, surface damage must be included according to the electric field distributions during irradiation.

A calculation of the electric field in the oxide was done in [WUN97b] for 10 μm gap pixels with a pitch of 50 μm. Fig. 8.12 shows the simulated electric oxide field for *von Neumann* boundary conditions (a) and *gate* boundary conditions (b) for a bias voltage of 100 V. As can be seen easily, the results are different. In the von Neumann case, field maxima are observed at the edges of the implantations whereas the field in the gap region is low. Under gate boundary conditions high electric fields are generated in the middle of the gap, decreasing to the implantations, although there are some lower field maxima left very close to the implants. Thus, depending on the electrical boundary conditions, the distribution of surface damage is completely different across the gap which must be taken into account. A further result presented in [WUN97b] is, that enclosed electron layers could be identified on surface barrier detectors using a proton micro beam. The enclosed layers were correlated with the high-field regions, having the highest concentration of oxide charges. Thus, the effect of electron accumulation is supported by these results, too.

The geometry of the enclosed electron accumulation layer dependends on the lateral surface damage distribution as a result of the electric field during irradiation. As was shown in [RIC96] and[WUN97b], the boundary conditions, i.e. the potential on the sensor surface, have major impact on this. The tested detector had no nitride passivation, thus the potential on the surface was influenced by the surrounding ambient and the irradiation was performed under high vacuum. Therefore von Neumann equiv-

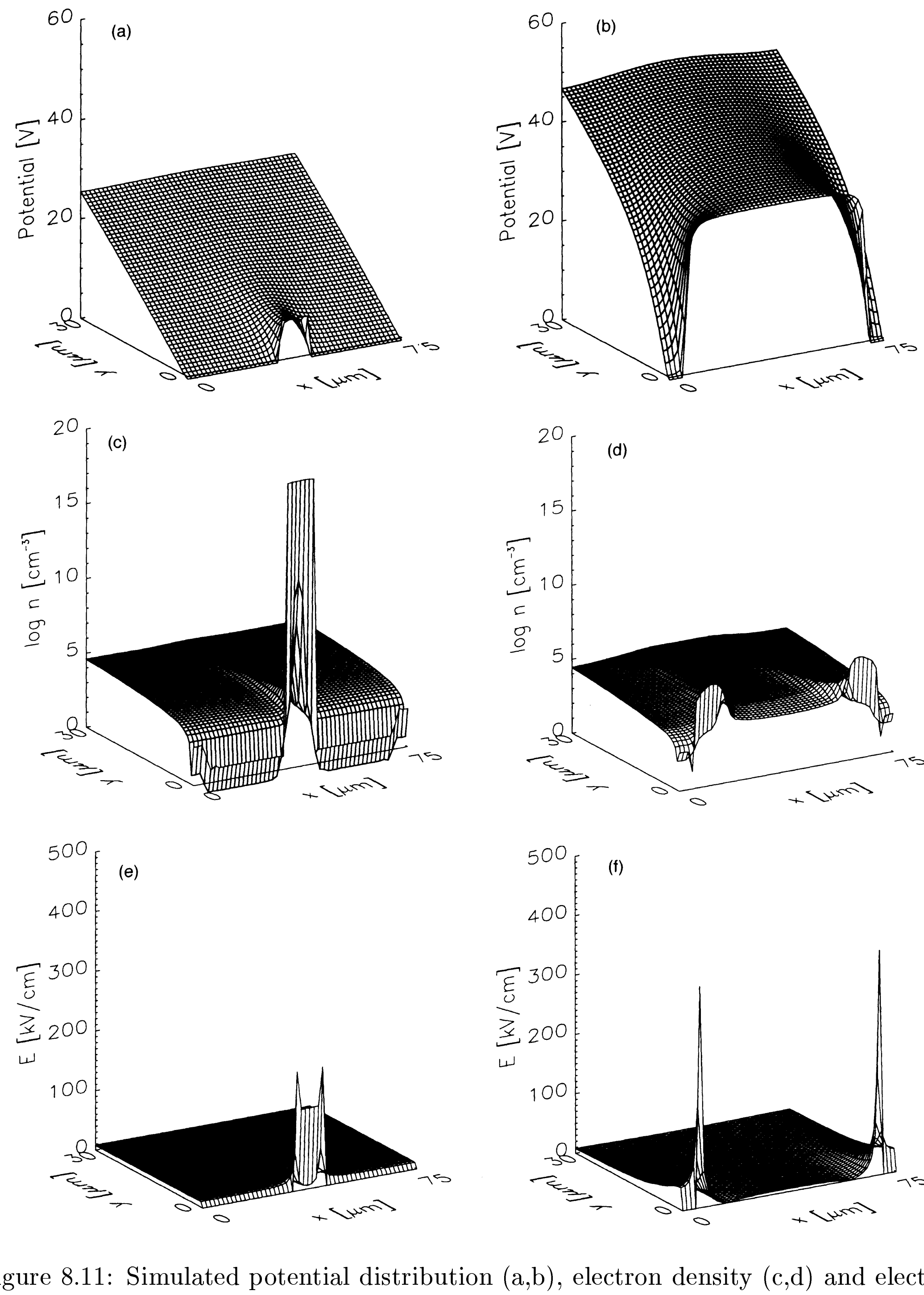


Figure 8.11: Simulated potential distribution (a,b), electron density (c,d) and electric field (e,f) for 75 μm pitch and 10 μm (left) respectively 65 μm (right) gap width for gate boundary conditions. A uniform distribution of the oxide charge density of $3{\cdot}10^{12}\mathrm{cm}^{-2}$ was used. An oxide thickness of 220 nm and a bias voltage of 130 V have been adjusted. The x-axis is directed in parallel to the interface, the y-axis into the depth of the detector [RIC96].

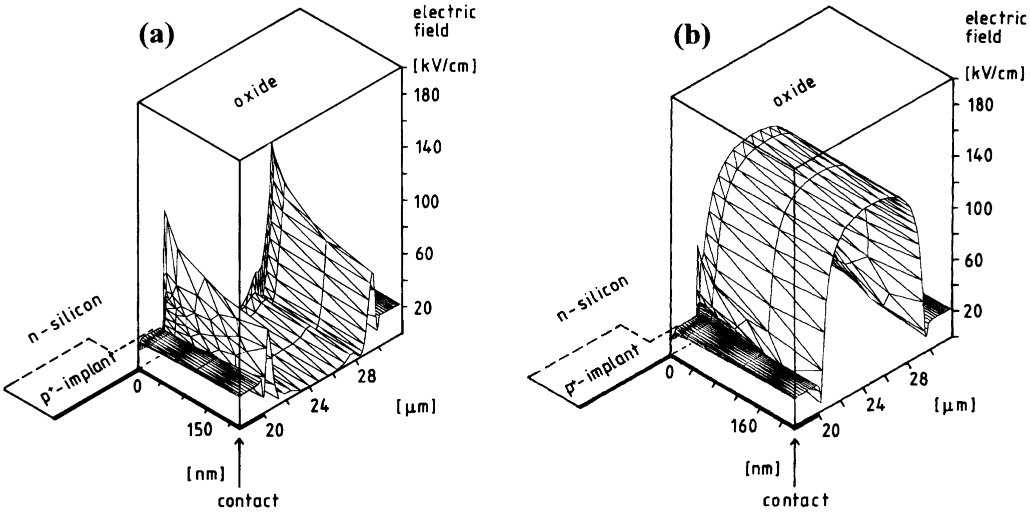


Figure 8.12: Electric field distribution in the oxide of a depleted detector (V_{bias}=100 V) with 10 μm gap width and 50 μm pitch, using von Neumann (a) and gate boundary onditions (b) [WUN97b].

alent conditions are likely. On the other hand, there are in many cases small traces of dirt on the surface left, which might enhance surface conduction and thus establish gate-boundary conditions. So, probably the field distribution during irradiation was somewhere in between both conditions. A final conclusion concerning the geometry of the accumulation layer therefore is not possible. Further investigation using a proton micro beam probe would provide further insight here.

Nevertheless, the simulated results clearly show the sensitivity of the measured effects on the potential distribution on the oxide surface. For this reason it would be very useful to evaluate how far explicit gate boundary conditions applied to the silicon oxide changes the I-V characteristic. This is certainly not a standard feature of the test device, but could be realised by adding an artificial gate with some silver loaded glue on the gap between two neighbour pixel cells as is depicted in fig. 8.13. This little trick enabled the comparison of both conditions on the identical pixel. The corresponding I-V curves are shown in fig. 8.14 for the two cases, i.e. small and wide gap. Looking to the wide gap result in fig. 8.14, a significant difference in the curves is seen. Whereas the curve without gate contact is equivalent to the characteristic shown in fig. 8.9, the added gate contact changes the pixel performance completely. For lower bias voltages the total current is higher, but remains on a nearly constant level up to 200 V, there is no indication for a break down at all. Apparently the gate contact stabilises the pixel current and results in much better performance. Fig. 8.15 shows the I-V curve together with the high-frequency C-V characteristic of the wide gap cell. The two measurements clearly show the correlation of the flat-band voltage, observable as the characteristic capacitance decrease in the C-V curve, and the current step, which is due to interface

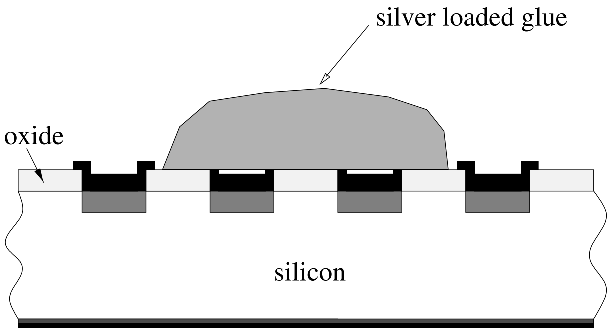
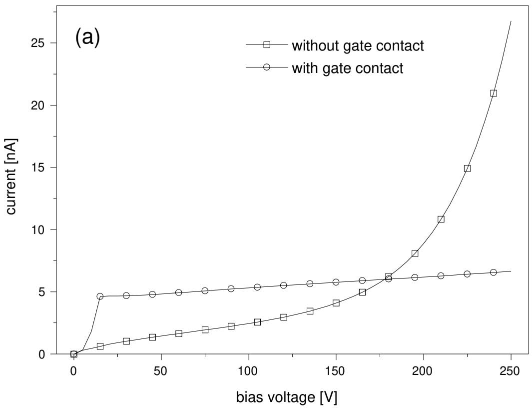
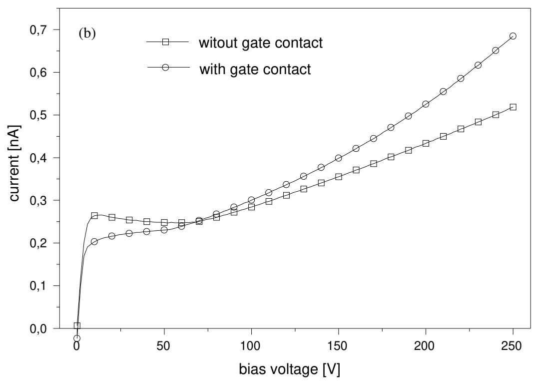


Figure 8.13: Schematic drawing showing the added gate contact.



(a) Wide gap design.



(b) Small gap design.

Figure 8.14: I-V curves after irradiation before and after adding an artificial gate contact [WUE99].

generation current. It can be concluded here that now the total non-implanted surface contributes to the interface generation current, because depletion underneath the gate contact and therefore the electrical break down have vanished.

In case of the small gap design there is no significant change in the I-V curve due to the additional gate contact visible in fig. 8.14(b). At higher voltages a slightly exponential increase is measured under both conditions. Taking the normalised interface current of the wide gap pixels it is possible to estimate the interface generation current for the small gap design, which should be two times higher than actually measured. This indicates that only a fraction of the surface is depleted, an enclosed accumulation layer is still present, even for high bias voltages. On the other hand, the wide gap pixels are fully depleted when the gate contact is present. The same result was achieved after long waiting times, when the surface potential had auto adjusted to comparable conditions by environmental influences.

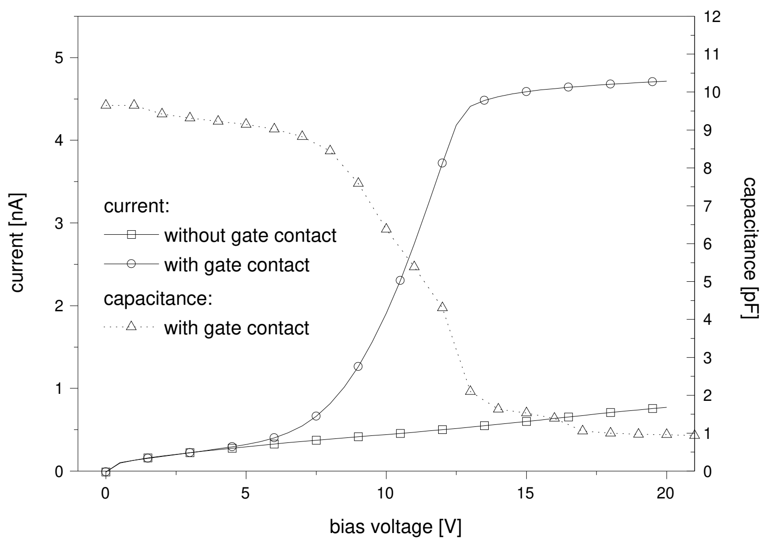


Figure 8.15: *Enlarged view of the low voltage region of fig. 8.14(a), measured on the wide gap pixel before and after adding the artificial gate contact. A high-frequency C-V curve measured on the same pixel cell after adding the gate contact is depicted for a visualisation of the correlation between current step at 7 V and the flat-band voltage [WUE99].*

Concerning the exponential current increase observed for all designs after irradiation, it is not possible to calculate the electric field distributions close to the accumulation layer and thus predict the current. Instead, an empirical parametrisation gained from the measured I-V curves was evaluated. When plotting the current-voltage characteristics on a half-logarithmic scale, as is done in fig. 8.16, the results are linear and thus motivate the previously introduced assumption of an exponential dependence,

$$I(V_{\text{bias}}) = b \cdot \exp(a \cdot V_{\text{bias}}), \tag{8.3}$$

with a and b being fit parameters, both depending on the gap width and the dose. Finally, a fit results in the following parametrisations for a and b,

$$\begin{aligned} a &= (3.7 \cdot 10^{-7} \cdot D \cdot d_{\text{gap}} + 4.1 \cdot 10^{-5} \cdot d_{\text{gap}} + 3.0 \cdot 10^{-3})\ \text{V}^{-1} && (8.4) \\ b &= (4.3 \cdot 10^{-4} \cdot D + 2.8 \cdot 10^{-2}) \cdot d_{\text{gap}}^{0.54}\ \text{nA}, && (8.5) \end{aligned}$$

where D denotes the ionising dose in kGy and d_{gap} the gap distance measured in μm.

Interpixel capacitance

Fig. 8.17(a) shows the interpixel capacitance measured to two neighbours as a function of the ionising dose. The interpixel capacitances show a pronounced increase for pixels

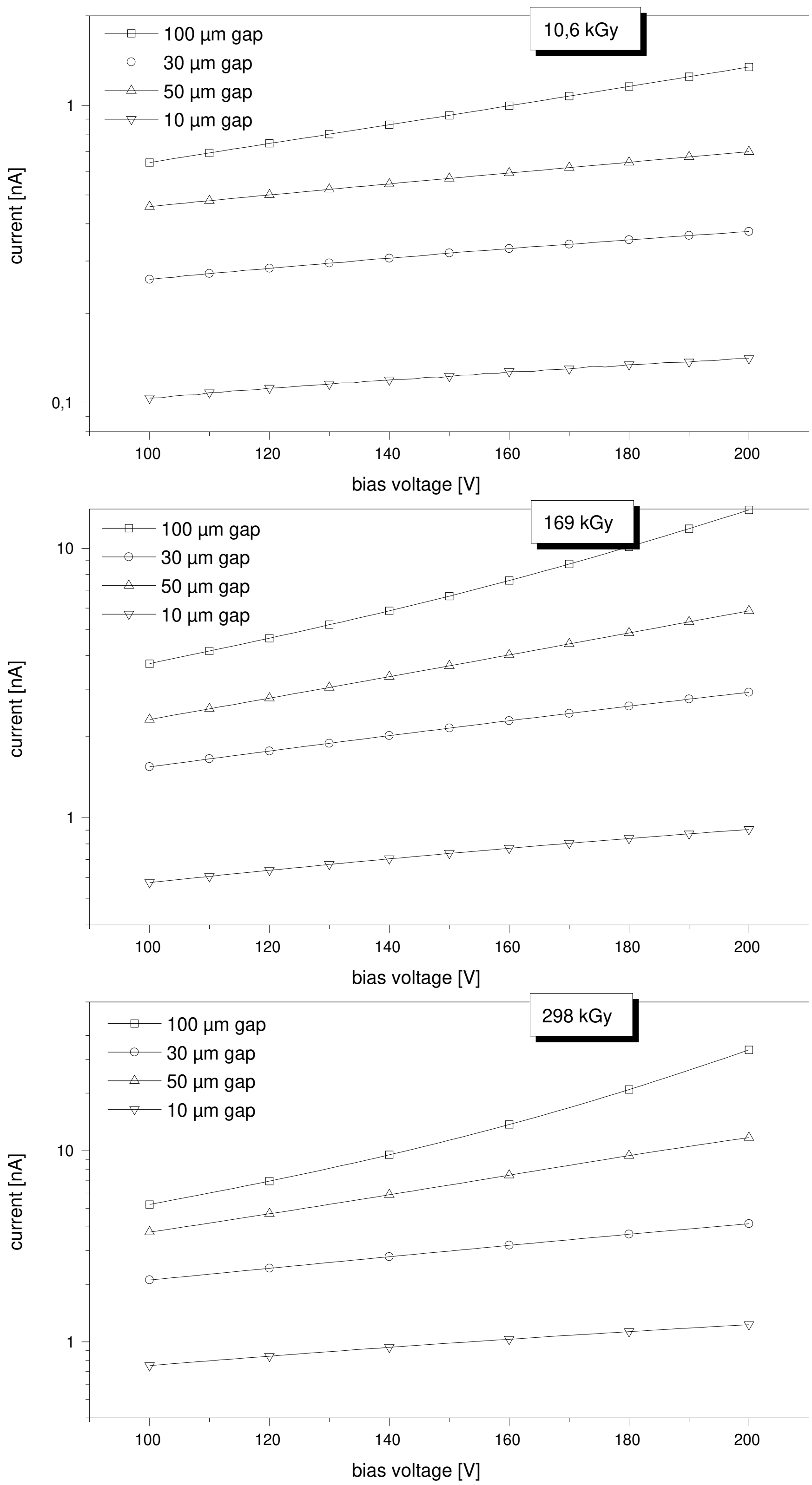
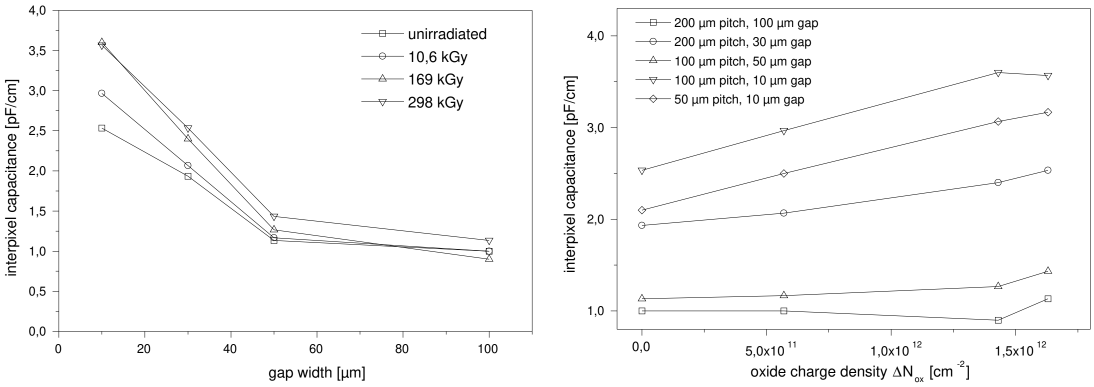


Figure 8.16: Halflogarithmic representation of all pixel current characteristics in the interval of 100 V to 200 V after different dose levels.



(a) Interpixel capacitance vs. dose.   (b) Interpixel capacitance vs. N_{ox}.

Figure 8.17: *The development of the interpixel capacitance as a function of the gap width and the ionising dose.*

with small gap design after surface damage. In case of the 10 μm gap pixel an increase of 60 percent between unirradiated and 300 kGy was measured. On the other hand the capacitative coupling of pixel cells with wider gaps did not change significantly with dose, for the 100 μm gap option no radiation induced alteration could be observed.

The development of the interpixel capacitance after surface damage is explainable by electron accumulation, too. In case of a small gap a stable accumulation layer builds up which then is responsible for the growing coupling capacitance, whereas wide gap cells are almost unaffected by this after waiting long enough, which is generally recommended for interpixel capacitance measurements [WUE97]. For the value determined in this work a waiting time of 3 hours was necessary.

The measured capacitances for 170 kGy and 300 kGy do not differ very much, this may be due to an occuring saturation of oxide charge density as was observed on the monitor MOS capacitor already. In fig. 8.17(b) the interpixel capacitances are plotted as a function of the oxide charge density. Using this data, a parametrisation of the capacitance increase depending on the gap distance and the oxide charge density is obtained,

$$C_{\rm ip} = (-1.7\cdot10^{-14}\cdot\Delta N_{\rm ox}\cdot d_{\rm gap}+8.5\cdot10^{-13}\cdot\Delta N_{\rm ox}-2.8\cdot10^{-2}\cdot d_{\rm gap}+2.7)\ {\rm pF/cm}, \quad (8.6)$$

applicable for a gap distance of typically 50 μm or less. Equation 8.6 is valid for sensors with nitride passivation or after long waiting times, i.e. when the potential on the surface has adjusted.

8.3 n-in-n sensors

8.3.1 p-spray isolation

Interpixel isolation in sensors employing p-spray is maintained as long as holes are accumulated at the silicon surface in the p-spray region. A radiation induced increase of positive oxide charges in the silicon oxide leads to a reduction of hole concentration in the accumulation layer. Depending on the p-spray doping concentration ionisation induced oxide charges may lead to a depletion of holes from the surface and a subsequent inversion layer build-up, consisting of electrons. The inversion layer forms a conducting channel and causes an electrical short-cut between neighbour pixel cells. Therefore, when inversion is established in the p-spray, the interpixel isolation is lost. From these arguments the requirement follows that the surface doping concentration of the p-spray layer must be high enough to withstand the maximum expected oxide charge density without reaching inversion. On the other hand, high p-spray concentration result in high electric fields at the edges of the n-type pixel implantations because of the high charge concentration gradient.

Main problem for the determination of the inversion point is that neither the doping concentration of the p-spray nor the according depth profile are known, because for processing only the dose for the p-implantation is specified. Thus, the doping concentration and the depth profile can only experimentally be determined e.g. using MOS capacitors and MOSFETs.

For this purposes MOSFETs and MOS capacitors have been included as monitor devices in the n-side ATLAS Pixel Wafer layouts. As they are being processed on the n-side of the wafer, the p-spray underneath their gates is the same as used for pixel isolation. Fig. 8.18 shows a schematic cross-section of the p-spray MOS capacitor and the according p-spray MOSFET. The MOS capacitor is surrounded by an additional

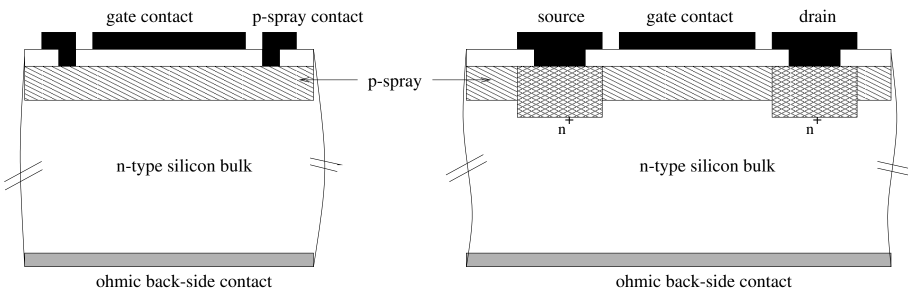
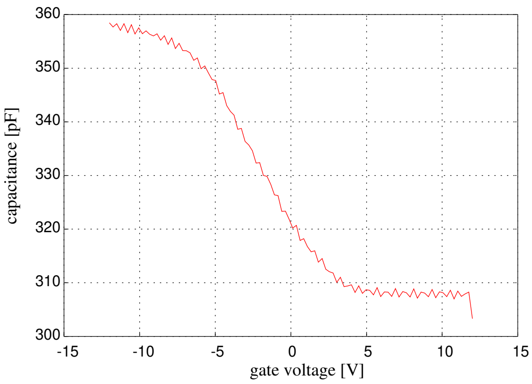
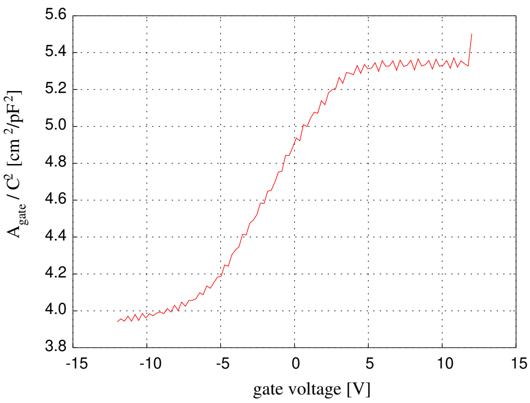


Figure 8.18: *Schematic cross-section of a MOS capacitor (left) and a MOSFET (right) with a p-spray isolation layer under their gate region. Both devices provide experimental access to crucial p-spray parameters and are part of the ATLAS Pixel Sensor wafer layout.*

metal ring which provides electrical contact to the p-spray layer through an opening in the oxide. This contact can be used to adjust p-spray potential which would not be possible using the ohmic back-side contact due to the pn-junction created by the n-bulk and the p-spray layer. The MOSFET has a p-spray layer under its gate and therefore allows to investigate the performance of the isolation layer as a function of gate potential. The current flowing from source to drain at a constant voltage difference can be measured as a function of gate potential, very similar to an interpixel current measurement.



(a) C versus V_{gate}.



(b) $1/C^2$ versus V_{gate}.

Figure 8.19: Capacitance characteristic of a p-spray MOS capacitor used for evaluating the surface doping profile of the p-spray..

Fig. 8.19 shows the high-frequency capacitance characteristic of a p-spray MOS capacitor. First of all, it is noticeable that inversion occurs for positive gate bias voltages, whereas accumulation is established for negative gate voltages. This behaviour is typical for p-type MOS devices and demonstrates that really the p-spray layer is measured instead of the n-type bulk. The low gradient of the curve in the transition range from accumulation to inversion indicates already a high doping concentration in the order of $10^{16}\mathrm{cm}^{-3}$ or more.

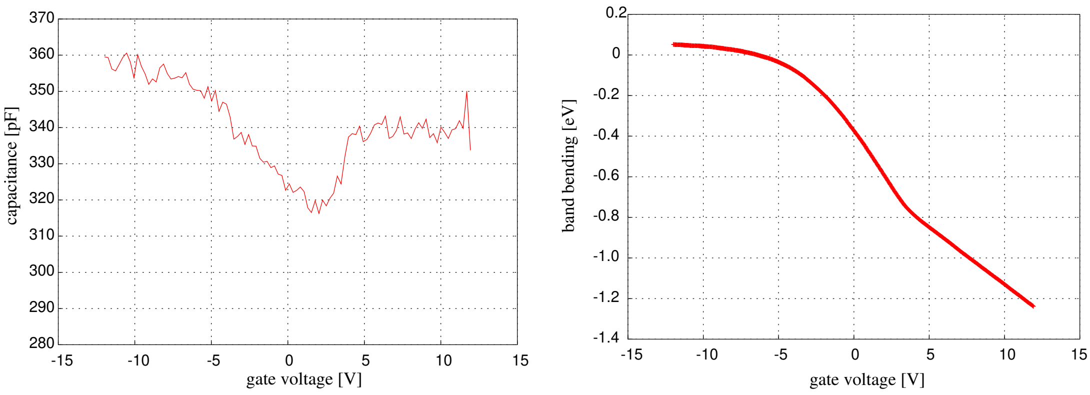
In section 5.2.5 a method for an experimental determination of the surface doping profile and the doping concentration from a high-frequency C-V characteristic of a MOS capacitor was introduced. Fig. 8.19(b) shows the high-frequency C-V curve of the p-spray MOS capacitor in the representation of $1/C^2$ plotted against the gate bias voltage. The linear dependence between 0 V and -5 V indicates a constant doping concentration across the depth of the surface depletion zone. Using equation 5.81 a doping concentration of

$$N_{\mathrm{A}} = 8.6 \cdot 10^{16}\mathrm{cm}^{-3} \tag{8.7}$$

is obtained. The corresponding energy gap between intrinsic and Fermi-level then is

$$\phi_{\mathrm{B}} = 0.41 \text{ eV}. \tag{8.8}$$

The correlation of gate voltage and surface band bending was calculated from a quasi-static current-voltage characteristic, which is depicted in fig. 8.20. Looking at



(a) C versus V$_{gate}$.

(b) ψ_s versus V$_{gate}$.

Figure 8.20: Quasi-static capacitance curve of a MOS capacitor with standard p-spray in the gate region and the extracted correlation of band-bending and applied gate-bias voltage. The linear decrease for voltages above 5 V is an artefact due to the deep depletion effect.

fig. 8.20(a) it is remarkable that the inversion capacitance level remains significantly below the oxide capacitance observed in accumulation. A possible explanation for this unexpected behaviour is that there are not enough minority charge carriers available to generate an inversion layer of a sufficient charge density. This consequently results in deep depletion for charge neutrality conservation reasons and reduces the inversion capacitance.

In fig. 8.20(b) the surface band-bending is plotted versus gate bias. The linear decrease for gate voltages higher than ≈5 V is an artefact due to the low inversion capacitance. Looking up the according gate voltage to ϕ_B of equ. 8.8, weak inversion is reached at 0.4 V gate bias and strong inversion at

$$V(2\phi_{\mathrm{B}}) = 4.6\ \mathrm{V}. \tag{8.9}$$

In addition to the capacitance measurements on the MOS device, the source-drain current as a function of the gate potential was measured at a constant source-drain voltage using the p-spray MOSFET device, represented by the dashed line in fig. 8.21. For a better observation of any correlations between the I-V curve and the C-V measurments, high and low frequency capacitance characteristics of the MOS capacitor have been added in fig. 8.21. Good agreement of the inversion voltage determined by the capacitance analysis and the threshold voltage of the MOSFET is found, showing that the interpixel isolation would break down when strong inversion of the p-spray is reached. Furthermore, the consistency of inversion and threshold voltage could only be

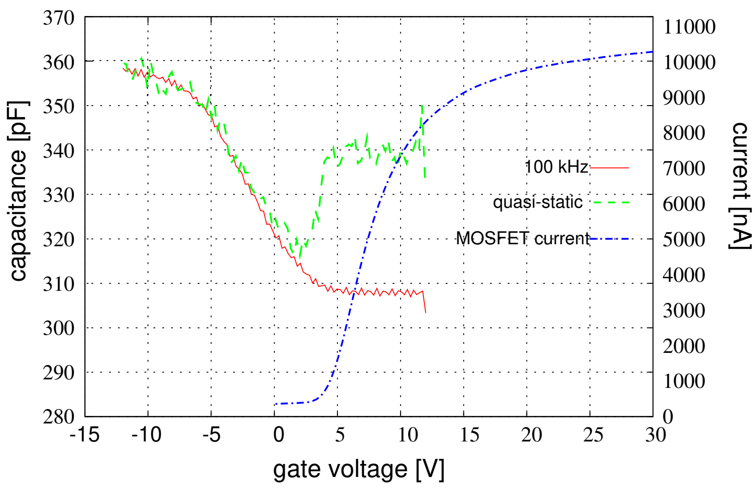


Figure 8.21: Both capacitance curves of a p-spray (high dose) MOS capacitor and the source-drain current of the according p-spray MOSFET. Good agreement between strong inversion and threshold point of the MOSFET can be seen.

achieved for a proper determination of the p-spray doping concentration, confirming the results from the C-V analysis.

Similar to the analysis procedure used for n-type MOS devices, the extrinsic Debye-length and the flat-band capacitance can be calculated,

$$\lambda_{\mathrm{p}} = 13.8 \text{ nm} \tag{8.10}$$

and

$$C(V_{\mathrm{fb}}) = 353 \text{ pF}. \tag{8.11}$$

In fig. 8.19(a) the flat-band voltage is found to be

$$V_{\mathrm{fb}} = -6.5 \text{ V}. \tag{8.12}$$

For an oxide thickness of 240 nm this corresponds to an oxide charge density of

$$N_{\mathrm{ox}} = 5.1 \cdot 10^{11} \text{ cm}^{-2}, \tag{8.13}$$

which is in good agreement with the values determined on p-side MOS devices.

One more important piece of information can be obtained from the high-frequency C-V curve of fig. 8.19(a), namely the maximum depth of the surface depletion zone by extracting the silicon surface capacitance in strong inversion,

$$C_{\mathrm{S}} = \frac{C_{\mathrm{ox}} \cdot C_{\mathrm{ges}}}{C_{\mathrm{ox}} - C_{\mathrm{ges}}} = 2.13 \text{ nF}. \tag{8.14}$$

This capacitance is equivalent to a maximum depletion depth of

$$x_{\mathrm{d}} = \frac{\epsilon_{\mathrm{Si}} \cdot \epsilon_0 \cdot A_{\mathrm{gate}}}{C_{\mathrm{S}}} = 110 \text{ nm}, \tag{8.15}$$

generating a space charge in the depletion region of

$$\rho = N_{\mathrm{A}} \cdot x_{\mathrm{d}} = 9.5 \cdot 10^{11}\ \mathrm{cm}^{-2}. \tag{8.16}$$

ρ is a direct measure for the concentration of oxide charges which can be compensated by surface depletion, namely a charge density of $9.5{\cdot}10^{11}\mathrm{cm}^{-2}$ is tolerable before inversion must occur for further compensation.

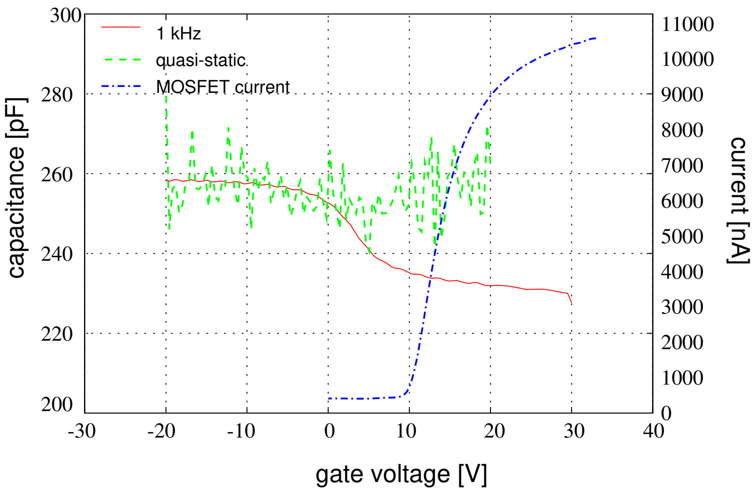


Figure 8.22: Both capacitance curves of a p-spray (low dose) MOS capacitor and the source-drain current of the according p-spray MOSFET. Good agreement between strong inversion and threshold point of the MOSFET can be seen..

The same analysis steps have been applied to devices with moderated, i.e. reduced, p-spray concentration. A surface doping concentration of

$$N_{\mathrm{A}} = 5.3 \cdot 10^{16}\ \mathrm{cm}^{-3} \tag{8.17}$$

was found, which is approximately 40 percent lower than for standard p-spray. Thus, the moderation of the p-spray has occured as specified to around one half of the standard concentration. At maximum surface depletion depth a space charge of

$$\rho = 5.7 \cdot 10^{11}\ \mathrm{cm}^{-2} \tag{8.18}$$

is created, compensating a maximum oxide charge of the same value before inversion is reached. Thus, a lower p-spray doping concentration reduces the compensation capability for positive oxide charges. Fig. 8.22 shows the C-V curves and the source-drain current characterisic for moderated p-spray. Again, a good matching of threshold and inversion voltage was achieved.

Beside positive oxide charge concentration, interface state density is increasing during exposure to ionising radiation, too. Thus, beside the flat-band voltage shift, the

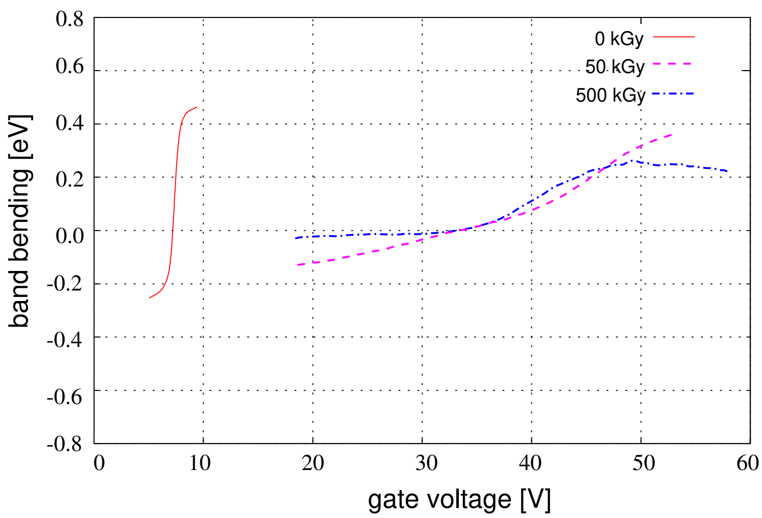


Figure 8.23: Correlation of gate bias and surface band bending before and after irradiation to 50 kGy respectively 500 kGy. With increasing dose levels the curves are stretched out.

correlation of band-bending and gate potential alters, which is a consequence of the charge neutrality requirement in thermal equilibrium. Considering a MOS device without any interface states, a small variation $\delta\mathrm{Q}_{\mathrm{gate}}$ in gate charge must be compensated by a corresponding charge alteration $\delta\mathrm{Q}_{\mathrm{S}}$ at the silicon surface by adjusting the energy bands accordingly. It is required that

$$\delta Q_{\mathrm{gate}} + \delta Q_{\mathrm{S}} = 0. \tag{8.19}$$

In case of non-zero interface state density, additional charges are trapped at the interface. They must be considered too, thus

$$\delta Q_{\mathrm{gate}} + \delta Q_{\mathrm{S}} + \delta Q_{\mathrm{it}} = 0. \tag{8.20}$$

The amount of compensation charges provided by the silicon is less than before surface damage, because of the $\delta\mathrm{Q}_{\mathrm{it}}$ contribution. Therefore, less band-bending is required, and an increase in interface states results in smaller band-bending per gate-voltage step. Using quasi-static measurements on irradiated MOS capacitors, this can qualitatively be verified as depicted in fig. 8.23, showing surface band-bending versus gate voltage for different dose levels.

The above given results and arguments are now successively applied to an unirradiated p-spray MOSFET to quantitatively predict its performance after irradiation. Starting from an unirradiated MOSFET, curve 1 in fig. 8.24 represents its source-drain current characteristic. The threshold voltage of the unirradiated MOSFET is marked by V_{th}. Introducing surface damage to the device, results in a decrease of the flatband voltage which shifts the curve to lower gate bias voltages as is indicated, resulting

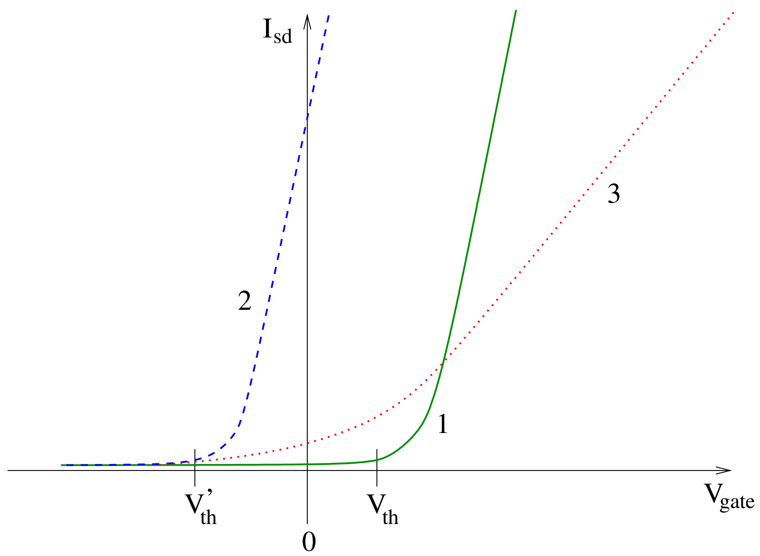
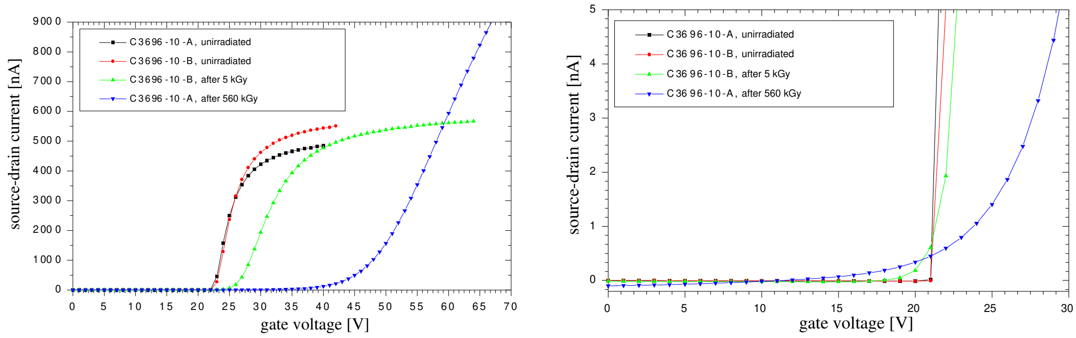


Figure 8.24: *Schematic source-drain current characteristics of a p-spray MOSFET before and after irradiation. Curve (1) represents the characteristic of an unirradiated device (ΔN_{ox}=0, ΔD_{it}=0). (2) is a virtual curve, obtained from (1) by accounting for a radiation induced shift of the flat-band voltage only (ΔN_{ox} >0, ΔD_{it}=0) For curve (3) a radiation induced change of the gate voltage dependence of the band bending is included additionally (ΔN_{ox} >0, ΔD_{it} >0). Curve 3 represents the characteristic expected after irradiation.*

curve 2. Additionally, increase interface states must be considered, too, stretching-out the relation of band-bending and gate voltage. Especially between weak and strong inversion, the charge concentration of the inversion layer grows exponentially with the band-bending according to equ. 5.64. The minority charge carrier concentration is mainly responsible for the channel resistance in the subthreshold mode, thus determining the current flowing from source to drain. After irradiation the altered dependence of band-bending from gate voltage is weakened, resulting in an exponential increase with a lower gradient. Curve 2 is altered by this and becomes equivalent to curve 3, which represents the source-drain current curve of an irradiated MOSFET. The lower gradient of the I-V characteristic in strong inversion is a consequence of an irradiation induced degradation of the charge carrier mobility in the conducting channel.

Source-drain characterstics obtained on a MOSFET with low dose p-spray are shown in fig. 8.25, whereas (b) is a zoomed view of the subthreshold voltage region of (a). Looking at fig 8.25(a) it is noticable that isolation capability seems to be even enhanced for increasing dose levels. Whereas the unirradiated MOSFET apparently is turned on for low gate voltages, much more gate bias must be applied to achieve the same effect after 560 kGy. This behaviour seems to be in contradiction to the expected degradation of interpixel isolation after surface damage. However, it is not, as becomes



(a) Source-drain current.

(b) Source-drain current, zoomed excerpt of subthreshold region.

Figure 8.25: Measured source-drain current voltage characteristics of a p-spray MOS-FET before and after irradiation [WUN01].

clear from fig. 8.25(b), depicting the subthreshold region. Whereas source-drain current is switched on very sharply around 20 V, the exponential shape of the current curves is pronounced more for increasing dose levels, although the gradient gets lower. Additionally, the starting voltage is shifted to lower gate biases. Thus, the measured behaviour is in good agreement with curve 3 of fig. 8.24.

Furthermore, the exponential shape of the source-drain current is depicted in fig. 8.26. The gradient of the curves is decreasing with dose, indeed. Again, this supports that the correlation of gate bias and band bending has changed according to the above discussed mechanism.

Finally, fig. 8.27 shows the interpixel current measured between two adjacent pixels on an ATLAS Pixel sensor, employing p-spray isolation, as a function of the interpixel voltage. The device was exposed to a total dose of 560 kGy, operated at a bias voltage of 150 V during irradiation. Whereas the interpixel resistance is only 170 kΩ without reverse biasing during the measurement, it increases to 7.7 MΩ when applying reverse bias. Two conclusions can be drawn from these results. First, when underdepleted, the interpixel current mainly flows through the undepleted n-type silicon bulk which explains the low resistance. It is impossible to obtain information about the interpixel isolation capability of the p-spray layer in this operating mode. Second, at or above full depletion, the interpixel resistance is increasing strongly because of the high resistance of the depletion region [HUE01]. A lack of isolation properties of the p-spray layer would be easy to detect by a low interpixel resistance. But the obtained value of 7.7 MΩ nicely demonstrates that the isolation is fully operational.

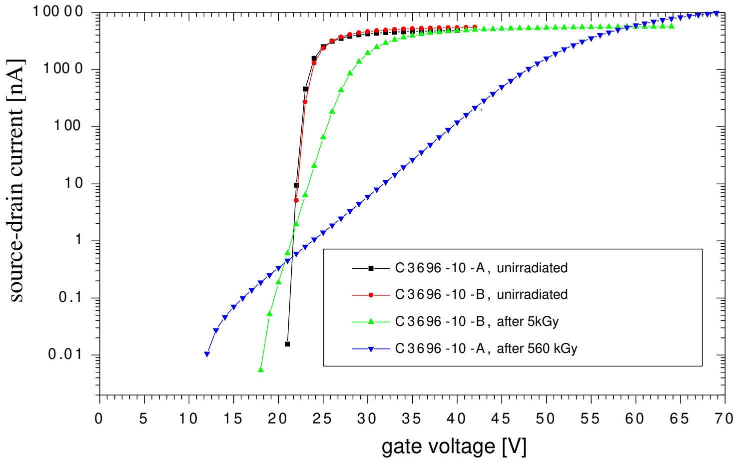


Figure 8.26: Half logarithmic plot of the subthreshold current of a p-spray MOSFET before and after irradiation [WUN01].

8.3.2 p-stop isolation

The presence of positive oxide charges results in the accumulation of electrons at the non-implanted silicon surface as for p-in-n devices. With increasing oxide charge density, the accumulation layer concentration grows accordingly. Fig. 8.28 shows a schematic cross-section of a pixel sensor employing p-stop interpixel isolations, the accumulated electrons are depicted, too. An increasing electron concentration at the surface directly results in peaking electric fields at the border of the p^+-implantations of the p-stop because of the high gradient in charge density. Electric break down is strongly enhanced therefore, reducing noise performance and high voltage stability after irradiation. A comparison of the noise performance of p-spray and p-stop sensors after irradiation with charged hadrons, which cause both bulk and surface damage, shows the unacceptable performance of p-stop isolation. Whereas the noise level of all p-spray sensors is below 300 ENC even for the design fluence of $1{\cdot}10^{15}\mathrm{n_{eq}cm^{-2}}$ and at high voltages, the noise of the p-stop exceeded more than 2600 ENC at 300 V !

The electrical break down mechanism of a p-stop sensor can be emulated using the enhanced gate-controlled diode as described in chapter 6. The reverse current characteristic of the central diode is measured as function of the (constant) gate potential on the innermost gate ring, applied to establish an electron accumulation. The concentration of electrons was adjusted by the gate potential, thus emulating radiation induced growth of accumulation layer charge concentration. The obtained I-V curves [LIC99] are depicted in fig. 8.30, showing the degradation of high voltage stability for growing electron surface concentration. This effect could even be quantitatively studied, which would require the electron concentrations according to the gate biases. Thus, it would be necessary to determine the correlation of gate bias and surface band bending by e.g.

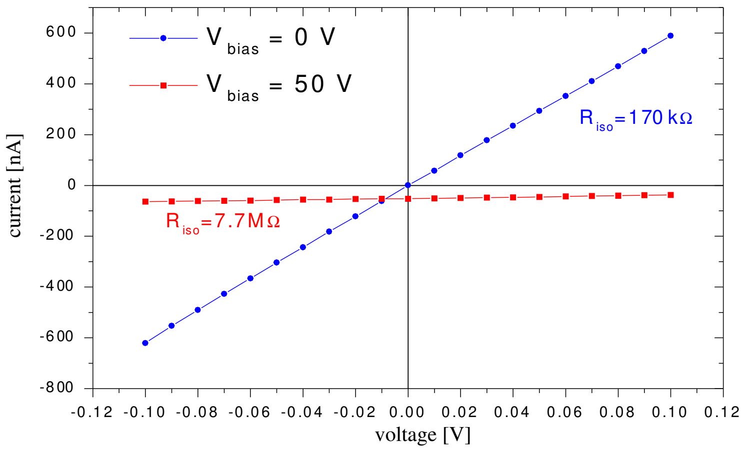


Figure 8.27: Measurement of the interpixel current of an irradiated ATLAS Pixel sensor with moderated p-spray design after 560 kGy. The measurement was performed for 0 V and 50 V reverse bias applied to the sensor while measuring the current flow between two neighbour pixels as a function of the voltage difference applied to them [WUN01].

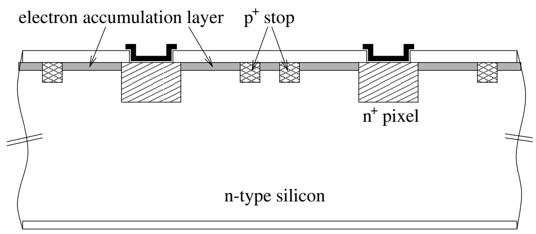


Figure 8.28: Schematic cross-section of an n-in-n pixel sensor with p-stop isolation. Due to the presence of positive oxide charges an electron accumulation layer has established.

evaluating the quasi-static C-V characteristic.

A p-stop sensor design was included in the first prototype wafer of the ATLAS Pixel Sensor but was not operable after high ionisation dose.

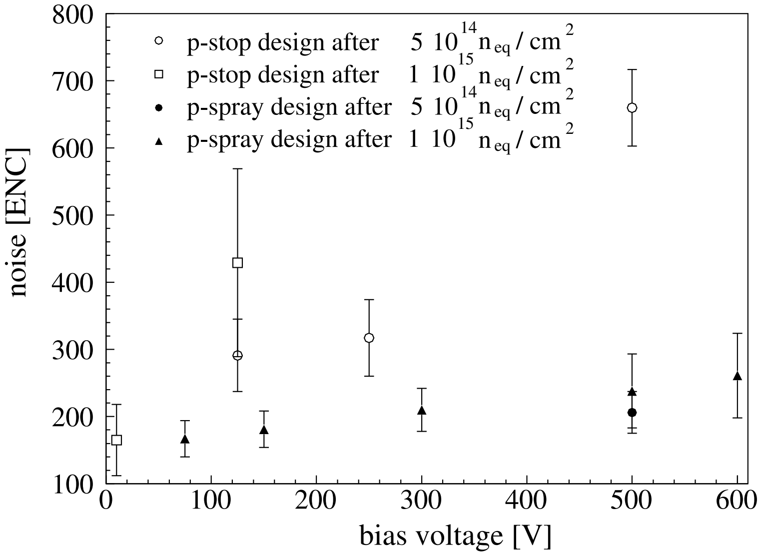


Figure 8.29: Comparison of the noise levels of p-spray and p-stop design after irradiation with charged hadrons as a function of bias voltage [ROH01]. The noise level of the highly irradiated p-stop sensor was above 2600 ENV at 300 V.

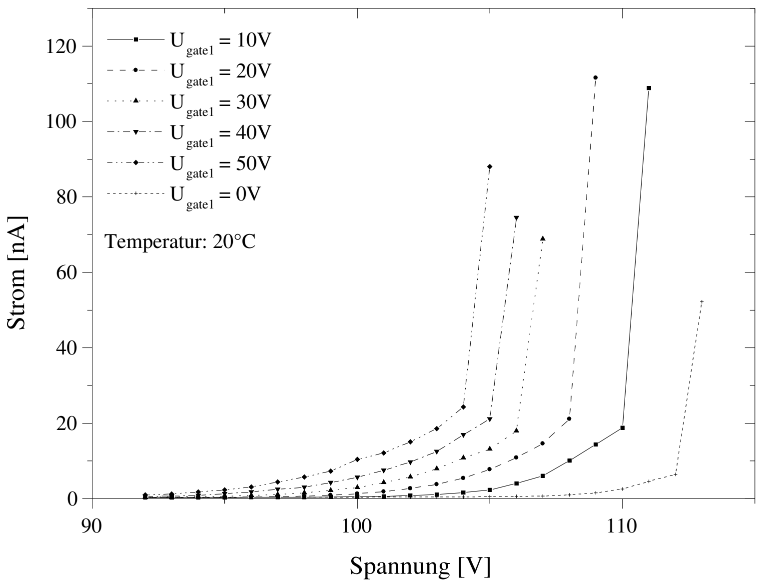


Figure 8.30: *Reverse current of the central diode of a gate-controlled diode as a function of the accumulation potential on the innermost gate ring [LIC99].*

Chapter 9

Discussion

9.1 Saturation of oxide charge density

9.1.1 Electric field

The irradiation tests of materials and processes presented in chapter 7 have all been performed with zero gate bias applied during exposure, i.e. without any electric field in the oxide layer. The evaluation of radiation tolerance was done using the saturation levels of the oxide charge density obtained for a dose (500 kGy) which was one order of magnitude higher than the minimum saturation dose (<50 kGy). An important question which has to be discussed here is if the obtained saturation levels for zero electric field would be altered, i.e. increased, by an electric field during irradiation.

For this discussion additional data from literature have been collected, namely saturation oxide charge densities obtained from similar irradiation experiments, but all obtained for non-zero gate bias voltages during irradiation. The data set used in the following is compiled into tab. 9.1, containing the received ionisation dose, the measured oxide charge density, the ratio of perimeter to gate size, the applied bias voltage and the irradiation temperature. All N_{ox} values have been determined from the flat-

No.	Dose [kGy]	N_{ox} [10^{12}cm^{-2}]	perimeter/gate area	V_{irr} [V]	T [K]	Reference
1	3.3	1.7	*)	-20	293	[WUN92]
2	5.0	4.2	26.6	-55	293	[GRO01]
3	5.0	3.5	*)	-80	293	[WUN96]
4	200	2.9	1.4	-30	273	[LIC99]
5	200	2.0	1.4	-30	293	[LIC99]
6	>50	3.5	1.4	0	293	this work

Table 9.1: *Saturation values for the positive oxide charge density N_{ox} achieved under different biasing conditions. Values not available are denoted by *).*

band voltage using high-frequency C-V curves. All the test samples were processed on n-type silicon, thus the direction of the electric field was identical to the field direction in operated sensors, although the field strength was chosen as a worst case scenario.

Before any conclusions are drawn from the N_{ox} values of tab. 9.1, one must be aware of some systematic effects to be considered which are "hidden" in the data of tab. 9.1. First, for dose levels below the saturation dose the increase of the positive oxide charge density for a certain dose step is much higher when a field is present as for zero field. Thus, the dose when saturation is reached is a function of the applied gate bias, i.e. a higher integrated dose level is required to achieve the saturation level in the no-field case. Second, border effects must be taken into account for samples with a high perimeter-to-size ratio. For example, stray capacitances result in a shift of the capacitance characteristic along the capacitance axis, leading to a higher reading of the flat-band voltage. Third, in case of a non-zero gate bias voltage there is a high gradient in the potential at the border of the gate contact because the surface potential in the surrounding of the gate is around zero. A consequence from this are peaking electric fields at the border region, causing a very non-uniform distribution of surface damage there. Especially for small gate contacts, the measured results are systematically influenced by this.

The influence of the electric field on the saturation level can be analysed taking the oxide charge densities of no. 2, 5 and 6 of tab. 9.1 considering the systematic influences described in the above paragraph. Value no. 2 was the result of an irradiation under -55 V gate bias and determined after an annealing of 3 hours identical to the scenario used in this work. As test-device the MOS array, depicted in fig. 6.8 was employed. Due to the small size of the gate contact the perimeter-to-size ratio is large. Furthermore, each MOS capacitor is surrounded by a common gate contact to keep the silicon surface in accumulation in the neighbourhood. This contact generates an additional stray capacitance as well as a large electric field due to the gradient of the potential, which in this case drops from -55 V down to zero volts over a gap distance of 5 μm (corresponding to an electric field of $1 \cdot 10^5$ V/cm). The N_{ox} value no. 2 of tab. 9.1 of $4.2 \cdot 10^{12} \mathrm{cm}^{-2}$ cannot be corrected for these effects and is thus too high. This explanation is supported by the result no. 3, which was determined for even higher gate bias but for a device with a larger gate area and results an oxide charge density level which is 20 percent lower.

The result no. 5 was obtained for a gate bias of -30 V at room-temperature, using the DEBE facility and a testfield. The MOS capacitor of the testfield has a perimeter-to-area ration of only 1.4. Thus, border effects are much less significant than for the MOS array. The oxide charge density of $2.0 \cdot 10^{12} \mathrm{cm}^{-2}$ was measured after a dose level of 200 kGy and an annealing step of more than 24 hours, reducing the oxide charge concentration compared to the value achieved after 3 hours [GRO01]. Therefore the result no. 5 is significantly lower than after 3 hour annealing.

The dose level of no. 1 was too low to reach the final saturation level at all, even when accounting for enhanced damage generation due to the electric field and thus cannot be used for comparison.

The saturation level which would have been obtained for the scenario used in this work but or an irradiation under non-zero bias must be expected from the above considerations in an interval of $2.0{\cdot}10^{12}\text{cm}^{-2}$ and $4.2{\cdot}10^{12}\text{cm}^{-2}$. Thus, within the interval it is identical to the saturation level of $3.2{\cdot}10^{12}\text{cm}^{-2}$ obtained for zero field. The saturation level of the positive oxide charge density therefore is independent of the electric field applied during irradiation. This was already expected from the microscopic damage mechanisms described in chapter 4.

9.1.2 Dose rate

In section 6.3.2 the influence of the dose rate on the introduced surface damage was discussed. It was shown that damage generation is enhanced for low dose rates. Concerning radiation tolerance tests for the LHC experiments, dose rates suitable for tests in the laboratory must be much higher than the dose rates of the experiments. Therefore, it is necessary to analyse systematic dose rate effects of the test results.

Assuming an operation periode of 100 days per years over a total runtime of 10 years, the dose rate in the ATLAS Pixel Detector is around

$$\dot{D}_{\mathrm{APIX}} = 6 \cdot 10^{-6}\ \mathrm{Gy/s}, \tag{9.1}$$

which is seven orders of magnitude less than the typical dose rates of the DEBE facility,

$$\dot{D}_{\mathrm{DEBE}} = 100\ \mathrm{Gy/s}. \tag{9.2}$$

Generally, according to the discussion of section 6.3.2, space charge effects within the oxide do not play any role in case of the extremely low dose rate in the ATLAS Pixel Detector, but have to be considered for irradiations performed at the DEBE facility. This was tested in [BEL95] for very low dose rates far below the saturation levels.

In this work as well as for ATLAS the saturation values are of major interest. The basic question therefore is, if dose rate effects are still significant for dose levels far above the saturation dose. The maximum dose received by the testfields in the tests of this work was 500 kGy, which is an order of magnitude higher than the saturation dose of less than 50 kGy. Even when assuming that only 10 percent of the generated holes result in surface damage and 90 percent are lost due to the space charge effect, it is still possible to establish the same saturation oxide charge density.

V_{fb} [V]	t_{anneal}	T_{irr} [^{o}C]
33	3 hours	20
15	5 month	20
16	3 hours	85

Table 9.2: *Flat-band voltages determined after different stages of annealing and for different temperature scenarios.*

Therefore the dose rate effect was tested experimentally. For this purpose a testfield was irradiated under exactly identical conditions which were used for the process evaluation except it was heated up to 85^{o}C during irradiation. As described in [BEL95], an elevated device temperature during a high dose rate irradiation leads to similar results than a low dose rate experiment at room-temperature. Comparing the flat-band voltages of tab. 9.2 obtained after 500 kGy for both temperatures, no difference as found when accounting for the temperature dependence of the annealing which is accellerated for higher temperatures [LIC99].

The conclusion from the above is, that the observed saturation levels of the oxide charge density are not dependent on the dose rate.

9.2 Conclusions for sensor design

9.2.1 p-in-n design

The performance of p-in-n sensor designs is significantly influenced by surface effects before and after exposure to ionising radiation. As the most important design parameter in this context the gap width between neighbour implantations was identified, although its role is changed by irradiation. On an unirradiated sensor the surface related interface generation current is proportionally growing with the gap width. Depending on the design and the particular process, it can easily contribute more than 50 percent of the total reverse current, but without affecting high voltage stability. From the linear dependence of the interface generation current contribution on the gap width while keeping all other design parameters constant must be concluded that the whole surface area is depleted without any dead regions. For sensor development in non-radiating environments, surface effects can be reduced by decreasing the gap width, which is possible without changing the pitch of the pixel cells and thus without affecting the spatial resolution. On the other hand, care must be taken of growing interpixel capacitances, which approximately grow with the inverse gap width.

The role of the gap width becomes more complex in sensors which were exposed to ionising radiation. The reverse current of single pixel cells are now fully dominated by surface effects even after dose levels as low as 11 kGy. A large current increase of several orders of magnitude was observed and is mostly caused by electrical break downs occuring near the enclosed electron accumulation layer and, different to before irradiation, is not due to interface generation current. The formation of the electron accumulation layer is both influenced by the gap design and the potential distribution on the sensor surface. Whereas for small gaps it is completely impossible to remove the surface accumulation layer, a uniform potential distribution on the surface between pixel cells allows to fully deplete pixel cells with wide gaps. The criterion if full surface depletion is possible or not can be used to distinguish between wide and small gaps. Although full surface depletion of a pixel cell results in a maximum contribution of radiation increased interface generation current even at low voltages. This may first look like a disadvantage but it is the preferred choice. As characteristic for the interface current, it is voltage independent above the flat-band voltage and therefore remains constant up to high voltages. In case of the enclosed electron accumulation, the reverse current is lower at low bias voltages, but then increases exponentially even before depletion is reached and results in a quickly increasing reverse current, being much higher than in case of full surface depletion. Furthermore, the interpixel capacitance of wide gap designs is nearly unaffected by surface damage, whereas the capacitance of small gap cells is increased.

An additional silicon nitride passivation could help to adjust a uniform potential across the whole sensor surface and stabilise operating conditions. Furthermore, silicon nitrid avoids sensitivity of the sensor performance to environmental conditions like dirt or humidity, which can badly influence long-term stability. Beside enhanced mechanical stability, a silicon nitride layer acts as a gate contact in between the pixel implantations, which leads to a well defined electric field during irradiation. Designs employing a nitride layer can be described by gate boundary conditions in device simulations and thus allow a good comparison between simulated and measured results.

9.2.2 n-in-n design

Radiation tolerance of n-in-n sensors is determined by the design of the interpixel isolation, which can be realised by p-stop implantations, by a homogenous p-spray layer or by moderated p-spray.

Sensors with p-stop design show significant performance degradation after exposure to ionsing radiation due to surface effects. Radiation induced growth of the electron accumulation layer concentration is responsible for high electric fields at the edges of the p-stop implantations. Therefore, high voltage stability is reduced after irradiation as well as unacceptable high noise levels were observed. Sensors employing p-stops show a good performance when unirradiated because of intrinsically low pixel capacitances and good noise performance before irradiation [ROH01]. It is not possible to implement a bias grid into p-stop design which is a major disadvantage for quality assurance tests [HUE01].

The p-spray sensor design has turned out to be radiation tolerant, sufficient interpixel isolation is maintained up to very high dose levels like 500 kGy. The p-spray technique benefits from the radiation induced increase of interface state density, which results in a weaker correlation between gate voltage and silicon surface band bending. Although the critical inversion point is shifted to lower voltages by irradiation, the increase of inversion layer charge concentration with gate bias is lower than before irradiation, keeping up a sufficient interpixel isolation after surface damage. Sensors with p-spray isolation therefore are qualified for high radiation environments. A further advantage is that p-spray isolation can be easiliy implemented into the sensor design because no additional mask is needed, at least for standard p-spray. High voltage stability is even enhanced by irradiation because maxima of the electric fields at the edges of the pixel implantations are reduced. This is a consequence of decreasing hole concentration with increasing oxide charge density [HUE01].

9.3 Process and material considerations

The set of testfields of various process and material combinations evaluated in chapter 7 was carefully chosen, accounting for two important material topics presently under discussion among sensor developers and producers. These are the oxygen diffusion process and the influence of the crystal orientation of the silicon substrate on surface performance.

The diffusion oxygenation process has no significant influence on the surface quality. All obtained parameters are in the same range as those measured for non-diffused material before and after irradiation. The radiation tolerance of the surfaces of the diffused materials is fully qualified for sensor production. Thus, sensors produced of diffusion oxygenated silicon can benefit without any restrictions from the enhancement of bulk radiation tolerance. Due to its overall good performance, the new material is the optimum choice for silicon sensors operated in high radiation environments. For example the ATLAS Pixel sensor wafers are made of oxygen diffused silicon. Using oxygen diffused silicon, the pixel sensors would be operational during the full 10 year runtime of ATLAS. In fact, presently there is no read-out electronics available which would survive ten years.

Concerning the influence of the crystal orientation on surface performance and radiation hardness, <111> and <100> silicon has been evaluated. Neither before nor after irradiation any systematic differences could be identified. There was no indication found for supporting a better performance of surfaces processed on <100> substrates within an interval of $3.5 \cdot 10^{11}\,\mathrm{cm}^{-2}$ before and $1 \cdot 10^{12}\,\mathrm{cm}^{-2}$ oxide charges after irradiation.

It was not the intention of this work to evaluate vendor specific process variations with the goal to generate a "ranking list" of good and less good processes. In fact, the vendors chosen for the tests represent typical processes often found in sensor production. Main goal was to test the developed characterisation methods and procedures using a small set of process and material combinations. Thus, the sensitivity of the applied methods to process variations was checked, forming the groundwork for later quality assurance tests or monitoring of radiation hardness. All tested processes and materials were of the same high quality and are fully qualified for use in sensor production.

9.4 Consequences for quality assurance

Concluding from the analysis performed in chapter 7, the two key parameters for process evaluation and monitoring are the positive oxide charge density and the surface recombination velocity. Both characteristic parameters allow a sufficient monitoring of radiation tolerance of the tested surface, too. It has turned out that additional measurements, like the combined capacitance analysis resulting the interface state density, are not necessary if only monitoring is required. The interface state density can be calculated from S_0, using an average value for the effective capture cross-sections for charge carriers at the interface. Thus, it is not recommended to include the complex and time consuming determination of the interface state density into standard process monitoring and quality assurance procedures. Nevertheless, this method still provides additional information about the uniformity of D_{it} around the midgap level, which might be interesting for other more detailed testing of process parameters. Furthermore, it is possible to derive an experimental correlation between gate bias and silicon surface band bending from the quasi-static capacitance voltage characteristic. This correlation is needed for the understanding of the behaviour of p-spray MOSFETs after irradiation.

Ionisation induced radiation damage can easily be created using low energetic electrons. This is even possible for standard quality assurance procedures. A mimimum irradiation scenario should reach a total dose above at least 50 kGy to evaluate saturation oxide charge density. It has turned out that an irradiation under zero bias leads to identical results concerning saturation values than tests under bias as far as monitor structures with uniform field distributions are concerned. An annealing of at least three hours after irradiation is suggested to avoid systematic errors due to time dependent effects during characterisation.

Irradiation tests performed on sensors are recommended to be performed under biasing conditions which are equivalent to the standard operating modes. This guarantees that the electric field and thus the damage distribution occuring in the application is achieved. It is possible to evaluate and qualify e.g. pixel cell designs with respect to ionisation induced surface damage by this method. A monitoring of the p-spray concentration and its isolation capabilities is prefered to be done on a p-spray MOSFET. For this purpose a measurement of the source-drain current is suitable for fixed source-drain voltage as a function of gate potential. This characterisation should be performed before irradiation to check if the p-spray has been implemented at all and be repeated after irradiation up to the saturation dose for N_{ox}. An independent testing of interpixel isolation can directly be performed on an irradiated sensor by measuring the interpixel current as a function of reverse bias. Additional measurements which evaluate e.g. the p-spray doping concentration or the doping profile are not required for routine quality control procedures, but are a powerful option in case of unidentified problems concerning p-spray.

It is suggested here to implement the testfield and MOSFETs as process monitoring devices into wafer layouts for sensor prototypes as well as for production. Generally, a slightly simplified gate-controlled diode can be used, consisting of two large gate rings, of which the inner one is used for measurements and the outer one to be kept in accumulation. Especially, when comparing different processes and materials, a strictly systematic characterisation procedure is required, guaranteeing an identical treatment of all devices. The procedures presented in the appendix have been optimised for this purpose. The measurement parameters which were included provide full sensitivity to all surface effects relevant for quality assurance and process monitoring.

Up to now, the testfields have been included into numerous mask layouts for sensor productions for various detector systems like the ATLAS Pixel Detector, the CMS Pixel Detector or in the set of test devices of the ROSE collaboration to be produced by different vendors and with different materials.

9.5 Implementation of surface damage in simulations

Static I-V and C-V measurements allow a characterisation of the performance of silicon detectors with respect to e.g capacitance and current, high voltage stability and power consumption. But particular performance aspect, especially after radiation damage, cannot be sufficiently explained only from static measurements. For example, a further investigation of the enclosed electron accumulation layer problem presented in this work, would require deeper insight into e.g. the potential distribution, charge carrier concentrations and the electric field. Here, device simulations are a very helpful tool.

A realistic implementation of surface damage into the simulation requires numerous input parameters. First of all, the design must be precisely included. In the next step it is necessary to calculate the distribution of the electric field in the oxide under operating conditions. According to the obtained results, oxide charge density and surface recombination velocity must be included as a function of the field. This affords experimental damage calibration studies, i.e. an evaluation of N_{ox} and S_0 as a function of the dose, the process and the electric field during irradiation,

$$N_{\mathrm{ox}} = N_{\mathrm{ox}}(\mathrm{dose,\ process,\ electric\ field}) \tag{9.3}$$

and

$$S_0 = S_0(\mathrm{dose,\ process,\ electric\ field}). \tag{9.4}$$

The damage calibration can be obtained using test-fields which are irradiated under different bias voltages and MOS arrays for the same purpose. The first set of different processes which has been evaluated in this work already allows to calibrate for the vendor specific process. For example,

$$N_{\mathrm{ox}}(5\ \mathrm{kGy},\ \mathrm{CiS\ standard\ process},\ 6\cdot10^5\ \mathrm{V/cm}) = 1.7\cdot10^{12}\ \mathrm{cm}^{-2} \tag{9.5}$$

or

$$S_0(50\ \mathrm{kGy},\ \mathrm{IRST\ standard\ process},\ 0\ \mathrm{V/cm}) = 1100\ \mathrm{cm/s}, \tag{9.6}$$

using the data of chapter 7.

The simulation results finally in the potential distribution in the sensor as well as electron and hole concentrations or the electric field. It is possible to identify design dependent weak points or origins of radiation induced performance degradation.

Simulated surface effects can furthermore be experimentally evaluated using e.g. a proton microbeam probe to survey depletion zones or the EBIC[1] method for characterising electric surface fields.

Device simulations including ionisation induced surface damage have already been used for the development of the ATLAS Pixel Sensor [HUE01].

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[1]Electron Beam Induced Current

Chapter 10

Conclusions

The new proton-proton collider called LHC is presently being installed at the European Laboratory for Particle Physics (CERN) in Geneva, Switzerland. The machine will provide two proton beams colliding with a centre-of-mass energy of 14 TeV and will be used by two multipurpose experiments, ATLAS and CMS. These experiments have been designed for searching for the Higgs-bosons, testing of supersymmetric concepts and for other questions of present day particle physics. Data acquisition is foreseen for a total runtime of 10 years. Silicon strip and pixel sensors are utilized in the Inner Detector of the ATLAS Experiment due to their excellent performance, i.e. short signal rise times, very flexible design options. And silicon sensors can be produced in large numbers using commercial processes. Main requirements besides excellent tracking capabilities are fault tolerance, long-term stability and radiation hardness.

Large scale series productions required a systematic and reliable quality controll process. Especially for controlling process quality and radiation tolerance a set of characteristic parameters was needed together with optimised measurement techniques. Therefore, a systematic study of ionising radiation effects on materials like the oxygen diffused silicon or on special aspects of the sensors as e.g. the p-spray interpixel isolation was obligatory, too.

For these studies ionisation induced surface damage was generated in this work using the DEBE facility. The DEBE facility was designed especially for the purpose of controlled introduction of surface damage as part of radiation hardness tests for LHC experiments. The ionisation in the surface was created by a 20 keV electron beam. The selected beam energy was high enough to penetrate the full depth of oxide films but low enough to prevent the generation of defects in the silicon substrate. Dose rates around 100 Gy/s allowed to emulate the full surface damage level expected for the ATLAS Pixel Detector over 10 years in a few hours.

A systematic investigation of surface effects in segmented p-in-n sensors has lead to the following conclusions. Even before irradiation surface effects have to be considered in segmented sensors. It was possible to show that the reverse current of a single pixel cell is determined by both volume generation current and surface generation current. A systematic analysis of this behaviour showed that the interface current increases proportionally with the gap size between the pixel implantations. Thus, the gap is one of the relevant design parameters to be accounted for. After exposure to ionising radiation the pixel current was fully dominated by an exponentially growing current due to electrical break downs occuring at the surface due to the enclosure of accumulated electrons. It was possible for the first time to study the alteration of the current-voltage characteristics of the pixel cells after adjusting gate potential boundary conditions to the sensor surface by adding an artificial gate contact. For small gap widths, i.e. in the order of 10 μm, the electrical break down was still there under gate boundary conditions whereas it could be avoided in large gap pixel cells, i.e. around 100 μm, indicating that a full depletion of the silicon surface was achieved by removing the enclosed electrons. In practice, the same effect is obtained when implementing a silicon nitride passivation on the sensor surface. Generally, the criterion for the occurance of electron accumulation enclosure is whether the flat-band voltage in the gap region is reached before the depletion zones of neighbouring pixel cells connect or not. In the first case electron enclosure is the consequence, in the second a full surface depletion is possible without any dead regions.

For n-in-n sensors employing a p-spray interpixel isolation the enclosure of accumulated electrons cannot occur. In fact it was commonly assumed that the p-spray isolation employed in n-in-n sensors, like the ATLAS Pixel Sensor, could be lost due to high oxide charge densities after exposure to ionising radiation. The effects which might lead to an isolation break down were investigated for the first time in this work. Using p-spray MOSFETs and p-spray MOS capacitors it was shown that the interpixel isolation would be lost in case of a radiation induced inversion of the p-spray layer due to oxide charges. But at the same time the correlation of gate potential and band bending at the silicon surface was altered by radiation generated interface states in a way that the channel resistance between source and drain increases only very slowly. Thus, transfered to the p-spray isolation between two pixels, it was possible to conclude that a break down of the interpixel isolation cannot occur because of basic physical principles. This was verified by interpixel resistance measurements performed on ATLAS Pixel Sensors at dose levels even above 500 kGy and for irradiations under bias. These *worst case* tests showed that the interpixel p-spray isolation was still in operation. The overall conclusion is that p-spray sensors are *radiation hard* with respect to surface damage due to basic principles of semiconductor physics.

A systematic and comparative evaluation of surface effects of different silicon materials and processes has lead to the following conclusions about the saturation levels of the positive oxide charge density and the surface recombination velocity

Concerning the saturation level of the oxide charge density, a maximum value of $4{\cdot}10^{12}\text{cm}^{-2}$ measured immediately after irradiation was found which decayed after 3 hours room-temperature annealing down to $3{\cdot}10^{12}\text{cm}^{-2}$, but even further decreasing with time. This maximum value was valid for all tested processes and silicon materials. Furthermore, the total saturation level was independent of the electric field during irradiation. But it must be always kept in mind that for lower dose levels the increase of oxide charge density per dose step is much higher when an electric field is present due to an enhanced separation efficiency of electron-hole pairs. As a consequence from this, the saturation level of N_{ox} was reached for a lower dose level in case of irradiation under non-zero bias than under zero bias. Additionally, it was experimentally evaluated that the saturation level of the positive oxide charge density is independent of the dose rate. This enabled to perform irradiation tests in the laboratory with high dose rates compared to the dose rate in the ATLAS Pixel Detector, which will be eight orders of magnitude lower. The final damage levels are not altered by the different dose rates. Even in the case that radiation damage would be higher for low dose rate, i.e. in the ATLAS experiment, the much longer annealing time of 265 days per year occuring in ATLAS would overcompensate any dose rate effects. In fact, for this reason the high rate experiments done at the DEBE facility were worst case. Thus, this allowed an unrestricted use of e.g. the DEBE facility for radiation tolerance tests.

For the surface recombination velocity a starting saturation could be observed even at lower dose levels, but the saturation level was not reached at 500 kGy. This was in agreement with literature data [NIC82] obtained on silicon material utilized for electronic devices. Although a wide spreading of the recombination velocities measured at 500 kGy was observed, no systematic correlation to individual process parameters could be identified.

The evaluation of the saturation levels of the oxide charge density of different processes lead to the following results. The surface performance of <111> and <100> silicon substrates were identical before and after irradiation within an interval of $3.5 \cdot 10^{11} cm^{-2}$ before and $1 \cdot 10^{12} cm^{-2}$ oxide charges after irradiation. Thus, there was no indication found that one of these orientations should be preferred for silicon sensor processing. Another important result was that the additional oxygen diffusion step which introduces oxygen atoms into the silicon bulk to improve radiation tolerance against displacement damage, did not affect surface properties, regardless of the diffusion time in the evaluated range of 16 hours up to 72 hours. Thus, the oxygen diffused processes were fully qualified for the production of radiation tolerant silicon sensors. This has significant consequences for the production of *radiation hard* sensors. When combining the oxygen diffused silicon with the intrinsic radiation hard p-spray sensor design, overall radiation hardness is achieved against surface and displacement damage. This concept is now followed for the ATLAS Pixel Sensors.

Concerning device simulations, a proper implementation of surface damage effects is now possible. The required parameters were obtained using the tools presented in this thesis, i.e. the characterisation procedures and methods. In particular, the surface recombination velocity and the positive oxide charge density were evaluated as a function of the ionisation dose, the electric field and of the silicon material and process. It was demonstrated on an example how this implementation is achievable.

The characterisation procedures and measurement techniques of this work have been proven to be fully applicable to quality controll routines and monitoring of radiation hardness. They are the basis for a systematic process monitoring and surface quality evaluation. The presented test devices are needed as monitor devices for surface properties and have to be implemented into wafer mask layouts which was done for the

ATLAS Pixel Sensor wafers in consequence.

The surface recombination velocity S_0 and the positive oxide charge density N_{ox} were identified as the crucial parameters for the evaluation of surface quality and radiation hardness. The oxide charge density was extracted from the flat-band voltage obtained from high frequency capacitance voltage characteristics of a MOS capacitor, measured at an ac signal frequency of 100 kHz. The surface recombination velocity was determined from the interface generation current which was accessible from a gate-controlled diode. Both monitor devices were included in the testfield, which provided easy access to all relevant surface parameters before and after irradiation. As far as radiation hardness tests of the p-spray interpixel isolation in n-in-n sensors were concerned, p-spray MOSFETs and MOS capacitors on p-spray were very useful tools, providing direct access to the p-spray doping concentration, the surface doping profile and the threshold voltage. For further insight into the surface properties an additional quasi-static C-V measurement performed on MOS capacitors was required. In particular, the correlation of applied gate bias and surface band bending was obtained from it. This knowledge was crucial for the understanding of source-drain current curves determined on irradiated p-spray MOSFETs.

As far as "simple" monitor devices like MOS capacitors were concerned, it was completely sufficient to perform irradiation tests under zero gate bias conditions. For radiation hardness tests of sensor designs, an irradiation under operating conditions was still obligatory because of the non uniform damage distribution. Employing mini sensors as monitor devices is generally completely sufficient as long as their design is identical to their full size counterparts.

In this work a complete set of characterisation methods, parameters and procedures was developed and thoroughly tested. It provides all the tools needed for surface quality control and the evaluation of all relevant surface parameters. Concerning segmented sensors, p-spray based n-in-n silicon sensors processed on oxygen diffused material provide overall radiation hardness.

Appendix A

Frequency dependence after irradiation

In the ideal case high frequency measurements are done at a frequency above 1 GHz to avoid interface trap response. For example a systematic error will be introduced to the interface state density determined from the combined C-V analysis in case of a high frequency C-V curve still including an additional interface trap capacitance. In addition to this, stretch-out leads to a wrong reading of the flat-band voltage from the capacitance characteristic. On the other hand, it is practically impossible to use measurement frequencies above 1 MHz, in fact in many cases 100 kHz is the upper limit, e.g. in case of high resistivity silicon substrates. For this reason it is necessary to evaluate the frequency dependence of the capacitance on either unirradiated and irradiated MOS devices to find an optimum measurement frequency.

As a starting point, C-V characteristics of an unirradiated MOS capacitor have been measured as a function of the ac-signal frequency, ranging from 1 MHz down to quasi-static conditions. The curves are depicted in fig. A.1. The characteristics below 1 MHz look almost identical. From this observation a first conclusion concerning stretch-out can be drawn: even at smaller frequencies like 10 kHz or 1 kHz interface trap response does not have significant contribution to the C-V characteristic before irradiation. The 1 MHz characteristic shows a degradation in strong accumulation and near the flat-band voltage. Most probable explanation for the capacitance degradation in strong accumulation is a considerable series resistance, which is mainly caused by the high resistivity silicon substrate ($\rho \approx 2$ kΩcm).

Fig. A.2 shows an enlarged view of the characteristics of fig. A.1 around the flat-band point. The flat-band capacitance is marked by the straight line. In the zoomed view small but systematic deviations between the different curves are recognizable, indicating a frequency dependence of the voltage corresponding to the flat-band capacitance. The basic question here is how big the difference between the true flat-band voltage and the value taken from the curve is.

In fig. A.3 V(C_{fb}) is plotted against the ac signal frequency using a half logarithmic scale. All data points are on a straight line. Thus, the frequency dependence found is

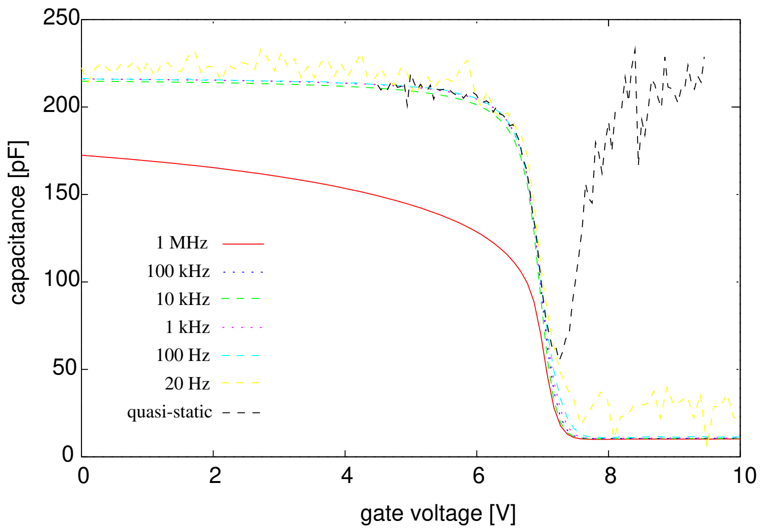

Figure A.1: *C-V characteristics of an unirradiated MOS capacitor. All curves were measured with identical parameters.*

parameterised by

$$V(\omega) = m \cdot \ln \frac{\omega}{\omega_0} + b, \tag{A.1}$$

where m denotes the rise of the curve and b the ordinate. A linear regression results in

$$V(\omega) = -(0.013 \pm 0.001)\ V \cdot \ln \frac{\omega}{\omega_0} + (7.274 \pm 0.647)\ V, \tag{A.2}$$

with ω_0:=1 s^{-1} and ω=2πf.

Using equ. A.2 it is possible to extrapolate to higher frequencies. Comparing for example the value at 100 kHz and 10 MHz results in a voltage difference of ΔV=0.06 V. This difference is in the order of 1 percent of the flat-band voltage and will introduce an error of 1 percent to the oxide charge density, too. Obviously, this error is completely negligible.

In the next step the study of the frequency dependence was extended to irradiated MOS devices, in this particular case exposed to a total dose of 500 kGy.

Fig. A.4 shows the C-V characteristics measured on a MOS capacitor of the same process type as used before irradiation. The curves were taken after 5 month annealing at room-temperature. There are several differences observable compare to the unirradiated device. First, all curves are shifted to higher gate-voltages due the irradiation induced increase of oxide charges. Second, a clear splitting up of the curves around the flat-band point with frequency is found. Due to the increase of interface states, the minimum capacitance of the quasi-static signal has risen significantly, the curve is almost flat.

As above, the voltages according to the flat-band capacitance have been read from the curves and plotted against the frequency, see fig. A.5. Again, a linear dependence

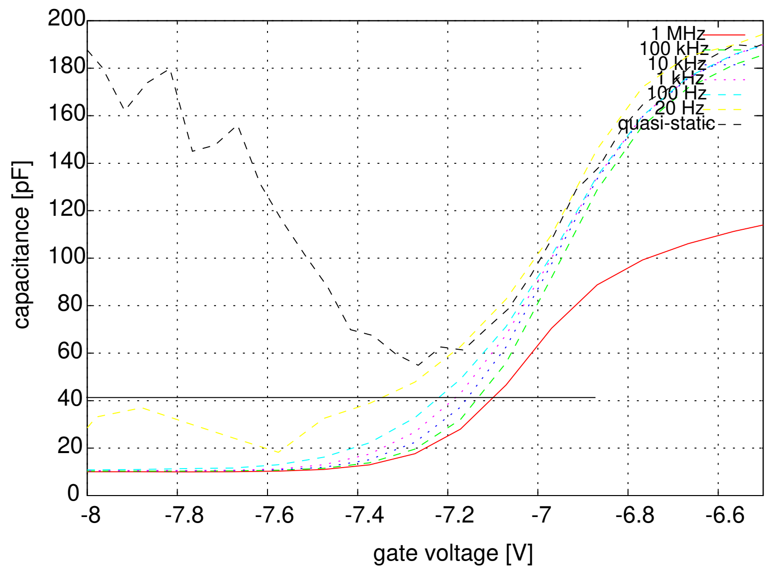

Figure A.2: *Zoomed view of fig. A.1.*

of the same type as in equ. A.1 is resulted. The linear regression leads to

$$V(\omega) = -(0.972 \pm 0.060)\ V \cdot \ln \frac{\omega}{\omega_0} + (26.021 \pm 0.588)\ V. \tag{A.3}$$

Comparing again the voltages at 100 kHz and 10 MHz results in a difference of ΔV=4.7 V. Apparently, when V(ω=100 kHz) is assumed to be the flat-band voltage, an over estimate of 30 percent may be possible, influencing the calculated oxide charge density in the same way.

Equations A.2 and A.3 provide the possibility to roughly estimate the systematic error when the flat-band voltage is read from a C-V curve measured at 100 kHz. The introduced error is negligible before irradiation but must be considered for higher doses.

The same type of frequency dependence was found before and after irradiation. An interesting question arises concerning the physical meaning of the parameters m and b. Apparently both parameters have a strong dose dependence. Beside this, a correltation with individual process prameters must be expected, i.e. m and b become vendor specific. Here, only the physical meaning of the ordinate parameter b is empirically discussed.

The effective substrate doping of the evaluated MOS capacitors was N_{eff}=1.2$\cdot 10^{12}$/cm^3, corresponding to ϕ_B=0.13 eV as energy difference between Fermi level and intrinsic level, i.e.the point when weak inversion is reached. ϕ_B is converted into a gate bias voltage using the plot of fig. A.6. It shows the correlation between gate bias and band bending, determined from the quasi-static capacitance characteristic of the unirradiated MOS capacitor. Flat-band case, weak and strong inversion are marked in fig. A.6, resulting an inversion voltage of V_{inv}=7.27 V. Comparing b and V_{inv}, good agreement

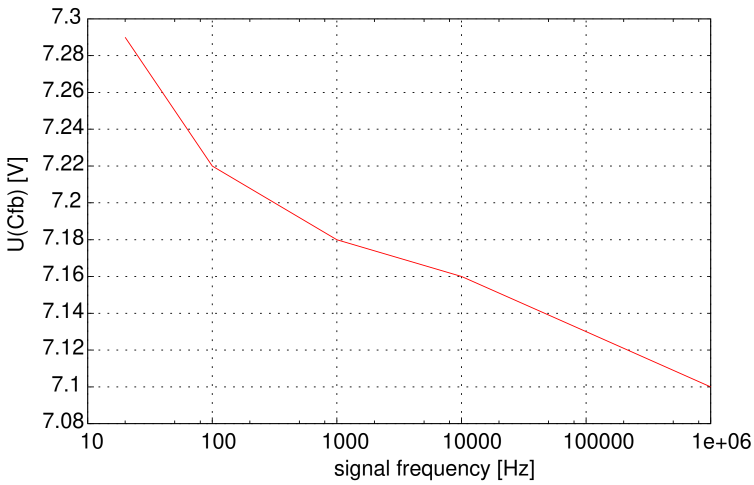

Figure A.3: *Voltage of the flat-band capacitance against frequency, measured on an unirradiated MOS capacitor.*

is found,

$$b = (7.27 \pm 0.65)\ V \tag{A.4}$$

$$V_{inv} = (7.27 \pm 0.10)\ V. \tag{A.5}$$

Therefore, b seems to be identical to the inversion voltage although this still must be proven testing further samples and after irradiation. Nevertheless, equations A.2 and A.3 are useful to correct flat-band voltage measurements done at frequencies of 100 kHz or 10 kHz, at least with a precision sufficient for quality assurance purposes.

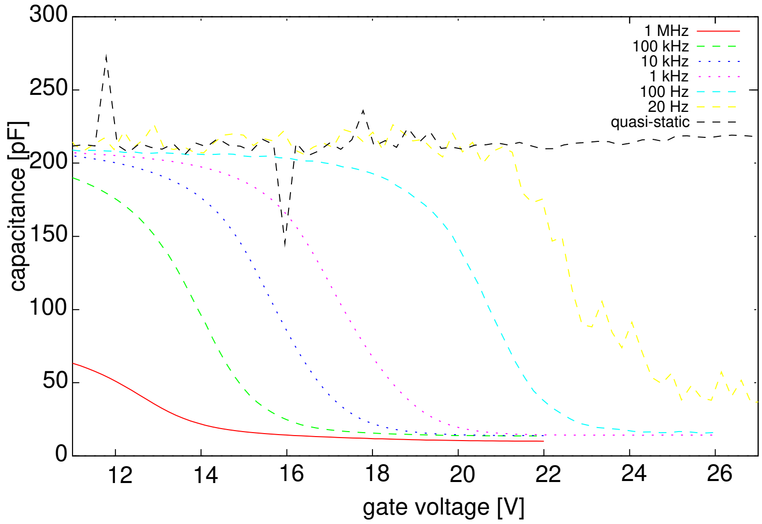

Figure A.4: *C-V characteristics of a MOS capacitor after 500 kGy and 5 month annealing at room-temperature. All curves were measured with identical parameters, especially the voltage ramp was always the same.*

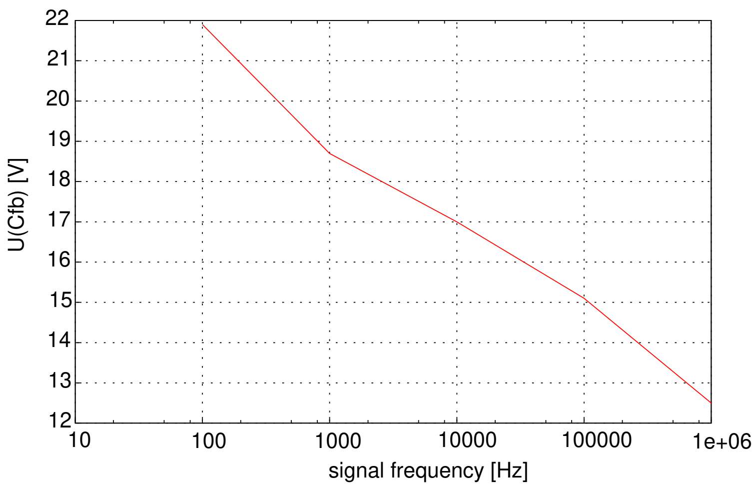

Figure A.5: *Voltage of the flat-band capacitance plotted agains frequency, measured on an irradiated MOS capacitor after 500 kGy dose and 5 month annealing..*

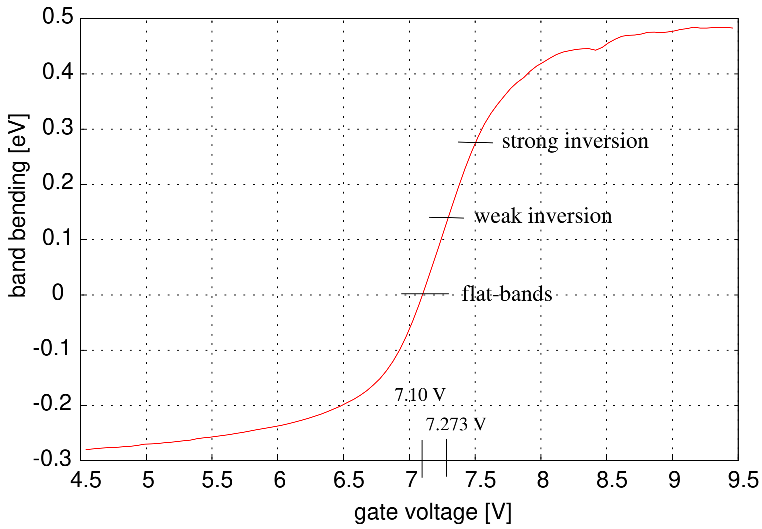

Figure A.6: *Correlation between applied gate bias and band bending. Determined from a quasi-static C-V measurement on an unirradiated MOS capacitor.*

Appendix B

Instructions for systematic test-field characterisation

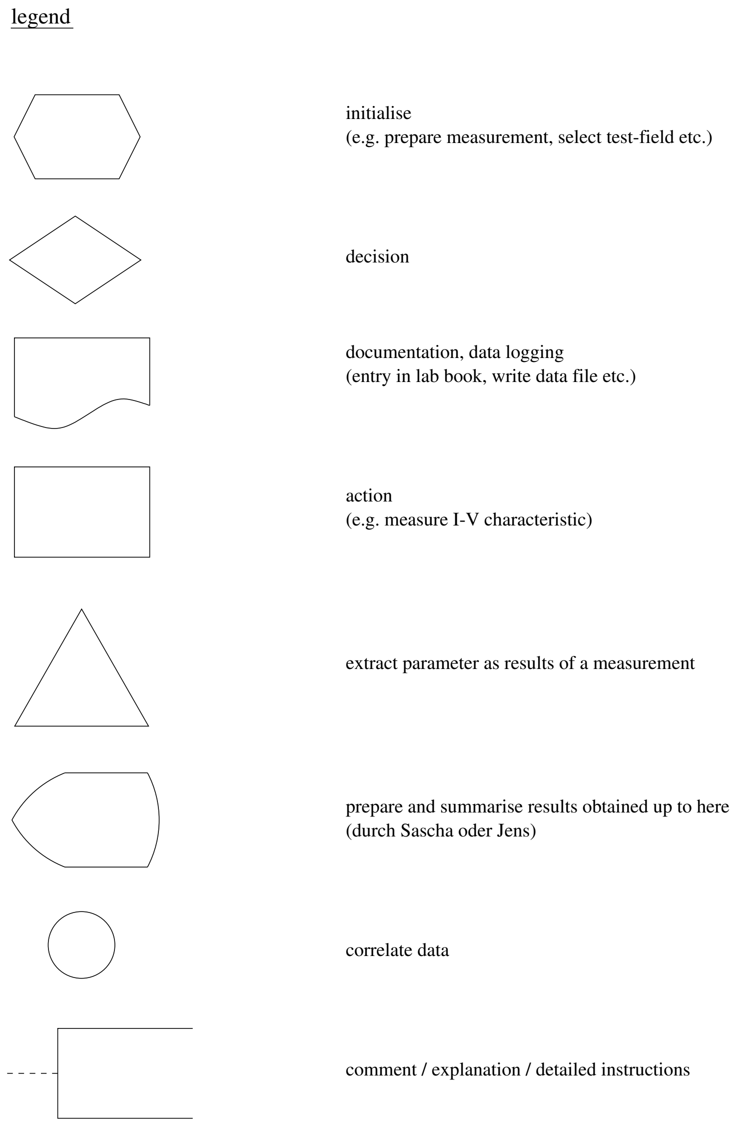

Figure B.1: *Definition of symbols used in the flow-charts.*

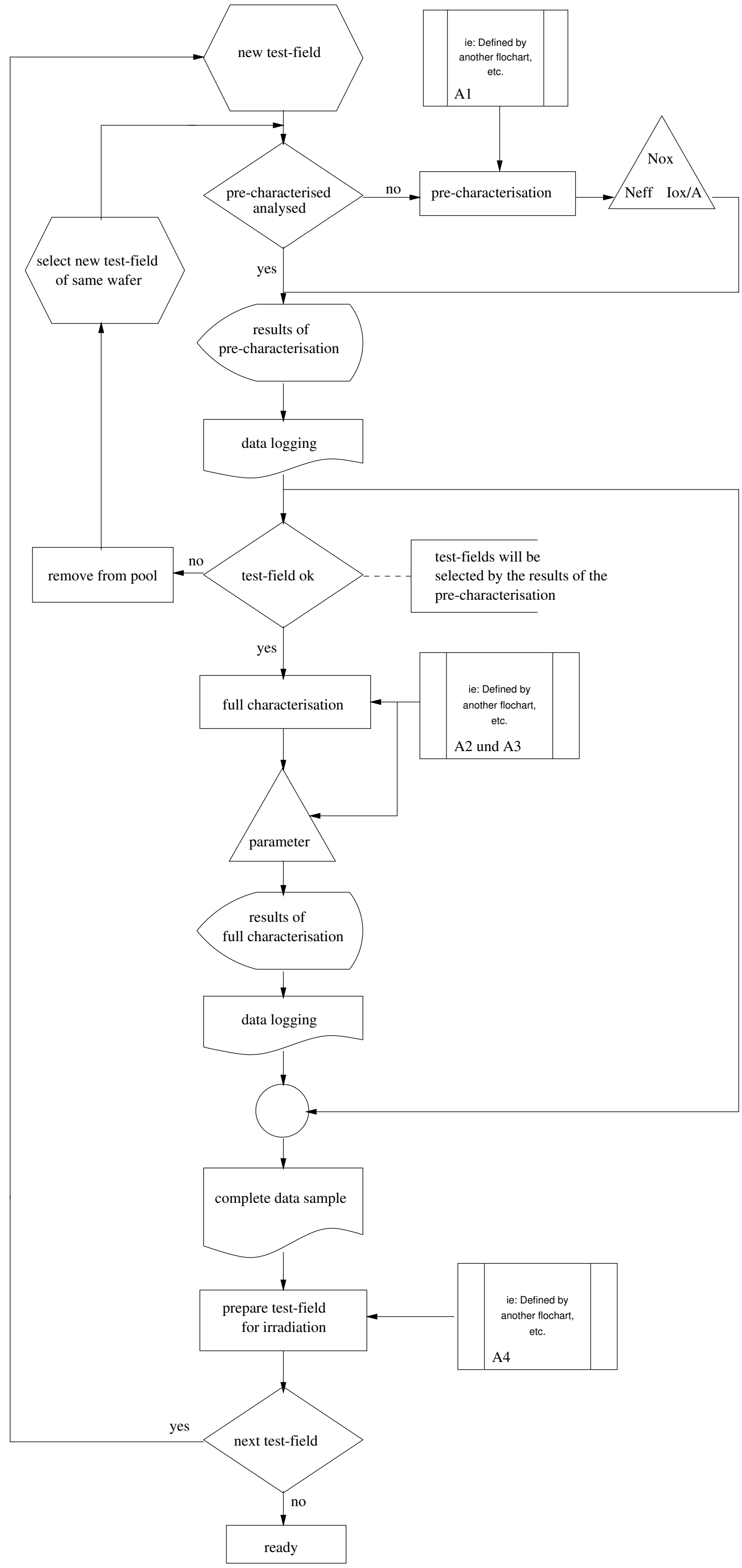

Figure B.2: *Flow-chart for the test-field characterisation.*

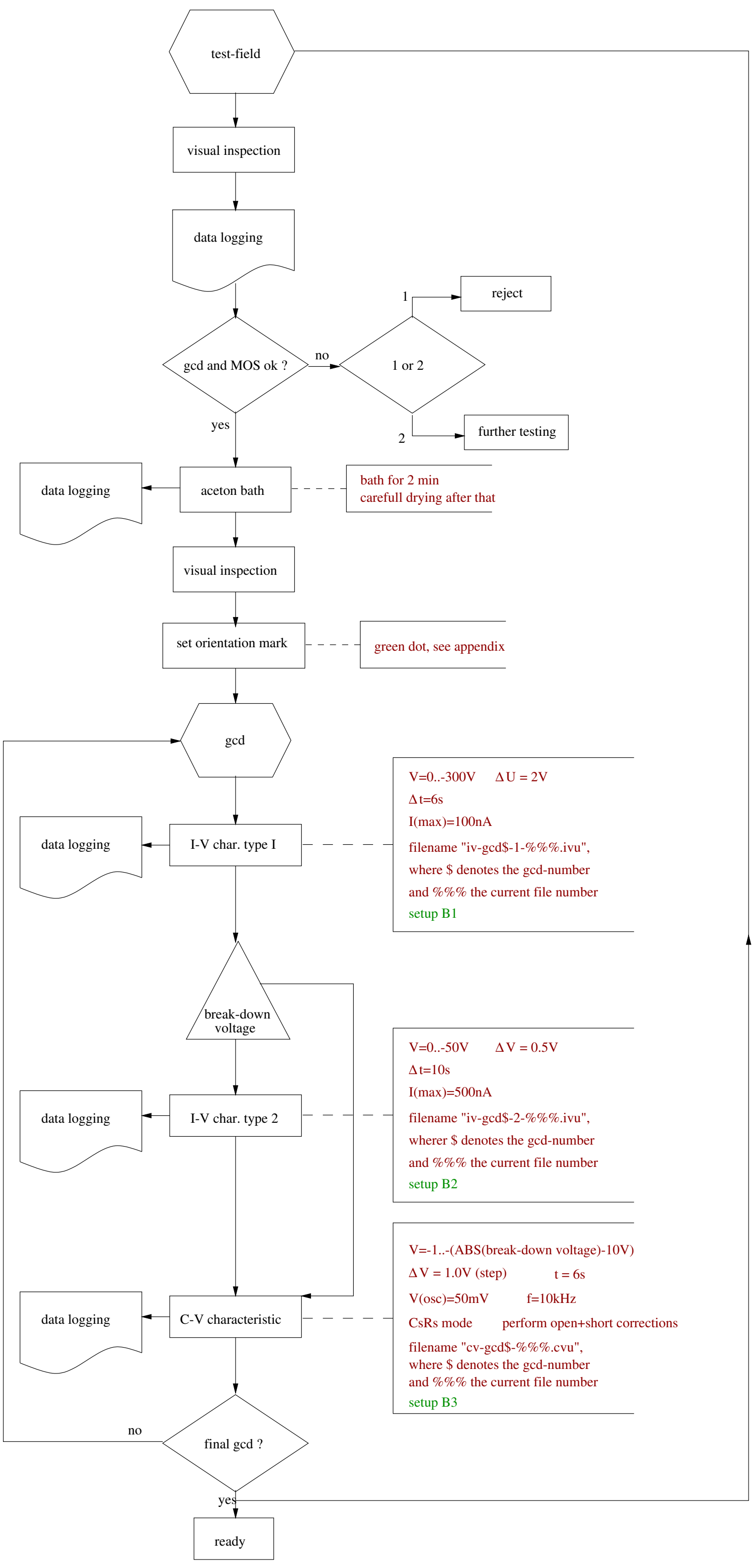

Figure B.3: *Flow-chart for the test-field pre-characterisation.*

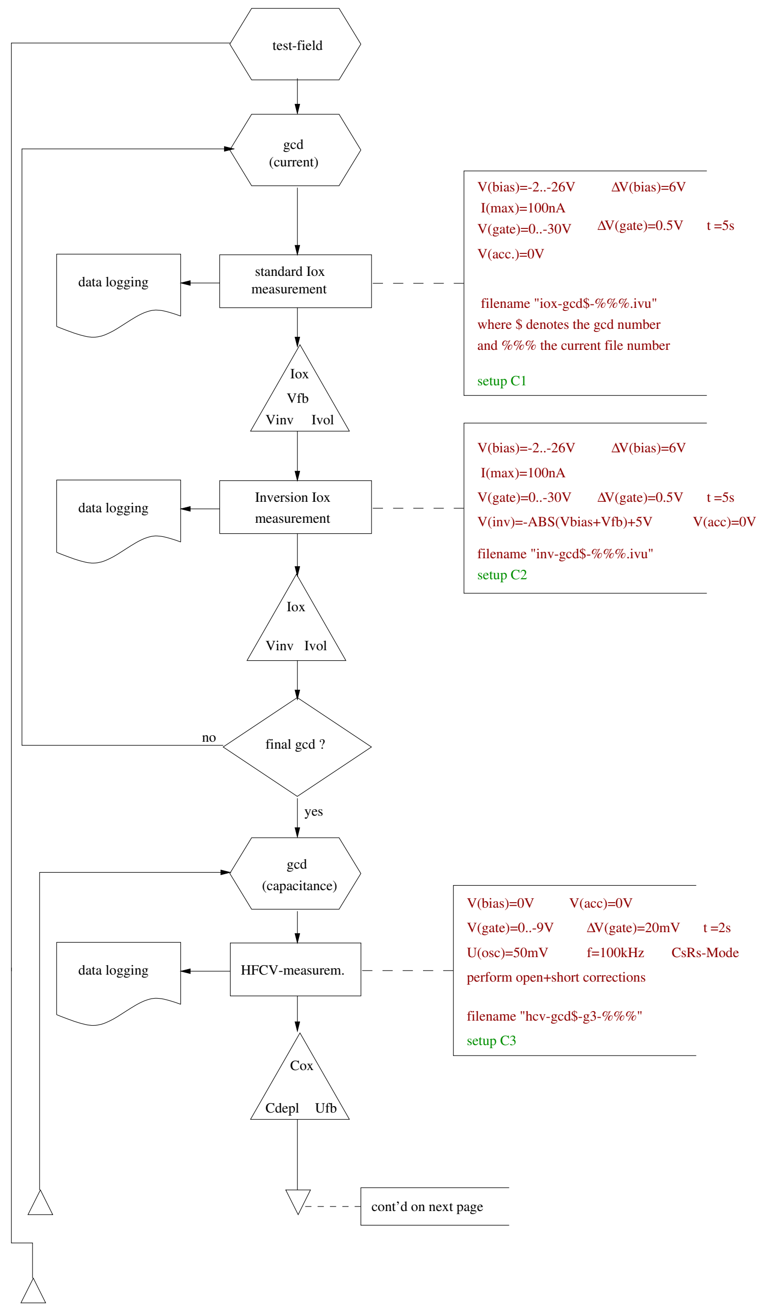

Figure B.4: *Flow-chart for the complete test-field characterisation.*

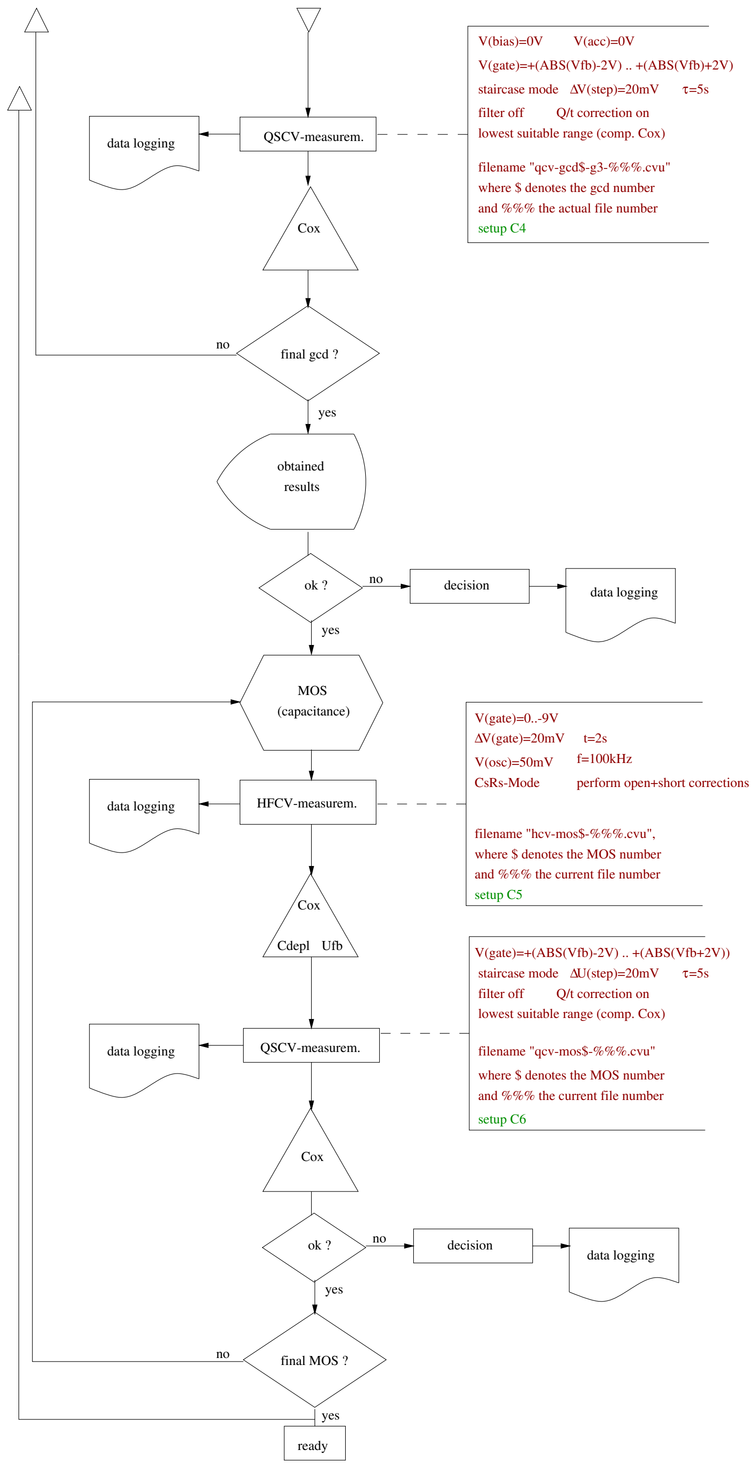

Figure B.5: *Continued flow-chart.*

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