Compensation Method to improve the Accuracy in Low-Dynamic PHIL Simulations of High-Power EV Charging Stations

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Abstract—**Laboratory testing of modern power systems often requires the use of both commercial products and prototypes. However, due to limitations in the availability of components and the need for greater flexibility in testing scenarios, the use of component emulators becomes essential. Among various approaches, the emulation of power system components using Power Hardware-in-the-Loop (PHIL) is widely adopted. Despite their advantages, PHIL setups are inherently complex, and the non-ideal behavior of the looped components necessitates the implementation of dedicated interface approaches and compensation methods. This work highlights the challenges associated with the accuracy of PHIL setups for the emulation of High-Power-Charging systems for Electric Vehicles. Particularly, it addresses the issue of maintaining correct active and reactive power flow between the setpoints provided by the real-time simulation and the output of the power interface at a given Point of Common Coupling. A novel and practical interface compensation method is proposed and successfully implemented to improve the overall accuracy and performance of the setup under various operational conditions. Results demonstrate that the suggested method significantly improves accuracy by reducing steady-state error of the power flow from up to 7.31 % to less than 0.01 % during low-dynamic charging operation.**

Index Terms—**Power hardware-in-the-loop, Electric Vehicles, High-Power-Charging.**

I. Introduction

The growing need for integration of Distributed Energy Resources (DER) along with the electrification of the energy sector increase the complexity of modern power systems. Technologies from diverse domains must properly be integrated and coordinated to ensure stability and resilience. Simulation and testing play a key role in validating new technologies and operational strategies before deployment, but the complexity of today's systems demands sophisticated, cross-domain models (e.g., communication, transport, heating). Power Hardware-in-the-Loop (PHIL)-based laboratory testing offers a practical solution to address this complexity. In a PHIL setup, one or more hardware components are connected in real-time to a simulated environment via Power

Amplifiers (PAs). This approach supports diverse use cases such as the emulation of power components to accelerate the validation of advanced functionalities [1], [2]. In this case, the PHIL system accurately emulates the dynamic behavior of power system components that otherwise would not be available as physical devices for a given testing requirement.

Despite its advantages, PHIL also introduces inherent challenges related to stability and accuracy due to the non-ideal behavior of closed-loop components. Particularly, a PHIL setup must be stable across the required operating range and sufficiently accurate to produce results that closely reflect real-world behavior. Prior work proposed different Interface Approachs (IAs) to expand stability margins [3]–[5]. Particularly, some IAs require adjustments to the software interface or the addition of power components at the PAs output to maintain stable operation. Among others, such adjustments often introduce delays that distort the reactive power flow, leading to a representation that does not accurately reflect the actual system behavior [6]. Several compensation approaches were proposed to mitigate those effects [7]–[9]. However, fewer studies address the impact of the overall elements of a PHIL setup to the accuracy. In fact, complex PHIL setups might require additional elements such as cables, power connectors and busbars to realize the overall testbed. These contribute to the total impedance of the setup resulting into voltage deviations and inaccurate active and reactive power flows, especially for high-power applications.

This work suggests a straightforward compensation method that improves the accuracy of both reactive and active power flow for a PHIL setup. Its implementation only requires the tuning of the controller parameter and results particularly effective in case of low-dynamic and high-power emulation setups. The rest of this paper is structured as follows. Section II highlights the PHIL accuracy issues addressed in this study. Section III provides a description of the suggested compensation approach along with its implementation under the use case of emulation of a High-Power-Charging (HPC) system. The related experimental results are provided in Section IV. In conclusion, the main findings and outlooks are discussed.

II. ADDRESSED ACCURACY CHALLENGES

This work focuses on accuracy issues caused by the auxiliary elements necessary for implementing complex PHIL setups. These may include long cable connections, transformers, or power connectors that are required to connect the power output of the PA to the Point of Common Coupling (PCC), which represents the boundary of the actual hardware component of interest. The impact of auxiliary setup components is especially critical in high-power PHIL applications where undesired voltage drops and deviations in power flow can be significant. In this case, also the inner regulator of switched-mode PAs can have an impact on the accuracy. In fact, the regulator parameters such as the proportional and integral gain along with the feed-forward compensation are typically tuned for a specific operating range. This is generally a trade-off resulting into operating ranges where certain controller parameters are more accurate than others. To compensate these effects the user should tune the inner regulator parameters specifically for the given PHIL setup. However, not always inner regulator parameters are made editable from the manufacturer of PAs. Moreover, manipulation of the inner regulator can lead to significant accuracy improvements in steady-state conditions but can turn into instability in dynamic conditions.

An alternative solution to compensate these effects consists on a manipulation of the reference signals at the software side. The work conducted in [10] demonstrate various compensations methods. However, these do not include auxiliary setup components and require accurate analytical model of all the looped parts of the PHIL setup. A more straightforward solution adjusts voltage references in the simulation to counteract these effects [11], though it simplifies impedance estimation and lacks reactive power compensation. The method proposed in [12] compensates reactive power deviations by adding a delay to the reference current. However, it is limited to a fixed power set-point and requires a prior uncompensated simulation run at each set-point to determine the phase difference before applying the delay. Further approaches using the adaptive Smith Predictor targets reactive power correction [13]–[15], but they do not effectively address active power deviations and demands detailed dynamic models, thereby complicating the overall hardware emulation.

The compensation method investigated in this work aims to mitigate both reactive and active power deviations while minimizing implementation complexity. This approach is demonstrated for the case study of emulation of HPC-Systems for Electric Vehicles (EVs). However, it is readily extendable to any other similar PHIL testbeds in which the compensation of auxiliary setup elements represents a critical requirement.

III. METHODOLOGY

The general architecture of the suggested compensation method is depicted in Fig. 1. The HPC system, representing the element to be emulated, is modeled within a real-time simulator and interfaced with the PA via the current-type Ideal Transformer Method (ITM). An auxiliary impedance, (Z_{line}) represents the impact of the connection between the output of the PA and the PCC. In addition to the voltage feedback signal, that is required to implement the ITM, two compensation loops are introduced. The primary objective of the overall compensation strategy is to achieve power flow consistency between the simulation and the PCC in steady-state condition:

$$P_{\mathrm{PCC}} = P_{\mathrm{HPC}}, \quad Q_{\mathrm{PCC}} = Q_{\mathrm{HPC}}, \qquad (1)$$

where the quantities with the subscripts PCC and HPC denote the measurements at the PCC and those obtained from the simulated model of the HPC-System, respectively.

The PA-compensation compensates for power flow deviations at the output of the PA with respect to power setpoints from the simulation. This is achieved by leveraging instantaneous voltage and current measurements from the PA, which are typically available within the simulation environment and transmitted to the real-time simulator at high data rates. High-frequency transmission is essential to meet the stability requirements of PHIL systems. This loop addresses both active and reactive power deviations, although the most significant discrepancies often arise in the reactive component due to communication delays, low-pass filtering, and potential steady-state errors inherent to the internal controllers of the switched-mode PA.

The Setup-compensation compensates for power deviations introduced by the auxiliary impedance Z_{line}. It addresses both active and reactive power deviations at the PCC, with active power discrepancies being more pronounced. Implementing this loop requires an additional power measurement device, which is typically available in complex testing infrastructures.

Both compensation loops ultimately generate instantaneous current signals that are used to correct the current reference provided by the simulated model. A more comprehensive description of each compensation loop is presented in the next subsection.

A. Compensation Approach

In this subsection, the compensation approach is detailed in an exemplary manner for active power, but the same structure is applied for reactive power. Fig. 2 shows the block diagrams related to the overall controller structure, including the PA-compensation loop (green), the Setup-compensation loop (purple) and the prediction of the measurements at the PCC (orange).

The PA's active power offset ($P_{\mathrm{O,PA}}$) to be compensated is determined as follows:

$$P_{\mathrm{O,PA}} = P_{\mathrm{sw}} - P_{\mathrm{PA}}, \qquad (2)$$

where P_{sw} represents the active power measured at the PHIL interface within the real-time simulator and P_{PA} is the active power output of the PA. The value for the reactive power offset ($Q_{\mathrm{O,PA}}$) is calculated similarly as in (2). This offset represents the reference signal for a PI controller providing the PA compensation power setpoint. Based on the momentary value of the voltage $v_{\mathrm{PA}}(t)$, the compensation current setpoint $i^*_{\mathrm{c,PA,P}}(t)$ is determined.
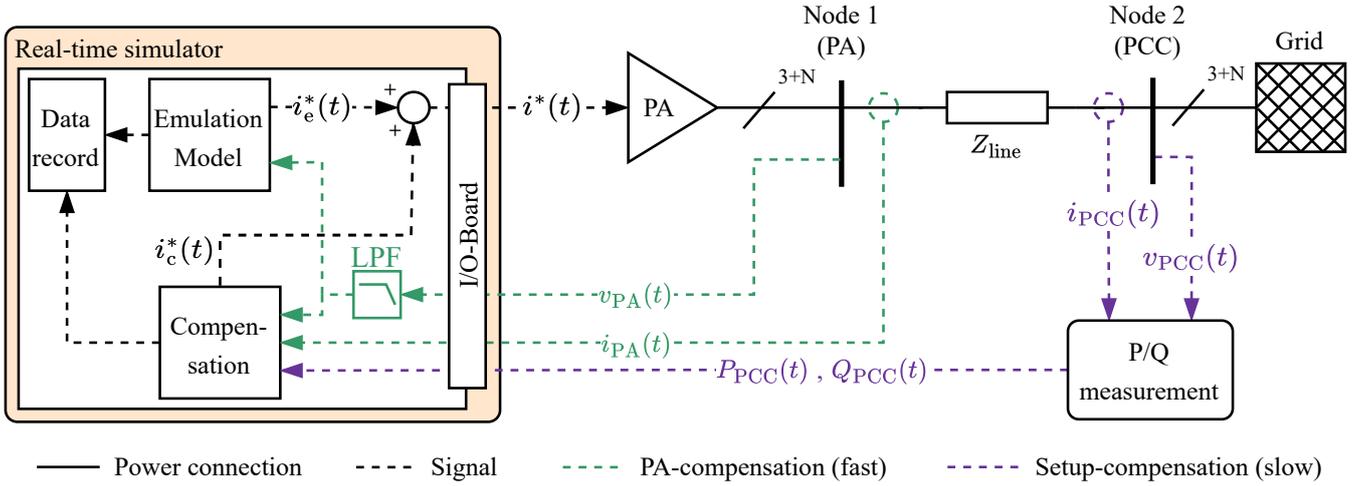
Fig. 1. PHIL emulation and compensation concept

The second stage compensates the impact of the laboratory setup, represented by Z_line in Fig. 1. A key challenge arises from the significantly slower update rate of the PCC measurements compared to the PA measurements. Thus, the above offset calculation cannot directly be applied in the form of the difference between P_PA and P_PCC. During the transition phase following adjustments to the power setpoint of the emulated charger, a virtual offset emerges. The PA measurements are updated with every timestep in the simulation. However, the limited message rate causes the PCC measurements to be available in the simulation only after a certain delay, yielding this discrepancy. To increase the PCC measurement dynamics and eliminate this systematic error, a straightforward prediction method is introduced. The prediction signal, denoted as $\hat{P}_\text{PCC}$, is calculated in the real-time simulation to approximate the physical measurement P_PCC. By updating this signal at each simulation timestep, limitations arising from communication with the P/Q measurement device can effectively be mitigated.

The PCC signal prediction method is highlighted in orange in Fig. 2. Considering the target of steady-state power flow consistency according to (1), the signal P_HPC is used as an auxiliary variable in a feed-forward control to construct the signal $\hat{P}_\text{PCC}$ ensuring its required high update rate. The actual PCC measurement serves as reference signal for a PI controller continuously correcting $\hat{P}_\text{PCC}$ so it converges toward P_PCC in steady-state. To mitigate overshoot of P_corr during changing charging power setpoint, a reset logic is implemented within the prediction controller. The reset signal (R) keeps the PI controller inactive until P_PCC stabilizes at its new value which is detected through monitoring peaks in $\frac{d}{dt} P_\text{PCC}$ followed by a waiting period. This dual approach enables both rapid updates during dynamic scenarios and accurate steady-state operation based on physical measurements at the PCC.

The prediction signal $\hat{P}_\text{PCC}$ is subsequently used for the calculation of the laboratory setup compensation current $i^*_\text{c,Lab,P}(t)$ as depicted in Fig. 2 (purple). Due to the high

signal update rate, the same structure as for PA compensation can be applied. Both current setpoints are added and represent the current $i^*_\text{c,P}(t)$ required to compensate the deviations in active power flow. Similarly, the signal $i^*_\text{c,Q}(t)$ is determined in order to mitigate deviations in reactive power flow.

The high update rate of the inner loop allows a more aggressive tuning of the PA-compensation PI controller compared to the Setup-compensation controller. This enhances the dynamic response as only the deviation between PA output and PCC remains for the slower setup compensation controller. The response time of the latter is improved through the proposed PCC signal prediction method.

B. Laboratory Implementation

The PHIL emulation and compensation concept depicted in Fig. 1 is implemented at the Smart Grid Technology Lab (SGTL) of TU Dortmund University [16]. The laboratory is equipped with a real-time simulator, and two groups of switched-mode PAs, each rated at 100 kVA, which are deployed in the experiments presented in this paper. Particularly, the real-time simulator hosts the emulation model, i.e., the HPC system comprising an average-model AC-DC and DC-DC converter stage as well as a basic EV battery model. The charger model is designed to study opportunities and limitations of grid-supportive charging, for example the injection of reactive power through HPC systems. For this purpose it incorporates independent control of the chargers' active and reactive power setpoint via a Modbus TCP interface. This way, charging algorithms can be deployed independently from the model and communicate the requested setpoints to the real-time simulator. The conventional EV charger control scheme with fixed DC-link as described in [17] is implemented for control of the AC-DC and DC-DC converters of the model. The charger model is coupled with the physical laboratory setup through the current-type ITM IA. The measured three-phase voltage $v_\text{PA}(t)$ at Node 1 is represented in the simulation
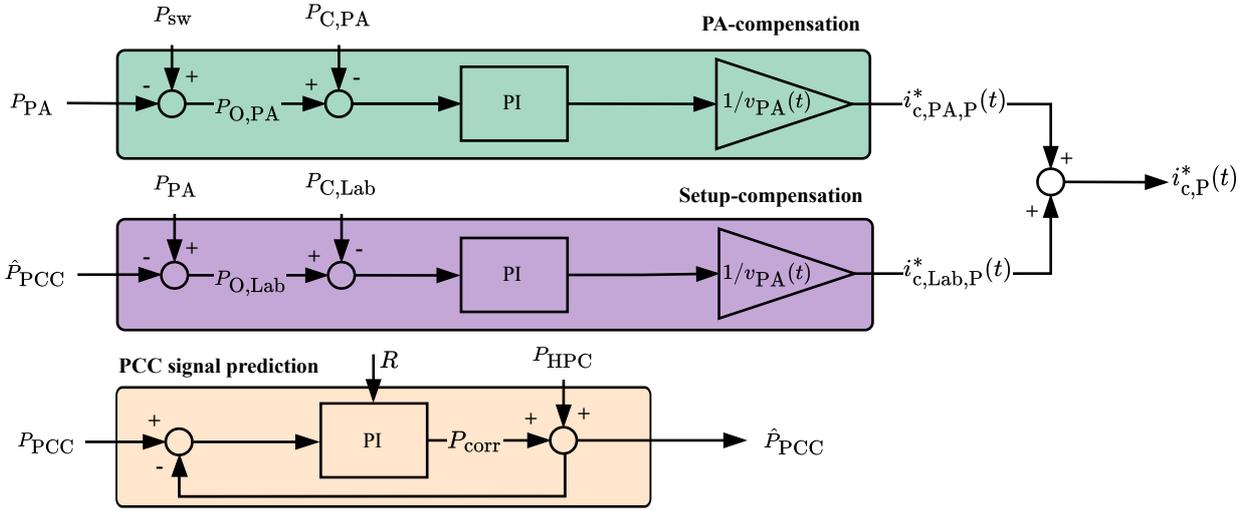
Fig. 2. Block diagram of the compensation method: PA-compensation (green), Setup-compensation (purple), PCC measurement prediction (orange)

by ideal controlled voltage sources, which are connected to the chargers' grid interface. To enhance stability and mitigate high-frequency disturbances, this voltage feedback is conditioned by a low-pass filter (LPF). As a trade-off between its effectiveness and the resulting dynamic restrictions a cutoff frequency of 2 kHz is selected. The current drawn by the charger is measured in the simulation and represents the emulation setpoint $i_e^*(t)$, to which the compensation current $i_c^*(t)$ is added. The communication between the real-time simulator and the PA is established through a fiber optic connection yielding a setpoint update rate of 250 kHz (green inner loop in Fig. 1) [2].

For P/Q measurement at the PCC, a power quality analyzer (KoCoS EPPE PX) is placed at Node 2. The values of P_{PCC} and Q_{PCC} are transmitted to the real time simulator using Modbus TCP communication protocol at an update rate of 500 ms. This signal feedback represents the purple outer loop in Fig. 1 and is significantly slower than the inner loop due to the inherently limited message rate of Modbus TCP. A NodeRED instance hosts a user interface for setpoint control of the emulated charger, a dashboard for monitoring of measurements, and a database for measurement logging. Moreover, it acts as Modbus master forwarding the PCC measurements to the real-time simulator.

IV. Results

The performance of the suggested compensation approach is evaluated by applying a defined time series of setpoints for the emulated charger for active and reactive power, respectively. The first part of the time series comprises an increase of the setpoint from 0 kW to 100 kW in steps of 10 kW with each setpoint kept for one minute. Similarly, the power is decreased stepwise to 0 kW. The second part consists of intermittent charging to test the response of the compensation approach in more dynamic scenarios. Beginning with 100 kW, the intermit-

tent charging power is decreased in steps of 20 kW. The same time series profile is applied for reactive power setpoints. For both active and reactive power time series, tests are performed with compensation controllers inactive as the reference case as well as active, leading to four distinct operational scenarios. The following two subsections describe the results of the measurements performed with active power time series and reactive power time series. Lastly, the analytical assessment of the dynamics and steady-state accuracy is provided in the third subsection.

A. Active Power Test Case

Fig. 3 shows the power flow at the PCC during the active power time series (the index r indicates reference case, while the index a represents the measurements with active compensation). While $P_{PCC,r}$ coincides relatively well with P^* at deviations of up to 1.4 kW, the error in reactive power flow is much more pronounced. Although the setpoint Q^* remains zero during the test, an initial offset of -2.4 kvar as well as a positive correlation between $Q_{PCC,r}$ and $P_{PCC,r}$ can be observed. At 100 kW charging power, the emulation setup draws additional 14.5 kvar inductive reactive power from the grid at the PCC.

With compensation active, $P_{PCC,a}$ follows P^* more accurately which is especially clear at higher power flow. However, the settling time of the compensation PI controller lead to a slight overshoot in dynamic scenario after minute 20. A similar effect can be observed for $Q_{PCC,a}$: while the reactive power flow can be kept close to zero in the first part of the time series, more pronounced overshoots appear in the dynamic scenario. After approximately 30 s, $Q_{PCC,a}$ approaches zero and the deviation is compensated.

B. Reactive Power Test Case

From Fig. 4, showing the results of the reactive power test case, it can be seen that the value of $Q_{PCC,r}$ follows
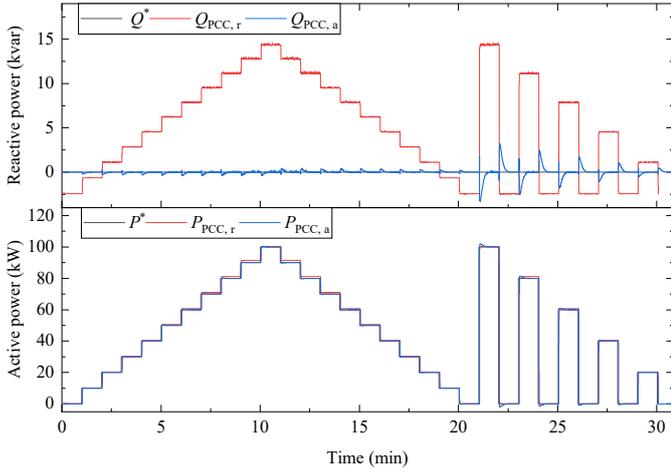
Fig. 3. Active power test case: power flow at the PCC with active and inactive compensation compared to setpoints
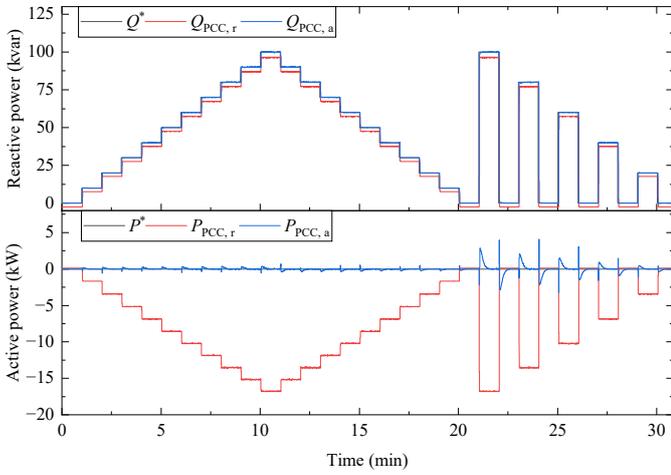

Fig. 4. Reactive power test case: power flow at the PCC with active and inactive compensation compared to setpoints of the charger

the setpoint Q^* with a relatively consistent offset of -2.5 kvar to -4 kvar with inactive compensation. A positive correlation is observed between $P_{\text{PCC,r}}$ and $Q_{\text{PCC,r}}$ during the active power time series. The reactive power time series test reveals a similar, but negative correlation. With increasing inductive $Q_{\text{PCC,r}}$, the PA injects active power of up to -16.8 kW at 100 kvar.

The steady-state offset of $Q_{\text{PCC,r}}$ is effectively removed once the compensation is activated as can be seen from the graph of $Q_{\text{PCC,a}}$ closely following the setpoint Q^*. During the stepwise change of Q^*, $P_{\text{PCC,a}}$ remains within a range of $\pm\,0.7$ kW around zero. In the dynamic scenario after 20 min, peaks of up to 4 kW can be measured at the PCC. Similar to the active power test case, the limited dynamic response of the compensation approach becomes visible in settling times of around 30 s.

C. Dynamics Performance and Accuracy Analysis

Beside the visual inspection of the power flow profiles in Fig. 3 and 4, the dynamic characteristics and steady-state accuracy of the compensation approach is evaluated analytically. In each of the four tests, average values of stationary bias, absolute error and settling time are determined based on the measurement log obtained by the NodeRED instance. This data source is chosen over the data record of the real-time simulator as the additional delay due to forwarding of the measurements to the simulator is circumvented.

The evaluation is detailed exemplary for active power but is similarly applied to reactive power. First, the stationary value of P_{PCC} is determined for each setpoint stage by calculating the average power of the last 30 s before P^* changes to another value. As can be seen from Fig. 3, the power flow is stable during this period so it is considered as steady-state operation. For all non-zero setpoints, the relative stationary bias incorporating the signed deviation from the setpoint P^* is calculated in percentage. Additionally, the absolute error is determined in percentage based on the absolute deviation of P_{PCC} from P^*. Ultimately, the average stationary bias and absolute error provide criteria to evaluate systematic deviations and the stationary accuracy of the compensation.

As a third parameter, the settling time $T_{2\%}$ is determined for each setpoint change to assess the impact of the compensation approach on the dynamic characteristics of the PHIL emulation. It is defined as the time required until the step response of a system reaches its stationary value under consideration of a tolerance band of 2 % and stays within this band [18]. The average settling time $\overline{T}_{2\%}$ is determined as the average across all setpoints where the 2 %-band around the stationary value is reached within the 60 s of constant setpoint. The only setpoint which may be excluded here is $P^* = 0$ with active compensation as the stationary value is close to zero resulting in a very narrow tolerance band.

Table I summarizes the three average values for all performed tests. The stationary bias and absolute error of 1.20 % for the active power reference test underline the relatively accurate active power control of the PA which is already observed in Fig. 3. However, with active compensation, both values can be lowered to almost zero. The slightly lowered settling time indicates even a small positive impact on the dynamic response. The continuous offset independent from the setpoint which is observed in Fig. 4 also appears in the stationary bias (-7.31 %) and its standard deviation (5.86 %).

TABLE I
STATIONARY BIAS, ABSOLUTE ERROR AND SETTLING TIME OF THE POWER FLOW AT THE PCC (AVERAGE VALUES).

Scenario	Stationary bias	Absolute error	Settling time
P (ref.)	$1.20 \pm 0.34\,\%$	$1.20\,\%$	1.35 ± 0.32 s
P (active)	$0.0004 \pm 0.003\,\%$	$0.002\,\%$	1.27 ± 0.30 s
Q (ref.)	$-7.31 \pm 5.86\,\%$	$7.31\,\%$	1.28 ± 0.33 s
Q (active)	$-0.0020 \pm 0.0141\,\%$	$0.009\,\%$	1.23 ± 0.33 s

This deviation is much more pronounced than the active power deviation previously described but is still effectively mitigated by the compensation. With activated compensation controller, the stationary bias is reduced to -0.0020 $\pm$ 0.0141 %. Also in this case, the settling time is slightly lowered confirming no negative impact on the response of the system.

V. Conclusion

This paper presents a compensation method to improve accuracy of complex Power Hardware-in-the-Loop (PHIL) testbeds in low-dynamics applications. Particularly, active and reactive power accuracy issues caused by the auxiliary elements necessary for implementing complex PHIL setups are addressed. The implementation of this compensation method only requires an additional power measurement device to be installed at the PCC of a PHIL setup. The effectiveness of the suggested compensation method is evaluated under the use case of PHIL-based emulation of HPC systems. Results show that the average stationary absolute error can drastically be reduced from up to 7.31 % to less than 0.01 % while the dynamic characteristics of the emulation setup is not negatively affected. Notably, significant reactive power injection during variation of active power flow, and vice versa, can be effectively mitigated. However, due to highly individual laboratory configurations and variety of measurement systems, a certain manual effort to properly tuning the required PI controller remains. To overcome this limitation, future work will target the requirement of individual adjustment of the compensation PI controllers by an adaptive controller tuning approach. Moreover, beside the validation of the proposed compensation method additional work must be carried out to validate the implemented HPC model. For the scope of this paper, this is however of secondary relevance as the inner dynamic behavior of the simulated model does not affect the performance of the suggested compensation approach.

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